# PFE3000-12-069RA

## 3000 W AC-DC Front-End Power Supply

The **PFE3000-12-069RA** is a 3000 Watt AC/DC power-factor-corrected (PFC) and DC-DC power supply that converts standard AC mains power or high voltage DC bus voltages into a main output of 12 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches.

The PFE3000-12-069RA meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

### Key Features & Benefits

- Best-in-class, Platinum efficiency
- Wide input voltage range: 90-300 VAC
- AC input with power factor correction
- DC input voltage range: 192-400 VDC
- Hot-plug capable
- Parallel operation with active current sharing thru analog bus
- Full digital controls for improved performance
- High density design: 30.5 W/in$^3$
- Small form factor: 69 x 42 x 555 mm
- I2C communication interface with PMBus® protocol for monitoring, control, and firmware update via bootloader
- Overtemperature, output overvoltage and overcurrent protection
- RoHS Compliant
- 2 Status LEDs: AC OK and DC OK with fault signaling
- Safety-approved to IEC/EN 60950-1 and UL/CSA 60950-1 2nd ed.
- US Patent Pending

### Applications

- High Performance Servers
- Routers
- Switches

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## 1.  ORDERING INFORMATION

| PFE | 3000 | - | 12 | - | 069 | R | A | Option Code |
|---|---|---|---|---|---|---|---|---|
| Product Family | Power Level | Dash | V1 Output | Dash | Width | Airflow | Input | **Blank:** Standard model **S366:** Screw for Key-in feature is installed. |
| PFE Front-Ends | 3000 W | | 12 V | | 69 mm | R: Reversed[1] | A: AC | |

[1]      Front to Rear

## 2.  OVERVIEW

The PFE3000-12-069RA is a fully DSP controlled, highly efficient front-end power supply. It incorporates resonant-soft-switching technology and interleaved power trains to reduce component stresses, providing increased system reliability and very high efficiency. With a wide input operating voltage range and minimal linear derating of output power with respect to ambient temperature, the PFE3000-12-069RA maximizes power availability in demanding server, switch, and router applications. The power supply is fan cooled and ideally suited for server integration with a matching airflow path.

The PFC stage is digitally controlled using a state-of-the-art digital signal processing algorithm to guarantee best efficiency and unity power factor over a wide operating range.

The DC-DC stage uses soft switching resonant techniques in conjunction with synchronous rectification. An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems. The always-on +12V standby output provides power to external power distribution and management controllers. Its protection with an active OR-ing device provides for maximum reliability.

Status information is provided with front-panel LEDs. In addition, the power supply can be monitored and controlled (i.e. fan speed setpoint) via I²C communication interface with PMBus® protocol. It allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures.  The same I²C bus supports the bootloader to allow field update of the firmware in the DSP controllers.

Cooling is managed by a fan, controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I²C bus.
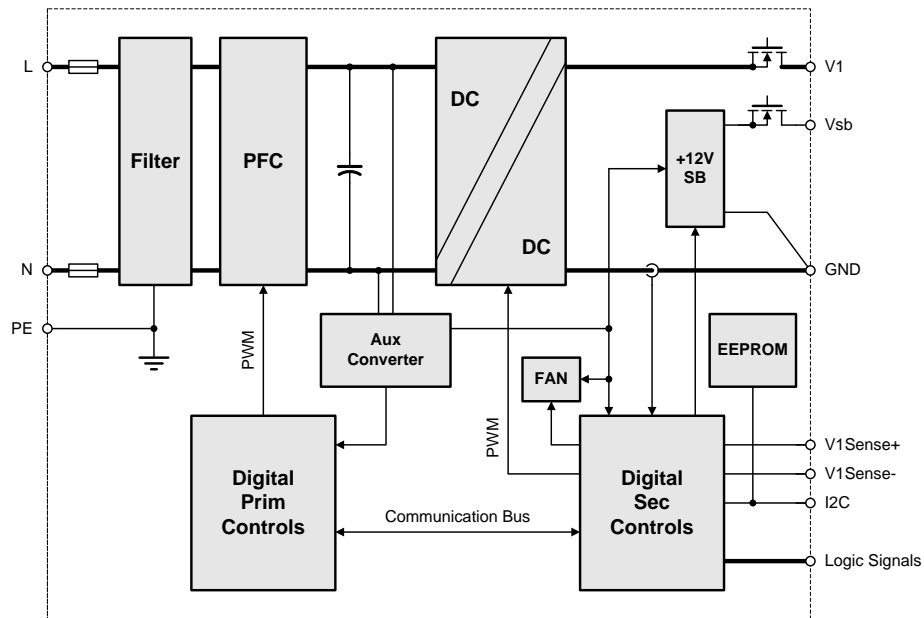


*Figure 1 - PFE3000-12-0069RA Block Diagram*

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## 3. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the supply.

| PARAMETER | | CONDITIONS / DESCRIPTION | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| $V_{i\,maxc}$ | Maximum Input | Continuous | | 300 | VAC |

## 4. INPUT

General Condition: $T_A = 0\ldots 45\,°C$ unless otherwise noted.

| PARAMETER | | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{i\,nom}$ | AC Nominal Input Voltage | | 100 | 230 | 277 | VAC |
| $V_i$ | AC Input Voltage Ranges | Normal operating ($V_{i\,min}$ to $V_{i\,max}$) | 90 | | 300 | VAC |
| $V_{inom\,DC}$ | DC Nominal input voltage | | 240 | | 380 | VDC |
| $V_{i\,DC}$ | DC Input voltage ranges | Normal operating ($V_{i\,min}$ to $V_{i\,max}$) | 192 | | 400 | VDC |
| $V_{i\,red}$ | *Derated Input Voltage Range* | See *Figure 20* and *Figure 33* | 90 | | 180 | VAC |
| $I_{i\,max}$ | Max Input Current | $V_i > 200\ VAC, >100\ VAC$ | | | 17 | $A_{rms}$ |
| $I_{i\,p}$ | Inrush Current Limitation | $V_{i\,min}$ to $V_{i\,max}$, $0\,°\ T_{NTC} = 25°C$ (Figure 5) | | | 50 | $A_p$ |
| $F_i$ | Input Frequency | | 47 | 50/60 | 63 | Hz |
| PF | Power Factor | $V_{i\,nom}$, 50Hz, $> 0.3\ I_{1\,nom}$ | 0.96 | | | W/VA |
| $V_{i\,on}$ | Turn-on Input Voltage[2] | Ramping up | 80 | | 87 | VAC |
| $V_{i\,off}$ | Turn-off Input Voltage[2] | Ramping down | 73 | | 85 | VAC |
| η | Efficiency without Fan | $V_{i\,nom}$, $0.1 \cdot I_{x\,nom}$, $V_{x\,nom}$, $T_A = 25°C$ | 90.0 | 91.85 | | % |
| | | $V_{i\,nom}$, $0.2 \cdot I_{x\,nom}$, $V_{x\,nom}$, $T_A = 25°C$ | 93.0 | 94.40 | | |
| | | $V_{i\,nom}$, $0.5 \cdot I_{x\,nom}$, $V_{x\,nom}$, $T_A = 25°C$ | 94.5 | 94.95 | | |
| | | $V_{i\,nom}$, $I_{x\,nom}$, $V_{x\,nom}$, $T_A = 25°C$ | 93.0 | 93.75 | | |
| $T_{hold}$ | Hold-up Time | After last AC zero point, $V_1 > 10.8\ V$, $V_{SB}$ within regulation, $V_i = 230\ VAC$, $P_{x\,nom}$ | 12 | | | ms |

[2]    The Front-End is provided with a minimum hysteresis of 3 V during turn-on and turn-off within the ranges

### 4.1 INPUT FUSE

Quick-acting 25 A input fuses (6.3 × 32 mm) in series with both the L- and N-line inside the power supply protect against severe defects. The fuses are not accessible from the outside and are therefore not serviceable parts.

### 4.2 INRUSH CURRENT

The AC-DC power supply exhibits an X capacitance of only 4.3µF, resulting in a low and short peak current, when the supply is connected to the mains. The internal bulk capacitor will be charged through an NTC which will limit the inrush current.

**NOTE:**
Do not repeat plug-in / out operations below 90sec interval time at maximum input, high temperature condition, or else the internal in-rush current limiting device (NTC) may not sufficiently cool down and excessive inrush current or component failure(s) may result.

**Asia-Pacific**
+86 755 298 85888

**Europe, Middle East**
+353 61 225 977

**North America**
+1 408 785 5200

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## 4.3 INPUT UNDER-VOLTAGE

If the RMS value of input voltage (either AC or DC) stays below the input undervoltage lockout threshold Vi on, the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again.

## 4.4 POWER FACTOR CORRECTION

Power factor correction (PFC) (see *Figure 4*) is achieved by controlling the input current waveform synchronously with the input voltage. A fully digital controller is implemented giving outstanding PFC results over a wide input voltage and load ranges. The input current will follow the shape of the input voltage. If for instance the input voltage has a trapezoidal waveform, then the current will also show a trapezoidal waveform. At DC input voltage the PFC is still in operation, but the input current will be DC in this case.

## 4.5 EFFICIENCY

The high efficiency (see *Figure 2*) is achieved by using state-of-the-art silicon power devices in conjunction with soft-transition topologies minimizing switching losses and a full digital control scheme. Synchronous rectifiers on the output reduce the losses in the high current output path. The rpm of the fan is digitally controlled to keep all components at an optimal operating temperature regardless of the ambient temperature and load conditions.
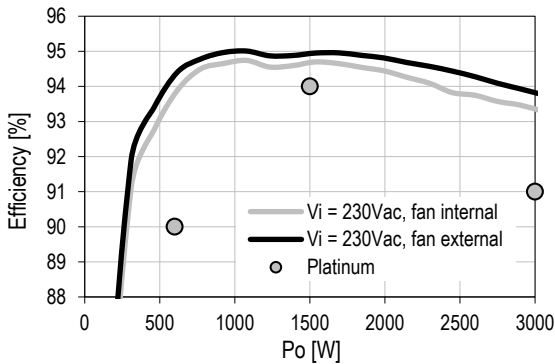*Figure 3* shows efficiency when input voltage is supplied from a high voltage DC source.



Figure 2 – AC Input Efficiency vs. Load current
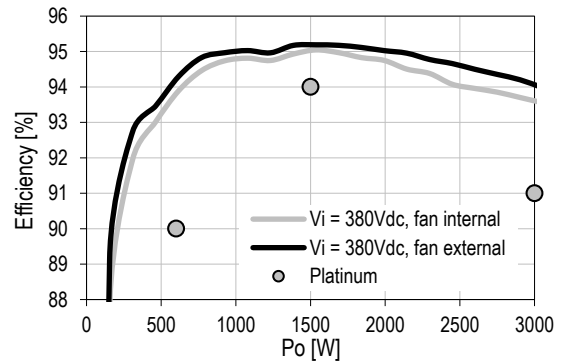(ratio metric loading)



Figure 3 - DC Input Efficiency vs. load current
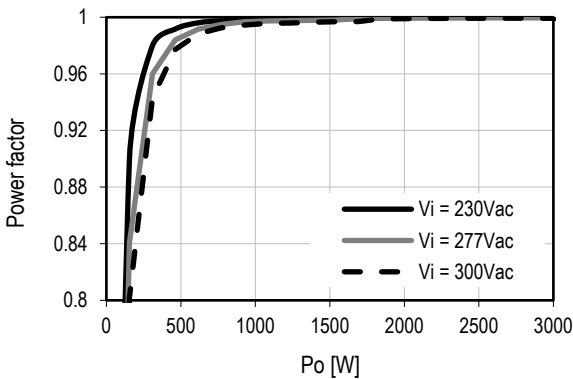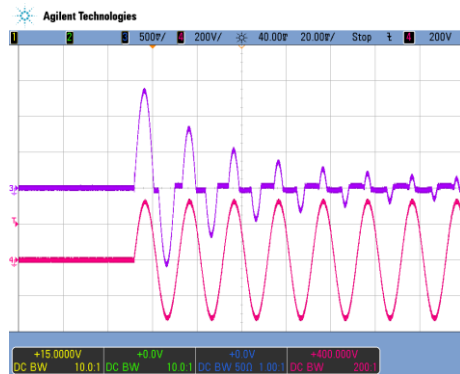(ratio metric loading)



Figure 4 - Power factor vs. Load current



Figure 5 - Inrush current, Vin = 230 Vac, 0°phase angle
CH4: Vin (200 V/div), CH3: Iin (10 A/div)

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## 5. OUTPUT

General Condition: $T_A = 0\ldots45\,°C$ unless otherwise noted.

| PARAMETER | | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Main Output V1** | | | | | | |
| $V_{1\,nom}$ | Nominal Output Voltage | $0.5 \cdot I_{1\,nom}$, $T_{amb} = 25\,°C$ | | 12.3 | | VDC |
| $V_{1\,set}$ | Output Setpoint Accuracy | | -0.5 | | +0.5 | % $V_{1\,nom}$ |
| $dV_{1\,tot}$ | Total Regulation | $V_{i\,min}$ to $V_{i\,max}$, 0 to 100% $I_{1\,nom}$, $T_{a\,min}$ to $T_{a\,max}$ | -1 | | +1 | % $V_{1\,nom}$ |
| $P_{1\,nom}$ | Nominal Output Power | $V_1 = 12.3$ VDC, Vin < 180 VAC | | 1400 | | W |
| $I_{1\,nom}$ | Nominal Output Current | $V_1 = 12.3$ VDC, Vin < 180 VAC | | 114 | | ADC |
| $P_{1\,nom}$ | Nominal Output Power | $V_1 = 12.3$ VDC, Vin > 180 VAC | | 3000 | | W |
| $I_{1\,nom}$ | Nominal Output Current | $V_1 = 12.3$ VDC, Vin > 180 VAC | | 244 | | ADC |
| $I_{V1\,ol}$ | Short time over load current | $V_1 = 12.3$ VDC, Vin > 180 VAC $T_{a\,min}$ to $T_{a\,max}$, maximum duration 20 ms (See Section 5.2) | | | 292 | A |
| $v_{1\,pp}$ | Output Ripple Voltage | $V_{1\,nom}$, $I_{1\,nom}$, 20 MHz BW (See Section 5.1) | | | 160 | mVpp |
| $dV_{1\,Load}$ | Load Regulation | $V_1 = V_{1\,nom}$, 0 - 100 % $I_{1\,nom}$ | | 170 | | mV |
| $dV_{1\,Line}$ | Line Regulation | $V_1 = V_{i\,min}\ldots V_{i\,max}$ | | 0 | | mV |
| $I_{V1\,ol\,lim}$ | Current limitation | $V_i < 180$ VAC, $T_a < 45°C$<br>$V_i < 180$ VAC, $T_a = 55\,°C$ [3]<br>$V_i > 180$ VAC, $T_a < 45°C$<br>$V_i > 180$ VAC, $T_a = 55\,°C$ [3] | 120<br>92<br>248<br>186 | | 127<br>99<br>274<br>212 | ADC |
| $dI_{share}$ | Current Sharing | Deviation from $I_{tot}$ / N, $I_1 > 25\%$ $I_{nom}$ | -5% | | +5% | A |
| $dV_{dyn}$ | Dynamic Load Regulation | $\Delta I_1 = 50\%$ $I_{1\,nom}$, $I_1 = 5\ldots100\%$ $I_{1\,nom}$, $dI_1/dt = 1A/\mu s$, $f_{\Delta I1} = 0.05\ldots10$ kHz, $Duty_{\Delta I1} = 10\ldots90\%$, recovery within 1% of $V_1$ final steady state | -0.6 | | +0.6 | V |
| $T_{rec}$ | Recovery Time | | | | 0.5 | ms |
| $t_{AC\,V1}$ | Start-up Time from AC | $V_1 = 10.8$ VDC (see *Figure 7*) | | | 3 | sec |
| $t_{V1\,rise}$ | Rise Time | $V_1 = 10\ldots90\%$ $V_{1\,nom}$ (see *Figure 8*) | | 2.5 | | ms |
| $C_{Load}$ | Capacitive Loading | $T_a = 25°C$ | | | 30000 | µF |

[3]    See *Figure 20* for linear derating > 45°C

| PARAMETER | | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Stanby Output V$_{SB}$** | | | | | | |
| $V_{SB\,nom}$ | Nominal Output Voltage | $I_{SB\,nom}$, $T_{amb} = 25°C$ | | 12 | | VDC |
| $V_{SB\,set}$ | Output Setpoint Accuracy | | -0.5 | | +0.5 | % $V_{SBnom}$ |
| $dV_{SB\,tot}$ | Total Regulation | $V_{i\,min}$ to $V_{i\,max}$, $I_{SB\,nom}$, $T_{a\,min}$ to $T_{a\,max}$ | -1 | | +1 | % $V_{SBnom}$ |
| $P_{SB\,nom}$ | Nominal Output Power | $V_{SB} = 12$ VDC | | 60 | | W |
| $I_{SB\,nom}$ | Nominal Output Current | $V_{SB} = 12$ VDC | | 5 | | ADC |
| $V_{SB\,pp}$ | Output Ripple Voltage | $V_{SB\,nom}$, $I_{SB\,nom}$, 20 MHz BW (See Section 5.1) | | | 300 | mVpp |
| $dV_{SB}$ | Droop | 0 - 100 % $I_{SB\,nom}$ | | 400 | | mV |
| $I_{VSB\,lim}$ | Current Limitation | | 6 | | 9 | ADC |
| $dV_{SBdyn}$ | Dynamic Load Regulation | $\Delta I_{SB} = 50\%$ $I_{SB\,nom}$, $I_{SB} = 5\ldots100\%$ $I_{SB\,nom}$, $dI_0/dt = 1A/\mu s$, $f_{\Delta I1} = 0.05\ldots10$kHz, $Duty_{\Delta I1} = 10\ldots90\%$, recovery within 1% of $V_{SB}$ final steady state | -0.6 | | +0.6 | $V_{SBnom}$ |
| $T_{rec}$ | Recovery Time | | | | 0.5 | ms |
| $t_{AC\,VSB}$ | Start-up Time from AC | $V_{SB} = 90\%$ $V_{SB\,nom}$ (see *Figure 7*) | | | 3 | sec |
| $t_{VSB\,rise}$ | Rise Time | $V_{SB} = 10\ldots90\%$ $V_{SB\,nom}$ (see *Figure 9*) | | 10 | | ms |
| $C_{Load}$ | Capacitive Loading | $T_{amb} = 25°C$ | | | 3000 | µF |

## 5.1 OUTPUT VOLTAGE RIPPLE

The internal output capacitance at the power supply output (behind OR-ing element) is minimized to prevent disturbances during hot plug. In order to provide low output ripple voltage in the application, external capacitors should be added close to the power supply output.

The setup of *Figure 6* has been used to evaluate suitable capacitor types. The capacitor combinations of Table 1 and Table 2 should be used to reduce the output ripple voltage.

The ripple voltage is measured with 20 MHz BWL, close to the external capacitors.
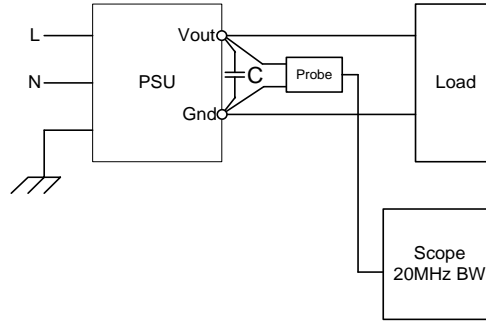


*Figure 6 - Output Ripple Test Setup*

**NOTE:** Care must be taken when using ceramic capacitors with a total capacitance of 1 µF to 50 µF on output V1, due to their high quality factor the output ripple voltage may be increased in certain frequency ranges due to resonance effects.

| External Capacitor V1 | dV1max | Unit |
|---|---|---|
| 2Pcs 47µF/16V/X5R/1210 | 160 | mVpp |
| 1Pcs 1000µF/16V/Low ESR Aluminum/ø10x20 | 160 | mVpp |
| 1Pcs 270µF/16V/Conductive Polymer/ø8x12 | 160 | mVpp |
| 2Pcs 47µF/16V/X5R/1210 plus 1Pcs 270µF Conductive Polymer OR 1Pcs 1000µF Low ESR AlCap | 90 | mVpp |

*Table 1 - Suitable Capacitors for V1*

| External capacitor VSB | dVSBmax | Unit |
|---|---|---|
| 1Pcs 10µF/16 V/X7R/1206 | 300 | mVpp |

*Table 2 - Suitable Capacitors for VSB*

The output ripple voltage on VSB is influenced by the main output V1. Evaluating VSB output ripple must be done when maximum load is applied to V1.

## 5.2 SHORT TIME OVERLOAD

The main output has the capability to allow load current up to 20% above the nominal output current rating for a maximum duration of 20 ms. This allows the system to consume extended power for short time dynamic processes.

## 5.3 OUTPUT ISOLATION

Main and standby output and all signals are isolated from the chassis and protective earth connection, although the applied voltage must not exceed 100 Vpeak to prevent any damage of the supply.

Internal to the supply the main output ground, standby output ground and signal ground are interconnected through 10Ω resistors to prevent any circulating current within the supply. In order to prevent any potential difference in outputs or signals within the application these 3 grounds must be directly interconnected at system level. See also section 14 for pins to be interconnected.

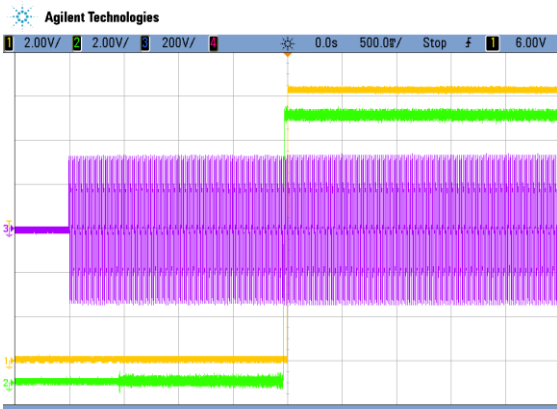tech.support@psbel.com
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Figure 7 - Turn-On AC Line 230 VAC, full load (500 ms/div)
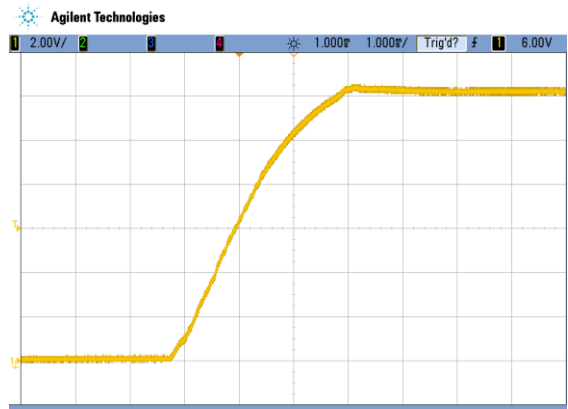CH1: V1 (2 V/div); CH2: VSB (2 V/div); CH3: Vin (200 V/div)



Figure 8 - Turn-On AC Line 230 VAC, full load (1 ms/div)
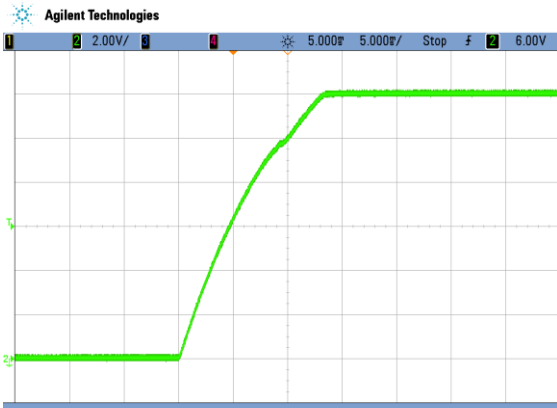CH1: V1 (2 V/div)



Figure 9 - Turn-On AC Line 230 VAC, full load (5 ms/div)
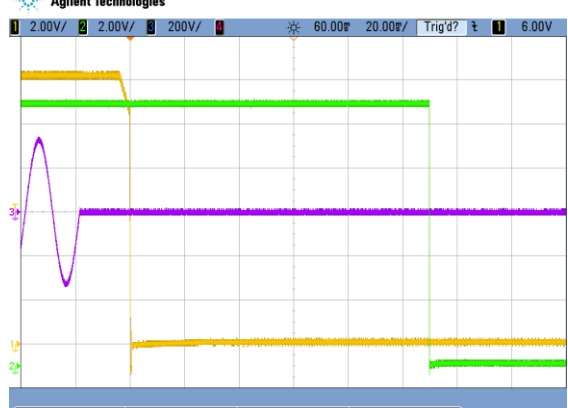CH2: VSB (2 V/div)



Figure 10 - Turn-Off AC Line 230 VAC, full load (20 ms/div)
CH1: V1 (2 V/div); CH2: VSB (2 V/div); CH3: Vin (200 V/div)



Figure 11 - Short circuit on V1 (50ms/div)
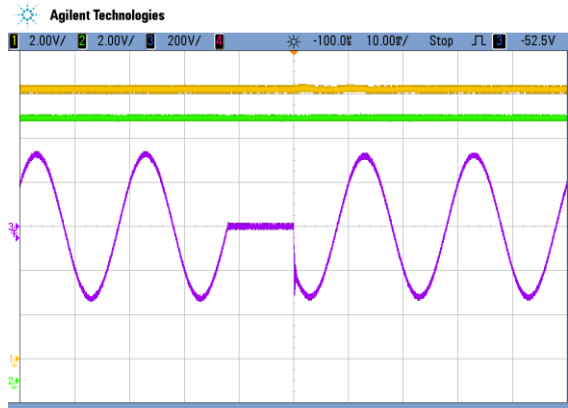CH1: V1 (2V/div) CH2: VSB (2V/div) CH4: I1 (200A/div)



Figure 12 - AC drop out 12ms (10ms/div)
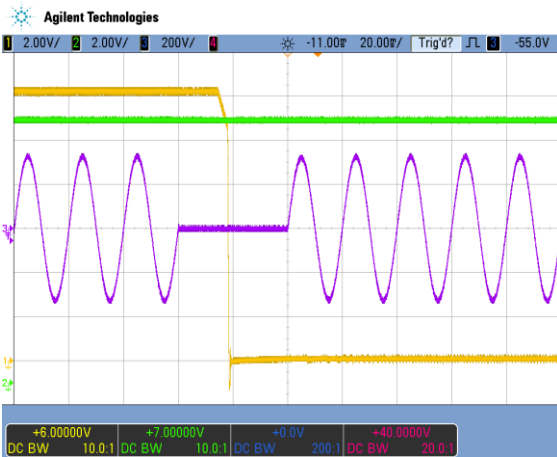CH1: V1 (2V/div) CH2: VSB (2V/div) CH3: Vin (200V/div)

*Figure 13 - AC drop out 40 ms, full load (20 ms/div)*
*CH1: V1 (2 V/div); CH2: VSB (2 V/div); CH3: Vin (200 V/div)*



*Figure 14 - AC drop out 40 ms, full load (200 ms/div),V1 restart*
*after 1 sec CH1: V1 (5 V/div); CH2: VSB (2 V/div);*
*CH3: I1 (200 V/div)*



*Figure 15 - Load transient V1, 3 to 125 A (500 µs/div)*
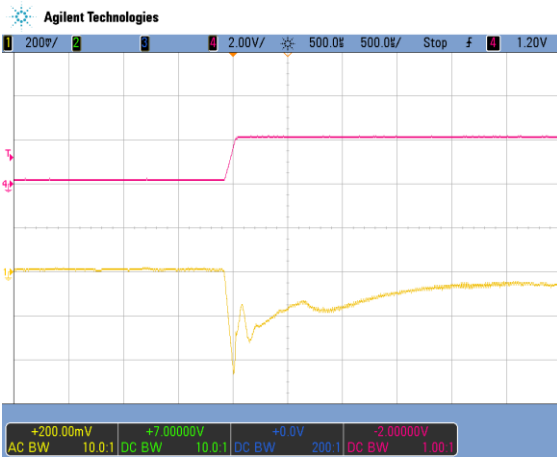*CH1: V1 (200 mV/div); CH4: I1 (100 A/div)*



*Figure 16 - Load transient V1, 125 to 3 A (500 µs/div)*
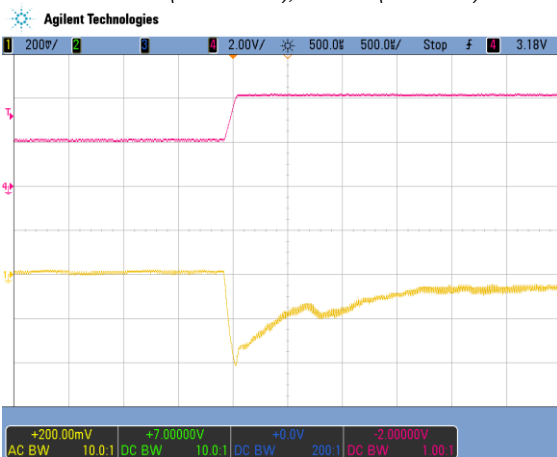*CH1: V1 (200 mV/div); CH4: I1 (100 A/div)*



*Figure 17 - Load transient V1, 122 to 244 A (500 µs/div)*
*CH1: V1 (200 mV/div); CH4: I1 (100 A/div)*



*Figure 18 - Load transient V1, 244 to 122 A (500 µs/div)*
*CH1: V1 (200 mV/div); CH4: I1 (100 A/div)*

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## 6. PROTECTION

| PARAMETER | | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $F$ | Input Fuses (L+N) | Not user accessible, quick-acting (F) | | 25 | | A |
| $V_{1\,OV}$ | OV Threshold $V_1$ | | 13.6 | 14.2 | 14.8 | VDC |
| $t_{OV\,V1}$ | OV Latch Off Time $V_1$ | | | | 1 | ms |
| $V_{SB\,OV}$ | OV Threshold $V_{SB}$ | | 13.3 | 13.9 | 14.5 | VDC |
| $t_{OV\,VSB}$ | OV Latch Off Time $V_{SB}$ | | | | 1 | ms |
| $I_{V1\,lim}$ | Current limitation | $V_1 < 180$ VAC, $T_a < 45°C$<br>$V_1 < 180$ VAC, $T_a = 55\ °C$ [4]<br>$V_1 > 180$ VAC, $T_a < 45°C$<br>$V_1 > 180$ VAC, $T_a = 55\ °C$ [4] | 120<br>92<br>248<br>186 | | 127<br>99<br>274<br>212 | A |
| $t_{V1\,lim}$ | Current limit blanking time | Time to latch off when in over current | 20 | 22 | 24 | ms |
| $I_{V1\,ol\,lim}$ | Current limit during short time overload $V_1$ | Maximum duration 20 ms | 292 | 300 | 308 | A |
| $I_{V1\,SC}$ | Max Short Circuit Current $V_1$ | $V_1 < 3$ V | | | 350 [5] | A |
| $t_{V1\,SC\,off}$ | Short circuit latch off time | Time to latch off when in short circuit | | 10 | | ms |
| $I_{VSB\,lim}$ | Current limitation $V_{SB}$ | | 6 | | 9 | A |
| $t_{VSB\,lim}$ | Current limit blanking time | Time to hit hiccup when in over current | | | 1 | ms |
| $T_{SD}$ | Over temperature on critical points | Inlet Ambient Temperature<br>PFC Primary Heatsink Temperature<br>Secondary Sync Mosfet Temperature<br>Secondary OR-ing Mosfet Temperature | | | 60<br>80<br>115<br>125 | °C |

[4]    See Figure 20 for linear derating > 45°
[5]    Limit set don't include effects of main output capacitive discharge.

### 6.1 AUTOMATIC RETRY

For all fault conditions except current limitation on Standby output, the supply will shut down for 10sec and restart automatically.  The supply will auto-restart from a fault up to 5 times, after that it will latch off.  The latch and restart counter can be cleared by recycling the input voltage or the PSON_L input. A failure on the Standby output will shut down both Main and Standby outputs.  A failure on the Main output will shut down only the Main output, while Standby continues to operate.

### 6.2 OVERVOLTAGE PROTECTION

The PFE front-ends provide a fixed threshold overvoltage (OV) protection implemented with a HW comparator. Once an OV condition has been triggered, the supply will shut down and latch the fault condition.

### 6.3 UNDERVOLTAGE DETECTION

Both main and standby outputs are monitored. LED and PWOK_L pin signal if the output voltage exceeds ±7% of its nominal voltage.
Output undervoltage protection is provided on both outputs. When either V1 or VSB falls below 93% of its nominal voltage, the output is inhibited.

## 6.4 CURRENT LIMITATION

**MAIN OUTPUT**

Two different over current protection features are implemented on the main output.
A static over current protection will shut down the output, if the output current does exceed $I_{V1\,lim}$ for more than 20 ms. If the output current is increased slowly this protection will shut down the supply. The main output current limitation level $I_{V1\,lim}$ will decrease if the ambient (inlet) temperature increases beyond 45 °C (see *Figure 20*). Note that the actual current limitation on V1 will kick in at a current level approximately 20 A higher than what is shown in *Figure 20* (see also section 9 for additional information).
The 2nd protection is a substantially rectangular output characteristic controlled by a software feedback loop. This protects the power supply and system during the 20ms blanking time of the static over current protection. If the output current is rising fast and reaches $I_{V1\,ol\,lim}$, the supply will immediately reduce its output voltage to prevent the output current from exceeding $I_{V1\,ol\,lim}$. When the output current is reduced below $I_{V1\,ol\,lim}$, the output voltage will return to its nominal value.
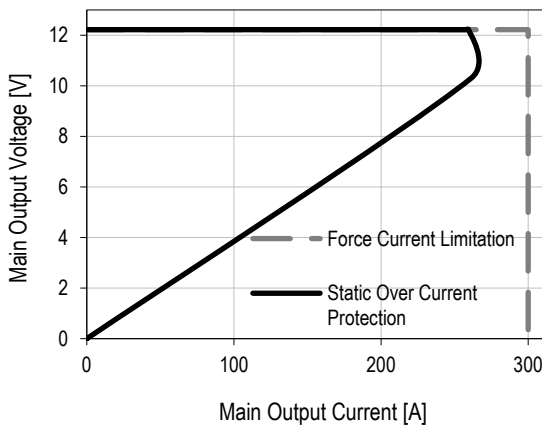


*Figure 19 - Current Limitation on V₁ (Vᵢ = 230VAC)*
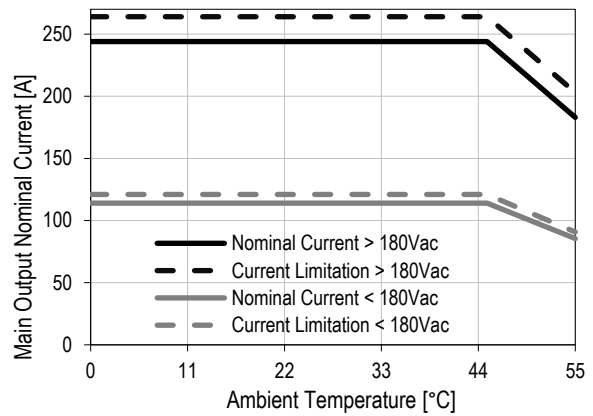


*Figure 20 - Derating on V1 vs. Ta*

**STANDBY OUTPUT**

On the standby output a hiccup type over current protection is implemented. This protection will shut down the standby output immediately when standby current reaches or exceeds $I_{VSB\,lim}$. After an off-time of 1s the output automatically tries to restart. If the overload condition is removed the output voltage will reach again its nominal value. At continuous overload condition the output will repeatedly trying to restart with 1s intervals.



*Figure 21 - Current Limitation on V_SB*

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## 7. MONITORING

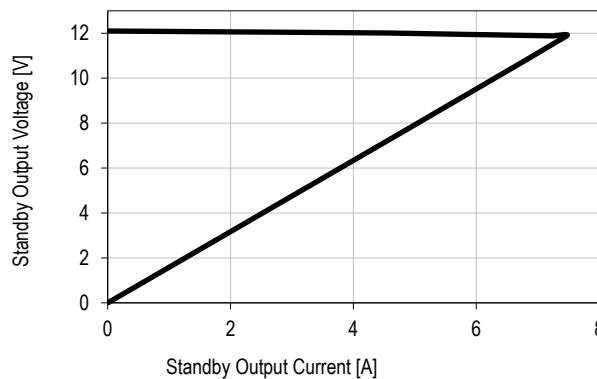| PARAMETER | | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{i\,mon}$ | Input RMS Voltage | $V_{i\,min} \leq V_i \leq V_{i\,max}$ | -2.5 | | +2.5 | % |
| $I_{i\,mon}$ | Input RMS Current | $I_i > 4\ A_{rms}$ | -5 | | +5 | % |
| | | $I_i \leq 4\ A_{rms}$ | -0.2 | | +0.2 | $A_{rms}$ |
| $P_{i\,mon}$ | True Input Power | $P_i > 700\ W$ | -5 | | +5 | % |
| | | $P_i \leq 700\ W$ | -35 | | +35 | W |
| $E_{i\,mon}$ | Total Input Energy | $P_i > 700\ W$ | -5 | | +5 | % |
| | | $P_i \leq 700\ W$ | -35 | | +35 | Wh |
| $V_{1\,mon}$ | $V_1$ Voltage | | -2 | | +2 | % |
| $I_{1\,mon}$ | $V_1$ Current | $I1 > 30\ A$ | -2 | | +2 | % |
| | | $I1 \leq 30\ A$ | -0.6 | | +0.6 | A |
| $P_{o\,nom}$ | Total Output Power | $Po > 200\ W$ | -5 | | +5 | % |
| | | $Po \leq 200\ W$ | -10 | | +10 | W |
| $E_{o\,mon}$ | Total Output Energy | $Po > 200\ W$ | -5 | | +5 | % |
| | | $Po \leq 200\ W$ | -10 | | +10 | Wh |
| $V_{SB\,mon}$ | Standby Voltage | | -2 | | +2 | % |
| $I_{SB\,mon}$ | Standby Current | $I_{SB} \leq I_{SB\,nom}$ | -0.3 | | +0.3 | A |

## 8. SIGNALING AND CONTROL

### 8.1 ELECTRICAL CHARACTERISTICS

| PARAMETER | DESCRIPTION / CONDITION | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **PSKILL / PSON_L inputs** | | | | | | |
| $V_{IL}$ | Input low level voltage | | -0.2 | | 0.8 | V |
| $V_{IH}$ | Input high level voltage | | 2.0 | | 3.6 | V |
| $I_{L, H}$ | Maximum input sink or source current | | 0 | | 1 | mA |
| $R_{puPSKILL}$ | Internal pull up resistor on PSKILL | | | 10 | | kΩ |
| $R_{puPSON\_L}$ | Internal pull up resistor on PSON_L | | | 10 | | kΩ |
| **PWOK_L output** | | | | | | |
| $V_{OL}$ | Output low level voltage | $I_{sink} < 4$ mA | -0.2 | | 0.4 | V |
| $V_{puPWOK\_L}$ | External pull up voltage | | | | 12 | V |
| $R_{puPWOK\_L}$ | Recommended external pull up resistor on PWOK_L at $V_{puPWOK\_L} = 3.3$ V | | | 10 | | kΩ |
| Low level output | All outputs are turned on and within regulation | | | | | |
| High level output | In standby mode or $V_1/V_{SB}$ have triggered a fault condition | | | | | |
| **INOK_L output** | | | | | | |
| $V_{OL}$ | Output low level voltage | $I_{sink} < 4$ mA | -0.2 | | 0.4 | V |
| $V_{puINOK\_L}$ | External pull up voltage | | | | 12 | V |
| $R_{puINOK\_L}$ | Recommended external pull up resistor on INOK_L at $V_{puINOK\_L} = 3.3$ V | | | 10 | | kΩ |
| Low level output | Input voltage is within range for PSU to operate | | | | | |
| High level output | Input voltage is not within range for PSU to operate | | | | | |
| **SMB_ALERT_L output** | | | | | | |
| $V_{OL}$ | Output low level voltage | $I_{sink} < 4$ mA | -0.2 | | 0.4 | V |
| $V_{puSMB\_ALERT\_L}$ | External pull up voltage | | | | 12 | V |
| $R_{puSMB\_ALERT\_L}$ | Recommended external pull up resistor on SMB_ALERT_L at $V_{puSMB\_ALERT\_L} = 3.3$ V | | | 10 | | kΩ |
| Low level output | PSU in warning or failure condition | | | | | |
| High level output | PSU is ok | | | | | |

### 8.2 INTERFACING WITH SIGNALS

A 15V zener diode is added on all signal pins versus signal ground SGND to protect internal circuits from negative and high positive voltage. Signal pins of several supplies running in parallel can be interconnected directly. A supply having no input power will not affect the signals of the paralleled supplies.

ISHARE pins must be interconnected without any additional components. This in-/output also has a 15 V zener diode as a protection device and is disconnected from internal circuits when the power supply is switched off.

### 8.3 FRONT LEDs

The front-end has 2 front LEDs showing the status of the supply. LED number one is green and indicates AC power is on or off, while LED number two is bi-colored: green and yellow, and indicates DC power presence or fault situations. For the position of the LEDs see *Table 3* listing the different LED status.

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| OPERATING CONDITION | LED SIGNALING |
|---|---|
| **AC LED** | |
| AC Line within range | Solid Green |
| AC Line UV condition | Off |
| **DC LED\*** | |
| Normal Operation | Solid Green |
| PSON_L High | Blinking Yellow (1:1) |
| $V_1$ or $V_{SB}$ out of regulation | |
| Over temperature shutdown | |
| Output over voltage shutdown ($V_1$ or $V_{SB}$) | Solid Yellow |
| Output under voltage shutdown ($V_1$ or $V_{SB}$) | |
| Output over current shutdown ($V_1$ or $V_{SB}$) | |
| Over temperature warning | Blinking Yellow/Green (2:1) |
| Minor fan regulation error (>5%, <15%) | Blinking Yellow/Green (1:1) |

\* The order of the criteria in the table corresponds to the testing precedence in the controller.

*Table 3 - LED Status*

## 8.4 PRESENT_L

The PRESENT_L is normally a trailing pin within the connector and will contact only once all other connector contacts are closed. This active-low pin is used to indicate to a power distribution unit controller that a supply is plugged in. The maximum sink current on PRESENT_L pin should not exceed 10 mA.
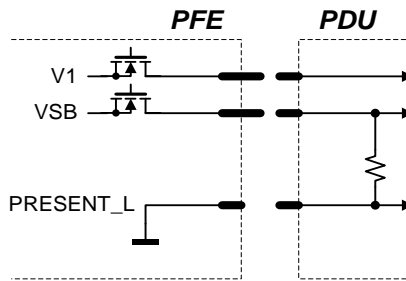


*Figure 22 - PRESENT_L signal pin*

## 8.5 PSKILL INPUT

The PSKILL input is an active-low and normally a trailing pin in the connector and is used to disconnect the main output as soon as the power supply is being plugged out. This pin should be connected to SGND in the power distribution unit. The standby output will remain on regardless of the PSKILL input state.

## 8.6 AC TURN-ON / DROP-OUTS / INOK_L

The power supply will automatically turn-on when connected to the AC line under the condition that the PSON_L signal is pulled low and the AC line is within range. The INOK_L is an open collector output that requires an external pull-up to a maximum of 12 V indicating whether the input is within the range the power supply can use and turn on. The INOK_L signal is active-low. The timing diagram is shown in *Figure 23* and referenced in Table 4.

| OPERATING CONDITION | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{AC\ VSB}$ | AC Line to 90% $V_{VSB}$ | | 3 | sec |
| $t_{AC\ V1}$ | AC Line to 90% $V_1$ | | 3 | sec |
| $t_{INOK\_L\ on1}$ | INOK_L signal on delay (start-up) | | 1800 | ms |
| $t_{INOK\_L\ on2}$ | INOK_L signal on delay (dips) | 0 | 100 | ms |
| $t_{V1\ holdup}$ | Effective $V_1$ holdup time | 12 | 300 | ms |
| $t_{VSB\ holdup}$ | Effective $V_{SB}$ holdup time | 40 | 300 | ms |
| $t_{INOK\_L\ V1}$ | INOK_L to $V_1$ holdup | 7 | | ms |
| $t_{INOK\_L\ VSB}$ | INOK_L to $V_{SB}$ holdup | 27 | | ms |
| $t_{V1\ off}$ | Minimum $V_1$ off time | 1000 | 1200 | ms |
| $t_{VSB\ off}$ | Minimum $V_{SB}$ off time | 1000 | 1200 | ms |
| $t_{V1dropout}$ | Minimum $V_1$ dropout time | 12 | | ms |
| $t_{VSBdropout}$ | Minimum $V_{SB}$ dropout time | 40 | | ms |

*Table 4 - AC Turn-on / Dip Timing*
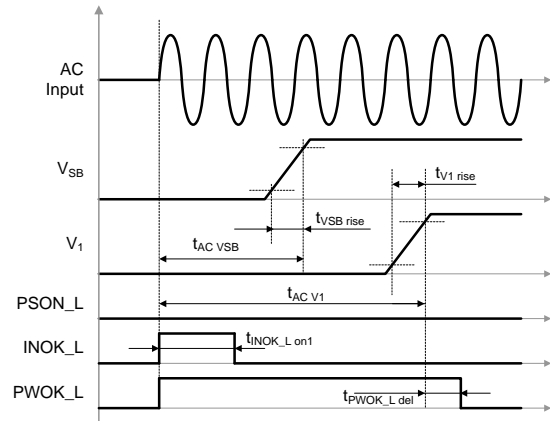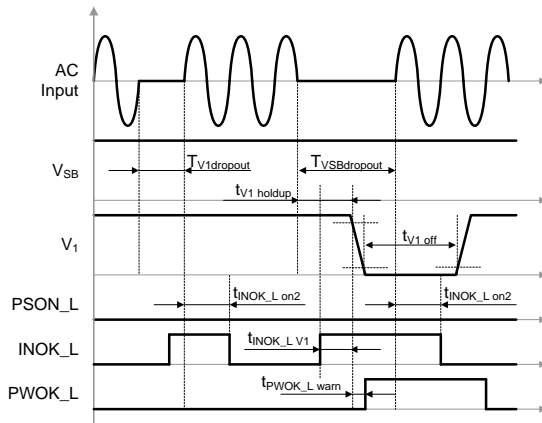


*Figure 23 - AC turn-on timing*
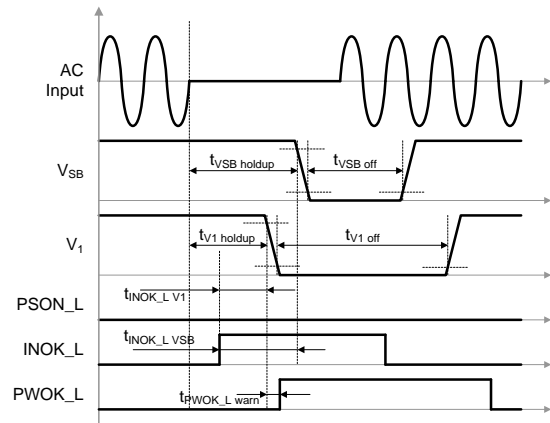


*Figure 24 - AC short dips*



*Figure 25 - AC long dips*

## 8.7  PSON_L INPUT

The PSON_L is an internally pulled-up (3.3 V) input signal to enable / disable the main output V1 of the front-end. This active-low pin is also used to clear any latched fault condition. The timing diagram is given in *Figure 26* and the parameters in *Table 5*.

| OPERATING CONDITION | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{PSON\_L\ V1on}$ | PSON_L to $V_1$ delay (on) | 190 | 220 | ms |
| $t_{PSON\_L\ V1off}$ | PSON_L to $V_1$ delay (off) | 0 | 100 | ms |

*Table 5 - PSON_L timing*

## 8.8  PWOK_L SIGNAL

The PWOK_L is an open collector output that requires an external pull-up to a maximum of 12 V indicating whether both VSB and V1 outputs are within regulation. This pin is active-low.
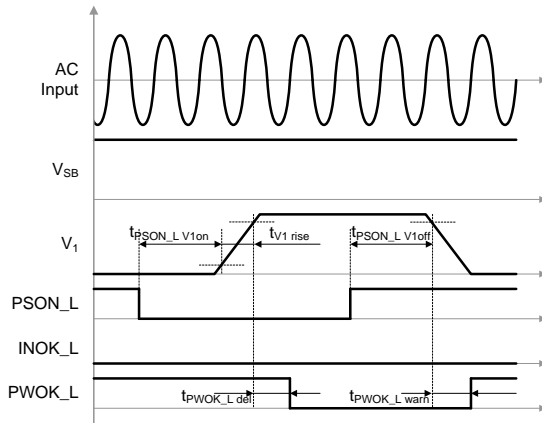The timing diagram is shown in Figure 26 and referenced in Table 6.

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Figure 26 - PSON_L turn-on/off timing

| OPERATING CONDITION | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{PWOK\_L\ del}$ | $V_1$ to PWOK_L delay (on) | 250 | 350 | ms |
| $t_{PWOK\_L\ warn}$ | $V_1$ to PWOK_L delay (off) | 0 | 5 | ms |

Table 6 - PWOK_L timing

## 8.9 CURRENT SHARE

The PFE front-ends have an active current share scheme implemented for V1. All the ISHARE current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.

The current share function uses an analog bus. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV.

The standby output uses a passive current share method (droop output voltage characteristic).

| No of paralleled PSUs | Maximum available power on main 12 V without redundancy | Maximum available power on main 12 V with n+1 redundancy | Maximum available power on standby output |
|---|---|---|---|
| 1 | 3000 W | - | 60 W |
| 2 | 5850 W | 3000 W | 60 W |
| 3 | 8700 W | 5850 W | 60 W |
| 4 | 11550 W | 8700 W | 60 W |
| 5 | 14400 W | 11550 W | 60 W |
| 6 | 17250 W | 14400 W | 60 W |

Table 7 - Power available when PSU in redundant operation

## 8.10    SENSE INPUTS

Main output has sense lines implemented to compensate for voltage drop on load wires. The maximum allowed voltage drop is 200 mV on the positive rail and 100 mV on the PGND rail.

With open sense inputs the main output voltage will rise by 250 mV. Therefore, if not used, these inputs should be connected to the power output and PGND close to the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

## 8.11    I2C / PMBus® COMMUNICATION

The interface driver in the PFE supply is referenced to the SGND. The PFE supply is a communication slave device only; it never initiates messages on the I[2]C bus by itself. The communication bus voltage and timing is defined in Table 8 and further characterized through:

# PFE3000-12-069RA

- There are 100 kΩ internal pull-up resistors
- The SDA/SCL IOs must be pull-up externally to 3.3 ± 0.3 V
- Pull-up resistor should be 2 – 5 kΩ to ensure SMBUS compliant signal rise times
- I²C clock speed up to 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
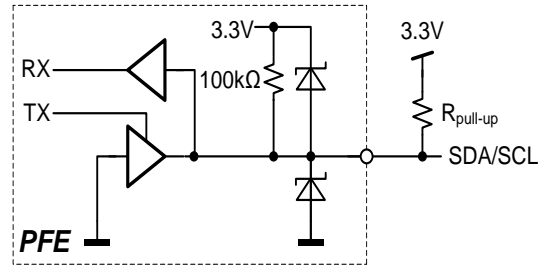- Recognizes any time Start/Stop bus conditions

*Figure 27 - Physical layer of communication interface*

The SMB_ALERT_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events.

Communication to the DSP or the EEPROM will be possible as long as the input AC (DC) voltage is provided. If no AC (DC) is present, communication to the unit is possible as long as it is connected to a live VSB output (provided e.g. by the redundant unit). If only V1 is provided, communication is not possible.

| PARAMETER | DESCRIPTION | CONDITION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{iL}$ | Input low voltage | | -0.2 | 0.4 | V |
| $V_{iH}$ | Input high voltage | | 2.1 | 3.6 | V |
| $V_{hys}$ | Input hysteresis | | 0.15 | | V |
| $V_{oL}$ | Output low voltage | 4 mA sink current | 0 | 0.4 | V |
| $t_r$ | Rise time for SDA and SCL | | $20+0.1C_b$* | 300 | ns |
| $t_{of}$ | Output fall time ViHmin → ViLmax | 10 pF < $C_b$* < 400 pF | $20+0.1C_b$* | 250 | ns |
| $I_i$ | Input current SCL/SDA | 0.1 VDD < Vi < 0.9 VDD | -10 | 10 | µA |
| $C_i$ | Capacitance for each SCL/SDA | | | 10 | pF |
| $f_{SCL}$ | SCL clock frequency | | 0 | 100 | kHz |
| $R_{pu}$ | External pull-up resistor | $f_{SCL}$ ≤ 100 kHz | | 1000 ns / $C_b$* | Ω |
| $t_{HDSTA}$ | Hold time (repeated) START | $f_{SCL}$ ≤ 100 kHz | 4.0 | | µs |
| $t_{LOW}$ | Low period of the SCL clock | $f_{SCL}$ ≤ 100 kHz | 4.7 | | µs |
| $t_{HIGH}$ | High period of the SCL clock | $f_{SCL}$ ≤ 100 kHz | 4.0 | | µs |
| $t_{SUSTA}$ | Setup time for a repeated START | $f_{SCL}$ ≤ 100 kHz | 4.7 | | µs |
| $t_{HDDAT}$ | Data hold time | $f_{SCL}$ ≤ 100 kHz | 0 | 3.45 | µs |
| $t_{SUDAT}$ | Data setup time | $f_{SCL}$ ≤ 100 kHz | 250 | | ns |
| $t_{SUSTO}$ | Setup time for STOP condition | $f_{SCL}$ ≤ 100 kHz | 4.0 | | µs |
| $t_{BUF}$ | Bus free time between STOP and START | $f_{SCL}$ ≤ 100 kHz | 4.7 | | µs |
| **EEPROM_WP** | | | | | |
| $V_{iL}$ | Input low voltage | | -0.2 | 0.4 | V |
| $V_{iH}$ | Input high voltage | | 2.1 | 3.6 | V |
| $I_i$ | Input sink or source current | | -1 | 1 | mA |
| $R_{pu}$ | Internal pull-up resistor to 3.3V | | 10k | | Ω |

\* Cb = Capacitance of bus line in pF, typically in the range of 10…400 pF

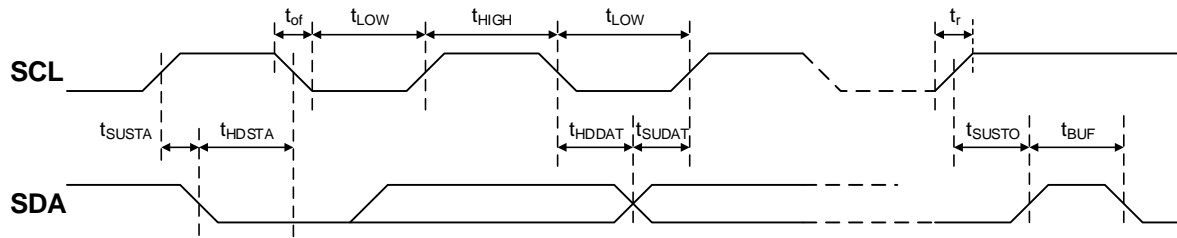*Table 8 - I²C / SMBus Specification*

*Figure 28 - I²C / SMBus Timing*

## 8.12 ADDRESS

The supply supports PMBus® communication protocol, address for PMBus® communication is at fixed to 0x20. The EEPROM is at fixed address = 0xA0.

## 8.13 CONTROLLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I²C bus physical layer (see *Figure 29*). In order to write to the EEPROM, the write protection needs to be disabled by setting EEPROM_WP input correctly.

If EEPROM_WP is High, write is not allowed to the EEPROM and if Low, write is allowed. The EEPROM provides 2k bytes of user memory. None of the bytes are used for the operation of the power supply.
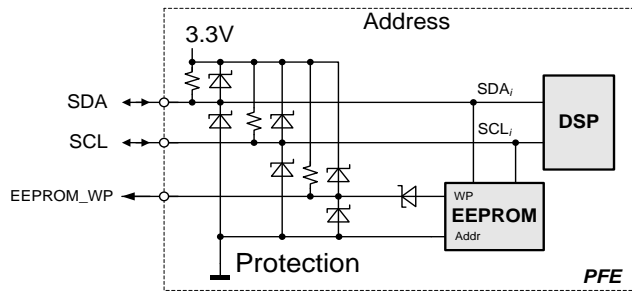


*Figure 29 - I²C Bus to DSP and EEPROM*

## 8.14 EEPROM PROTOCOL

The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.
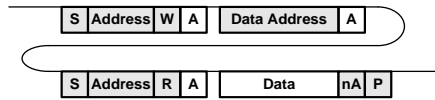
### WRITE

The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.

| S | Address | W | A | Data Address | A | Data | A | P |
|---|---------|---|---|--------------|---|------|---|---|

### READ

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.

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+86 755 298 85888

**Europe, Middle East**
+353 61 225 977

**North America**
+1 408 785 5200

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```
S | Address | W | A | Data Address | A
S | Address | R | A | Data | nA | P
```

## 8.15    PMBus® PROTOCOL

The Power Management Bus (PMBus®) is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at: www.powerSIG.org.

PMBus® command codes are not register addresses. They describe a specific command to be executed. PFE3000-12-069RA supply supports the following basic command structures:

- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

**WRITE**
The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).
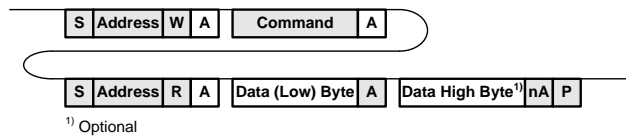
```
S | Address | W | A | Command | A
Data Low Byte1) | A | Data High Byte1) | A | P
```
1) Optional
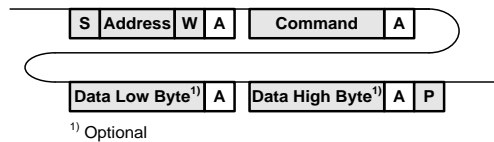
In addition, Block write commands are supported with a total maximum length of 255 bytes. See PFE3000-12-069RA PMBus® Communication Manual BCA.00070 for further information.

```
S | Address | W | A | Command | A | Byte Count | A
Byte 1 | A | --------- | Byte N | A | P
```
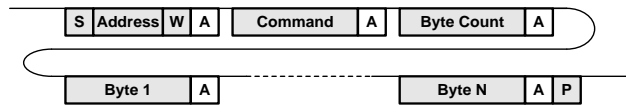
**READ**
The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.

```
S | Address | W | A | Command | A
S | Address | R | A | Data (Low) Byte | A | Data High Byte1) | nA | P
```
1) Optional

In addition, Block read commands are supported with a total maximum length of 255 bytes. See PFE3000-12-069RA PMBus® Communication Manual BCA.00070 for further information.
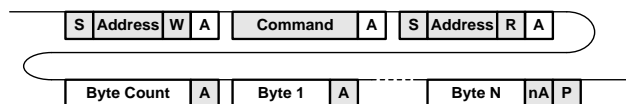
```
S | Address | W | A | Command | A | S | Address | R | A
Byte Count | A | Byte 1 | A | --- | Byte N | nA | P
```

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## 8.16    GRAPHICAL USER INTERFACE

Bel Power Solutions I²C Utility provides a Windows® Vista/Win7/8 compatible graphical user interface allowing the programming and monitoring of the PFE3000-12-069RA Front-End. The utility can be downloaded on belfuse.com/power-solutions and supports the PMBus® protocol.

The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.

If the GUI is used in conjunction with the PFE3000-12-069RA Evaluation Kit it is also possible to control the PSON_L pin(s) of the power supply.
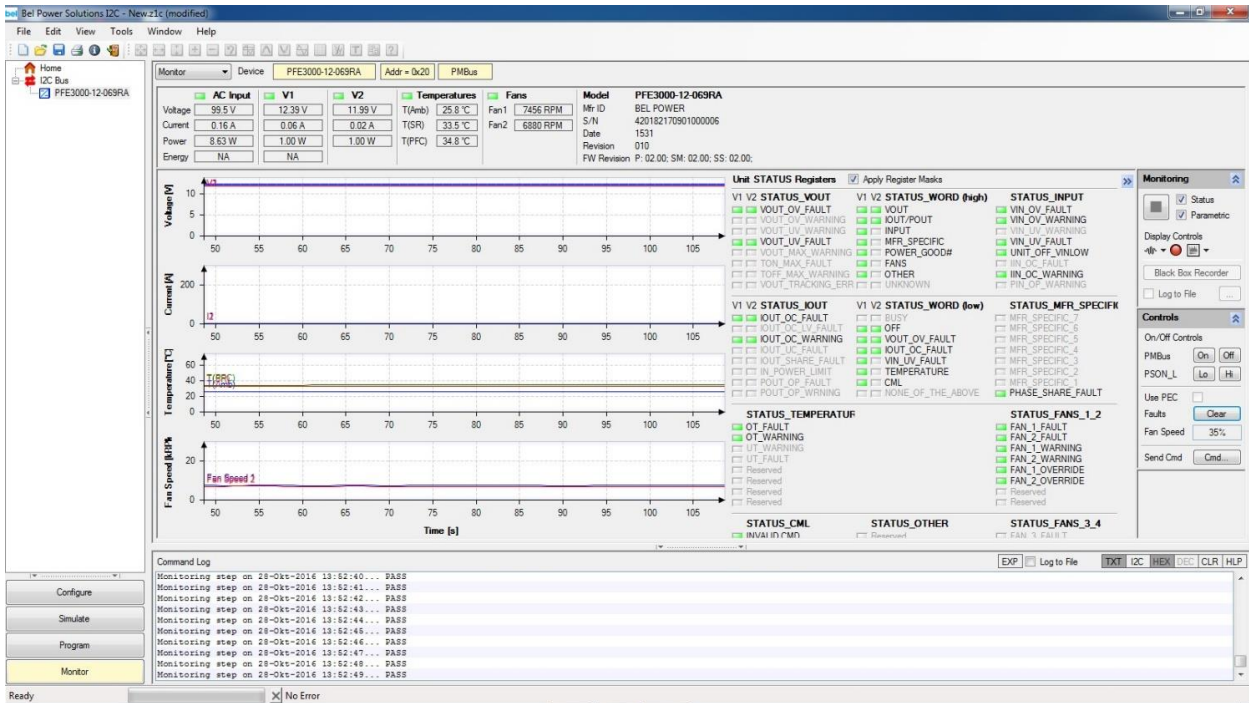


*Figure 30 - Monitoring dialog of the I2C Utility*

## 9.    TEMPERATURE AND FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the airflow at the rear of the supply by placing large objects directly at the output connector. The PFE3000-12-069RA is provided with a reverse airflow, which means the air enters through the front of the supply and leaves at the rear. PFE supplies have been designed for horizontal operation.

The fan inside of the supply is controlled by a microprocessor. The rpm of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.
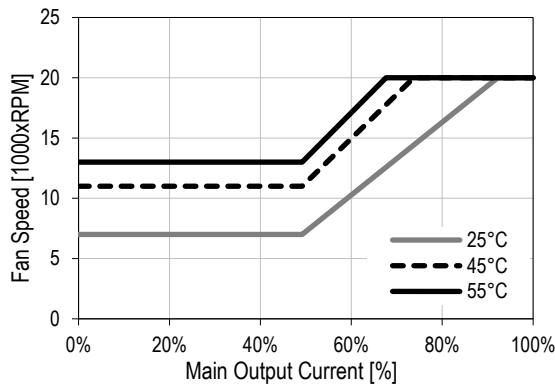


*Figure 31 - Airflow Direction*

| Asia-Pacific | Europe, Middle East | North America |
|---|---|---|
| +86 755 298 85888 | +353 61 225 977 | +1 408 785 5200 |

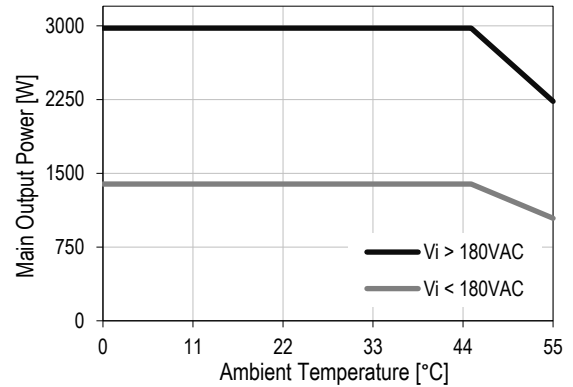Figure 32 - Fan speed vs. main output load for PFE3000-12-069RA



Figure 33 - Thermal derating for PFE3000-12-069RA

## 10. ELECTROMAGNETIC COMPATIBILITY

### 10.1    IMMUNITY

**NOTE:** Most of the immunity requirements are derived from EN 55024:1998/A2:2003.

| PARAMETER | DESCRIPTION / CONDITION | CRITERION |
|---|---|---|
| ESD Contact Discharge | IEC / EN 61000-4-2, ±8 kV, 25+25 discharges per test point (metallic case, LEDs, connector body) | A |
| ESD Air Discharge | IEC / EN 61000-4-2, ±15 kV, 25+25 discharges per test point (non-metallic user accessible surfaces) | A |
| Radiated Electromagnetic Field | IEC / EN 61000-4-3, 10 V/m, 1 kHz/80% Amplitude Modulation, 1 μs Pulse Modulation, 10 kHz…2 GHz | A |
| Burst | IEC / EN 61000-4-4, level 3 AC port ±2 kV, 1 minute DC port ±1 kV, 1 minute | A |
| Surge | IEC / EN 61000-4-5 Line to earth: level 3, ±2 kV Line to line: level 2, ±1 kV | A |
| RF Conducted Immunity | IEC/EN 61000-4-6, Level 3, 10 Vrms, CW, 0.1 … 80 MHz | A |
| Voltage Dips and Interruptions | IEC/EN 61000-4-11 1: Vi 230Volts,  100% Load,  Dip 100%, Duration 12ms 2: Vi 230Volts, 100% Load, Dip 100%, Duration < 150 ms 3. Vi 230Volts, 100% Load, Dip 100%, Duration > 150 ms | A V1: B, VSB: A B |

### 10.2    EMISSION

| PARAMETER | DESCRIPTION / CONDITION | CRITERION |
|---|---|---|
| Conducted Emission | EN55022 / CISPR 22: 0.15 … 30 MHz, QP and AVG | Class A |
| Radiated Emission | EN55022 / CISPR 22: 30 MHz … 1 GHz, QP | Class A |
| Harmonic Emissions | IEC61000-3-2, Vin = 115/230 VAC, 50 Hz, 100% Load | Class A |
| Acoustical Noise | Sound power statistical declaration (ISO 9296, ISO 7779, IS9295) @ 50% load | 60 dBA |
| AC Flicker | IEC / EN 61000-3-3, $d_{max}$ < 3.3% | PASS |

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## 11. SAFETY / APPROVALS

Maximum electric strength testing is performed in the factory according to IEC/EN 60950, and UL 60950. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

| | PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Agency Approvals | Approved to the latest edition of the following standards:<br>• IEC60950-1 2nd edition (CB)<br>• EN60950-1 2nd Edition (Nemko)<br>• UL/CSA0950-1 2nd Edition (cCSAus)<br>• CNS14336-1, CNS13438 (BSMI)<br>• EAC, TR-CU (Russia)<br>• BIS, (India)<br>• KCC Safety/EMC, (South Korea) | | | | |
| | Isolation Strength | Input (L/N) to case (PE)<br>Input (L/N) to output<br>Output to case (PE) | | Basic<br>Reinforced<br>Functional | | |
| $d_C$ | Creepage / Clearance | Primary (L/N) to protective earth (PE)<br>Primary to secondary | | | | |
| | Electrical Strength Test | Input to case<br>Input to output (tested by manufacturer only) | 2121<br>4242 | | | VDC |

## 12. ENVIRONMENTAL

| | PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $T_A$ | Ambient Temperature | $V_{i\,min}$ to $V_{i\,max}$, $I_{i\,nom}$, $I_{SB\,nom}$ at 4000 m | 0 | | +35 | °C |
| | | $V_{i\,min}$ to $V_{i\,max}$, $I_{i\,nom}$, $I_{SB\,nom}$ at 1800 m | 0 | | +45 | °C |
| $T_{Aext}$ | Extended Temp. Range | Derated output (see *Figure 20* and *Figure 33*) at 1800 m | +45 | | +55 | °C |
| $T_S$ | Storage Temperature | Non-operational | -40 | | +70 | °C |
| | Altitude | Operational, above Sea Level (see derating) | - | | 4000 | m |
| $N_a$ | Audible Noise | $V_{i\,nom}$, 50% $I_{o\,nom}$, $T_A = 25°C$ | | 60 | | dBA |
| | Cooling | System Back Pressure | | | 0.5 | in-H$_2$0 |

## 13. MECHANICAL

| | PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Dimensions | Width | | 69 | | mm |
| | | Heigth | | 42 | | mm |
| | | Depth | | 555 | | mm |
| $m$ | Weight | | | 2.60 | | kg |

**NOTE:** A 3D step file of the power supply casing is available on request.

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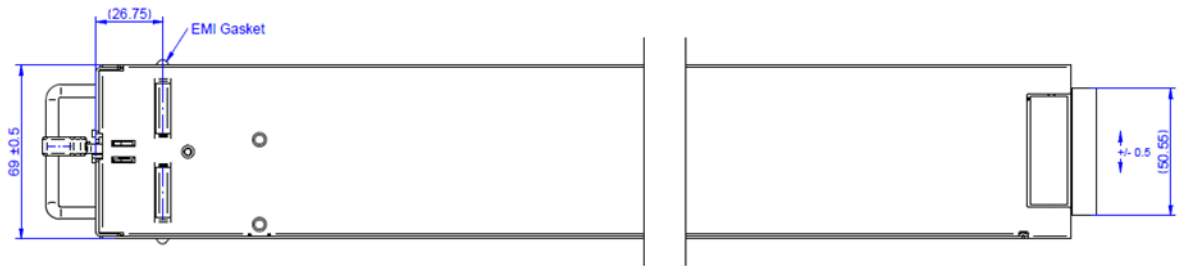| Asia-Pacific | Europe, Middle East | North America |
|---|---|---|
| +86 755 298 85888 | +353 61 225 977 | +1 408 785 5200 |

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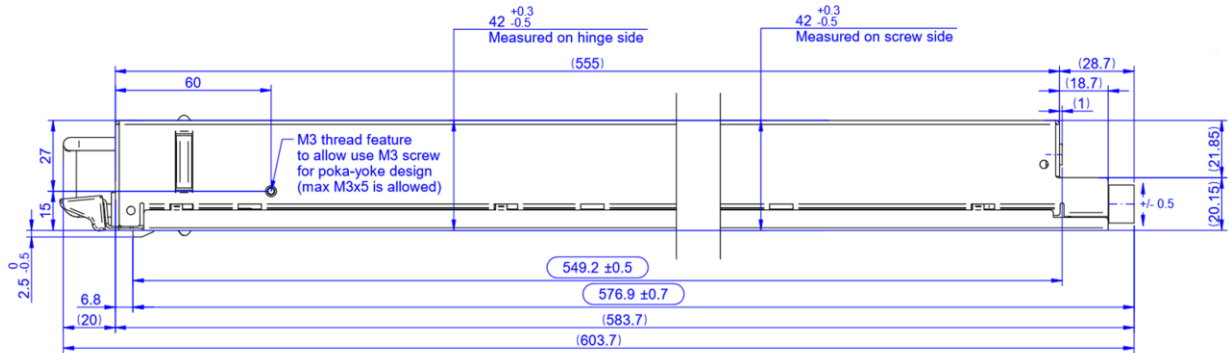
*Figure 34 - Bottom view*
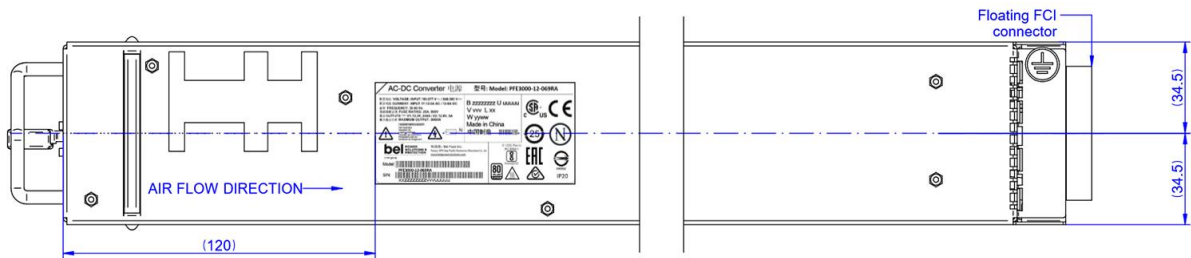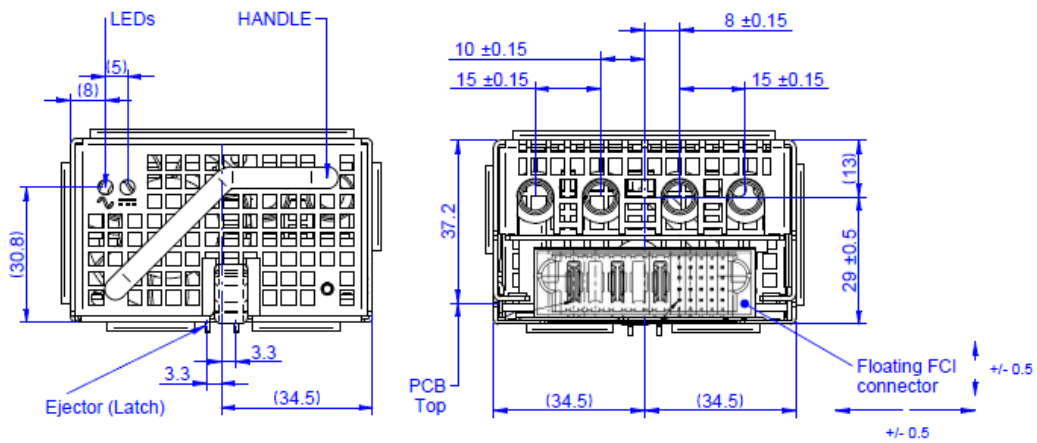
*Figure 35 - Side view*

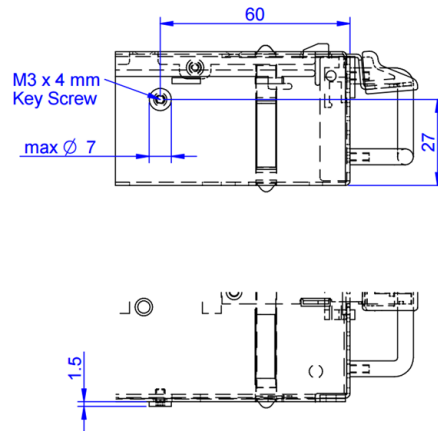*Figure 36 - Top view*

*Figure 37 - Front and Rear view*

*Figure 38 - PFE3000-12-069RA with Key-in screw dimension (Option code S366)*



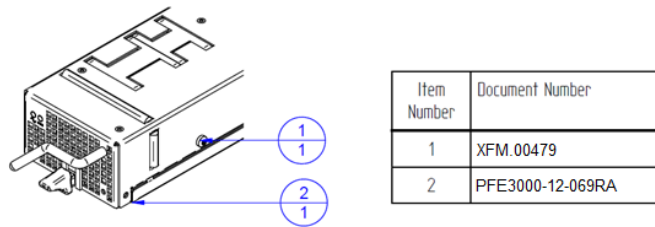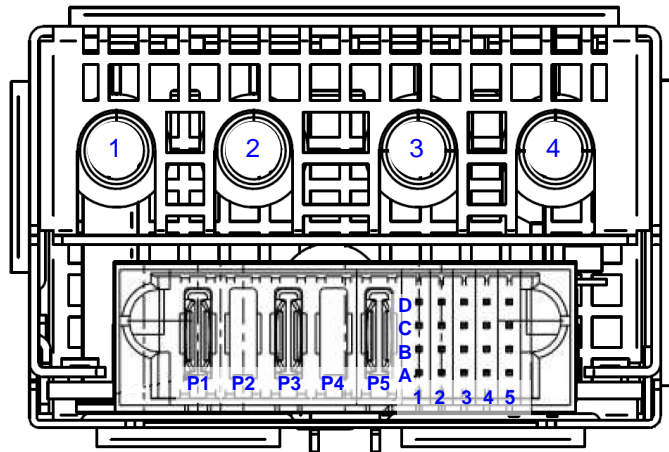| Item Number | Document Number |
|---|---|
| 1 | XFM.00479 |
| 2 | PFE3000-12-069RA |

*Figure 39 - PFE3000-12-069RA with Key-in screw (Option code S366)*

## 14. CONNECTORS



Unit:          FCI Connectors P/N 51939-768LF
Counterpart: FCI Connectors P/N 51915-401LF
                  For Main Output Pins, see section 15
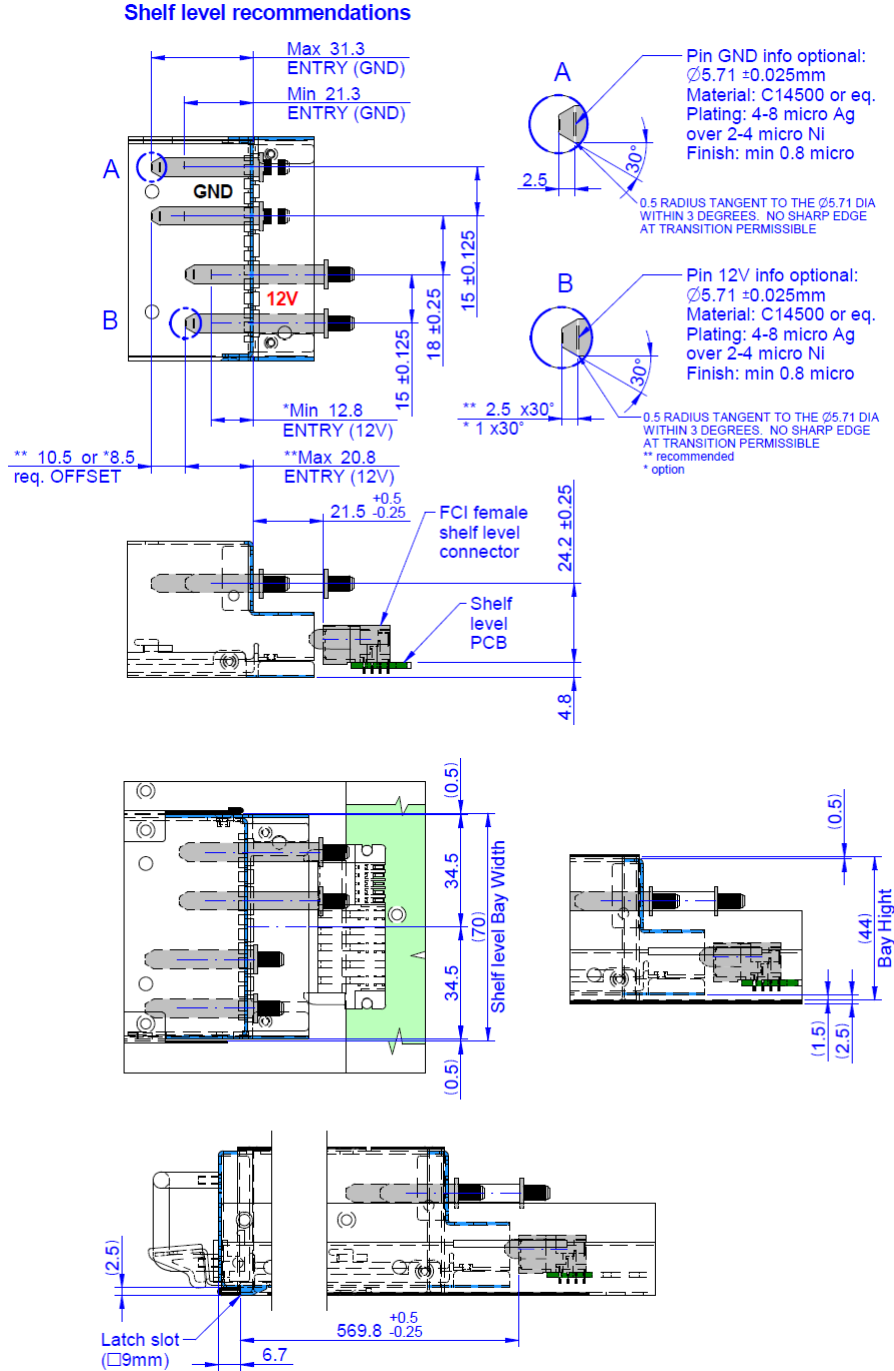
Note: A1 and A2 are Trailing Pin (short pins)

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| PIN | NAME | DESCRIPTION |
|------|------|-------------|
| *Output* | | |
| 3,4 | V1 | +12 VDC main output |
| 1,2 | PGND | +12 VDC main output ground |
| *Input Pins* | | |
| P1 | LIVE | AC Live Pin |
| P2 | N.C | No metal pin connection |
| P3 | NEUTRAL | AC Neutral Pin |
| P4 | N.C. | No metal pin connection |
| P5 | P.E. | Protective Earth Pin |
| *Control Pins* | | |
| A1 | PSKILL | Power supply kill (trailing pin): active-high |
| B1 | PWOK_L | Power OK signal output: active-low |
| C1 | INOK_L | Input OK signal: active-low |
| D1 | PSON_L | Power supply on input: active-low |
| A2 | PRESENT_L | Power supply present (trailing pin): active-low |
| B2 | SGND | Signal ground* (return) |
| C2 | SGND | Signal ground* (return) |
| D2 | SGND | Signal ground* (return) |
| A3 | SCL | I²C clock signal line |
| B3 | SDA | I²C data signal line |
| C3 | SMB_ALERT_L | SMB Alert signal output: active-low |
| D3 | ISHARE | $V_1$ Current share bus |
| A4 | EEPROM_WP | EEPROM write protect |
| B4 | RESERVED | Reserved |
| C4 | V1_SENSE_R | Main output negative sense |
| D4 | V1_SENSE | Main output positive sense |
| A5 | VSB | Standby positive output |
| B5 | VSB | Standby positive output |
| C5 | VSB_GND | Standby Ground* |
| D5 | VSB_GND | Standby Ground* |

* These pins should be connected to PGND on the system. See Section 8 for pull up resistor settings of signal pins.
All signal pins are referred to SGND

*Table 9 – Pin assignment*

## 15. SHELF LEVEL CONFIGURATION (PROVISIONAL)

The recommended pin configuration below is based on company's own Shelf design and provided here as reference. Customer pin lengths within the range indicated is acceptable.

**Shelf level recommendations**



Pin GND info optional:
⌀5.71 ±0.025mm
Material: C14500 or eq.
Plating: 4-8 micro Ag
over 2-4 micro Ni
Finish: min 0.8 micro

0.5 RADIUS TANGENT TO THE ⌀5.71 DIA
WITHIN 3 DEGREES.  NO SHARP EDGE
AT TRANSITION PERMISSIBLE

Pin 12V info optional:
⌀5.71 ±0.025mm
Material: C14500 or eq.
Plating: 4-8 micro Ag
over 2-4 micro Ni
Finish: min 0.8 micro

0.5 RADIUS TANGENT TO THE ⌀5.71 DIA
WITHIN 3 DEGREES.  NO SHARP EDGE
AT TRANSITION PERMISSIBLE
** recommended
* option

## 16. ACCESSORIES

| ITEM | DESCRIPTION | ORDERING PN | SOURCE |
|---|---|---|---|
| | **I²C Utility** Windows Vista/7/8 compatible GUI to program, control and monitor PFE Front-Ends (and other I²C units) | N/A | belfuse.com/power-solutions |
| | **Single Connector Board** Connector board to operate PFE3000-12-069RA unit. Includes an on-board USB to I²C converter (use I²C Utility as desktop software). | YTM.U0M00.0 | Bel Power Solutions |
| | **AC Can Filter** Recommended AC can filter used on system side. | C20F.0011 20GENG3E-R | Schurter Inc. Delta Electronics |
| | **Key-in Screw** Screw for PSU Orientation. | XFM.00479 | Focus Metal |

## 17. REVISION HISTORY

| REV | DESCRIPTION | PSU PRODUCT VERSION | DATE | AUTHOR |
|---|---|---|---|---|
| AA | Initial Release of Datasheet. | V001<br>V004<br>V007 | 11-27-2013 | GS |
| AB | ▪ Handle position and size has changed to a diagonal format to allow better handling/grip.<br>▪ +12VSB turn-on delay is changed from 2 seconds to 3 seconds. Main output will only turn on (if enabled by PSKILL and PSON) once +12VSB is in regulation.<br>▪ Datasheet format was changed to Bel Power Solution. | V008 | 10-22-2014 | GS |
| AC | ▪ Added option code model in ordering information.<br>▪ S101 denotes Screw for Key-in feature is added. | V009 | 12-22-2014 | GS |
| AD | ▪ +12VSB parameter change in output ripple voltage, droop, and current read back accuracy.<br>▪ PSU Fans is supplied only from Internal Auxiliary.<br>▪ Option code is changed from S101 to S366.<br>▪ Added Revision History. | V010 | 09-09-2015 | GS |
| AE | ▪ PSU Revision on product label was incremented due to internal documentation.<br>▪ Clarification on Dynamic Load Regulation, Mechanical Drawing and Key-in Screw accessory for option code S366. | V011 | 10-28-2016 | GS |
| AE | ▪ Passed EAC certification and added EAC logo on product label. | V204 | 04-06-2017 | GS |
| AF | ▪ PSKILL and SMB_ALERT_L pin active state description on section 14 was corrected but no functional change.<br>▪ PSU firmware was updated to support calibration of MFR Model suffix.<br>▪ Passed BIS certification and added BIS logo on product label.<br>▪ Transfer 80plus platinum logo on product label.<br>▪ Mechanical update on section 13 for PSU height tolerance. | V205 | 05-09-2017 | GS |
| AF1 | ▪ Mechanical update on section 13.<br>PSU height tolerance on hinge side was adjusted to 42 +0.3/-0.5mm.<br>Removed "80plus optional coloured label" on PSU drawing. | V205 | 08-14-2017 | GS |
|  | ▪ PSU firmware was updated to improve I2C during hot plug. | V206 | 11-28-2017 | GS |
| AG | ▪ Passed KCC certification and added KCC logo on product label.<br>▪ PMBus™ changed to PMBus®; a disclaimer added to the first page: Disclaimer: PMBus is a registered trademark of SMIF, Inc.<br>▪ Figure 28. I$^2$C / SMBus Timing updated | V207 | 01-09-2018 | GS |

## For more information on these products consult: tech.support@psbel.com

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