Datasheet

Operational Amplifier

Low Noise, Low Input Offset Voltage CMOS Operational Amplifier

LMR1802G-LB

General Description

This is the product guarantees long time support in Industrial market. And it is suitable for usage of industrial applications.

LMR1802G-LB precision single CMOS operational amplifier features low noise, low input offset voltage and low input bias current that are suitable for equipment operating from battery power and using sensors that an amplifier.

Features

- Long Time Support Product for Industrial Applications.
- Low Input-Referred Noise Voltage Density
- Driving High Capacitive Load
- Full-Swing Output

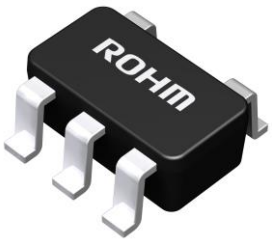
Applications

- Industrial Equipment
- Sensor Amplifiers
- Battery-powered Equipment
- Current Monitoring Amplifier
- ADC front ends, Buffer Amplifier
- Photodiode Amplifier
- Amplifiers

Key Specifications

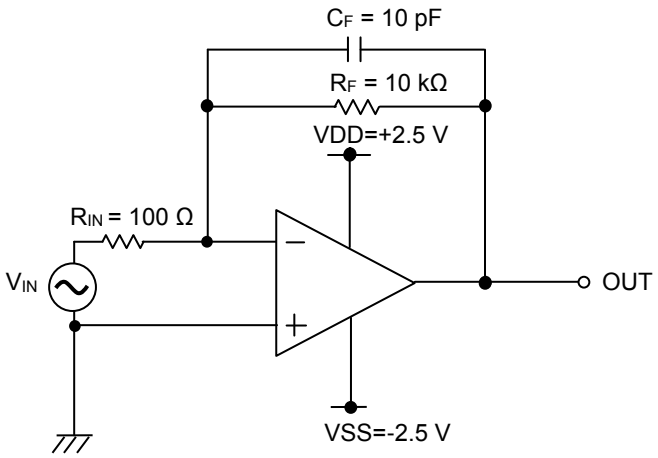
- Input Offset Voltage: 5 μV(Typ)
- Input Referred Noise Voltage Density
  - f=10Hz: 7.8 nV/√Hz(Typ)
  - f=1kHz: 2.9 nV/√Hz(Typ)
- Input Common Mode Voltage Range: V_{SS} to V_{DD}-1.0 V
- Input Bias Current: 0.5 pA(Typ)
- Operating Supply Voltage Range
  - Single Supply: 2.5 V to 5.5 V
  - Dual Supply: ±1.25 V to ±2.75 V
- Operating Temperature Range: -40 °C to +125 °C

Package	W(Typ) x D(Typ) x H(Max)
SSOP5	2.90 mm x 2.80 mm x 1.25 mm



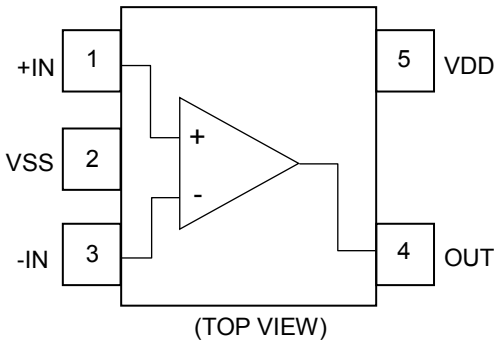
SSOP5

Typical Application Circuit



$$V_{OUT} = -\frac{R_f}{R_{IN}} V_{IN}$$

Pin Configuration

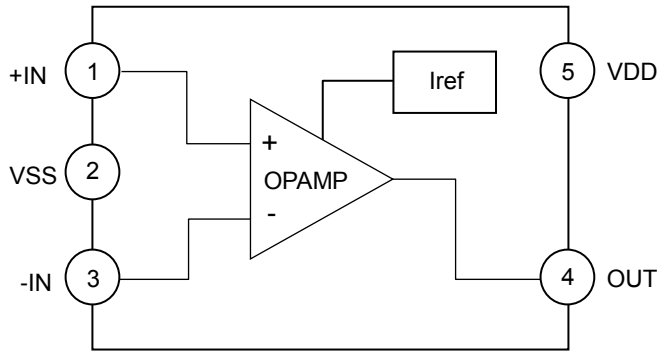


(TOP VIEW)

Pin Description

Pin No.	Pin Name	Function
1	+IN	Non-inverting input
2	VSS	Negative power supply / Ground
3	-IN	Inverting input
4	OUT	Output
5	VDD	Positive power supply

Block Diagram



Description of Blocks

1. OPAMP:
   This block includes a full-swing output operational amplifier with class-AB output circuit and low-noise-ground-sense differential input stage.

2. Iref:
   This block supplies reference current to operate OPAMP block.

Absolute Maximum Ratings (Ta=25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}-V_{SS}	7.0	V
Differential Input Voltage(Note 1)	V_{ID}	V_{DD} - V_{SS}	V
Common-mode Input Voltage Range	V_{ICMR}	(V_{SS} - 0.3) to (V_{DD} + 0.3)	V
Input Current	I_I	±10	mA
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	- 55 to + 150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) The differential input voltage indicates the voltage difference between inverting input and non-inverting input. The input pin voltage is set to V_{SS} or more.

Thermal Resistance(Note 2)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 4)	2s2p(Note 5)	
SSOP5				
Junction to Ambient	θ_{JA}	376.5	185.4	°C/W
Junction to Top Characterization Parameter(Note 3)	Ψ_{JT}	40	30	°C/W

(Note 2) Based on JESD51-2A(Still-Air).
(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 4) Using a PCB board based on JESD51-3.
(Note 5) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage	V_{DD}	2.5 ±1.25	5.0 ±2.5	5.5 ±2.75	V
Operating Temperature	Topr	-40	+25	+125	°C

Electrical Characteristics (Unless otherwise specified V_{DD}=5 V, V_{SS}=0 V, Ta=25 °C)

Parameter	Symbol	Temperature Range	Limit			Unit	Conditions
			Min	Typ	Max		
Input Offset Voltage *(Note 1,2)*	V_{IO}	25 °C	-	5	450	μV	-
		Full range	-	-	500		-
Input Offset Voltage Temperature Drift*(Note 1,2)*	$\Delta V_{IO}/\Delta T$	Full range	-	0.4	-	μV/°C	-
Input Offset Current *(Note 1)*	I_{IO}	25 °C	-	0.5	-	pA	-
Input Bias Current*(Note 1,2)*	I_B	25 °C	-	0.5	220.0	pA	-
		Full range	-	-	3000		
Supply Current*(Note 2)*	I_{DD}	25 °C	-	1100	1450	μA	R_L=∞, G=0 dB
		Full range	-	-	1500		
Output Voltage High	V_{OH}	25 °C	-	7	50	mV	R_L=10 kΩ, V_{OH}=V_{DD}-V_{OUT}
Output Voltage Low	V_{OL}	25 °C	-	5	50	mV	R_L=10 kΩ
Large Signal Voltage Gain *(Note 2)*	A_V	25 °C	120	140	-	dB	R_L=10 kΩ
		Full range	100	-	-		
Common-mode Input Voltage Range	V_{ICMR}	25 °C	0	-	4	V	V_{SS} to V_{DD}-1.0 V
Common-mode Rejection Ratio	CMRR	25 °C	85	105	-	dB	-
Power Supply Rejection Ratio	PSRR	25 °C	90	125	-	dB	-
Output Source Current*(Note 1,3)*	I_{OH}	25 °C	2.0	3.5	-	mA	V_{OUT}=V_{DD}-0.1 V
			25	50	-		V_{OUT}=V_{SS}
Output Sink Current*(Note 1,3)*	I_{OL}	25 °C	3	9	-	mA	V_{OUT}=V_{SS}+0.1 V
			25	50	-		V_{OUT}=V_{DD}
Slew Rate	SR	25 °C	-	1.1	-	V/μs	C_L=25 pF
Gain Bandwidth Product	GBW	25 °C	-	3	-	MHz	G=40 dB
Phase Margin	θ	25 °C	-	68	-	deg	G=40 dB
Gain Margin	Gm	25 °C	-	12	-	dB	-
Input-Referred Noise Voltage Density	Vn	25 °C	-	7.8	-	nV/√Hz	f=10 Hz
			-	2.9	-		f=1 kHz
Total Harmonic Distortion + Noise	THD+N	25 °C	-	0.0035	-	%	V_{OUT}=4 V_{P-P}, f=1 kHz, LPF=80 kHz

(Note 1) Absolute value

(Note 2) Full range: Ta=-40 °C to +125 °C

(Note 3) Consider the power dissipation of the IC under high temperature environment when selecting the output current value.
When the output pins are short-circuited continuously, the output current may decrease due to the temperature rise by the heat generation of inside the IC.

Description of Terms in Electrical Characteristics

Described below are descriptions of the relevant electrical terms used in this datasheet. Items and symbols generally used are also shown. Note that item names and symbols, and their meanings may differ from those on another manufacturer's or general documents.

1. Absolute Maximum Ratings

Absolute maximum rating items indicates the condition which must not be exceeded even if it is instantaneous. Applying of a voltage exceeding the absolute maximum ratings or use outside the temperature range which is provided in the absolute maximum ratings cause characteristic deterioration or destruction of the IC.

1.1 Supply Voltage (V_{DD}-V_{SS})
This indicates the maximum voltage that can be applied between the positive power supply pin and the negative power supply pin without deteriorating the characteristics of internal circuit or without destroying it.

1.2 Differential Input Voltage (V_{ID})
This indicates the maximum voltage that can be applied between the non-inverting input pin and the inverting input pin without deteriorating the characteristics of the IC or without destroying it.

1.3 Common-mode Input Voltage Range (V_{ICM})
This indicates the maximum voltage that can be applied to the non-inverting input pin and inverting input pin without deteriorating the characteristics of the IC or without destroying it. Common-mode Input Voltage Range of the maximum ratings does not assure normal operation of IC. For normal operation, use the IC within the Common-mode Input Voltage Range characteristics.

2. Electrical Characteristics

2.1 Input Offset Voltage (V_{IO})
This indicates the voltage difference between non-inverting and inverting pins. It can be translated as the input voltage difference required for setting the output voltage at 0 V.

2.2 Input Offset Voltage Temperature Drift ($\Delta V_{IO}/\Delta T$)
Denotes the ratio of the input offset voltage fluctuation to the ambient temperature fluctuation.

2.3 Input Offset Current (I_{IO})
This indicates the difference of input bias current between the non-inverting and inverting pins.

2.4 Input Bias Current (I_B)
This indicates the current that flows into or out from the input pin. It is defined by the average of input bias currents at the non-inverting and inverting pins.

2.5 Supply Current (I_{DD})
This indicates the current of the IC itself flowing under the specified conditions and under no-load or steady-state conditions.

2.6 Output Voltage High / Output Voltage Low (V_{OH}/V_{OL})
This indicates the voltage range of the output under specified load condition. It is divided into output voltage High and low. Output voltage high indicates the upper limit of output voltage. Output voltage low indicates the lower limit.

2.7 Large Signal Voltage Gain (A_V)
This indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting pin and inverting pin. It is normally the amplifying rate (gain) with reference to DC voltage.
A_V = (Output voltage) / (Differential input voltage)

2.8 Common-mode Input Voltage Range (V_{ICMR})
This indicates the input voltage range where IC normally operates.

2.9 Common-mode Rejection Ratio (CMRR)
This indicates the ratio of fluctuation of input offset voltage when Common-mode Input Voltage is changed. It is normally the fluctuation of DC.
CMRR = (Change of Input common-mode voltage)/(Input offset fluctuation)

2.10 Power Supply Rejection Ratio (PSRR)
This indicates the ratio of fluctuation of input offset voltage when supply voltage is changed.
It is normally the fluctuation of DC.
PSRR= (Change of power supply voltage)/(Input offset fluctuation)

Description of Terms in Electrical Characteristics - continued

2.11 Output Source Current/ Output Sink Current (I_{SOURCE} / I_{SINK})
The maximum current that can be output from the IC under specific output conditions. The output source current indicates the current flowing out from the IC, and the output sink current indicates the current flowing into the IC.

2.12 Slew Rate (SR)
This is a parameter representing the operational speed of the operational amplifier. This indicates the rate at which the output voltage can change in the specified unit time.

2.13 Gain Bandwidth (GBW)
This indicates the product of an arbitrary frequency and its gain in the range of the gain slope of -6 dB/octave.

2.14 Phase Margin (θ)
This indicates the margin of phase from the phase delay of 180 degree at the frequency which the gain of the operational amplifier is 1.

2.15 Gain Margin (Gm)
This indicates the margin of Gain from 0 dB at the frequency which the phase delay of 180 degree.

2.16 Input-Referred Noise Voltage (Vn)
Indicates a noise voltage generated inside the operational amplifier equivalent by ideal voltage source connected in series with input terminal.

2.17 Total Harmonic Distortion + Noise (THD+N)
This indicates the content ratio of harmonic and noise components relative to the output signal.

Typical Performance Curves

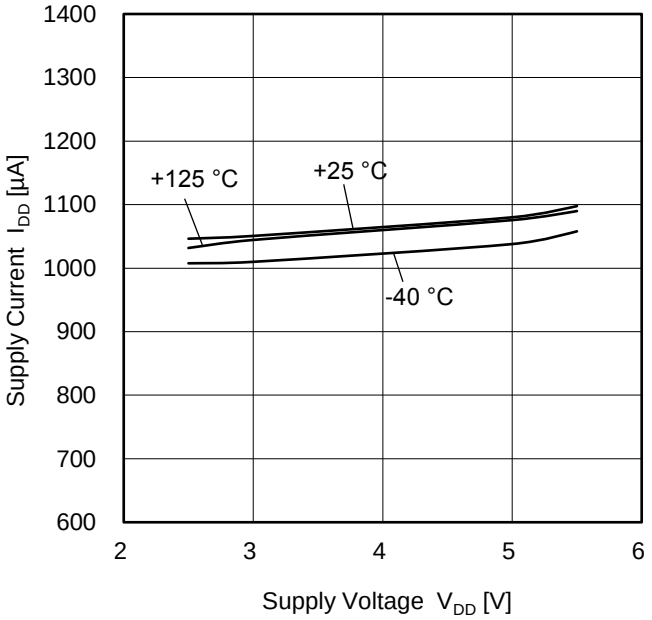


Figure 1. Supply Current vs Supply Voltage

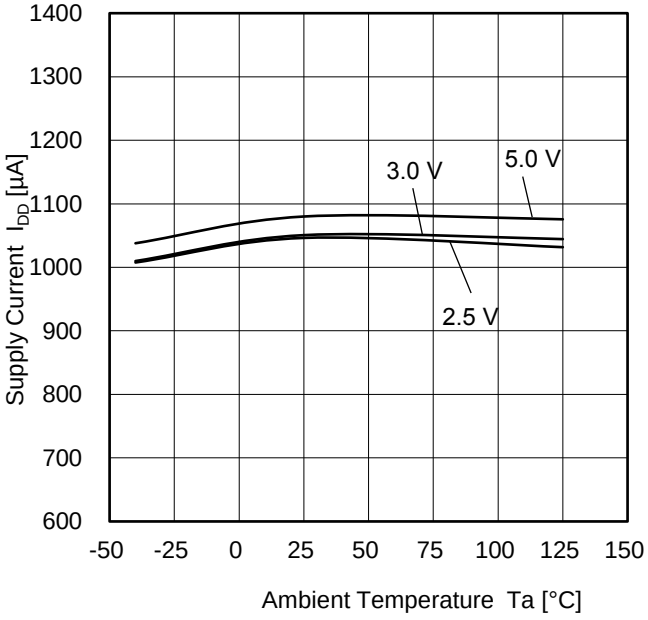


Figure 2. Supply Current vs Ambient Temperature

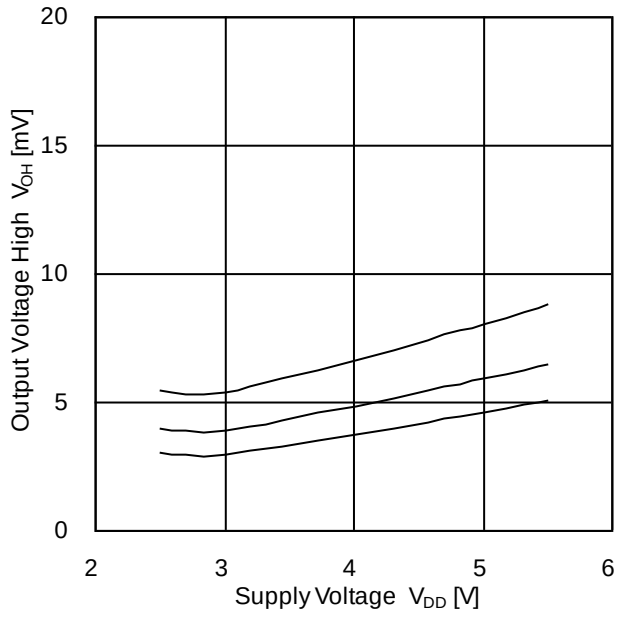


Figure 3. Output Voltage High vs Supply Voltage
(R_L=10 kΩ)

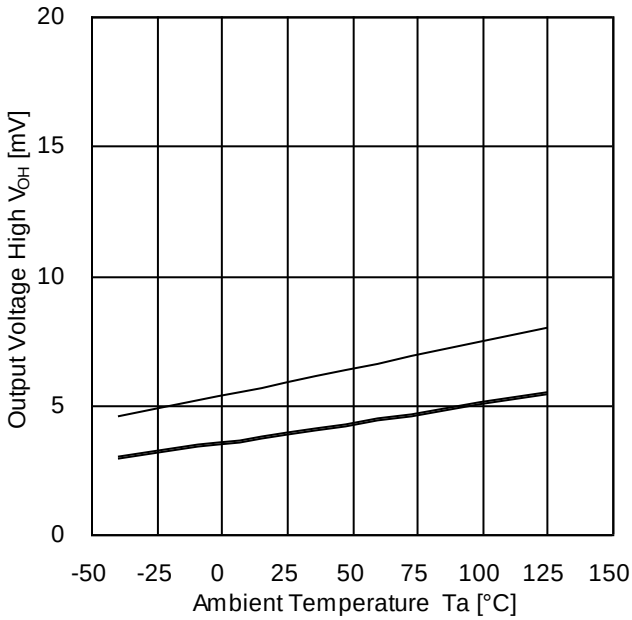


Figure 4. Output Voltage High vs Ambient Temperature
(R_L=10 kΩ)

Typical Performance Curves - continued

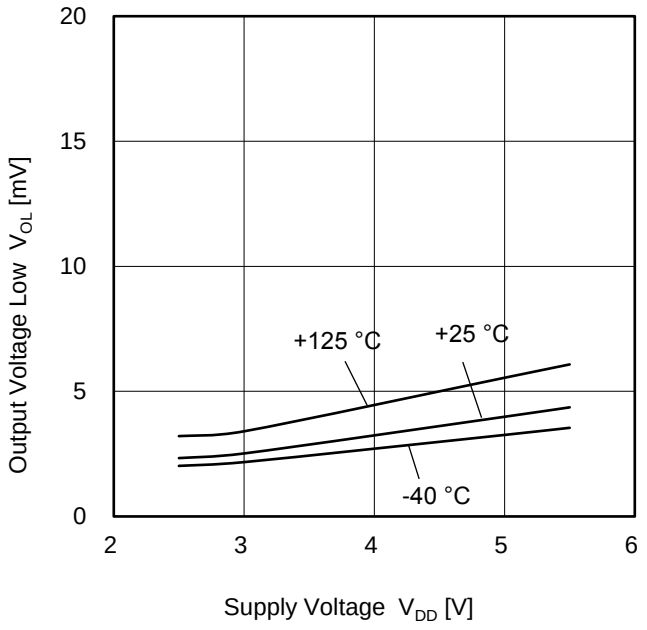


Figure 5. Output Voltage Low vs Supply Voltage
(R_L=10 kΩ)

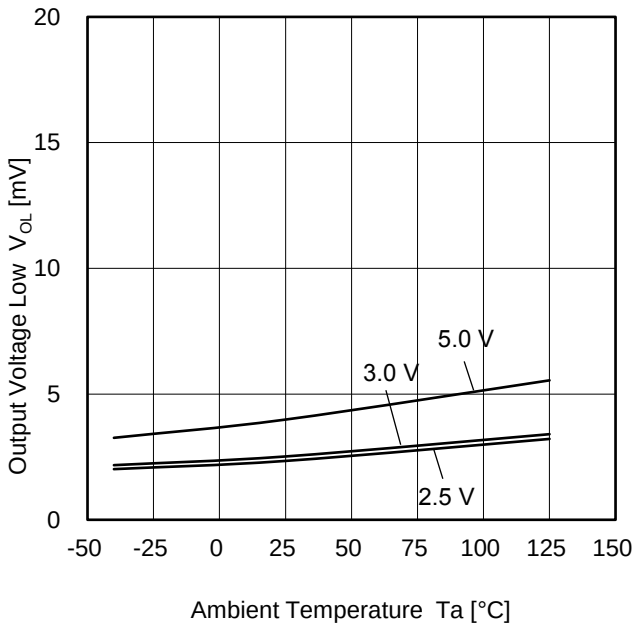


Figure 6. Output Voltage Low vs Ambient Temperature
(R_L=10 kΩ)

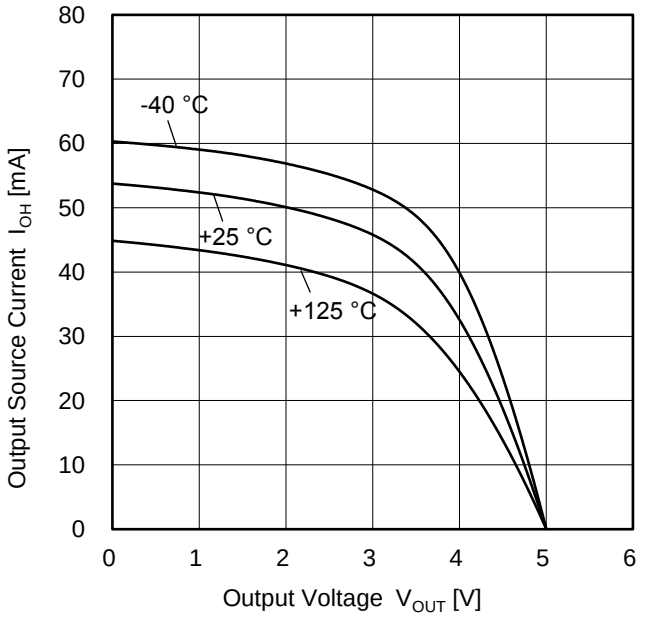


Figure 7. Output Source Current vs Output Voltage
(V_{DD}=5 V)

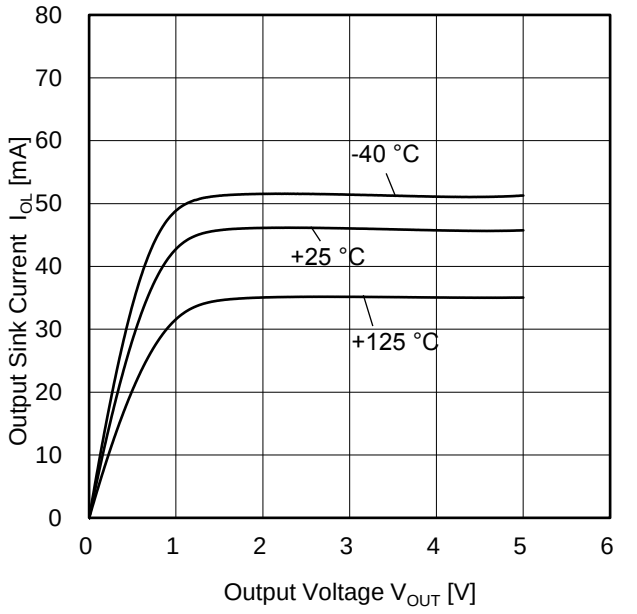


Figure 8. Output Sink Current vs Output Voltage
(V_{DD}=5 V)

Typical Performance Curves - continued

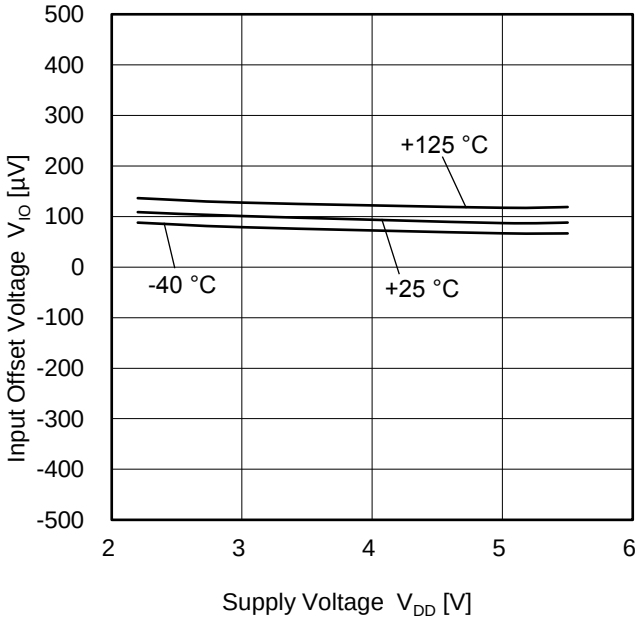


Figure 9. Input Offset Voltage vs Supply Voltage

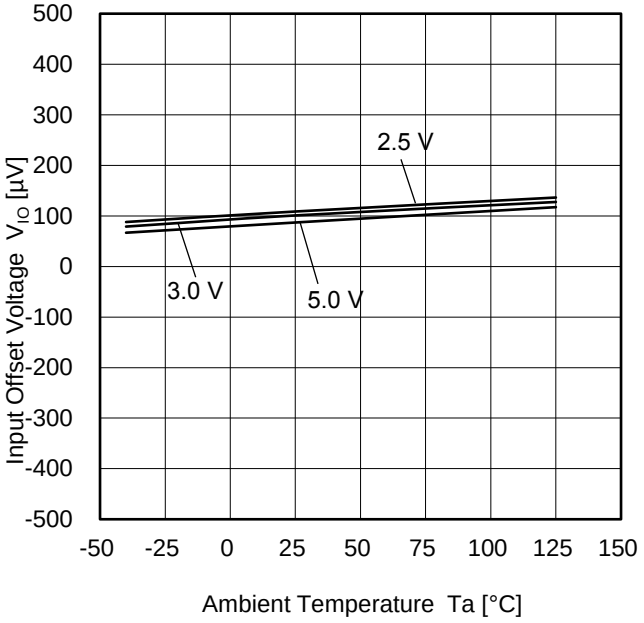


Figure 10. Input Offset Voltage vs Ambient Temperature

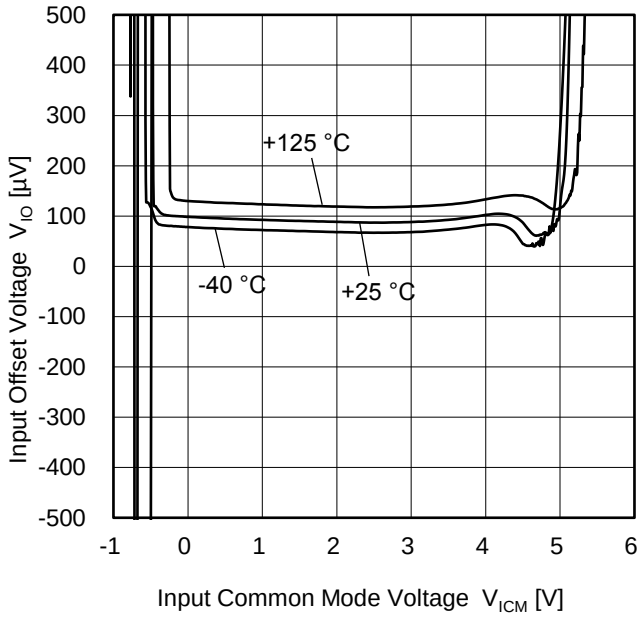


Figure 11. Input Offset Voltage vs Input Common Mode Voltage
(V_{DD}=5 V)

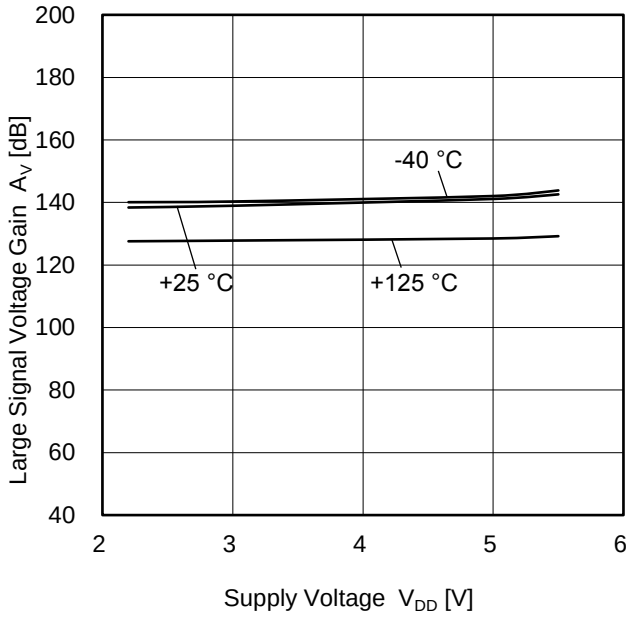


Figure 12. Large Signal Voltage Gain vs Supply Voltage
(R_L=10 kΩ)

Typical Performance Curves - continued

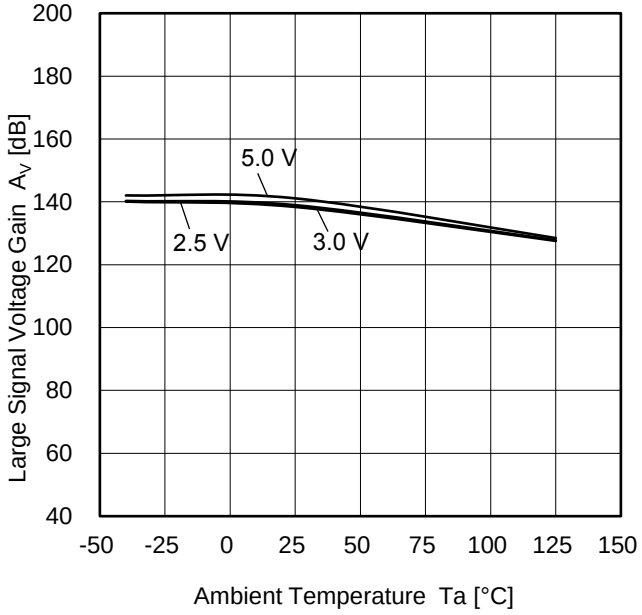


Figure 13. Large Signal Voltage Gain vs Ambient Temperature

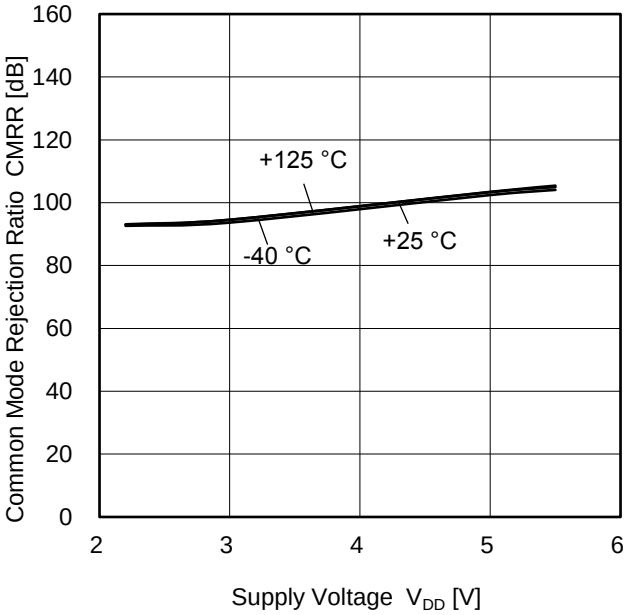


Figure 14. Common Mode Rejection Ratio vs Supply Voltage

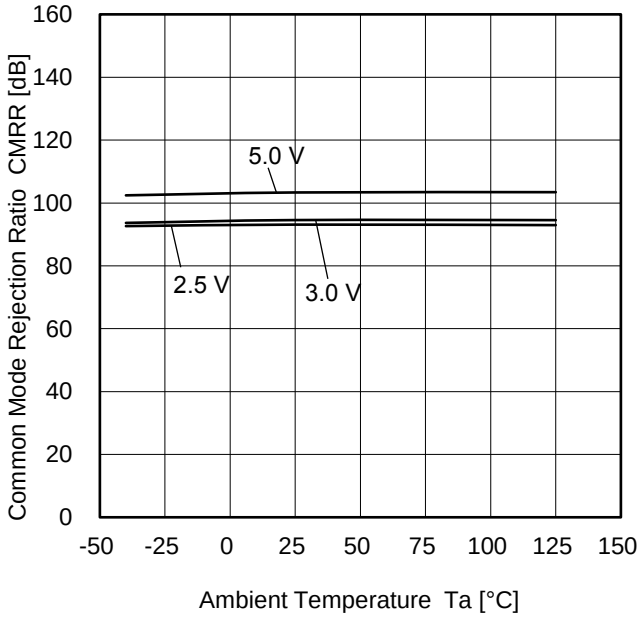


Figure 15. Common Mode Rejection Ratio vs Ambient Temperature

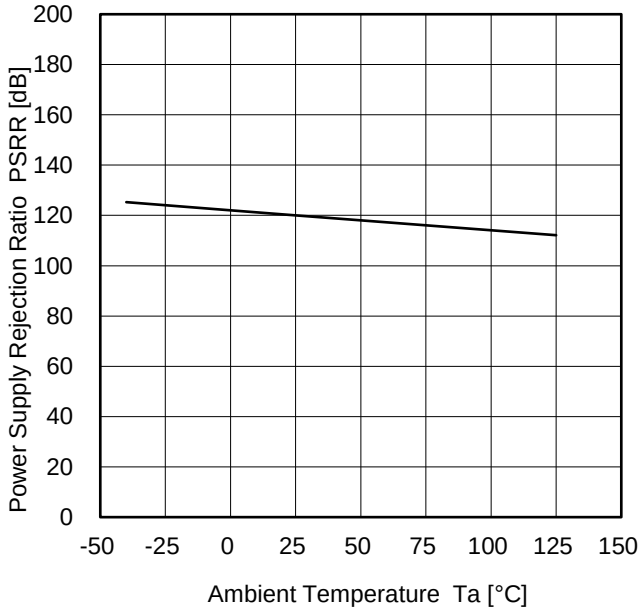


Figure 16. Power Supply Rejection Ratio vs Ambient Temperature

Typical Performance Curves - continued

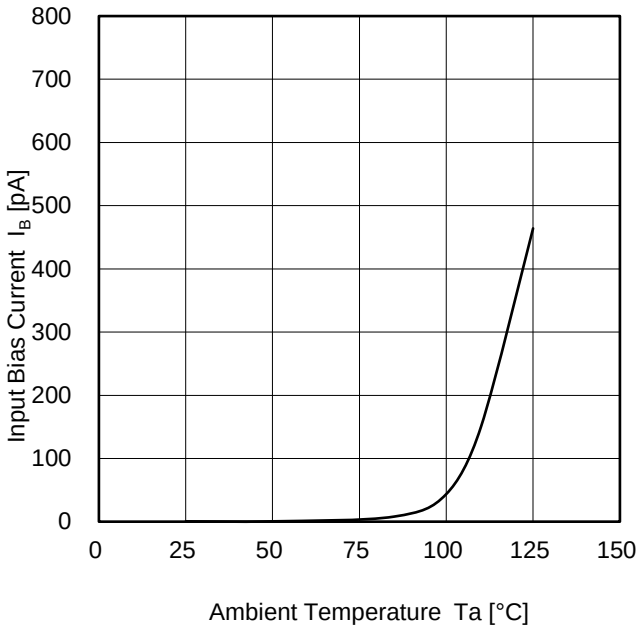


Figure 17. Input Bias Current vs Ambient Temperature
(V_{DD}=5 V)

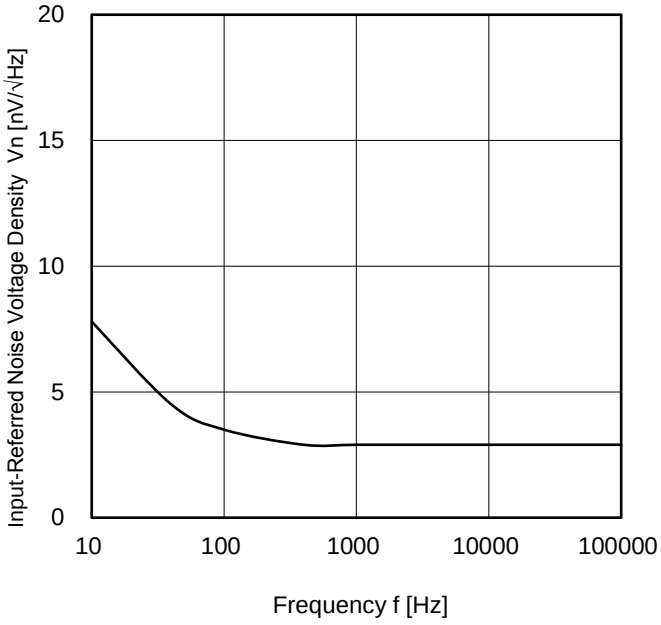


Figure 18. Input-Referred Noise Voltage Density vs Frequency
(V_{DD}=5 V)

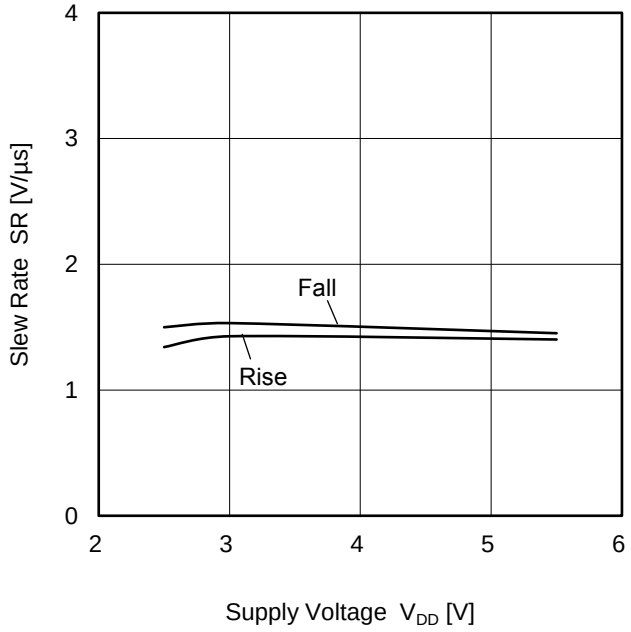


Figure 19. Slew Rate vs Supply Voltage

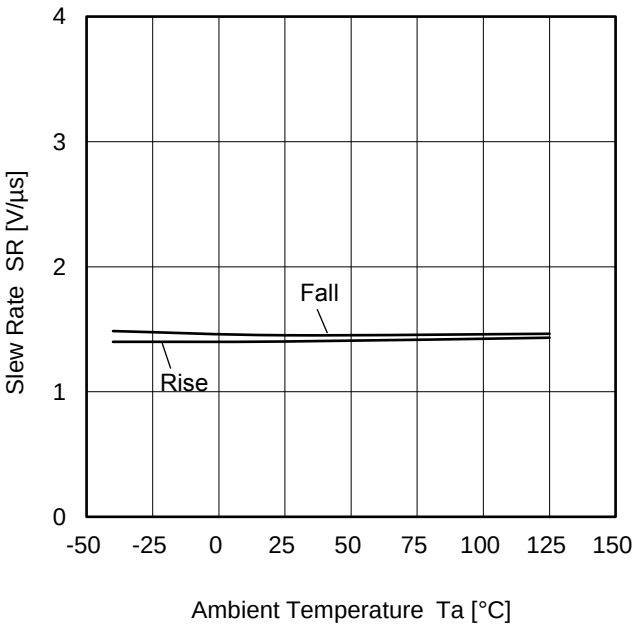


Figure 20. Slew Rate vs Ambient Temperature
(V_{DD}=5 V)

Typical Performance Curves - continued

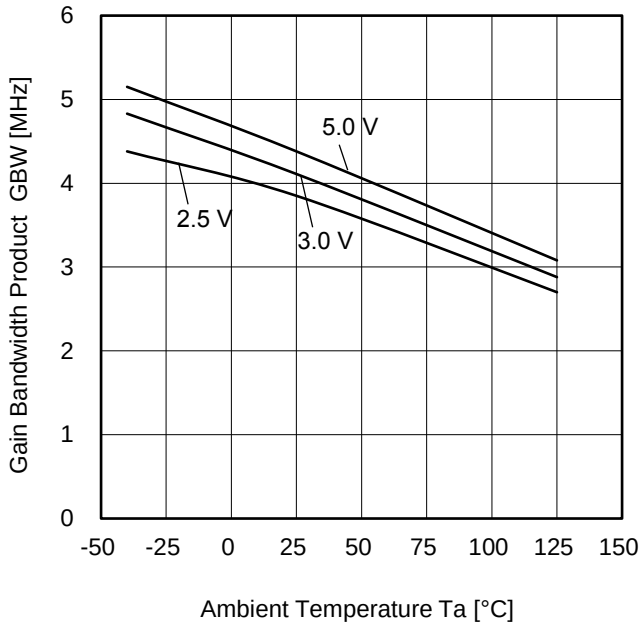


Figure 21. Gain Bandwidth Product vs Ambient Temperature

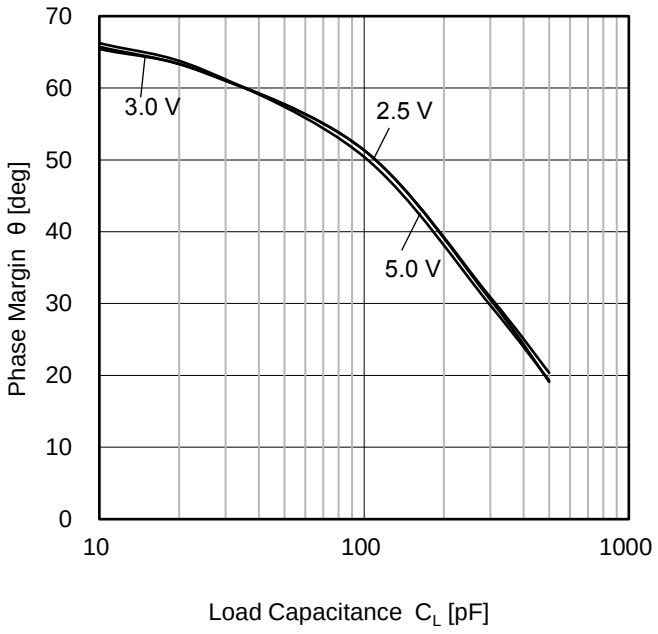


Figure 22. Phase Margin vs Load Capacitance
(R_F=10 kΩ, G=+40 dB)

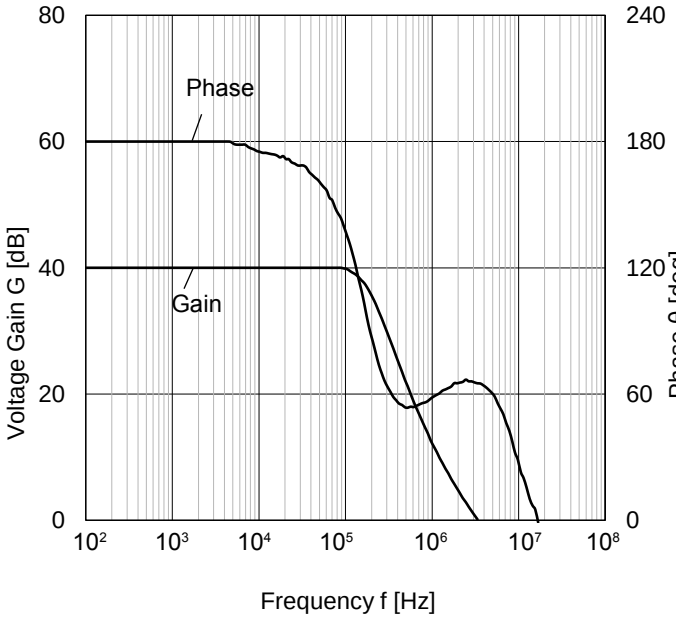


Figure 23. Voltage Gain, Phase vs Frequency
(V_{DD}=5 V)

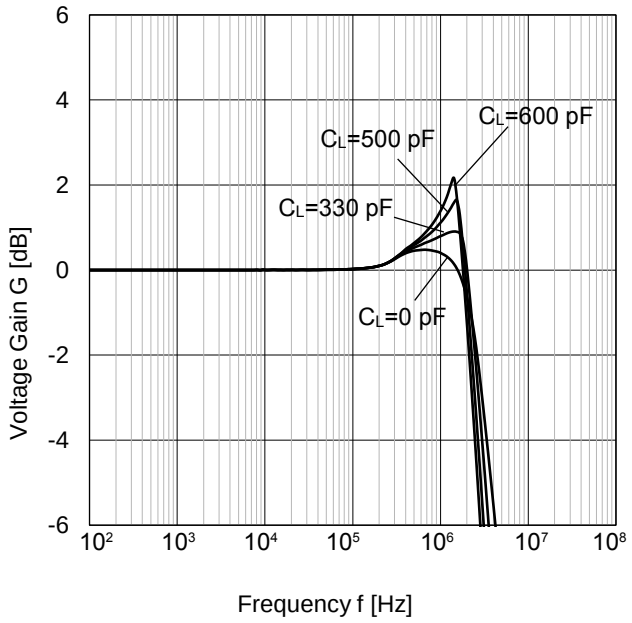
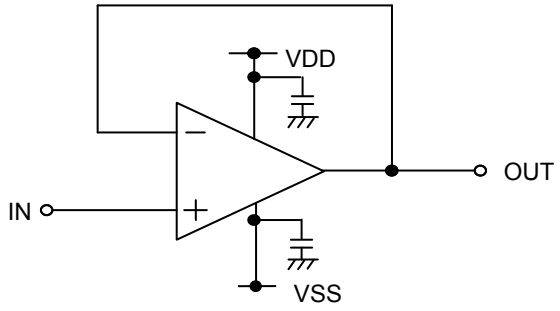


Figure 24. Voltage Gain vs Frequency
(V_{DD}=5 V, G=0 dB, V_{IN}=180 mV_{PP})

Application Examples

○Voltage Follower

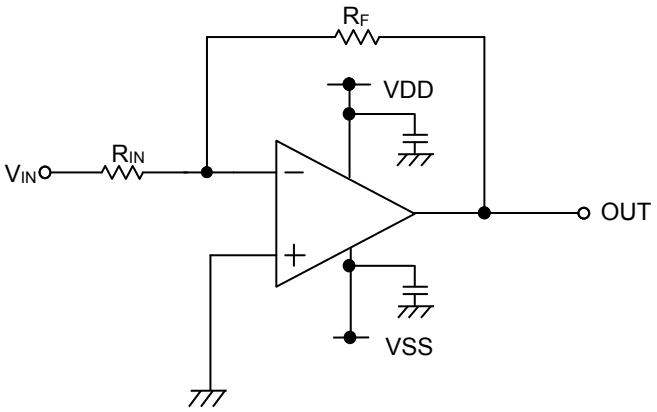


Voltage Follower Circuit

Using this circuit, the output voltage (V_{OUT}) is configured to be equal to the input voltage (V_{IN}). This circuit also stabilizes the output voltage (V_{OUT}) due to high input impedance and low output impedance. Computation for output voltage (V_{OUT}) is shown below.

$$\boldsymbol{V_{OUT} = V_{IN}}$$

○Inverting Amplifier



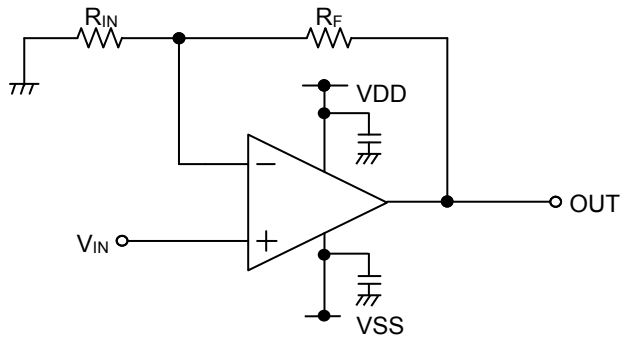
Inverting Amplifier Circuit

For inverting amplifier, input voltage (V_{IN}) is amplified by a voltage gain and depends on the ratio of R_{IN} and R_F. The out-of-phase output voltage is shown in the next expression.

$$\boldsymbol{V_{OUT} = -\frac{R_f}{R_{IN}} V_{IN}}$$

This circuit has input impedance equal to R_{IN}.

○Non-inverting Amplifier



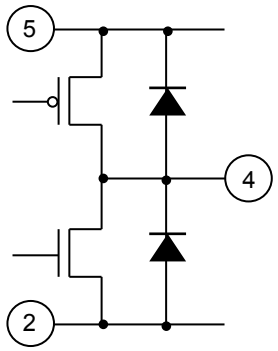
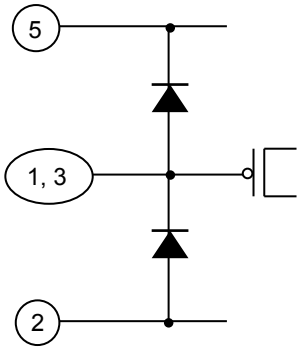
Non-inverting Amplifier Circuit

For non-inverting amplifier, input voltage (V_{IN}) is amplified by a voltage gain, which depends on the ratio of R_{IN} and R_F. The output voltage (V_{OUT}) is in-phase with the input voltage (V_{IN}) and is shown in the next expression.

$$\boldsymbol{V_{OUT} = \left(1 + \frac{R_f}{R_{IN}}\right) V_{IN}}$$

Effectively, this circuit has high input impedance since its input side is the same as that of the operational amplifier.

I/O Equivalence Circuits

Pin No.	Pin Name	Pin Description	Equivalence Circuit
4	OUT	Output	
1 3	+IN -IN	Input	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

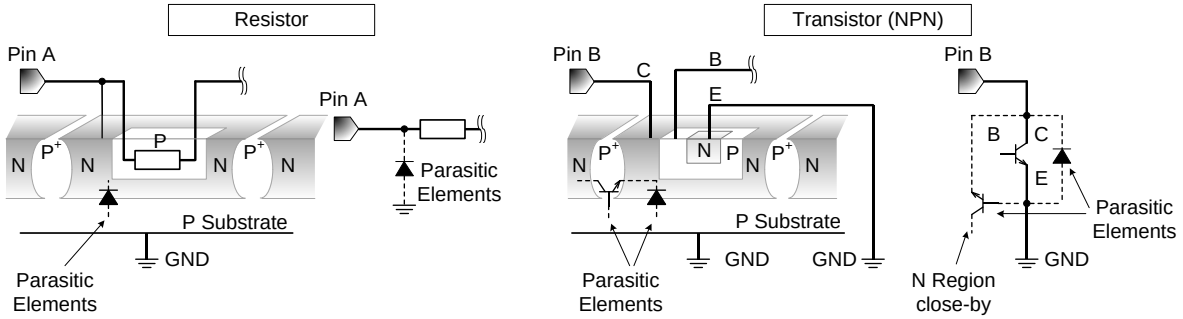
Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

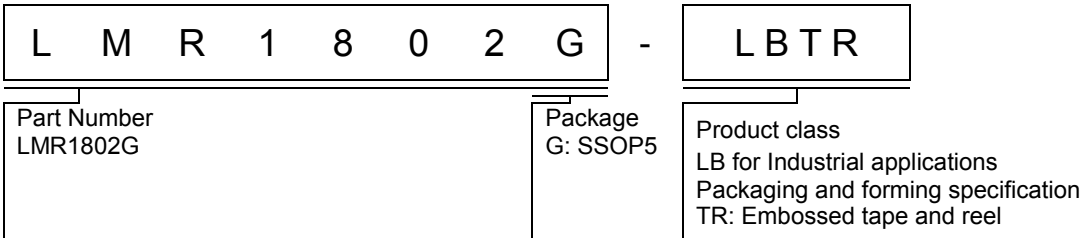


Example of monolithic IC structure

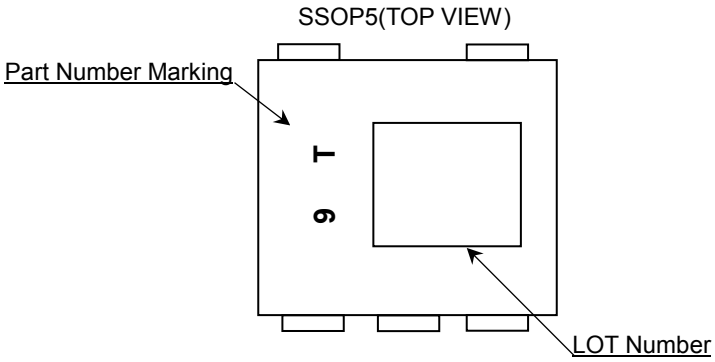
12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

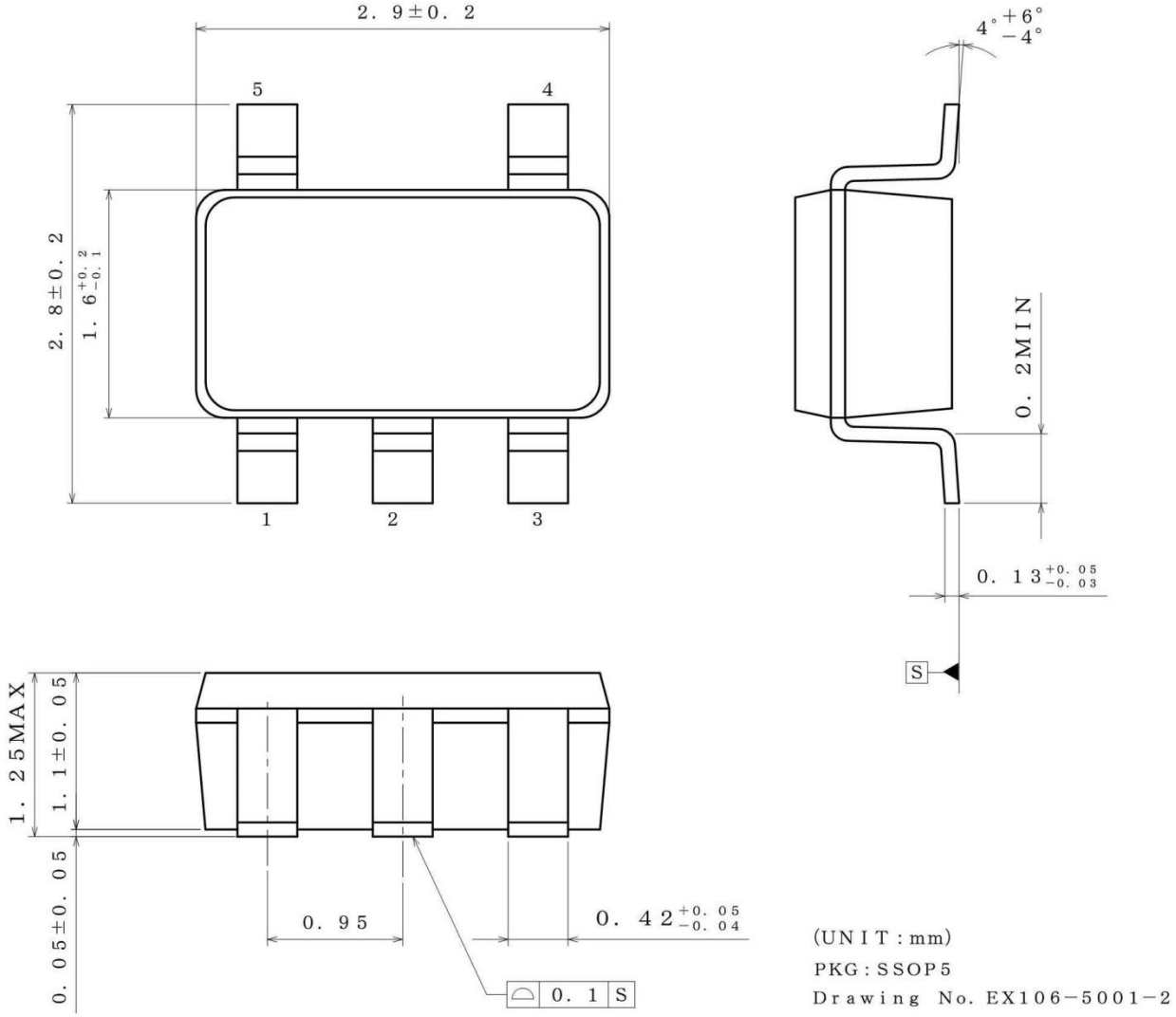


Marking Diagram



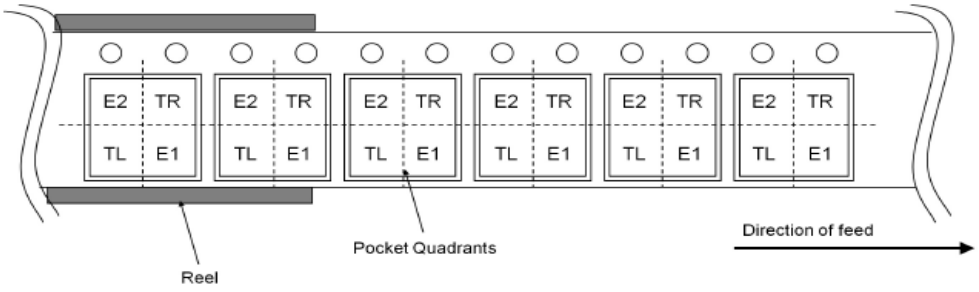
Physical Dimension and Packing Information

Package Name	SSOP5



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



Revision History

Date	Revision	Changes
07.May.2018	001	New Release
13.Jun.2018	002	Typical Application Circuit : Addition of C_F Electrical Characteristics(Output Voltage High) : Addition to the condition column Electrical Characteristics(Input Offset Voltage Temperature Drift) : Addition of Note 2

Notice

Precaution on using ROHM Products

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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