SIEMENS

SFH6700/6719
SFH6701/6711
SFH6702/6712
SFH6705

Low Input Current Logic Gate Optocoupler

Preliminary Data Sheet

FEATURES

- **Data Rate 5 MBits/s (2.5 MBit/s over Temperature)**
- **Buffer**
- **Isolation Test Voltage, 2500 VAC_{RMS} for 1 min.**
- **TTL, LSTTL and CMOS Compatible**
- **Internal Shield for Very High Common Mode Transient Immunity**
- **Wide Supply Voltage Range (4.5 to 15 V)**
- **Low Input Current (1.6 mA to 5 mA)**
- **Three State Output (SFH6700/19)**
- **Totem Pole Output (SFH6701/02/11/12)**
- **Open Collector Output (SFH6705)**
- **Specified from 0°C to 85°C**

APPLICATIONS

- **Industrial Control**
- **Replace Pulse Transformers**
- **Routine Logic Interfacing**
- **Motion/Power Control**
- **High Speed Line Receiver**
- **Microprocessor System Interfaces**
- **Computer Peripheral Interfaces**

DESCRIPTION

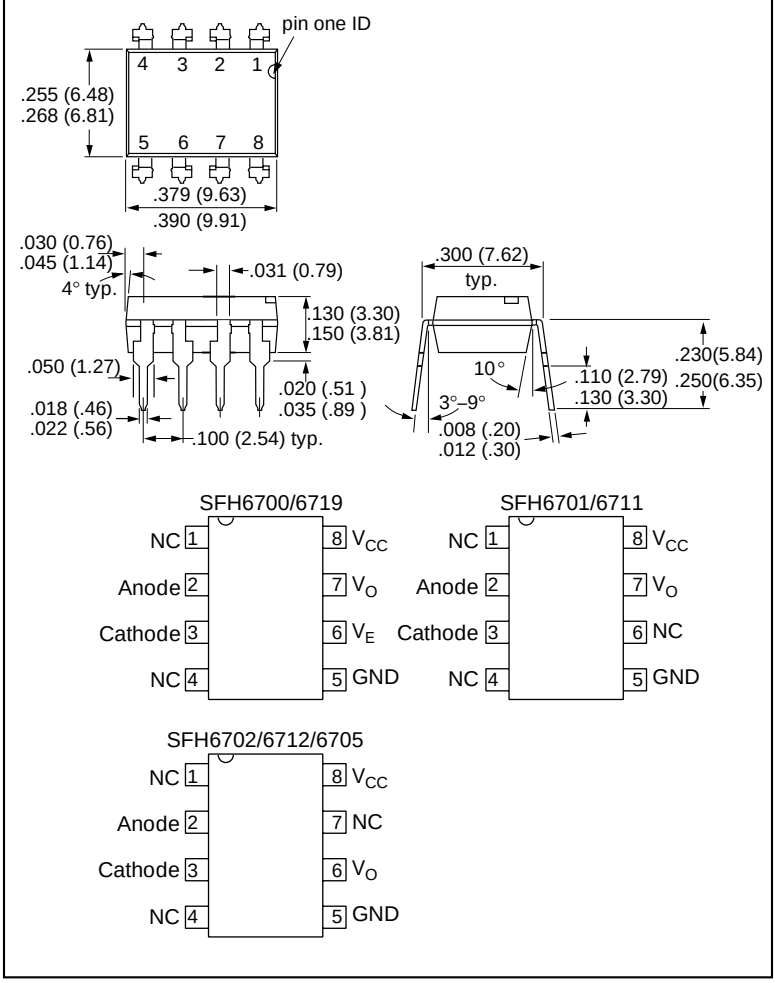
The SFH67xx high speed optocoupler series consists of a GaAlAs infrared emitting diode, optically coupled with an integrated photodetector. The detector incorporates a Schmitt-Trigger stage for improved noise immunity. Using the Enable input, the output can be switched to the high ohmic state, which is necessary for data bus applications. A Faraday shield provides a common mode transient immunity of1000 V/µs at V_{CM}=50 V for SFH6700/01/02/05 and 2500 V/µs at V_{CM}=400 V for SFH6711/12/19.

The SFH67xx uses an industry standard DIP8 package. With standard lead bending, creepage distance and clearance of ≥7 mm with lead bending options 6, 7, and 9 ≥8 mm are achieved.

Truth Table SFH6701/11/02/12/05 (Positive Logic)

IR Diode	Output
on	H
off	L

Dimensions in Inches (mm)



Truth Table SFH6700/19 (Positive Logic)

IR Diode	Enable	Output
on	H	Z
off	H	Z
on	L	H
off	L	L

Maximum Ratings

Parameter		Sym.	Min.	Max.	Units
Emitter					
Reverse Voltage		V_R		3	V
DC Forward Current		I_F		10	mA
Surge Forward Current (tp≤1 µs, 300 pulses/s)		I_{FSM}		1	A
Total Power Dissipation		P_{tot}		20	mW
Detector					
Supply Voltage		V_{CC}	–0.5	15	V
Three State Enable Voltage (SFH6700/19 only)		V_{EN}	–0.5	15	V
Output Voltage		V_O	–0.5	15	V
Average Output Current		I_O		25	mA
Total Power Dissipation		P_{tot}		100	mW
Package					
Storage Temperature Range		T_{STG}	–55	125	°C
Ambient Temperature Range		T_A	–40	85	°C
Lead Soldering Temperature (t=10 sec.)		T_S		260	°C
Isolation Test Voltage (t=1 min.)		V_{ISO}	2500		VAC_{RMS}
Pollution Degree				2	
Creepage Distance and Clearance	Standard Lead Bending		7		mm
	Options 6, 7, 9		8		
Comparative Tracking Index per DIN IEC112/ VDE 0303, part 1			175	400	
Isolation Resistance	V_{IO}=500 V, T_A=25°C	R_{ISO}	10^{12}		Ω
	V_{IO}=500 V, T_A=100°C		10^{11}		

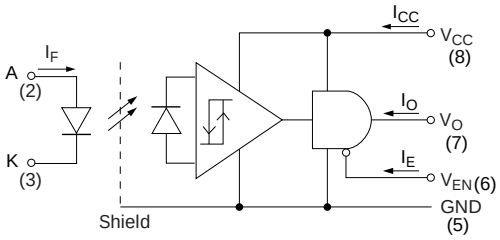
Recommended Operating Conditions

A 0.1 µF bypass capacitor connected between pins 5 and 8 must be used.

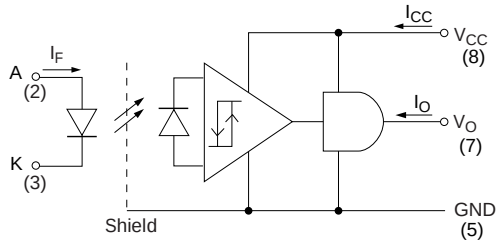
Parameter	Symbol	Min.	Max.	Unit
Supply Volage	V_{CC}	4.5	15	V
Enable Voltage High (SFH6700/19)	V_{EH}	2.0	15	V
Enable Voltage Low (SFH6700/19)	V_{EL}	0	0.8	V
Forward Input Current	I_{Fon}	1.6(1)	5	mA
Forward Input Current	I_{Foff}	–	0.1	mA
Operating Temperature	T_A	0	85	°C
Output Pull-up Resistor (SFH6705 only)	R_L	350	4k	Ω
Fan Out (SFH6705 at R_L=1 KΩ)	N		16	LS TTL Loads

1. We recommend using a 2.2 mA to permit at least 20% CTR degradation guard band.

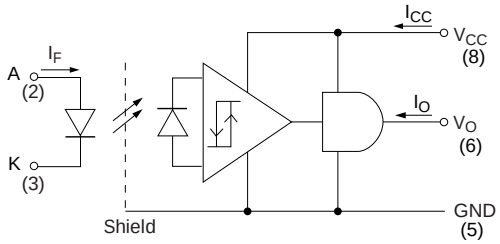
Figure 1. Schematics



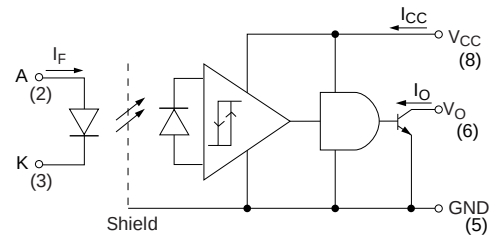
SFH6700/19



SFH6701/11



SFH6702/12



SFH6705

Characteristics

$0°C \leq T_A \leq 85°C$; $4.5\ V \leq V_{CC} \leq 15\ V$; $1.6\ mA \leq I_{Fon} \leq 5\ mA$; $2.0 \leq V_{EH} \leq 15\ V$; $0 \leq V_{EL} \leq 0.8\ V$; $0\ mA \leq I_{Foff} \leq 0.1\ mA$

Typical values: $T_A=25°C$; $V_{CC}=5\ V$; $I_{Fon}=3\ mA$ unless otherwise specified

Parameter	Sym.	Min.	Typ.	Max.	Unit	Test Condition
Emitter						
Forward Voltage	V_F		1.6	1.75	V	$I_F=5\ mA$, $T_A=25°C$
				1.8	V	$I_F=5\ mA$
Input Current Hysteresis	I_{HYS}		0.1		mA	$V_{CC}=5\ V$, $I_{HYS}=I_{Fon}-I_{Foff}$
Reverse Current	I_R		0.5	10	µA	$V_R=3\ V$, $T_A=25°C$
Capacitance	C_0		60		pF	$V_R=0\ V$, $f=1\ MHz$, $T_A=25°C$
Thermal Resistance	R_{thJA}		700		K/W	
Detector						
Logic Low Output Voltage	V_{OL}			0.5	V	$I_{OL}=6.4\ mA$
Logic High Output Voltage (except SFH6705)	V_{OH}	2.4	*		V	$I_{OH}=-2.6\ mA$, $*V_{OH}=V_{CC}-1.8\ V$
Output Leakage Current ($V_{OUT}>V_{CC}$) (except SFH6705)	I_{OHH}		0.5	100	µA	$V_O=5.5\ V$, $V_{CC}=4.5\ V$, $I_F=5\ mA$
			1	500	µA	$V_O=15\ V$, $V_{CC}=4.5\ V$, $I_F=5\ mA$
Output Leakage Current (SFH6705 only)	I_{OHH}		0.5	100	µA	$V_O=5.5\ V$, $V_{CC}=5.5\ V$, $I_F=5\ mA$
			1	500	µA	$V_O=15\ V$, $V_{CC}=15\ V$, $I_F=5\ mA$
Logic High Enable Voltage (SFH6700/19 only)	V_{EH}	2.0			V	
Logic Low Enable Voltage (SFH6700/19 only)	V_{EL}			0.8	V	
Logic High Enable Current (SFH6700/19 only)	I_{EH}			20	µA	$V_{EN}=2.7\ V$
				100	µA	$V_{EN}=5.5\ V$
			0.001	250	µA	$V_{EN}=15\ V$
Logic Low Enable Current (SFH6700/19 only)	I_{EL}	–320	–50		µA	$V_{EN}=0.4\ V$
High Impedance State Output Current (SFH6700/19 only)	I_{OZL}	–20			µA	$V_O=0.4\ V$, $V_{EN}=2.0\ V$, $I_F=5\ mA$
	I_{OZH}			20	µA	$V_O=2.4\ V$, $V_{EN}=2.0\ V$, $I_F=0$
				100	µA	$V_O=5.5\ V$, $V_{EN}=2.0\ V$, $I_F=0$
			0.001	500	µA	$V_O=15\ V$, $V_{EN}=2.0\ V$, $I_F=0$
Logic Low Supply Current	I_{CCL}		3.7	6.0	mA	$V_{CC}=5.5\ V$, $I_F=0$
			4.1	6.5	mA	$V_{CC}=15\ V$, $I_F=0$
Logic High Supply Current	I_{CCH}		3.4	4.0	mA	$V_{CC}=5.5\ V$, $I_F=5\ mA$
			3.7	5.0	mA	$V_{CC}=15\ V$, $I_F=5\ mA$
Logic Low Short Circuit Output Current	I_{OSL} (2)	25			mA	$V_O=V_{CC}=5.5\ V$, $I_F=0$
		40			mA	$V_O=V_{CC}=15\ V$, $I_F=0$
Logic High Short Circuit Output Current (except SFH6705)	I_{OSH} (2)			–10	mA	$V_{CC}=5.5\ V$, $Vo=0\ V$, $I_F=5\ mA$
				–25	mA	$V_{CC}=15\ V$, $Vo=0\ V$, $I_F=5\ mA$
Thermal Resistance	R_{thJA}		300		K/W	
Package						
Coupling Capacitance	C_{IO}		0.6		pF	f=1 MHz, pins 1–4 and 5–8 shorted together
Isolation Resistance	R_{ISO}	10^{12}			Ω	$V_{IO}=500\ V$, $T_A=25°C$
		10^{11}			Ω	$V_{IO}=500\ V$, $T_A=100°C$

2. Output short circuit time ≤10 ms.

Switching Times [3]

$0°C \leq T_A \leq 85°C$; $4.5\ V \leq V_{CC} \leq 15\ V$; $1.6\ mA \leq I_{Fon} \leq 5\ mA$; $2.0 \leq V_{EH} \leq 15\ V$ (SFH6700/19);
$0 \leq V_{EL} \leq 0.8\ V$ (SFH6700/19); $0\ mA \leq I_{Foff} \leq 0.1\ mA$
Typical values: $T_A=25°C$; $V_{CC}=5\ V$; $I_{Fon}=3\ mA$ unless otherwise specified

Parameter, SFH6700/01/02/11/12/19	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Propagation Delay Time to Logic Low Output Level	t_{PHL}		120		ns	Without Peaking Capacitor
			115	300		With Peaking Capacitor
Propagation Delay Time to Logic Low Output Level	t_{PLH}		125		ns	Without Peaking Capacitor
			90	300		With Peaking Capacitor
Output Enable Time to Logic High (SFH6700/19)	t_{PZH}		20		ns	
Output Enable Time to Logic Low (SFH6700/19)	t_{PZL}		25		ns	
Output Disable Time from Logic High (SFH6700/19)	t_{PHZ}		50		ns	
Output Disable Time from Logic Low (SFH6700/19)	t_{PLZ}		50		ns	
Output Rise Time	t_r		40		ns	10% to 90%
Output Fall Time	t_f		10		ns	90% to 10%

Switching Times [3]

Typical values: $T_A=25°C$, $V_{CC}=5\ V$; $I_{Fon}=3\ mA$, $R_L=390\ \Omega$, unless otherwise specified

Parameter, SFH6705	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Propagation Delay Time to Logic Low Output Level	t_{PHL}		115		ns	Without Peaking Capacitor
			105	300		With Peaking Capacitor
Propagation Delay Time to Logic Low Output Level	t_{PLH}		125		ns	Without Peaking Capacitor
			90	300		With Peaking Capacitor
Output Rise Time	t_r		25		ns	10% to 90%
Output Fall Time	t_f		4		ns	90% to 10%

Common Mode Transient Immunity $T_A=25°C$, $V_{CC}=5\ V$ [4]

Parameter	Device	Symbol	Min.	Unit	Test Condition
Logic High Common Mode Transient Immunity	SFH6700/01/02/05	$\lvert CM_H \rvert$ [4]	1000	V/µs	$\lvert V_{CM} \rvert=50\ V$, $I_F=1.6\ mA$
	SFH6711/12/19		2500	V/µs	$\lvert V_{CM} \rvert=400\ V$, $I_F=1.6\ mA$
Logic Low Common Mode Transient Immunity	SFH6700/01/02/05	$\lvert CM_L \rvert$ [4]	1000	V/µs	$\lvert V_{CM} \rvert=50\ V$, $I_F=0$
	SFH6711/12/19		2500	V/µs	$\lvert V_{CM} \rvert=400\ V$, $I_F=0$

3. A 0.1 µF bypass capacitor connected between pins 5 and 8 must be used.
4. CM_H is the maximum slew rate of a common mode voltage V_{CM} at which the output voltage remains at logic high level ($V_O>2\ V$).
   CM_L is the maximum slew rate of a common mode voltage V_{CM} at which the output voltage remains at logic low level ($V_O<0.8\ V$).

Figure 2. Permissible total power disipation vs. temperature

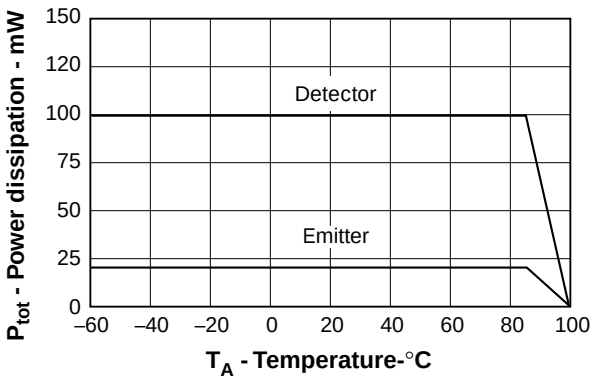


Figure 3. Typical iput diode forward current vs. forward voltage

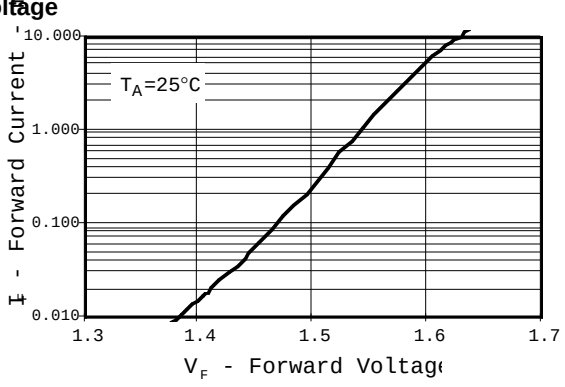


Figure 4. Typical forward input voltage vs. temperature

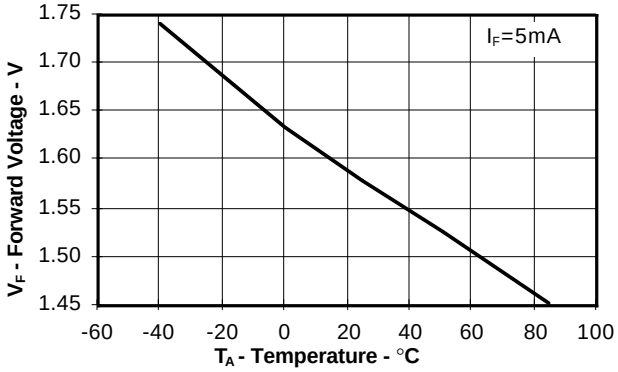


Figure 5. Typical output voltage vs. forward input current (except SFH6705)

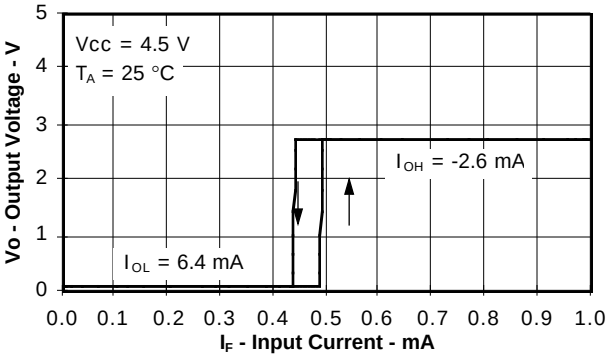


Figure 6. Typical output forward voltage vs. forward input current (only SFH6705)

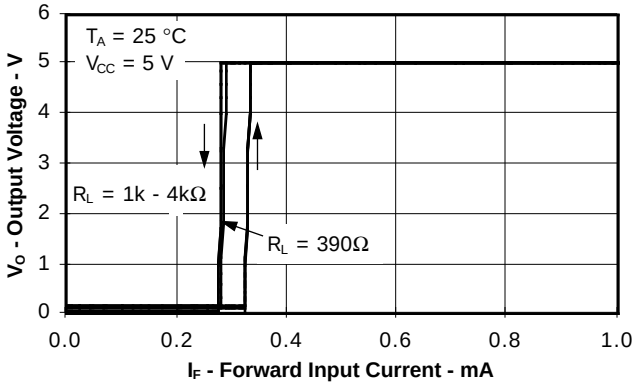


Figure 7. Typical supply current vs. temperature

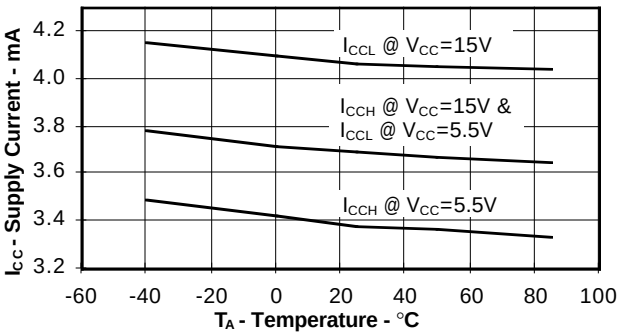


Figure 8. Typical output leakage current vs. temperature

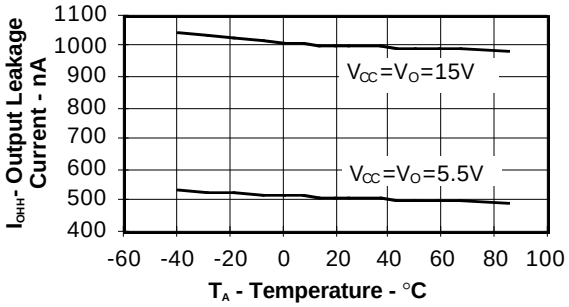


Figure 9. Typical low level output current vs. temperature

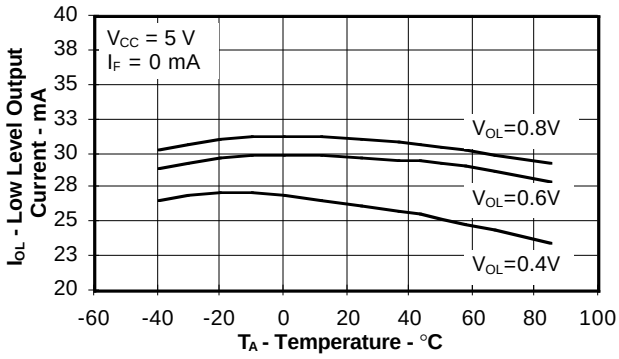


Figure 10. Typical low level output voltage vs. temperature

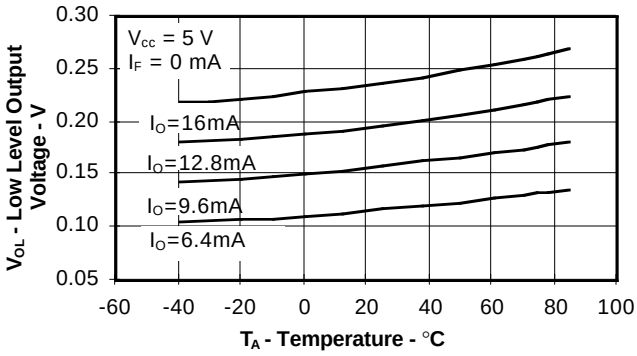


Figure 11. Typical high level output current vs. temperature (except SFH6705)

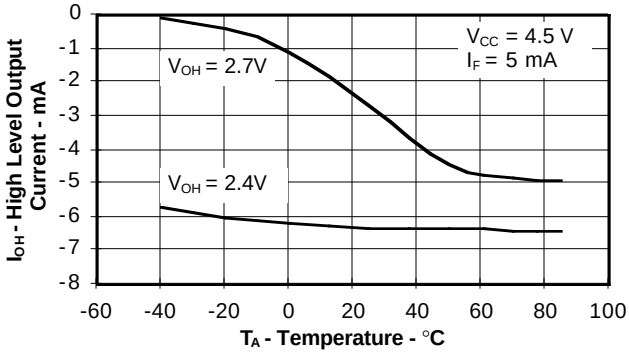


Figure 12. Typical rise, fall time vs. temperature (except SFH6705)

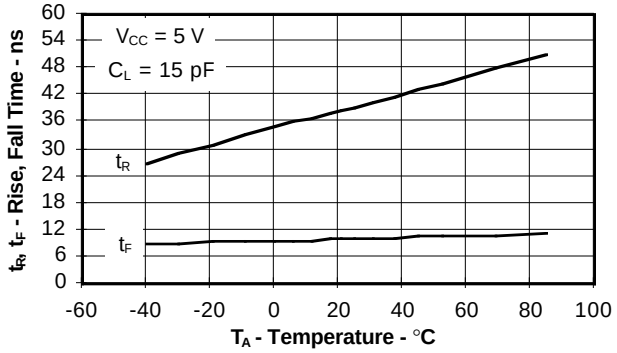


Figure 13. Typical propagation delays to logic high vs. temperature (except SFH6705)

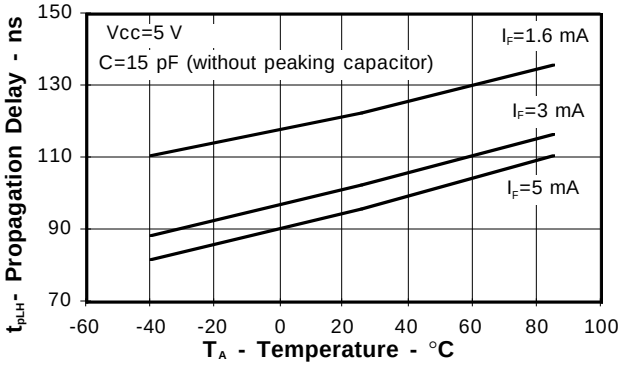


Figure 14. Typical propagation delays to logic low vs. temperature (except SFH6705)

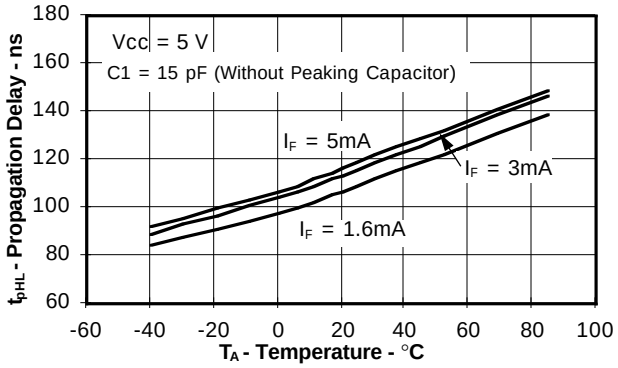


Figure 15. Typical propagation delays to logic high vs. temperature (except SFH6705)

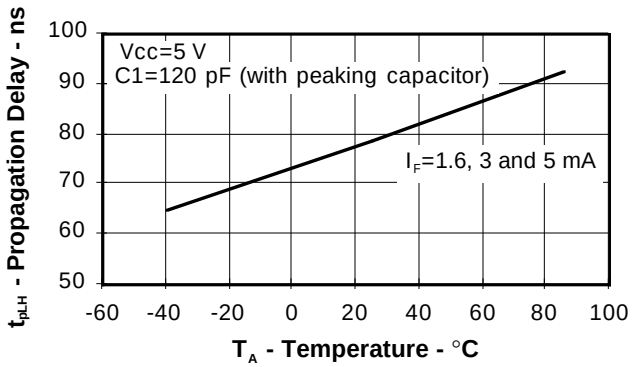


Figure 16. Typical propagation delays to logic low vs. temperature

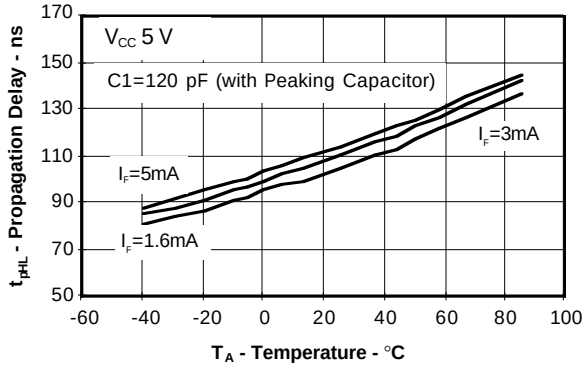


Figure 17. Typical propagation delays to logic high vs. temperature

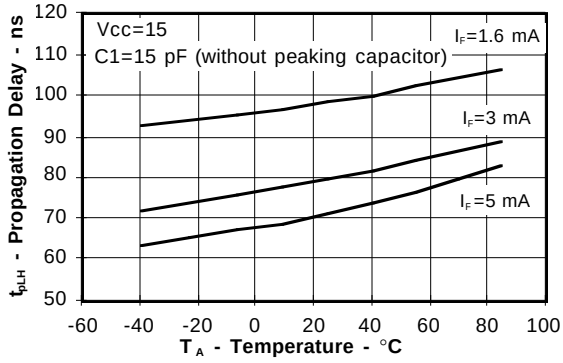


Figure 18. Typical propagation delays to logic low vs. temperature

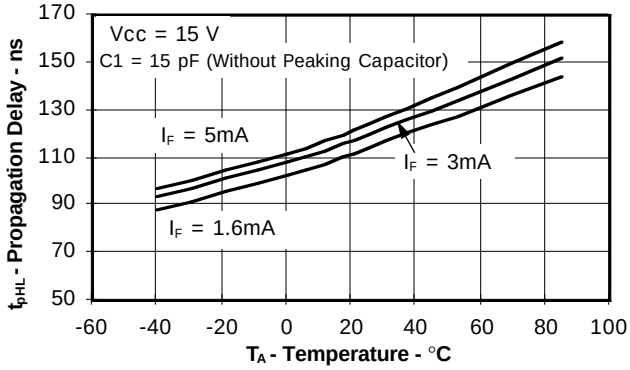


Figure 19. Typical propagation delays to logic high vs. temperature

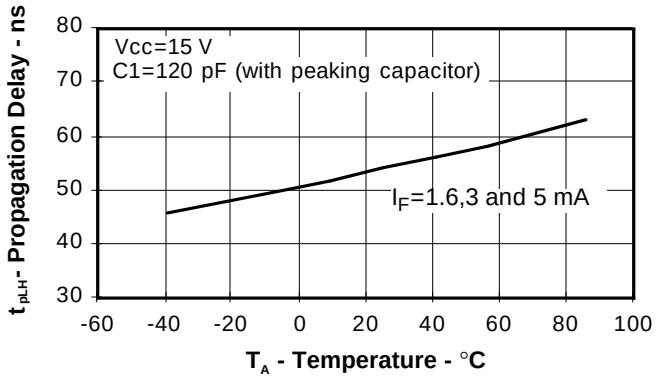


Figure 20. Typical propagation delays to logic low vs. temperature (except SFH6705)

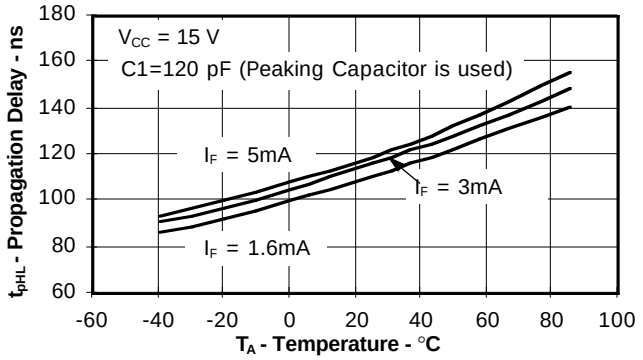


Figure 21. Typical logic low enable propagation delays vs. temperature (only SFH6700/11)

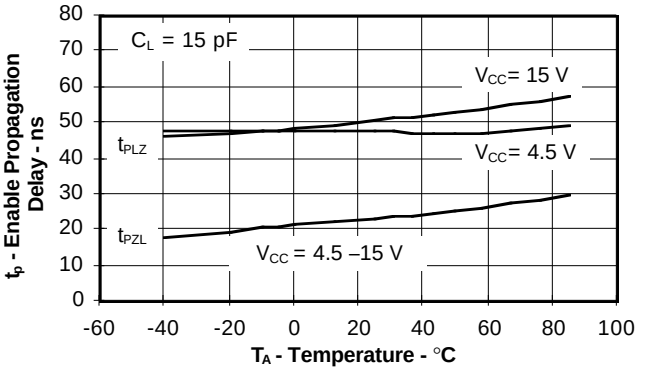


Figure 22. Typical logic high enable propagation delays vs. temperature (only SFH6700/11)

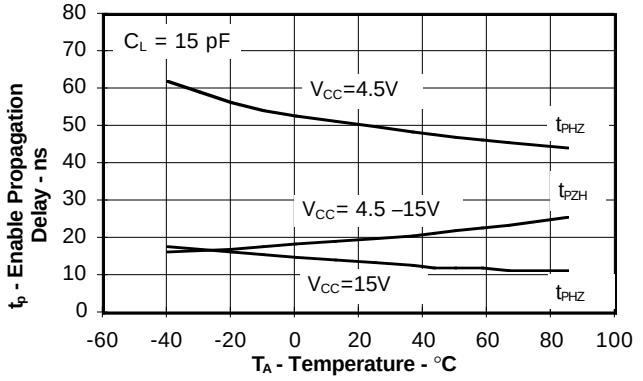


Figure 23. Typical propagation delays vs. pulse Input current (only SFH6705)

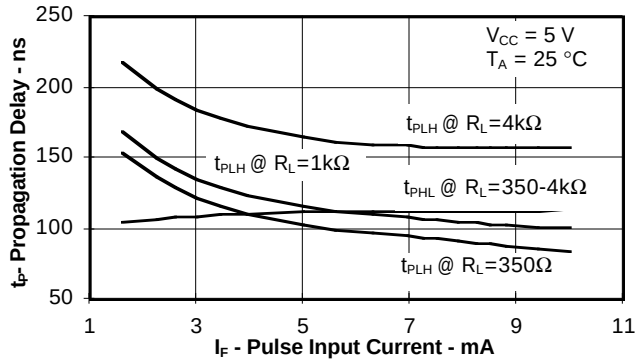


Figure 24. Typical propagation delays to high level vs. temperature (only SFH 6705)

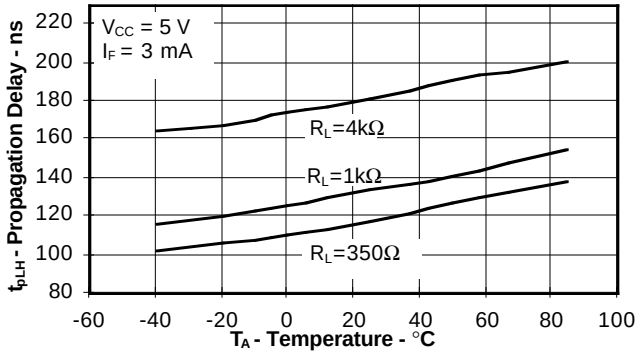


Figure 25. Typical progagation delays to low level vs. temperature (only SFH 6705)

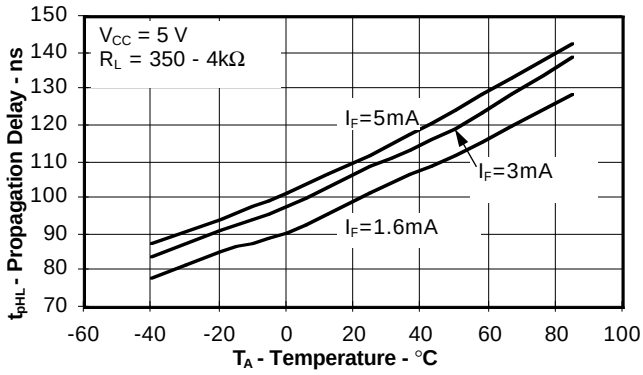


Figure 26. Typical rise, fall time vs. temperature (only SFH6705)

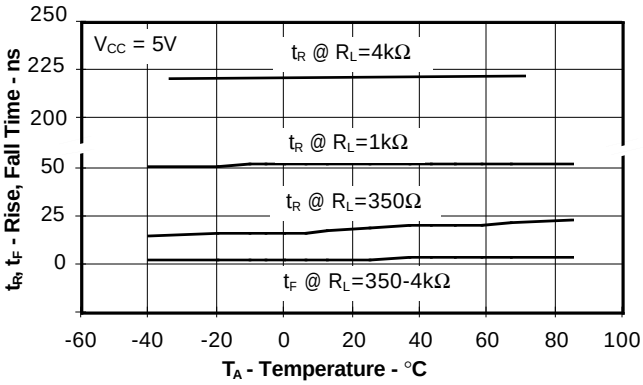
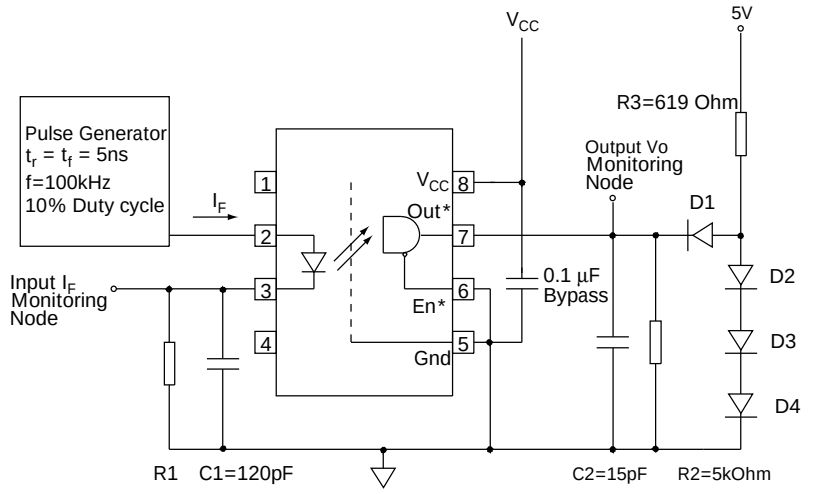


Figure 27. Test circuit for t_{PLH}, t_{PHL}, t_r and t_f—SFH6700/01/02/11/12/19



The Probe and Jig Capacitances are included in C1 and C2

All diodes are 1N916 or 1N3064

R1	2.15 kOhm	1.1 kOhm	681 Ohm
I_F (ON)	1.6 mA	3 mA	5 mA

* SFH6701/02/11/12 without V_{EN}

* SFH6702/12 Pin 6 V_{OUT} and Pin 7 n.c.

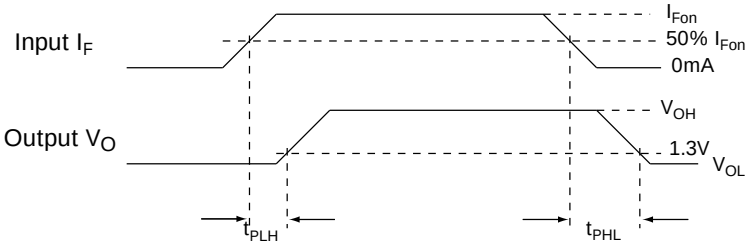
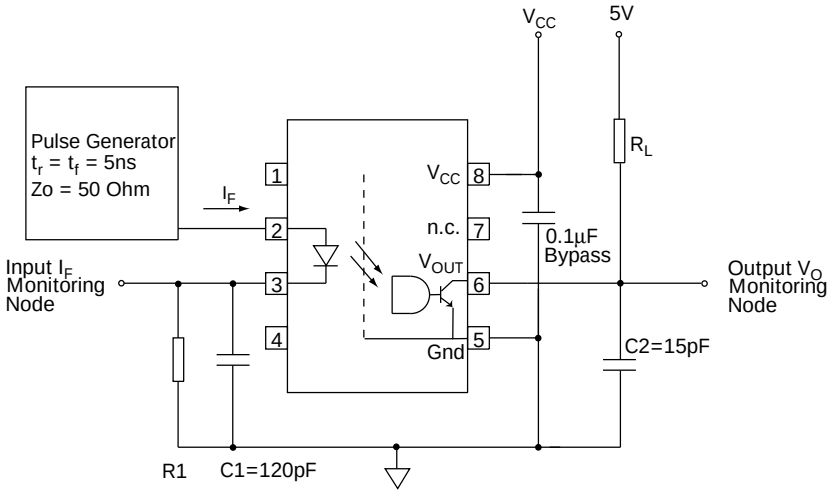


Figure 28. Test circuit for t_{PLH}, t_{PHL}, t_r and t_f—SFH6705



The Probe and Jig Capacitances are included in C1 and C2

R1	2.15 kOhm	1.1 kOhm	681 Ohm
I_F (ON)	1.6 mA	3 mA	5 mA

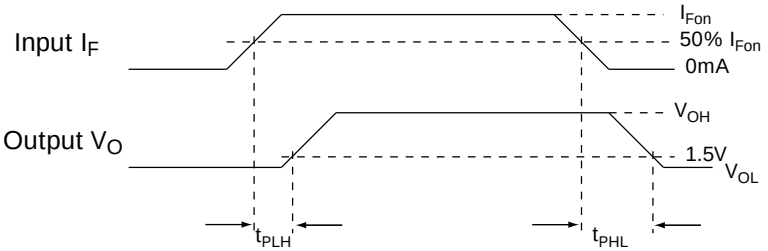


Figure 29. Test circuit for t_{PHZ}, t_{PZH}, t_{PLZ} and t_{PZL}–SFH6700/19

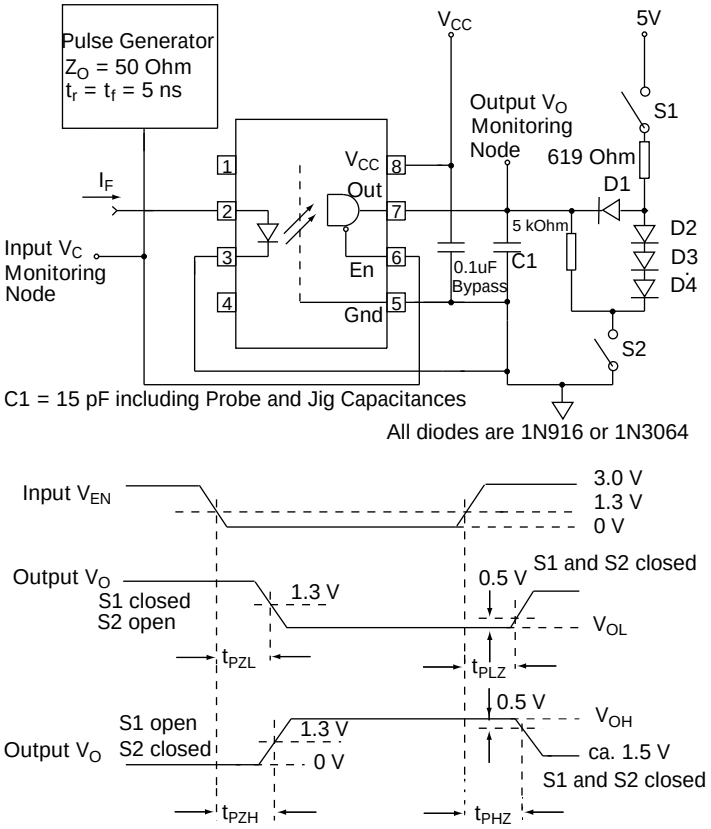


Figure 30. Test circuit for common mode transient immunity and typical waveforms—SFH 6700/01/02/11/12/19

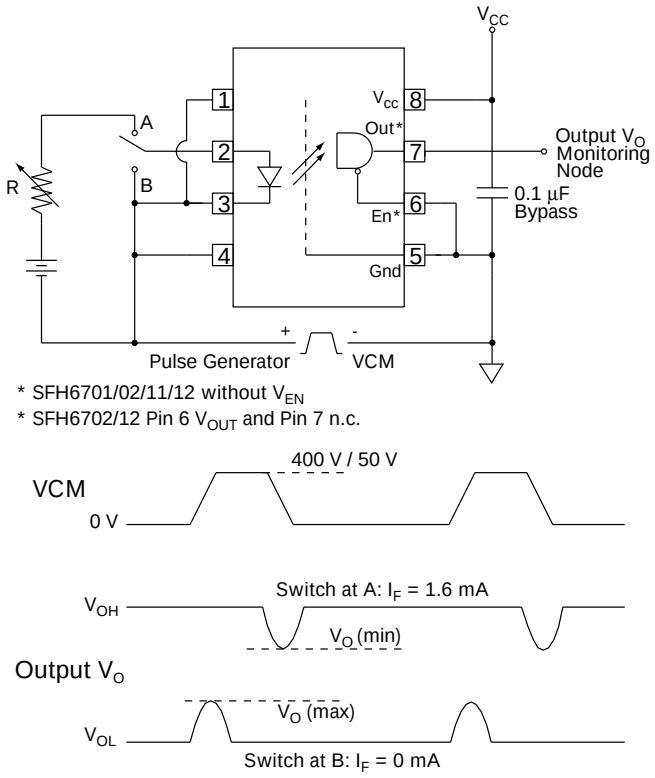


Figure 31. Test circuit for common modetransient immunity and typical waveforms—SFH6705$_L$