

# MAX38888

# Super Cap Regulator

## General Description

The MAX38888 is a super cap backup regulator designed to efficiently transfer power between a super cap and a system supply rail.

When the main battery is present and above the minimum system supply voltage, the regulator charges the super cap at up to a 500mA rate. Once the super cap is charged, the circuit draws only 2.5µA of current while it maintains the super cap in its ready state. When the main battery is removed, the regulator prevents the system from dropping below the minimum operating voltage, discharging the super cap at up to a 2.5A rate.

The MAX38888 is externally programmable for minimum and maximum super cap voltage, minimum system voltage, and maximum charge and discharge currents. The internal DC/DC converter requires only a 1µH inductor.

The MAX38888 is offered in a 14-pin TDFN package.

## Benefits and Features

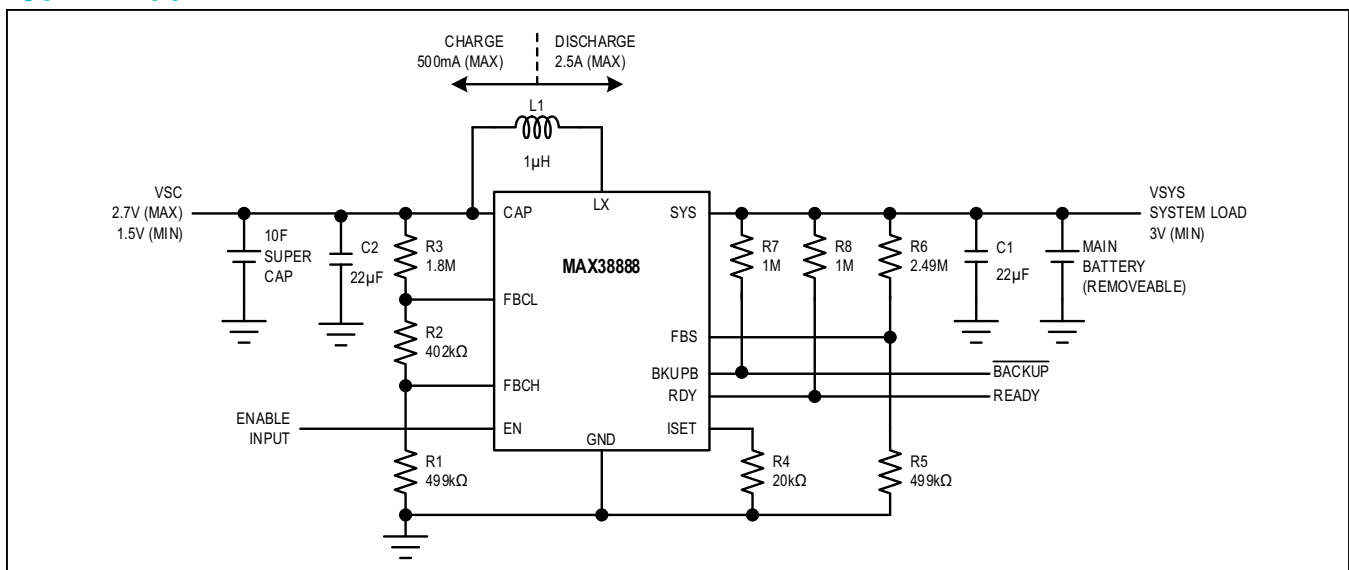
- 2.5V to 5V System Output Voltage
- 0.8V to 5V Super Cap Voltage Range
- Up to 2.5A Peak Discharge Current
- Programmable Voltage and Current Thresholds
- ±2% Threshold Accuracy
- Up to 95% Efficiency, Charge or Discharge
- 2.5µA Ready Quiescent Current
- Small Solution Size
- 3mm x 3mm x 0.75mm TDFN Package

*Ordering Information appears at end of data sheet.*

## Applications

- Handheld Industrial Equipment
- Portable Computers
- Portable Devices with a Removable Battery

## Typical Application Circuit



### Absolute Maximum Ratings

CAP, EN, SYS, LX, BKUPB, RDY to GND.....	-0.3V to +6V	Operating Temperature Range.....	-40°C to +125°C
FBCH, FBCL to GND .....	-0.3V to CAP + 0.3V	Storage Temperature Range.....	-65°C to +150°C
FBS, ISET to GND .....	-0.3V to SYS + 0.3V	Maximum Junction Temperature .....	+150°C
PGND to GND .....	-0.3V to +0.3V	Lead Temperature (soldering, 10 seconds).....	+300°C
Continuous Power Dissipation (T <sub>A</sub> = +70°C, TDFN, derate 24.4mW/°C above +70°C).....	1951.2mW	LX RMS Current.....	±2.0A <sub>RMS</sub>
		Output Short-Circuit Duration .....	Continuous

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

### Package Information

#### TDFN

Package Code	T1433+2C
Outline Number	<a href="#">21-0137</a>
Land Pattern Number	<a href="#">90-0063</a>
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient (θ <sub>JA</sub> )	41°C/W
Junction to Case (θ <sub>JC</sub> )	8°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## Electrical Characteristics

( $V_{SYS} = 3.7V$ ,  $V_{CAP} = 2.7V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$  (typical values at  $T_J = 25^{\circ}C$ ), circuit of [Figure 1](#), unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYS Voltage Range	$V_{SYS}$		2.5		5	V
CAP Voltage Range	$V_{VSC}$		0.8		5	V
SYS Shutdown Current	$I_{SYS\_SD}$	EN = 0V, $T_A = 25^{\circ}C$		0.01	1	$\mu A$
		EN = 0V		0.1		
SYS Charging Supply Current	$I_{SYS\_CHG}$	$V_{FBS} = 0.6V$ , $V_{FBCH} = V_{FBCL} = 0.485V$		1.5		mA
SYS Backup Supply Current	$I_{SYS\_BUP}$	$V_{FBS} = V_{FBCH} = V_{FBCL} = 0.515V$ , $T_A = 25^{\circ}C$		35	65	$\mu A$
		$V_{FBS} = V_{FBCH} = V_{FBCL} = 0.515V$		35		
SYS Ready Supply Current	$I_{SYS\_RDY}$	$V_{FBS} = 0.6V$ , $V_{FBCH} = V_{FBCL} = 0.515V$ , $T_A = 25^{\circ}C$		2.5	5	$\mu A$
		$V_{FBS} = 0.6V$ , $V_{FBCH} = V_{FBCL} = 0.515V$		2.5		
CAP Shutdown Current	$I_{CAP\_SD}$	EN = 0V, $T_A = 25^{\circ}C$		0.01	1	$\mu A$
		EN = 0V		0.1		
UVLO Threshold	$V_{UVLOF}$	$V_{SYS}$ falling, 100mV typical hysteresis	1.7	1.8	1.9	V
FBS Backup Voltage	$V_{FBS}$	FBS rising, when discharging stops	-2%	0.5	+2%	V
FBS Charging Threshold	$V_{TH\_FBS\_CHG}$	Above FBS Backup Voltage, when charging begins, 30mV typical hysteresis	25	60	95	mV
FBCH Threshold	$V_{TH\_FBCH}$	FBCH rising, when charging stops, 25mV typical hysteresis	-2%	0.5	+2%	V
FBCL Threshold	$V_{TH\_FBCL}$	FBCL falling, when preserve mode starts, 25mV typical hysteresis	-3.5%	0.475	+3.5%	V
EN Threshold	$V_{IL}$	When LX stops switching, EN falling	225	600		mV
	$V_{IH}$	EN rising		660	925	
ISET Resistor Range	$R_{ISET}$	Guaranteed by LX Peak Current Limits	20		100	k $\Omega$
LX Peak Backup Current Limit (Note 1)	$I_{DCHG}$	Circuit of <a href="#">Figure 1</a> , $V_{CAP} = 2V$ , $V_{SYS} = 2.9V$ , $R_{ISET} = 20k\Omega$	2.0	2.5	3.0	A
		Circuit of <a href="#">Figure 1</a> , $V_{CAP} = 2V$ , $V_{SYS} = 2.9V$ , $R_{ISET} = 100k\Omega$		0.50		
LX Peak Charge Current Limit (Note 1)	$I_{CHG}$	Circuit of <a href="#">Figure 1</a> , $V_{SYS} = 3.7V$ , $V_{CAP} = 2V$ , $R_{ISET} = 20k\Omega$	400	500	600	mA
		Circuit of <a href="#">Figure 1</a> , $V_{SYS} = 3.7V$ , $V_{CAP} = 2V$ , $R_{ISET} = 100k\Omega$		100		
FBS/FBCH/FBCL Input Bias Current	$I_{FBS/FBCH/FBCL}$	$V_{FBS/FBCH/FBCL} = 0.5V$ , $T_A = 25^{\circ}C$	-0.1	0.001	0.1	$\mu A$
		$V_{FBS/FBCH/FBCL} = 0.5V$		0.01		

### Electrical Characteristics (continued)

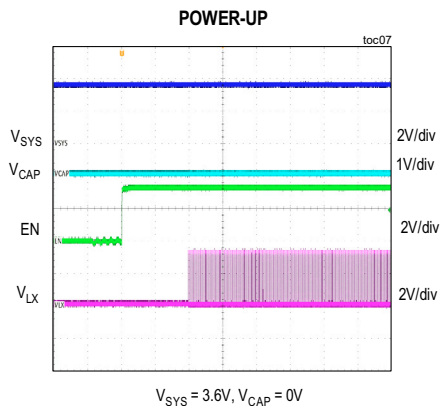
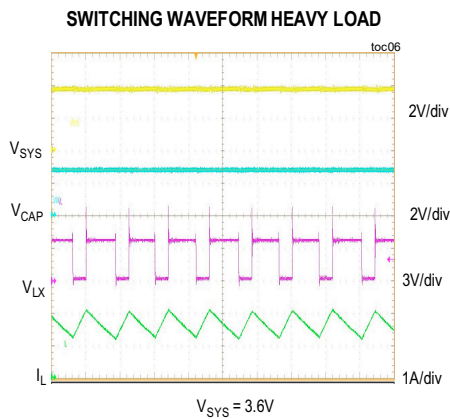
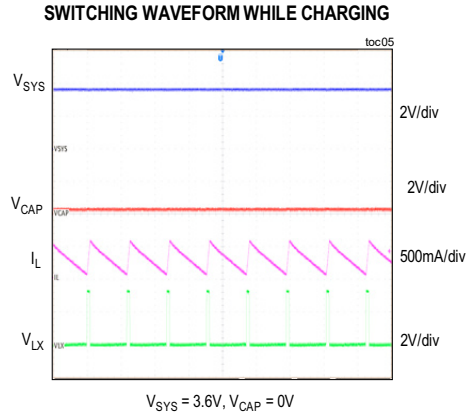
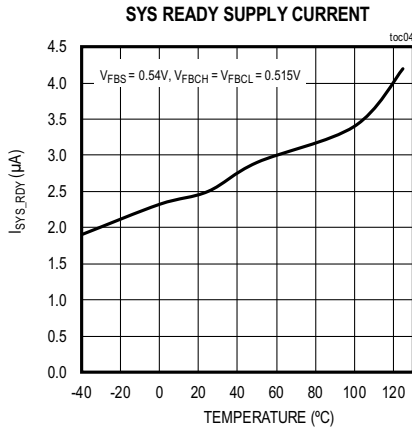
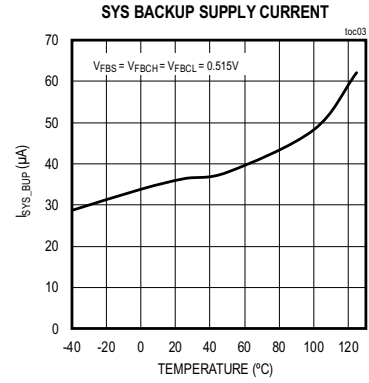
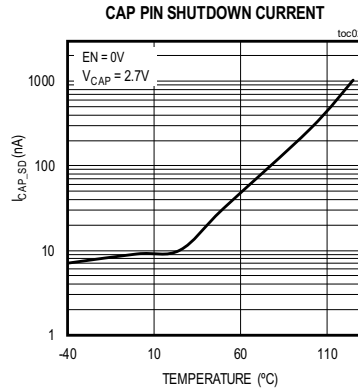
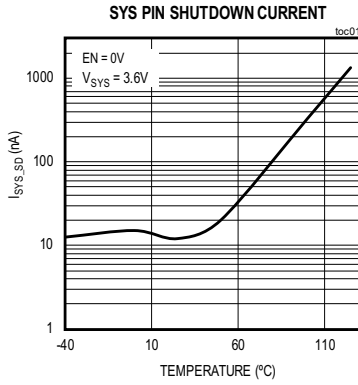
( $V_{SYS} = 3.7V$ ,  $V_{CAP} = 2.7V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$  (typical values at  $T_J = 25^{\circ}C$ ), circuit of [Figure 1](#), unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN Input Leakage Current	$I_{EN}$	$0V < V_{EN} < 5.5V$ , $T_A = 25^{\circ}C$	-0.1	0.001	0.1	$\mu A$
		$0V < V_{EN} < 5.5V$		0.01		
LX Switching Frequency	$f_{SW}$	Delivering maximum current from CAP		2		MHz
LX Low-Side FET Resistance	$R_{LOW}$	$V_{SYS} = 3V$ , LX switched to GND		50	100	m $\Omega$
LX High-Side FET Resistance	$R_{HIGH}$	$V_{SYS} = 3V$ , LX switched to SYS		80	160	m $\Omega$
LX Leakage Current	$I_{LX\_LKG}$	$V_{EN} = 0V$ , $V_{SYS} = 5V$ , $V_{LX} = 0V/5V$ , $T_A = 25^{\circ}C$	-1		1	$\mu A$
		$V_{EN} = 0V$ , $V_{SYS} = 5V$ , $V_{LX} = 0V/5V$		0.1		
Maximum On-Time	$t_{ON}$	Backup Mode, $V_{FBS} = 0.485V$	320	400	480	ns
Minimum Off-Time	$t_{OFF}$	Backup Mode, $V_{FBS} = 0.485V$	80	100	120	ns
Overtemperature Lockout Threshold	$T_{OTLO}$	$T_J$ rising, $15^{\circ}C$ typical hysteresis		165		$^{\circ}C$
High-Side FET Zero-Crossing	$I_{ZXP}$	Circuit of <a href="#">Figure 1</a> , $V_{CAP} = 2V$ , $V_{SYS} = 2.9V$ , Note 1	25	50	75	mA
Low-Side FET Zero-Crossing	$I_{ZYN}$	Circuit of <a href="#">Figure 1</a> , $V_{SYS} = 3.7V$ , $V_{CAP} = 2V$ , Note 1	25	50	75	mA
BKUPB Leakage Current	$I_{BKUPB}$	$V_{EN} = 0V$ , $V_{BKUPB} = 5V$ , $T_A = 25^{\circ}C$	-1		1	$\mu A$
		$V_{EN} = 0V$ , $V_{BKUPB} = 5V$		0.1		
BKUPB Output Voltage Low	$V_{BKUPB\_L}$	$V_{FBS} = 0.48V$ , $V_{FBCH} = V_{FBCL} = 0.515V$ , $I_{SINK} = 2mA$			0.4	V
RDY Leakage Current	$I_{RDY}$	$V_{FBCH} = 0.54V$ , $V_{RDY} = 5V$ , $T_A = 25^{\circ}C$	-1		1	$\mu A$
		$V_{FBCH} = 0.54V$ , $V_{RDY} = 5V$		0.1		
RDY Output Voltage Low	$V_{RDY\_L}$	$V_{EN} = 0V$ , $I_{SINK} = 2mA$			0.4	V

**Note 1:** DC measurement, actual peak current accuracy in circuit will be affected by the propagation delay time.

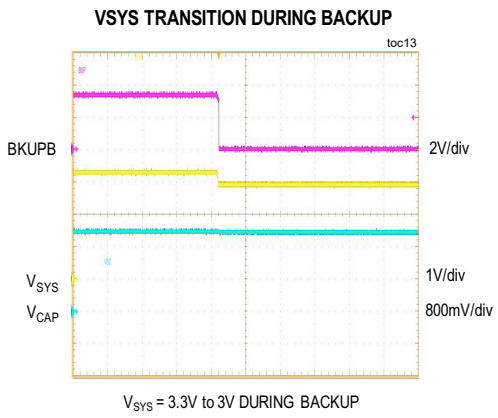
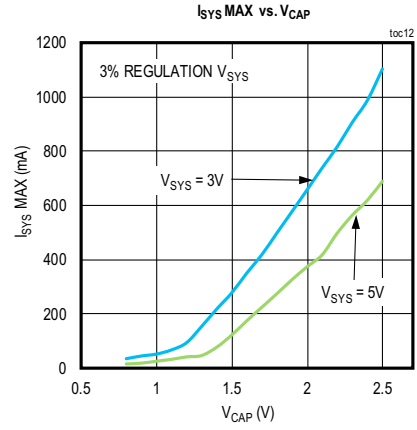
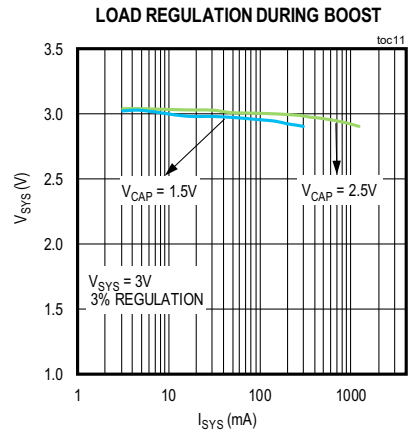
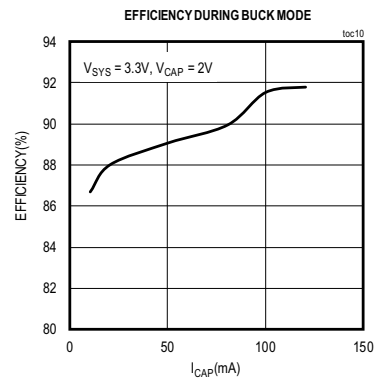
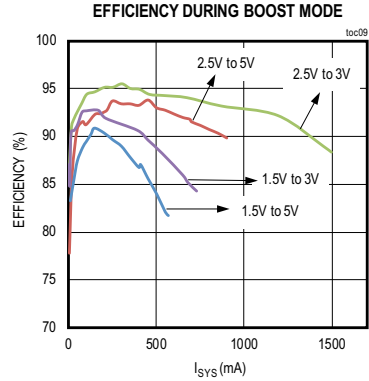
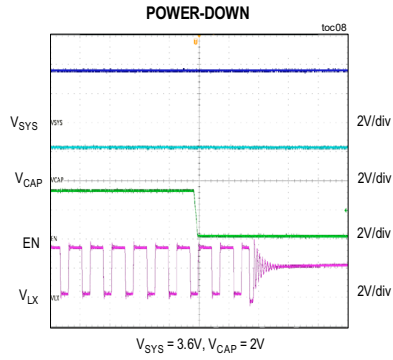
Typical Operating Characteristics

(MAX38888,  $V_{SYS} = 3.6V$ ,  $V_{CAP} = 2.0V$ ,  $C1 = 22\mu F$ ,  $C2 = 22\mu F$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

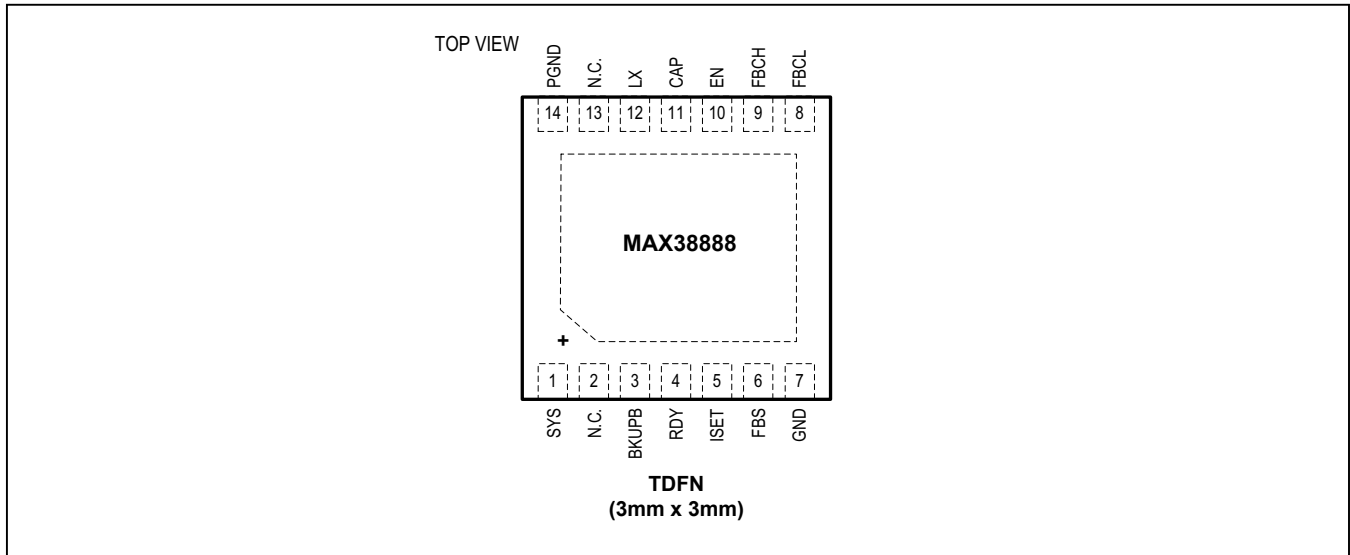


Typical Operating Characteristics (continued)

(MAX38888,  $V_{SYS} = 3.6V$ ,  $V_{CAP} = 2.0V$ ,  $C1 = 22\mu F$ ,  $C2 = 22\mu F$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



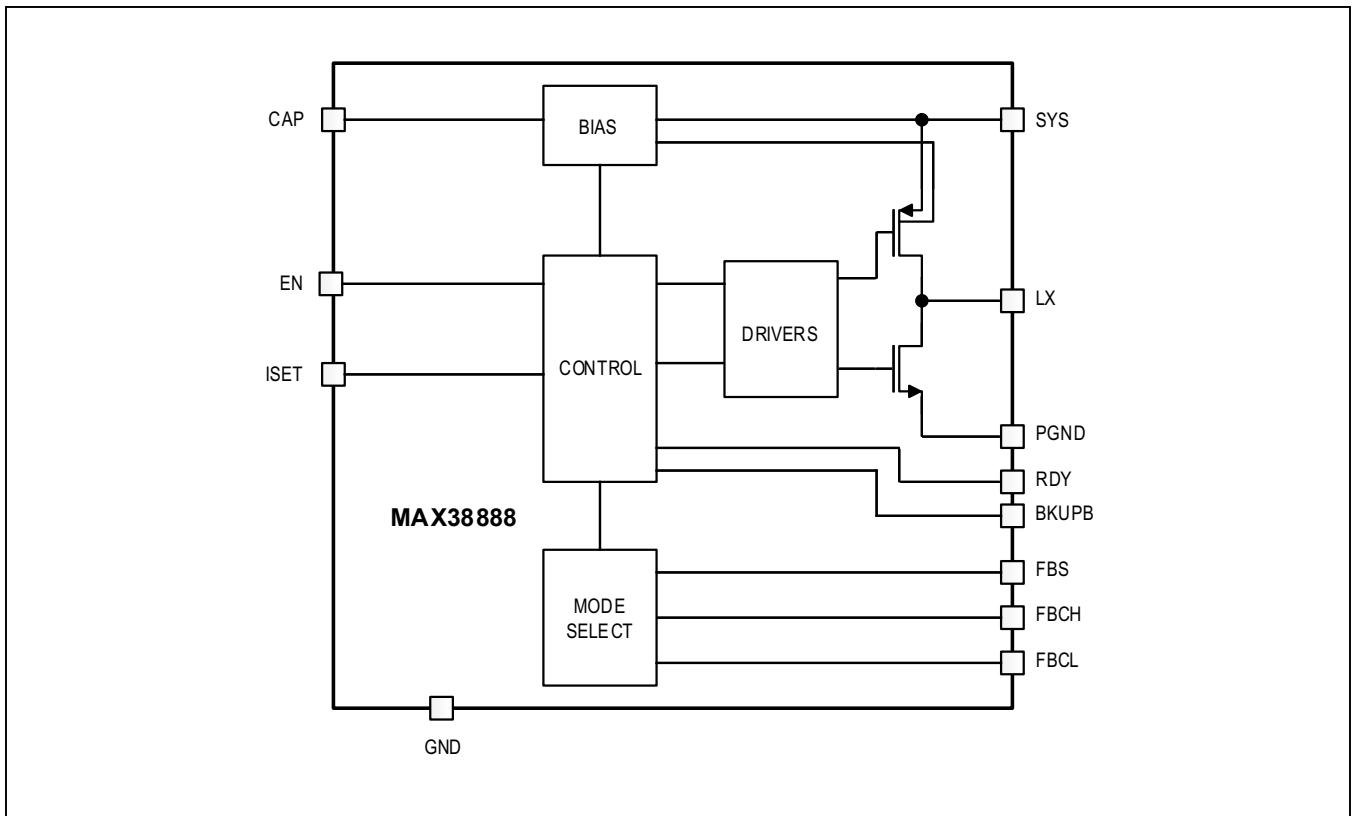
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	SYS	System Supply Rail. Connect to a system supply rail or removable battery between 2.5V and 5V and bypass with a 22µF capacitor to GND.
2	NC	No Connect.
3	BKUPB	Open-Drain Backup Indicator. BKUPB is held low when the part is in backup mode i.e. when $FBS < 0.5V$ and $FBCL > 0.5V$ . BKUPB is released High when $FBCL < 0.475V$ or $FBS > 0.56V$ . Connect to external pullup resistor.
4	RDY	Open-Drain Supercap Ready Indicator. RDY goes high when the supercap is fully charged (i.e., $FBCH > 0.5V$ ). RDY is pulled low when $FBCL < 0.475V$ . Connect to an external pullup resistor.
5	ISET	Charge/Discharge Current Input. The peak discharge current is set by $50kV/R_{ISET}$ while the peak charging current is 1/5 the discharging current.
6	FBS	SYS Feedback. Connect to the center point of a resistor divider from SYS to GND. SYS will boost to $0.5V \times (1 + R_{STop}/R_{SBot})$ when $V_{FBS} < 0.5V$ .
7	GND	Analog Ground.
8	FBCL	CAP Feedback. Connect to the upper point of a resistor divider from CAP to GND. Part enters preserve mode when $V_{FBCL} < 0.475V$ .
9	FBCH	CAP Feedback. Connect to the lower point of a resistor divider from CAP to GND. CAP will charge to $0.5V \times (1 + R_{CTop}/R_{CBot})$ when $V_{FBS} > 0.56V$ .
10	EN	Enable Input. Force this pin high to enable the regulator or force pin low to disable the part and enter shutdown. If not driven, tie it to the SYS rail.
11	CAP	Super Cap. Connect to a super cap rated between 0.8V to 5V with a maximum voltage less than $V_{SYS}$ .
12	LX	Inductor Switching Node. Connect a 1.0µH to 4.7µH inductor from LX to CAP.
13	NC	No Connect.
14, EP	PGND	Power Ground.

Functional Diagrams





### Detailed Description

The MAX38888 is a flexible super cap backup regulator efficiently transferring power between a super cap and a system supply rail.

When the main battery is present and its voltage above the minimum system supply voltage, the regulator operates in the charging mode of operation and charges the super cap at up to a 500mA rate. Once the super cap is charged, the RDY flag will assert and the circuit will draw only 2.5µA of current while maintaining the super cap in its ready state.

When the main battery is removed, the regulator prevents the system from dropping below the minimum operating voltage, boosting V<sub>SYS</sub> by discharging the super cap at up to a 2.5A rate. During this backup mode of operation, the MAX38888 utilizes a fixed on-time, current-limited, pulse-frequency-modulation (PFM) control scheme. Once MAX38888 is in the backup mode, the BKUPB flag is asserted.

The external pins allow a wide range of system and super cap voltage settings as well as charging and discharging current settings.

The MAX38888 implements a true shutdown feature disconnecting V<sub>SYS</sub> from V<sub>CAP</sub> as well as protecting against a SYS short or if V<sub>CAP</sub> > V<sub>SYS</sub>.

### Application Circuit

The typical application of the MAX38888 is shown in [Figure 1](#).

### Super Cap Voltage Configuration

The maximum super cap voltage is set using a resistor divider from CAP to FBCH to GND. Recommended value for R2 is 499kΩ. Because resistor tolerance will have direct effect on voltage accuracy, these resistors should have 1% accuracy or better.

$$R2 + R3 = R1 \times ((V_{CAP\ MAX}/0.5) - 1)$$

V<sub>CAP</sub> halts charging when V<sub>FBCH</sub> reaches 0.5V. The maximum super cap voltage is where the super cap will remain after the super cap is completely charged and ready for backup.

The minimum super cap discharge voltage is set using a resistor divider from CAP to FBCL to GND.

$$R3 = (R1 + R2) \times ((V_{CAP\ MIN}/0.5) - 1)$$

FBCL prevents the super cap from further discharge when V<sub>FBCL</sub> reaches 0.475V during a backup event in order to preserve the remaining capacity for keeping alive a real-time clock, memory, or other low-level function. In this preserve mode, the IC disconnects all circuitry from the super cap and draws 2.5µA current from it.

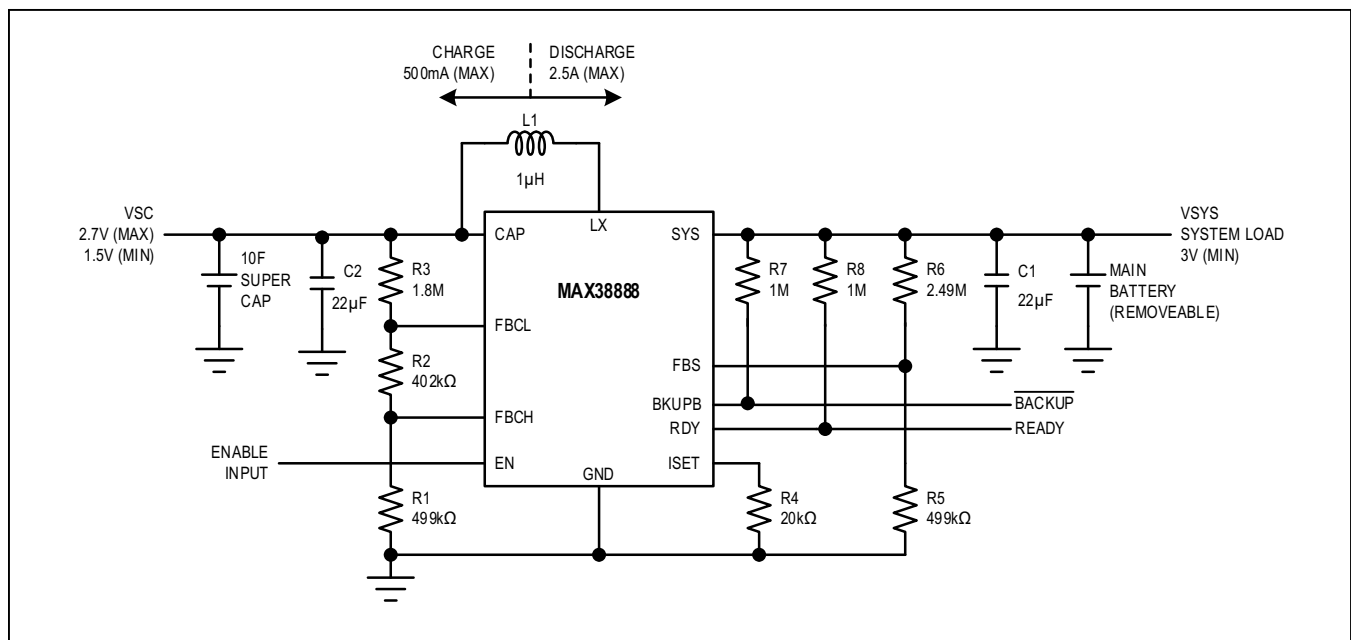


Figure 1. Typical Application

In applications where SYS voltage needs to be boosted to higher levels, selecting  $V_{CAP}$  min has to take into account duty cycle limitation of the boosting phase which is 80%.

MAX38888 detects when  $V_{SYS}$  falls below  $V_{CAP}$ . The device will not enable if  $V_{SYS}$  is below  $V_{CAP}$ . Raising  $V_{SYS}$  above the backup threshold re-initiates charging and backup.

**System Voltage Configuration**

The minimum system voltage is set using a resistor divider from SYS to FBS to GND. Recommended value for R5 is 499kΩ. Because resistor tolerance will have direct effect on voltage accuracy, these resistors should have 1% accuracy or better.

$$R6 = R5 \times ((V_{SYS\ MIN}/0.5) - 1)$$

When  $V_{FBS}$  is above 0.56V, the DCDC regulator will draw power from the SYS pin to charge the super cap to the

maximum voltage set by FBCH and be ready for backup. When the main battery is removed,  $V_{FBS}$  drops to 0.5V and the SYS pin is regulated to the programmed minimum voltage with up to 2A of CAP current.

**Charge/Discharge Current Configuration**

The peak discharge current is set by placing a resistor from ISET to GND. The values of  $R_{ISET}$  resistor is calculated by following formula:

$$I_{DISCHARGE} = 2.5A \times (20k\Omega/R_{ISET})$$

The super cap charging current is internally set to 1/5 of the discharge current.

$$I_{CHARGE} = 0.5A \times (20k\Omega/R_{ISET})$$

Value of  $R_{ISET}$  between 20kΩ and 100kΩ is recommended to ensure accurate current compliance.

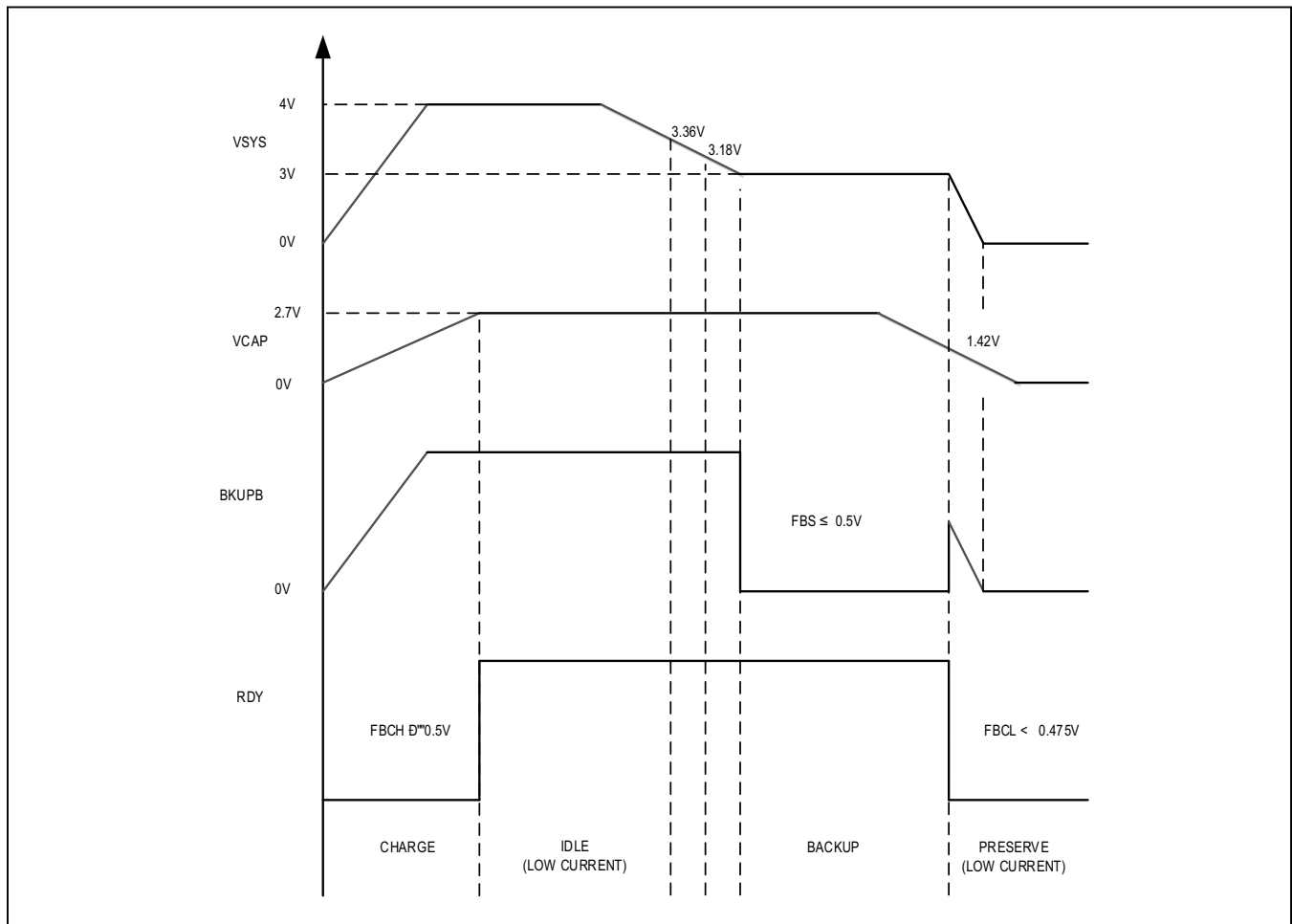


Figure 2. System Waveforms

**System Waveforms**

The waveforms in [Figure 2](#) represent system behavior of MAX38888 in the [Typical Application Circuits](#).

**Charging/Discharging Waveforms**

Assuming the typical application circuit, the rate of super capacitor discharge is calculated as:

$$dV/dt = I_{CAP}/C$$

where,

$I_{CAP}$  is an average current sourced by super capacitor which is 2A in this example.

C is capacitance of the super capacitor.

The SYS and CAP voltages would vary as in the application circuit ([Figure 3](#)).

**Applications Information**

**Capacitor Selection**

Capacitors at SYS and CAP pins reduce current peaks and increase efficiency. Ceramic capacitor are recommended because they have the lowest equivalent series resistance (ESR), smallest size, and lowest cost. Choose an acceptable dielectric such as X5R or X7R. Due to

ceramic capacitors' capacitance derating with DC bias standard 22µF ceramic capacitors are recommended at both pins for most applications.

**Inductor Selection**

MAX38888 works with 1µH inductor in most applications. In applications where lower peak currents are desired, larger inductance may be used in order to reduce the ripple. Recommended inductance range is from 1µH to 4.7µH. Select 4.7µH for higher RISET value [100k]. 1µH is not supported for 100k RISET value.

**Status Flags**

MAX38888 has two dedicated pins to report the device status to the host processor. Ready Output (RDY), which will be high when the super cap is fully charged (i.e., FBCH > 0.5V). RDY is pulled low when FBCL < 0.475V. The other status flag is the Backup Output (BKUPB), which will be held low when the part is in the backup mode (i.e., when FBS < 0.5V and FBCL > 0.5V). BKUPB is released high when FBCL < 0.475V or FBS > 0.56V. Both output pins are open-drain type and require external pullup resistors. Recommended values for the pullup resistors are 1MΩ. The pins should be pulled up to the SYS rail.

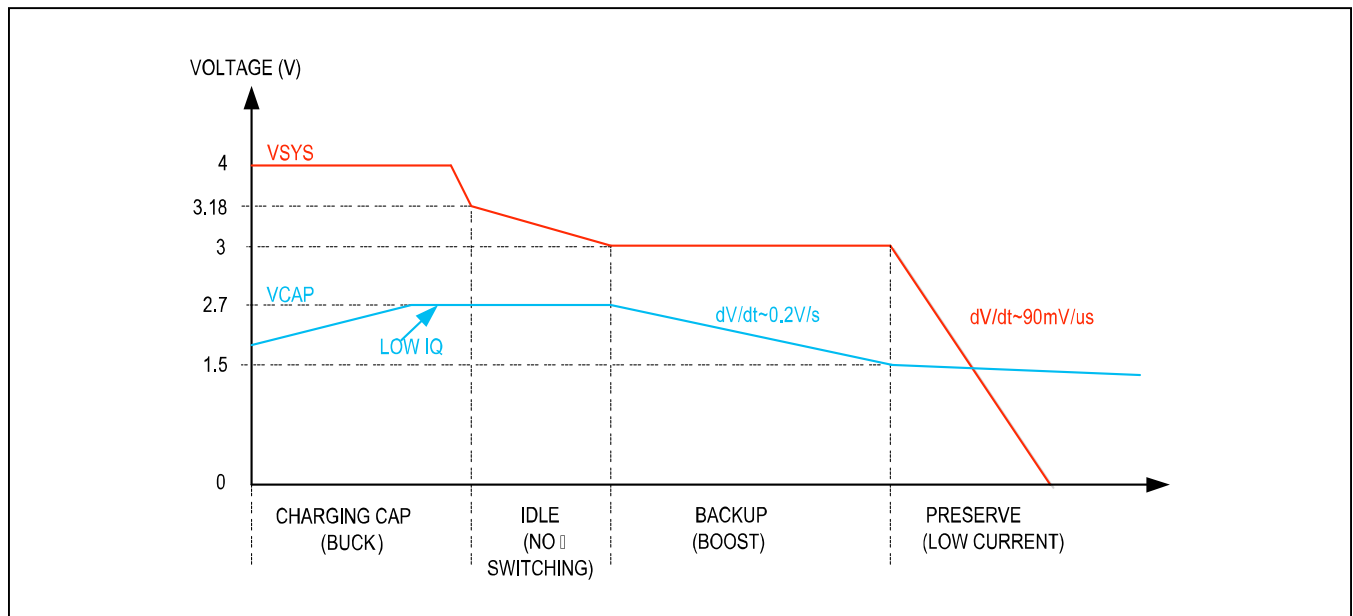


Figure 3. Charging/Discharging Waveforms

### Enabling Device

MAX3888 has dedicated enable pin. The pin can either be driven by a digital signal or pulled up or strapped to the SYS rail.

### PCB Layout Guidelines

Minimize trace lengths to reduce parasitic capacitance, inductance and resistance, and radiated noise. Keep the main power path from SYS, LX, CAP, and PGND as tight and short as possible. Minimize the surface area used for LX since this is the noisiest node. The trace between the feedback resistor dividers should be as short as possible and should be isolated from the noisy power path. Refer to the EV kit layout for best practices.

The PCB layout is important for robust thermal design. The junction to ambient thermal resistance of the package greatly depends on the PCB type, layout, and pad connections. Using thick PCB copper and having the SYS, LX, CAP, and PGND copper pours will enhance the thermal performance. The TDFN package has a large thermal pad under the package which creates excellent thermal path to PCB. This pad is electrically connected to PGND. Its PCB pad should have multiple thermal vias connecting the pad to internal PGND plane. Thermal vias should either be capped or have small diameter to minimize solder wicking and voids.

## Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	FEATURES
MAX38888ATD+	-40°C to +125°C	14 TDFN	Enable Input, Selectable Voltages and Currents

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/18	Initial release	—
1	7/18	Updated <i>General Description</i> and <i>Benefits and Features</i>	1

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at [www.maximintegrated.com](http://www.maximintegrated.com).

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