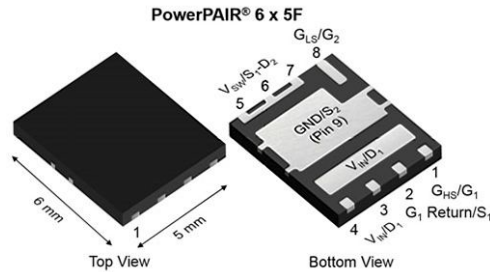


Dual N-Channel 25 V (D-S) MOSFET with Schottky Diode



FEATURES

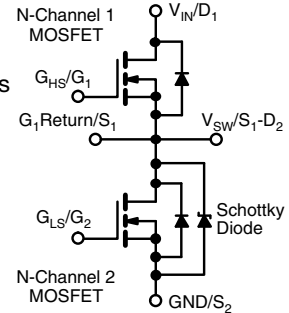
- TrenchFET® Gen IV power MOSFET
- SkyFET® low side MOSFET with integrated Schottky Diode
- G₁ return/S₁ pin for enhancing high side driving
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- CPU core power
- Computer / server peripherals
- POL
- Synchronous buck converter
- Telecom DC/DC



PRODUCT SUMMARY		
	CHANNEL-1	CHANNEL-2
V _{DS} (V)	25	25
R _{DS(on)} max. (Ω) at V _{GS} = 10 V	0.00380	0.00090
R _{DS(on)} max. (Ω) at V _{GS} = 4.5 V	0.00620	0.00150
Q _g typ. (nC)	6.6	31
I _D (A) ^a	40	60
Configuration	Dual	

ORDERING INFORMATION	
Package	PowerPAIR 6 x 5F
Lead (Pb)-free and halogen-free	SiZF914DT-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	CHANNEL-1	CHANNEL-2	UNIT	
Drain-source voltage	V _{DS}	25	25	V	
Gate-source voltage	V _{GS}	+20, -16	+16, -12		
Continuous drain current (T _J = 150 °C)	I _D	T _C = 25 °C	40 ^a	60 ^a	A
		T _C = 70 °C	40 ^a	60 ^a	
		T _A = 25 °C	23.5 ^{b, c}	52 ^{b, c}	
		T _A = 70 °C	19 ^{b, c}	42 ^{b, c}	
Pulsed drain current (t = 100 μs)	I _{DM}	130	110	A	
Continuous source-drain diode current	I _S	T _C = 25 °C	22		60 ^a
		T _A = 25 °C	2.8 ^{b, c}	6.7 ^{b, c}	
Single pulse avalanche current	I _{AS}	20	34	mJ	
Single pulse avalanche energy	E _{AS}	20	58		
Maximum power dissipation	P _D	T _C = 25 °C	26.6	60	W
		T _C = 70 °C	17	38	
		T _A = 25 °C	3.4 ^{b, c}	4 ^{b, c}	
		T _A = 70 °C	2.2 ^{b, c}	2.6 ^{b, c}	
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +150		°C	
Soldering recommendations (peak temperature) ^{d, e}		260			

THERMAL RESISTANCE RATINGS							
PARAMETER	SYMBOL	CHANNEL-1		CHANNEL-2		UNIT	
		TYP.	MAX.	TYP.	MAX.		
Maximum junction-to-ambient ^{b, f}	t ≤ 10 s	R _{thJA}	30	37	25	31	°C/W
Maximum junction-to-case (source)	Steady state	R _{thJC}	3.8	4.7	1.7	2.1	

Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- t = 10 s
- See solder profile (www.vishay.com/doc?73257). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 77 °C/W for channel-1 and 68 °C/W for channel-2



SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)									
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT			
Static									
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-1	25	-	-	V		
			Ch-2	25	-	-			
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-1	1.1	-	2.4			
			Ch-2	1.1	-	2.2			
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = +20\text{ V}, -16\text{ V}$	Ch-1	-	-	± 100	nA		
		$V_{DS} = 0\text{ V}, V_{GS} = +16\text{ V}, -12\text{ V}$	Ch-2	-	-	± 100			
Zero Gate voltage drain current	I_{DSS}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}$	Ch-1	-	-	1	μA		
			Ch-2	-	30	350			
		$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-1	-	-	5			
			Ch-2	-	200	3000			
On-state drain current ^b	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-1	20	-	-	A		
			Ch-2	20	-	-			
Drain-source on-state resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	Ch-1	-	0.00270	0.00380	Ω		
		$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	Ch-2	-	0.00060	0.00090			
		$V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$	Ch-1	-	0.00410	0.00620			
		$V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$	Ch-2	-	0.00095	0.00150			
Forward transconductance ^b	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-1	-	45	-	S		
		$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-2	-	105	-			
Dynamic ^a									
Input capacitance	C_{iss}	Channel-1 $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1	-	1050	-	μF		
			Ch-2	-	4670	-			
Output capacitance	C_{oss}		Ch-1	-	510	-	μF		
			Ch-2	-	1650	-			
Reverse transfer capacitance	C_{rss}		Channel-2 $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1	-	47	-	μF	
				Ch-2	-	370	-		
C_{rss}/C_{iss} ratio				Ch-1	-	0.036	0.072		
				Ch-2	-	0.062	0.125		
Total gate charge	Q_g			$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	Ch-1	-	14	21	nC
					Ch-2	-	65	98	
Gate-source charge	Q_{gs}	Channel-1 $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		Ch-1	-	6.6	10	nC	
				Ch-2	-	31	47		
Gate-drain charge	Q_{gd}			Ch-1	-	3.2	-		
				Ch-2	-	10.2	-		
Output charge	Q_{oss}	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}$	Ch-1	-	7.5	-	nC		
			Ch-2	-	27	-			
Gate resistance	R_g	$f = 1\text{ MHz}$	Ch-1	0.2	1	2	Ω		
			Ch-2	0.1	0.3	0.6			



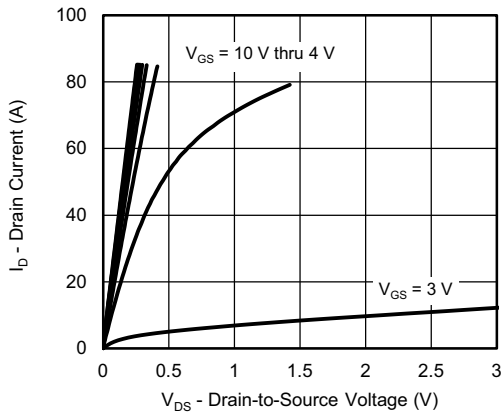
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Dynamic ^a							
Turn-on delay time	$t_{d(on)}$	Channel-1 $V_{DD} = 10\text{ V}, R_L = 2\ \Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\ \Omega$ Channel-2 $V_{DD} = 10\text{ V}, R_L = 2\ \Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\ \Omega$	Ch-1	-	20	40	ns
			Ch-2	-	32	60	
Rise time	t_r		Ch-1	-	50	100	
			Ch-2	-	60	120	
Turn-off delay time	$t_{d(off)}$		Ch-1	-	15	30	
			Ch-2	-	45	90	
Fall time	t_f		Ch-1	-	10	20	
			Ch-2	-	15	30	
Turn-on delay time	$t_{d(on)}$		Ch-1	-	12	25	
			Ch-2	-	16	30	
Rise time	t_r		Ch-1	-	5	10	
			Ch-2	-	30	60	
Turn-off delay time	$t_{d(off)}$	Ch-1	-	20	40		
		Ch-2	-	40	80		
Fall time	t_f	Ch-1	-	5	10		
		Ch-2	-	6	15		
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	$T_C = 25\text{ }^\circ\text{C}$	Ch-1	-	-	22	A
			Ch-2	-	-	60	
Pulse diode forward current ^a	I_{SM}		Ch-1	-	-	130	A
			Ch-2	-	-	110	
Body diode voltage	V_{SD}	$I_S = 5\text{ A}, V_{GS} = 0\text{ V}$	Ch-1	-	0.8	1.2	V
		$I_S = 3\text{ A}, V_{GS} = 0\text{ V}$	Ch-2	-	0.38	0.6	
Body diode reverse recovery time	t_{rr}	Channel-1 $I_F = 5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$ Channel-2 $I_F = 5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	Ch-1	-	36	70	ns
			Ch-2	-	66	130	
Body diode reverse recovery charge	Q_{rr}		Ch-1	-	36	50	nC
			Ch-2	-	72	150	
Reverse recovery fall time	t_a		Ch-1	-	20	-	ns
			Ch-2	-	30	-	
Reverse recovery rise time	t_b	Ch-1	-	16	-		
		Ch-2	-	36	-		

Notes

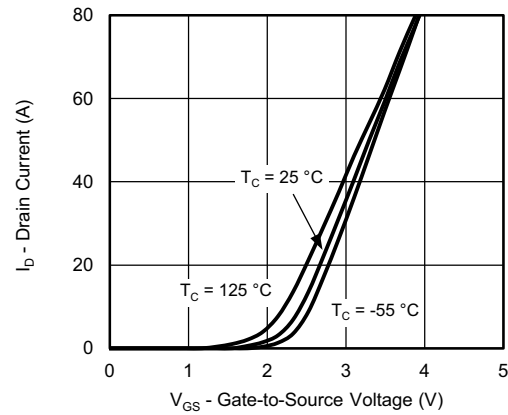
- a. Guaranteed by design, not subject to production testing
- b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

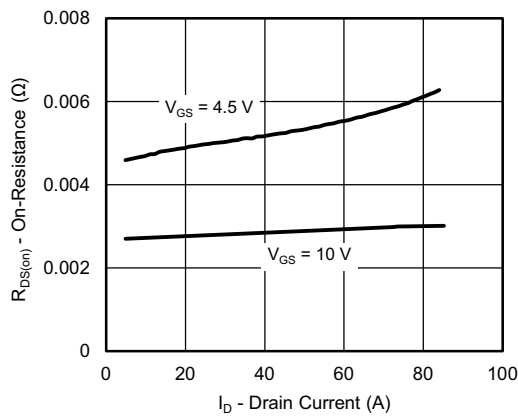
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



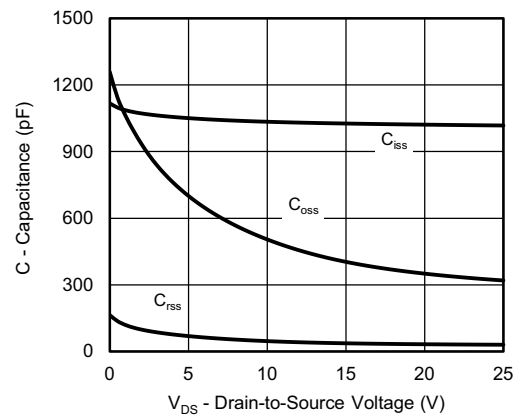
Output Characteristics



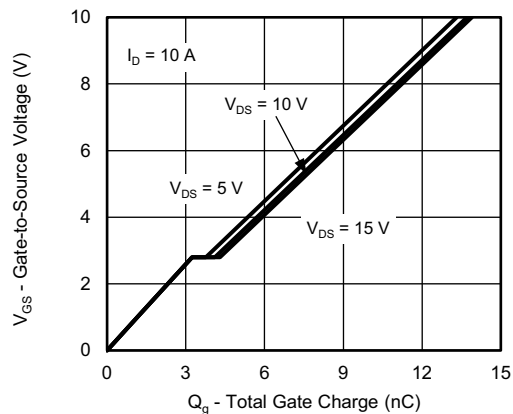
Transfer Characteristics



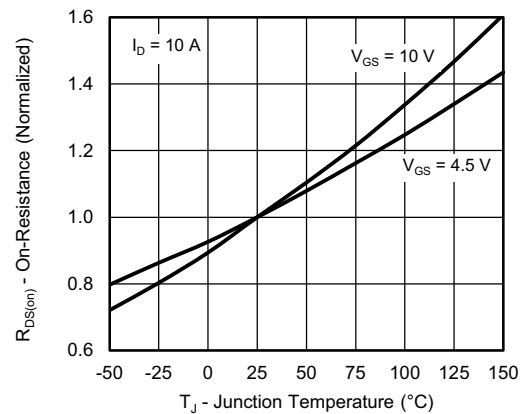
On-Resistance vs. Drain Current



Capacitance



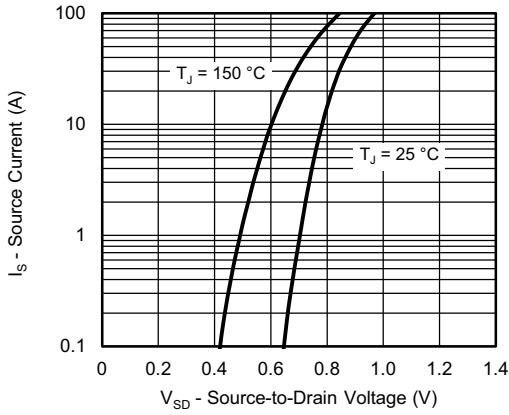
Gate Charge



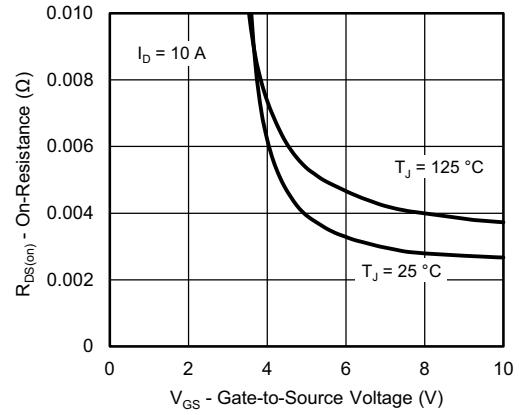
On-Resistance vs. Junction Temperature



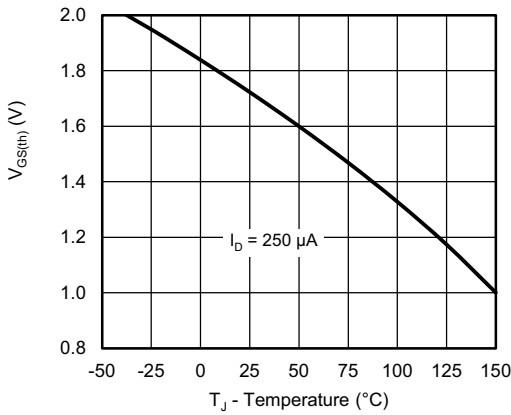
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



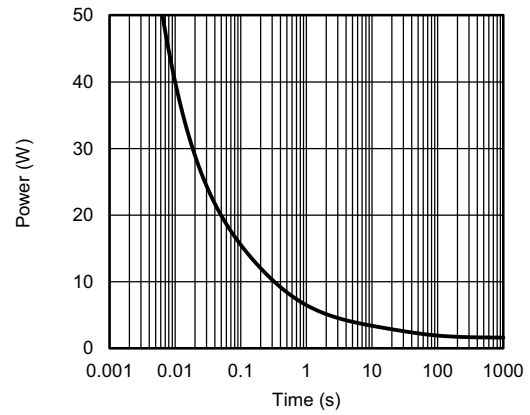
Source-Drain Diode Forward Voltage



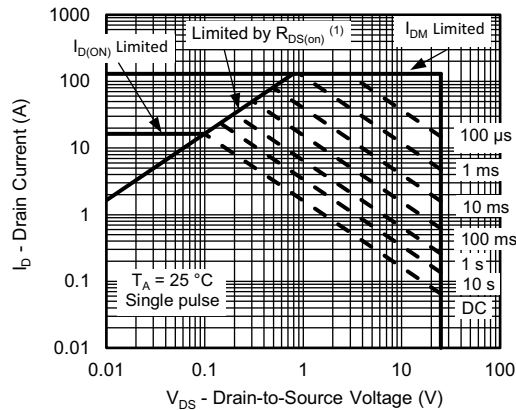
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



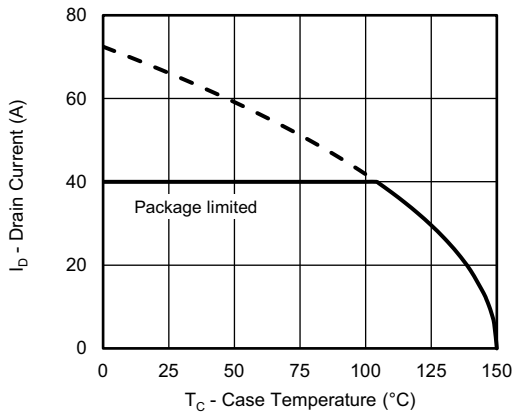
Single Pulse Power, Junction-to-Ambient



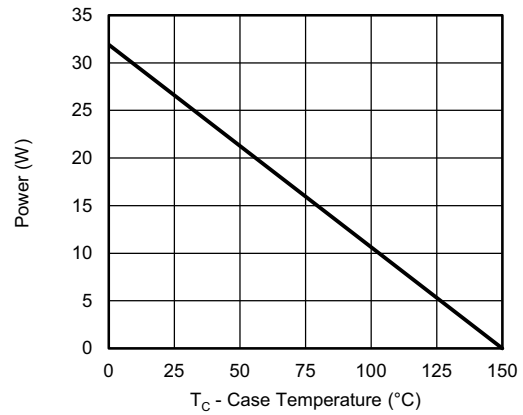
Safe Operating Area, Junction-to-Ambient



CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



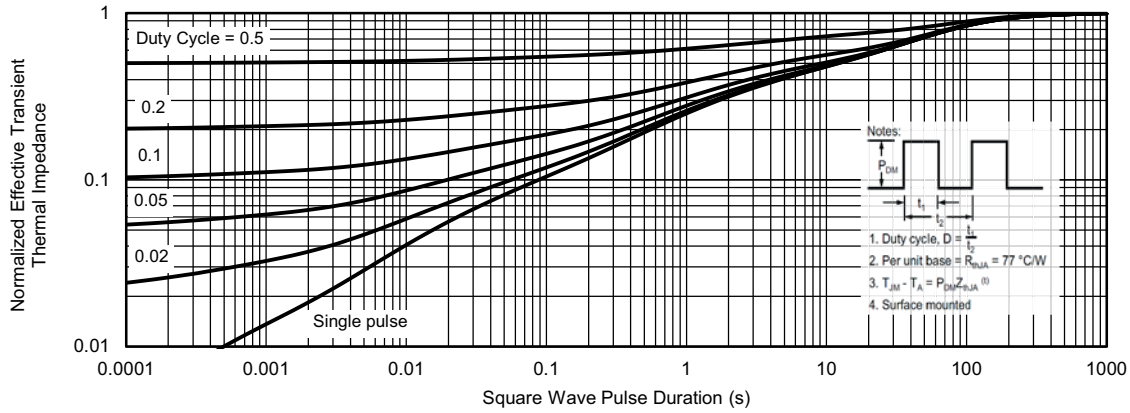
Power, Junction-to-Case

Note

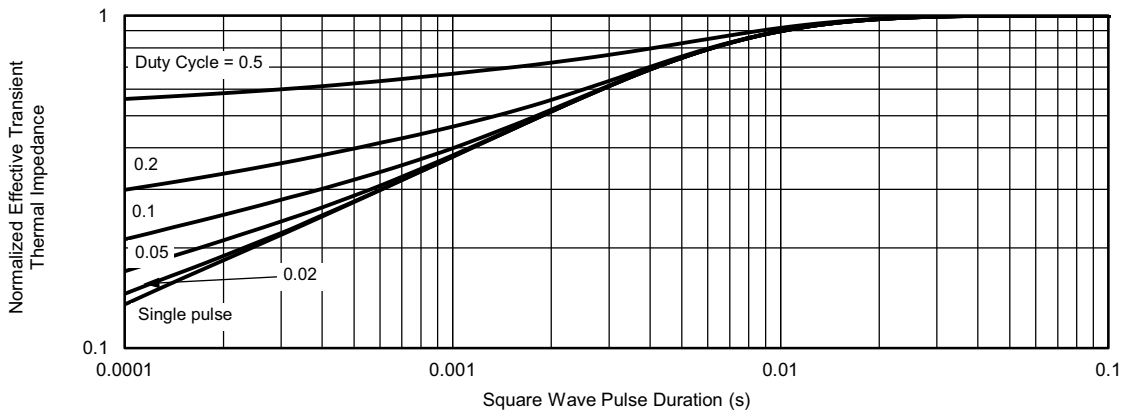
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



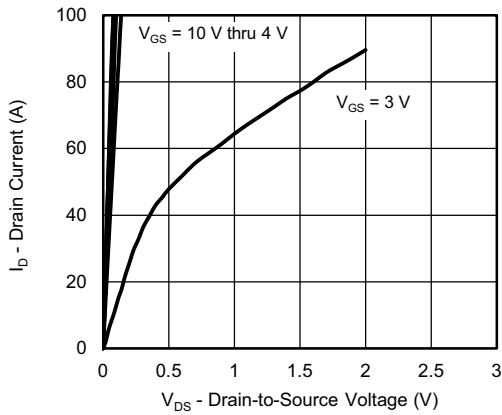
Normalized Thermal Transient Impedance, Junction-to-Ambient



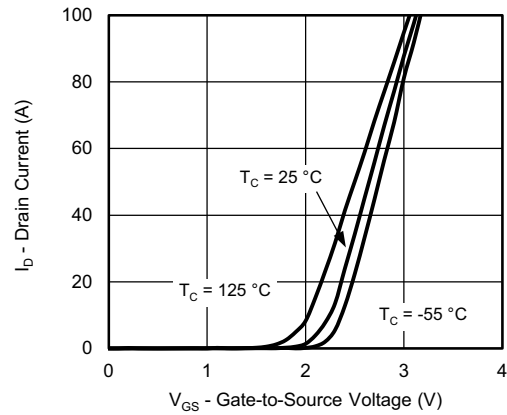
Normalized Thermal Transient Impedance, Junction-to-Case



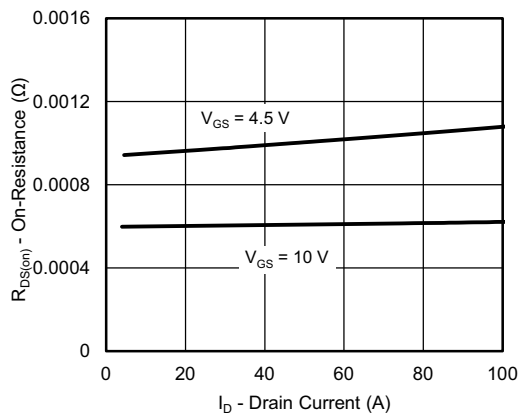
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



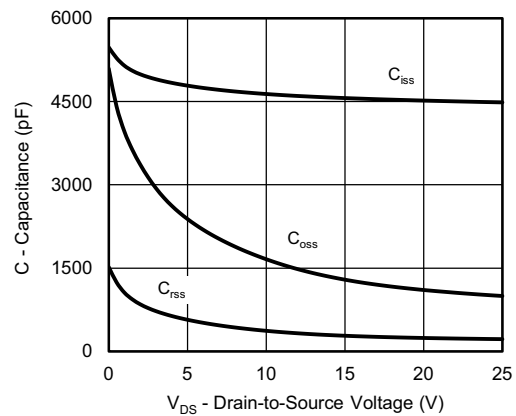
Output Characteristics



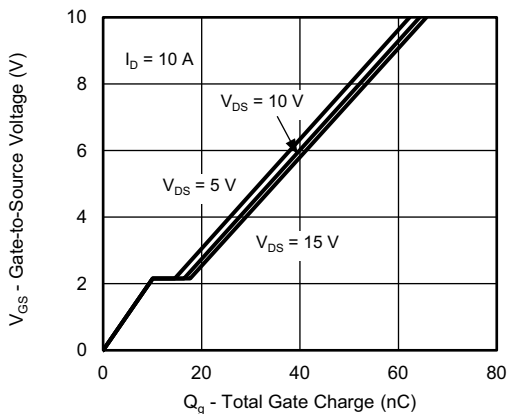
Transfer Characteristics



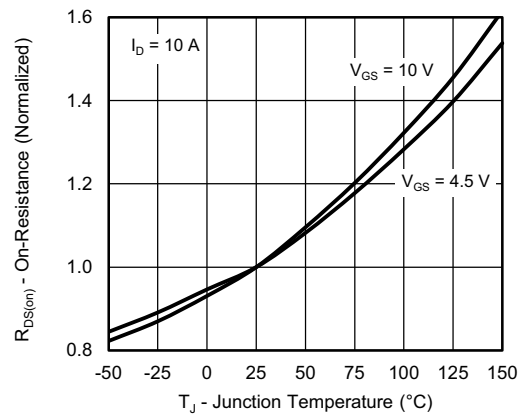
On-Resistance vs. Drain Current



Capacitance

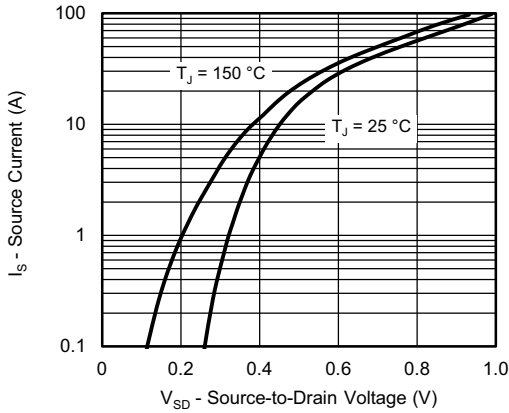


Gate Charge

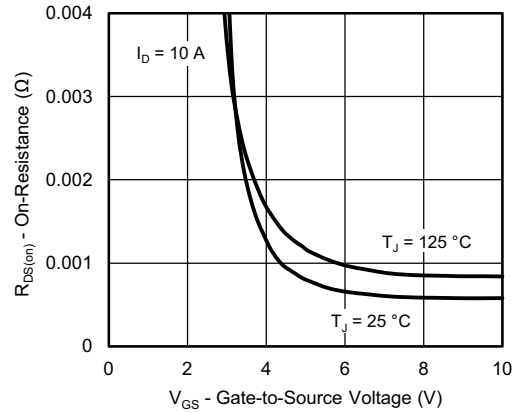


On-Resistance vs. Junction Temperature

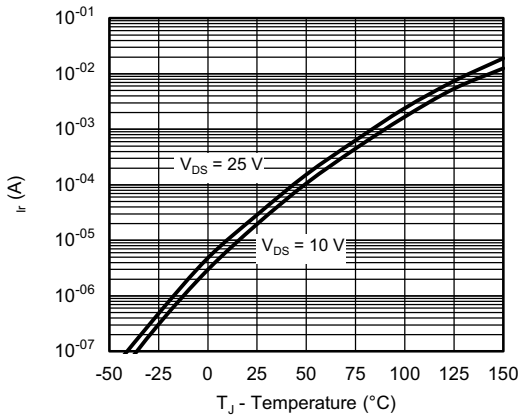
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



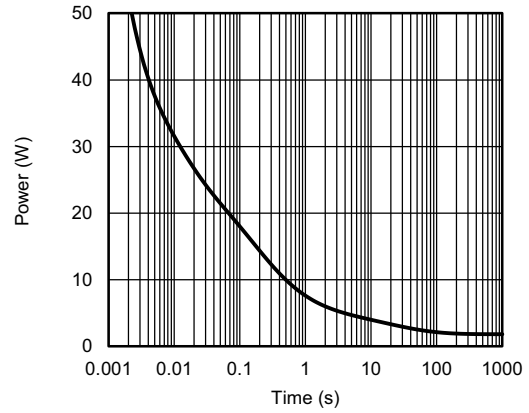
Source-Drain Diode Forward Voltage



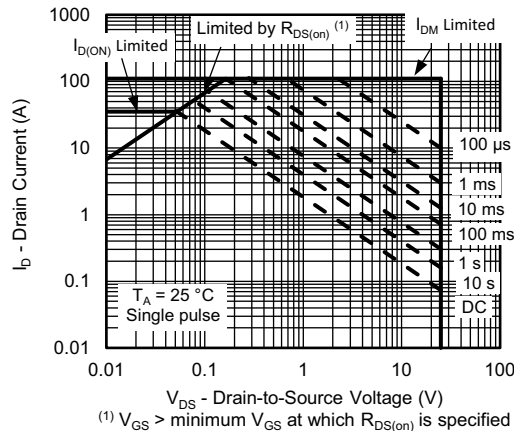
On-Resistance vs. Gate-to-Source Voltage



Reverse Current (Schottky)



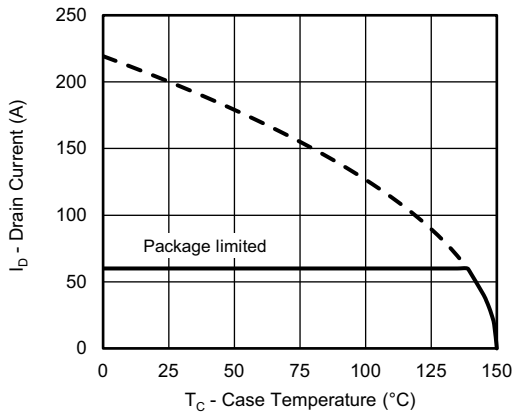
Single Pulse Power, Junction-to-Ambient



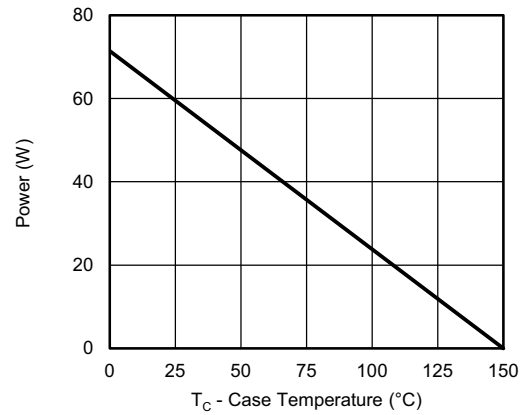
Safe Operating Area, Junction-to-Ambient



CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



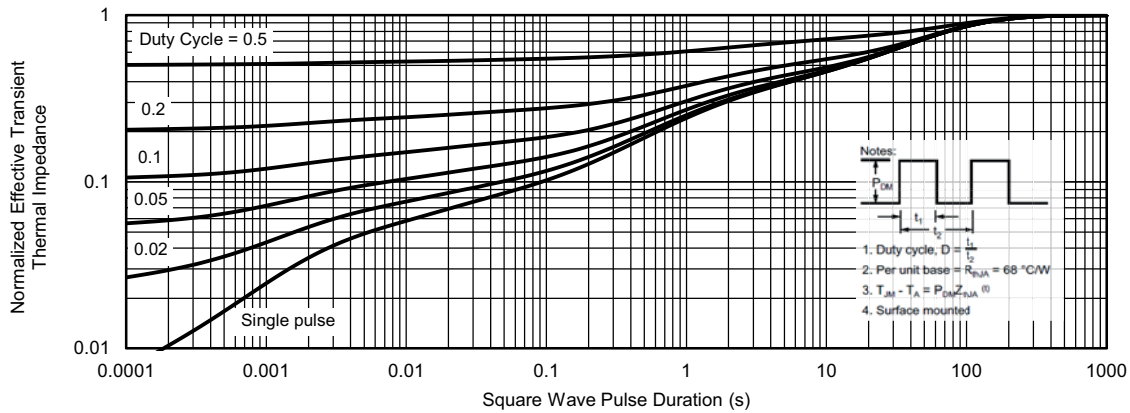
Power, Junction-to-Case

Note

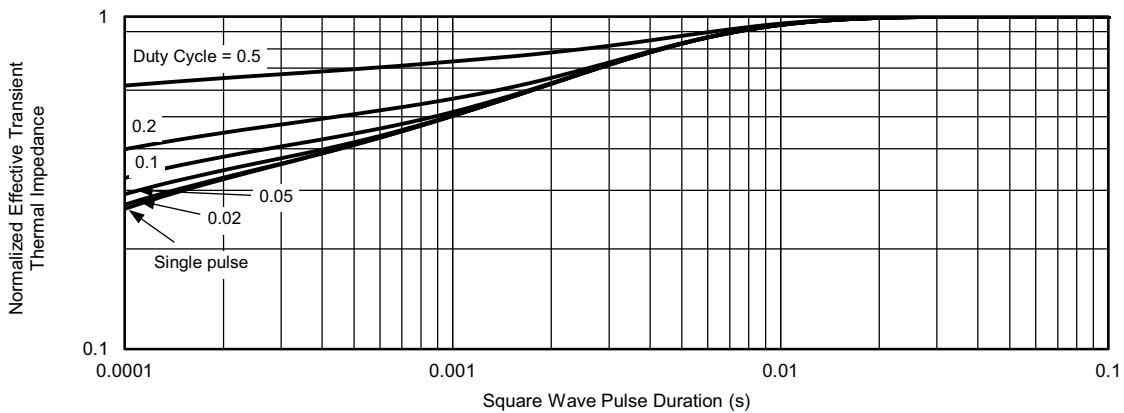
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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