


MDE029A128296RBW	128 x 296	3-Wire SPI Interface	E-Ink Module
<b>Specification</b>			
Version: 1		Date: 13/08/2018	
<b>Revision</b>			
1	08/01/2018	First Issue.	

Display Features			
Display Size	2.9"		
Resolution	128 x 296		
VGA Size	N/A		
Orientation	Portrait		
Appearance	Black, White, Red		
Logic Voltage	3V		
Interface	SPI		
Touchscreen	N/A		
Module Size	36.70 x 79.00 x 1.05 mm		
Operating Temperature	0°C ~ +50°C		
Pinout	24 - Way FFC	---	---

\* - For full design functionality, please use this specification in conjunction with the SSD1608 specification.(Provided Separately)

Display Accessories	
Part Number	Description

Optional Variants	
Appearances	Voltage



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## 1 General Description

EI290A128296WN is an Active Matrix Electrophoretic Display(AMEPD) , with interface and a reference system design. The 2.9' active area contains 128×296 pixels, and has 1-bit full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC. SRAM. LUT ,VCOM,and border are supplied with each panel.

## 2 Features

128×296 pixels display

White reflectance above 35%

Contrast ratio above 10: 1

Ultra wide viewing angle

Ultra low power consumption

Pure reflective mode

Bi-stable display Commercial temperature range

Landscape, portrait modes • manufacture • supply

Hard-coat antiglare display surface

Ultra Low current deep sleep mode

On chip display RAM

Waveform stored in On-chip OTP

Serial peripheral interface available

On-chip oscillator

On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage

I2C signal master interface to read external temperature sensor

## 3 Application

Electronic Shelf Label System



## 4 Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.9	Inch	
Display Resolution	128(H)×296(V)	Pixel	dpi:112
Active Area	29.05×66.89	mm	
Pixel Pitch	0.226×0.227	mm	
Pixel Configuration	Rectangle		
Outline Dimension	36.7(H)×79.0 (V) ×1.05(D)	mm	
Weight	4±0.5	g	

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# 5 Mechanical Drawing of EPD module

1	2	3	4	5	6	7	8	9
PART NUMBER		DESCRIPTION						
FRONT VIEW		SIDE VIEW		BOTTOM VIEW				
<p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>1. DISPLAY MODE 2.9" ARREY FOR EPD;</li> <li>2. DRIVE IC: SSD1608;</li> <li>3. RESOLUTION: 296gate X 128source;</li> <li>4. pixel size: 0.226mm X 0.227mm;</li> <li>5. Unspecified Tolerance: <math>\pm 0.20</math>;</li> <li>6. Material conform to the ROHS standard</li> </ol>		<p>易撕贴</p>		<p>易撕贴</p>				
PIN		SIGNAL						
1		NC						
2		GDR						
3		RESE						
4		VGL						
5		VGH						
6		TSCL						
7		TSDA						
8		BSI						
9		BUSY						
10		RES#						
11		D/C#						
12		CS#						
13		D0						
14		D1						
15		VDDIO						
16		VCI						
17		VSS						
18		VDD						
19		VPP						
20		VSH						
21		PREVGH						
22		VSL						
23		PREVGL						
24		VCOM						
DATE:		Eisen		Midas Displays Ltd				
01/08/2018		CHK.		TITLE MDE029A128296RBW				
SCALE: 1:1		APPD.		UNITS: mm				
PAGE: 1/1		NAME		VER: 0.1				
THIRD ANGLE PROJECTION		DATE		DWG.NO:				
		Donin						
NEW RELEASE		REVISION RECORD						
1	2	3	4	5	6	7	8	9

## 6 Input/Output Terminals

### 6.1 Pin out List

Pin #	Type	Single	Description	Remark
1		NC	No connection and do not connect with other NC pins	Keep Open
2	O	GDR	N-Channel MOSFET Gate Drive Control	
3	O	RESE	Current Sense Input for the Control Loop	
4	C	VGL	Negative Gate driving voltage	
5	C	VGH	Positive Gate driving voltage	
6	O	TSCL	I2C Interface to digital temperature sensor Clock pin	
7	I/O	TSDA	I2C Interface to digital temperature sensor Date pin	
8	I	BS1	Bus selection pin	Note 6-5
9	O	BUSY	Busy state output pin	Note 6-4
10	I	RES #	Reset	Note 6-3
11	I	D/C #	Data /Command control pin	Note 6-2
12	I	CS #	Chip Select input pin	Note 6-1
13	I/O	D0	serial clock pin (SPI)	
14	I/O	D1	serial data pin (SPI)	
15	I	VDDIO	Power for interface logic pins	
16	I	VCI	Power Supply pin for the chip	
17		VSS	Ground	
18	C	VDD	Core logic power pin	
19	C	VPP	Power Supply for OTP Programming	
20	C	VSH	Positive Source driving voltage	
21	C	PREVGH	Power Supply pin for VGH and VSH	
22	C	VSL	Negative Source driving voltage	
23	C	PREVGL	Power Supply pin for VCOM, VGL and VSL	
24	C	VCOM	VCOM driving voltage	

Note 6-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication:only when CS# is pulled LOW.

Note 6-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH,the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note 6-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 6-4: This pin (BUSY) is Busy state output pin. When Busy is Low the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin Low when the driver IC is working such as:

- Outputting display waveform; or
- Communicating with digital temperature sensor

Note 6-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

**Table: Bus interface selection**

<b>BS1</b>	<b>MPU Interface</b>
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) - 9 bits SPI



## 6.2 MCU Interface

### 6.2.1 MCU Serial Peripheral Interface (4-wire SPI)

The 4-wire SPI consists of SCLK (serial clock), SDIN (serial data), D/C# and CS#. D0 acts as SCLK and D1 acts as SDIN.

Table -1 : Control pins of 4-wire Serial Peripheral interface

Function	CS# pin	D/C# pin	SCLK pin
Write command	L	L	↑
Write data	L	H	↑

**Note:** ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register in the order of D7, D6, ... D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

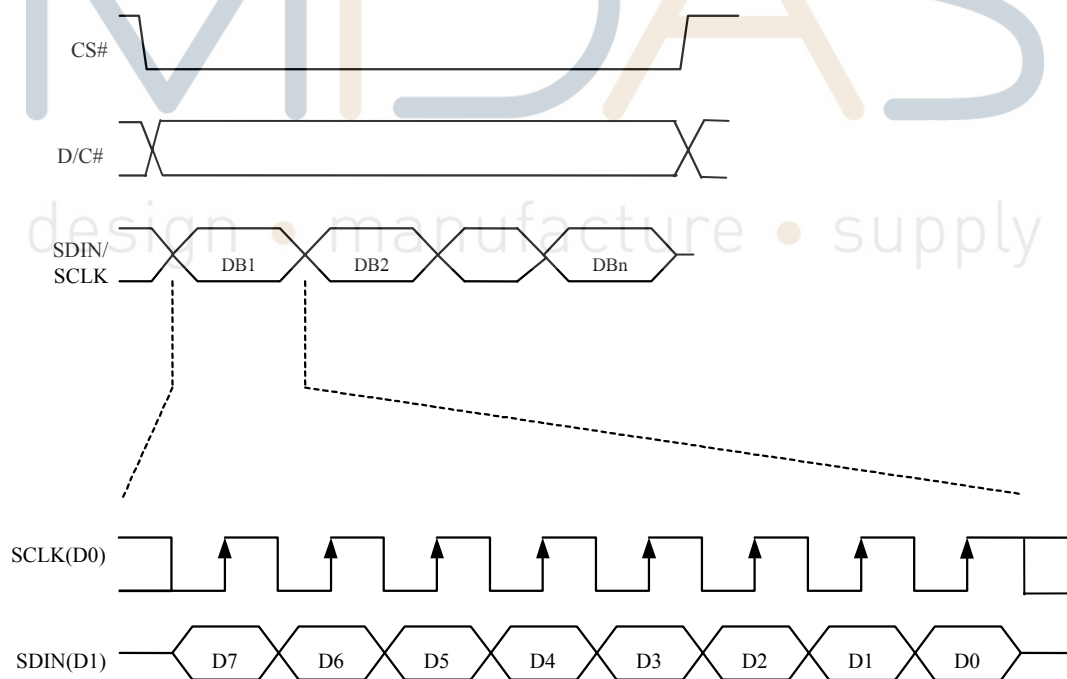


Figure 6-1 : Write procedure in 4-wire Serial Peripheral Interface mode





## 6.2.2 MCU Serial Peripheral Interface (3-wire SPI)

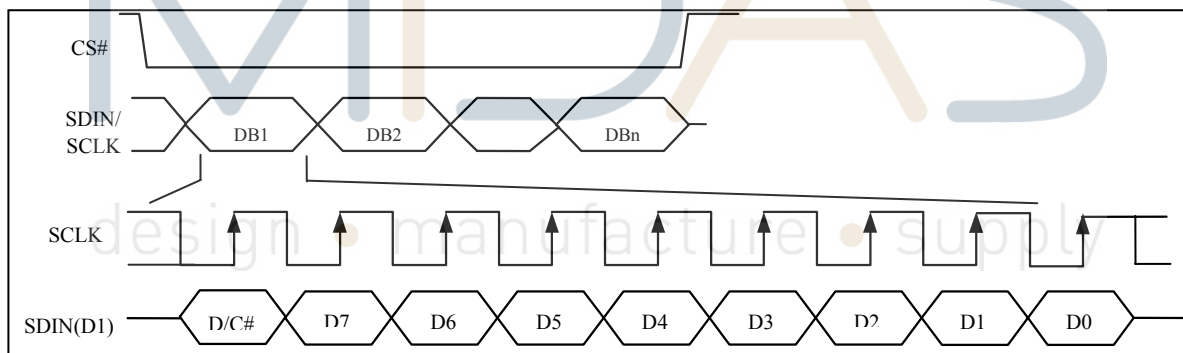
The 3-wire serial interface consists of SCLK (serial clock), SDIN (serial data) and CS#. In SPI mode, D0 acts as SCLK and D1 acts as SDIN. The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

**Table -2 : Control pins of 3-wire Serial Peripheral interface**

Function	CS# pin	D/C# pin	SCLK pin
Write command	L	Tie LOW	↑
Write data	L	Tie LOW	↑

**Note:** ↑ stands for rising edge of signal

**Figure 6-1 : Write procedure in 3-wire Serial Peripheral Interface mode**



### 6.3 External Temperature Sensor operation

There are two ways to let the module get the ambient temperature,

- 1) use the external temperature sensor interface, The module provides two I/O lines [TSDA and TSCL] for connecting digital temperature sensor for temperature reading sensing. TSDA will treat as SDA line and TSCL will treat as SCL line. They are required connecting with external pull-up resistor when they are used to connect to the temperature sensor, then the module will check the temperature automatically.
- 2) use any kinds of external temperature sensor to get the temperature value then converted to hex format, then use the spi interface send command 0x1A and the temperature value into the module. The temperature value how to converted to hex as the follow:
  1. When the Temperature value MSByte bit D11 = 0, the temperature is positive and value (DegC) = + (Temperature value)/16
  2. When the Temperature value MSByte bit D11 = 1, the temperature is negative and value (DegC) = ~ (2's complement of Temperature value)/16

12-bit binary (2's complement)	Hexadecimal Value	Decimal Value	Value [DegC]
0111 1111 0000	7F0	2032	127
0111 1110 1110	7EE	2030	126.875
0111 1110 0010	7E2	2018	126.125
0111 1101 0000	7D0	2000	125
0001 1001 0000	190	400	25
0000 0000 0010	002	2	0.125
0000 0000 0000	000	0	0
1111 1111 1110	FFE	-2	-0.125
1110 0111 0000	E70	-400	-25
1100 1001 0010	C92	-878	-54.875
1100 1001 0000	C90	-880	-55



## 7 Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description	
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting	
0	1		A7	A6	A5	A4	A3	A2	A1	A0		Set A[8:0] = 127h	
0	1		0	0	0	0	0	0	0	A8		Set B[2:0] = 0h	
0	1		0	0	0	0	0	B2	B1	B0			
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start Control	Set A[7:0] = CFh	
0	1		1	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		Set B[7:0] = CEh	
0	1		1	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>		Set C[7:0] = 8Dh	
0	1		1	C <sub>6</sub>	C <sub>5</sub>	C <sub>4</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>			
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control	
0	1		0	0	0	0	0	0	0	A <sub>0</sub>			
												A[0] :	Description
												0	Normal Mode [POR]
												1	Enter Deep Sleep Mode
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence	
0	1		0	0	0	0	0	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address.  00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR]  A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM.  AM= 0, the address counter is updated in the X direction. [POR] AM= 1, the address counter is updated in the Y direction.	
0	0	12	0	0	0	1	0	0	1	0	SWRESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode Note: RAM are unaffected by this command.	

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description						
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[7:0] – MSByte 01111111[POR] B[7:0] – LSByte 11110000[POR]						
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>								
0	1		B <sub>7</sub>	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	0	0	0	0								
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence  The Display Update Sequence Option is located at R22h  User should not interrupt this operation to avoid corruption of panel images.						
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	Option for Display Update Bypass Option used for Pattern Display, which is used for display the RAM content into the Display  OLD RAM Bypass option A [7] A[7] = 1: Enable bypass A[7] = 0: Disable bypass [POR]  A[4] value will be used as for bypass. A[4] = 0 [POR]  A[1:0] Initial Update Option - Source Control						
0	1		A <sub>7</sub>	0	0	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>								
												<table border="1"> <tr> <td>A[1:0]</td> <td>GSC</td> <td>GSD</td> </tr> <tr> <td>01 [POR]</td> <td>GS0</td> <td>GS1</td> </tr> </table>	A[1:0]	GSC	GSD	01 [POR]	GS0	GS1
A[1:0]	GSC	GSD																
01 [POR]	GS0	GS1																



R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description		
0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation		
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>			Parameter (in Hex)	
													Enable Clock Signal, Then Enable CP Then Load Temperature value Then Load LUT Then INITIAL DISPLAY Then PATTERN DISPLAY Then Disable CP Then Disable OSC	FF [POR]
													To Enable Clock Signal (CLKEN=1)	80
													To Enable Clock Signal, then Enable CP (CLKEN=1, CPEN=1)	C0
													To INITIAL DISPLAY + PATTEN DISPLAY	0C
													To INITIAL DISPLAY	08
													To DISPLAY PATTEN	04
													To Disable CP, then Disable Clock Signal (CLKEN=1, CPEN=1)	03
													To Disable Clock Signal (CLKEN=1)	01
												Remark: CLKEN=1: If CLS=VDDIO then Enable OSC If CLS=VSS then Enable External Clock CLKEN=0: If CLS=VDDIO then Disable OSC AND INTERNAL CLOCK Signal = VSS,		
0	0	24	0	0	1	0	0	1	0	0	Write RAM	After this command, data entries will be written into the RAM until another command is written. Address pointers will advance accordingly.		
0	0	2C	0	0	1	0	1	0	1	1	Write VCOM register	Write VCOM register from MCU interface		
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>				



R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description										
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU [240 bits], (excluding the VSH/VSL and Dummy bit)										
0	1		LUT [30 bytes]																			
0	1																					
0	1																					
...	...																					
0	0	3A	0	0	1	1	1	0	1	0	Set dummy line period	Set A[7:0] = 1Ah										
0	1		0	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>												
0	0	3B	0	0	1	1	1	0	1	1	Set Gate line width	Set B[3:0] = 8h										
0	1		0	0	0	0	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>												
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A [7] Follow Source at Initial Update Display A [7]=0: [POR] A [7]=1: Follow Source at Initial Update Display for VBD, A [6:0] setting are being overridden at Initial Display STAGE.  A [6] Select GS Transition/ Fix Level for VBD A [6]=0: Select GS Transition A[3:0] for VBD A [6]=1: Select FIX level Setting A[5:4] for VBD [POR] A [5:4] Fix Level Setting for VBD										
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	0	0	A <sub>1</sub>	A <sub>0</sub>												
												<table border="1" style="margin-left: 20px;"> <tr> <td>A[5:4]</td> <td>VBD level</td> </tr> <tr> <td>00</td> <td>VSS</td> </tr> <tr> <td>01</td> <td>VSH</td> </tr> <tr> <td>10</td> <td>VSL</td> </tr> <tr> <td>11[POR]</td> <td>HiZ</td> </tr> </table>	A[5:4]	VBD level	00	VSS	01	VSH	10	VSL	11[POR]	HiZ
A[5:4]	VBD level																					
00	VSS																					
01	VSH																					
10	VSL																					
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A [1:0]	GSA	GSB																				
01 [POR]	GS0	GS1																				



R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit  A[4:0]: XSA[4:0], XStart, POR = 00h B[4:0]: XEA[4:0], XEnd, POR = 1Dh
0	1		0	0	0	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	1		0	0	0	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit  A[8:0]: YSA[8:0], YStart, POR = 000h B[8:0]: YEA[8:0], YEnd, POR = 13Fh
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	1		0	0	0	0	0	0	0	A <sub>8</sub>		
0	1		B <sub>7</sub>	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>		
0	1		0	0	0	0	0	0	0	B <sub>8</sub>		
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[4:0]: XAD[4:0], POR is 00h
0	1		0	0	0	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: YAD8:0], POR is 000h
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	1		0	0	0	0	0	0	0	A <sub>8</sub>		

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## 8 MAXIMUM RATINGS

**Table 8-1: Maximum Ratings**

Symbol	Parameter	Rating	Unit
V <sub>CI</sub>	Logic supply voltage	-0.5 to +3.7	V
V <sub>IN</sub>	Logic Input voltage	-0.5 to V <sub>DDIO</sub> +0.5	V
V <sub>OUT</sub>	Logic Output voltage	-0.5 to V <sub>DDIO</sub> +0.5	V
T <sub>OPR</sub>	Operation temperature range	0 to 50	°C
T <sub>STG</sub>	Storage temperature range	-25 to 70	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

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## 9 ELECTRICAL CHARACTERISTICS

The following specifications apply for:  $V_{SS}=0V$ ,  $V_{CI}=3.0V$ ,  $T_{OPR}=25^{\circ}C$ .

**Table 9-1: DC Characteristics**

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
$V_{CI}$	VCI operation voltage		VCI	-	3.0	3.6	V
$V_{IH}$	High level input voltage		D1 (SDIN), D0 (SCLK), CS#, D/C#, RES#, BS1, TSDA, TSCL	$0.8V_{DDIO}$			V
$V_{IL}$	Low level input voltage					$0.2V_{DDIO}$	V
$V_{OH}$	High level output voltage	$I_{OH} = -100\mu A$	BUSY, TSDA,	$0.9V_{DDIO}$			V
$V_{OL}$	Low level output voltage	$I_{OL} = 100\mu A$	TSCL			$0.1V_{DDIO}$	V
$I_{update}$	Image update current			-	8.5	10	mA
$I_{standby}$	Standby panel current			-	-	5	$\mu A$

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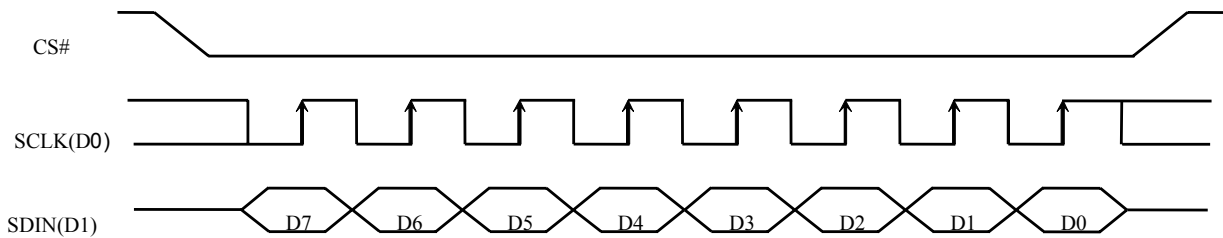
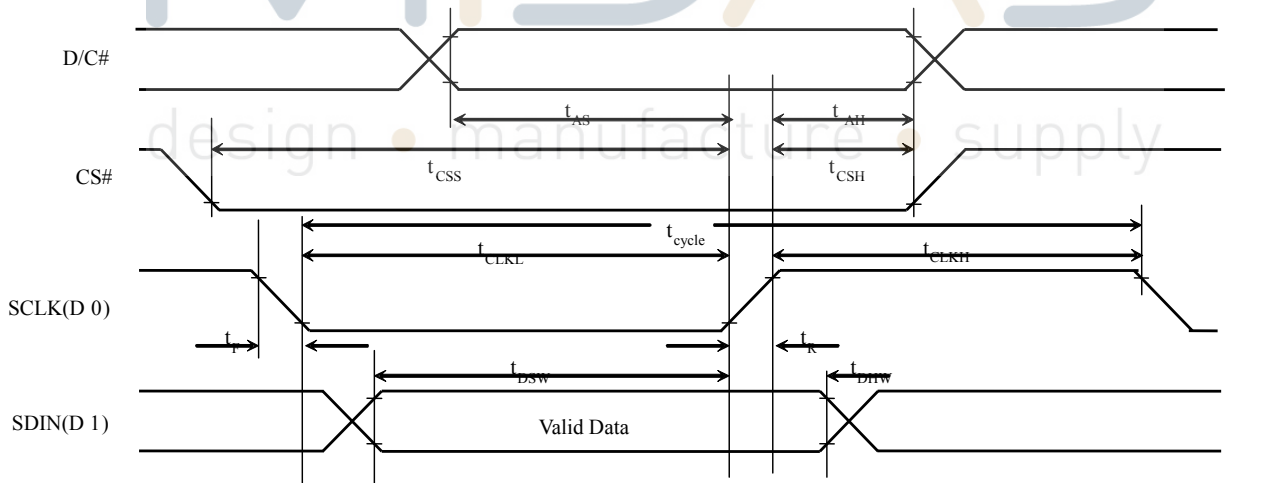
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## 10 Serial Peripheral Interface Timing

The following specifications apply for: VSS=0V, VCI=2.4V to 3.7V, T<sub>OPR</sub>=25°C

Symbol	Parameter	Min	Typ	Max	Unit
t <sub>cycle</sub>	Clock Cycle Time	250	-	-	ns
t <sub>AS</sub>	Address Setup Time	150	-	-	ns
t <sub>AH</sub>	Address Hold Time	150	-	-	ns
t <sub>CSS</sub>	Chip Select Setup Time	120	-	-	ns
t <sub>CSH</sub>	Chip Select Hold Time	60	-	-	ns
t <sub>DSW</sub>	Write Data Setup Time	50	-	-	ns
t <sub>DHW</sub>	Write Data Hold Time	15	-	-	ns
t <sub>CLKL</sub>	Clock Low Time	100	-	-	ns
t <sub>CLKH</sub>	Clock High Time	100	-	-	ns
t <sub>R</sub>	Rise Time [20% ~ 80%]	-	-	15	ns
t <sub>F</sub>	Fall Time [20% ~ 80%]	-	-	15	ns



## 11 Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	-	25.5	36	mW	-
Power consumption in standby mode	-	-	-	0.018	mW	-

## 12 Reference Circuit

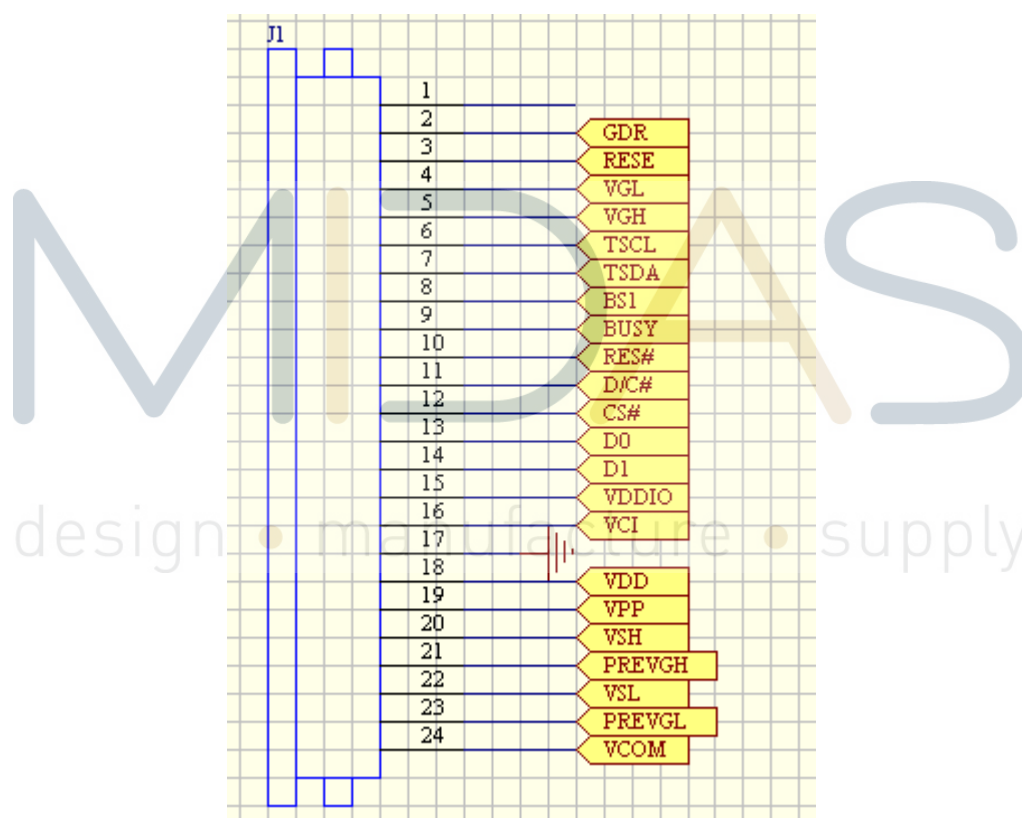


Figure . 12-1

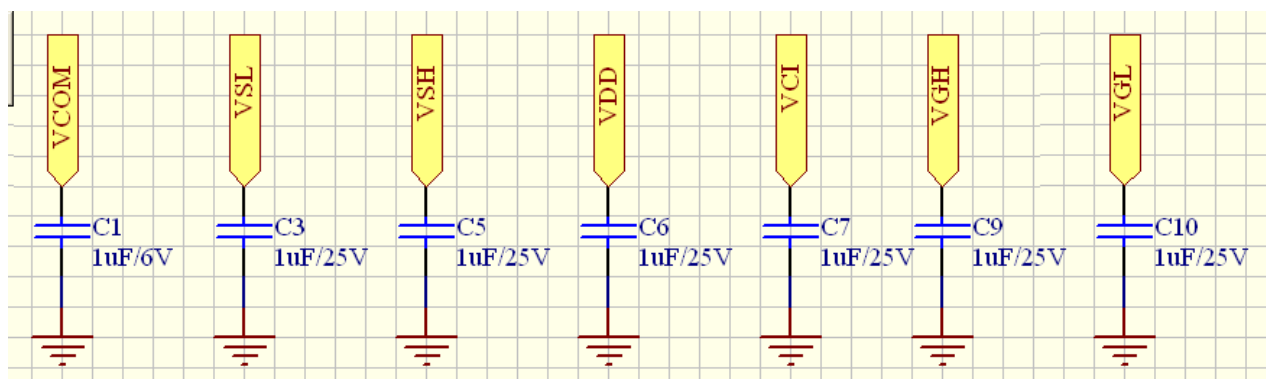


Figure . 12-2

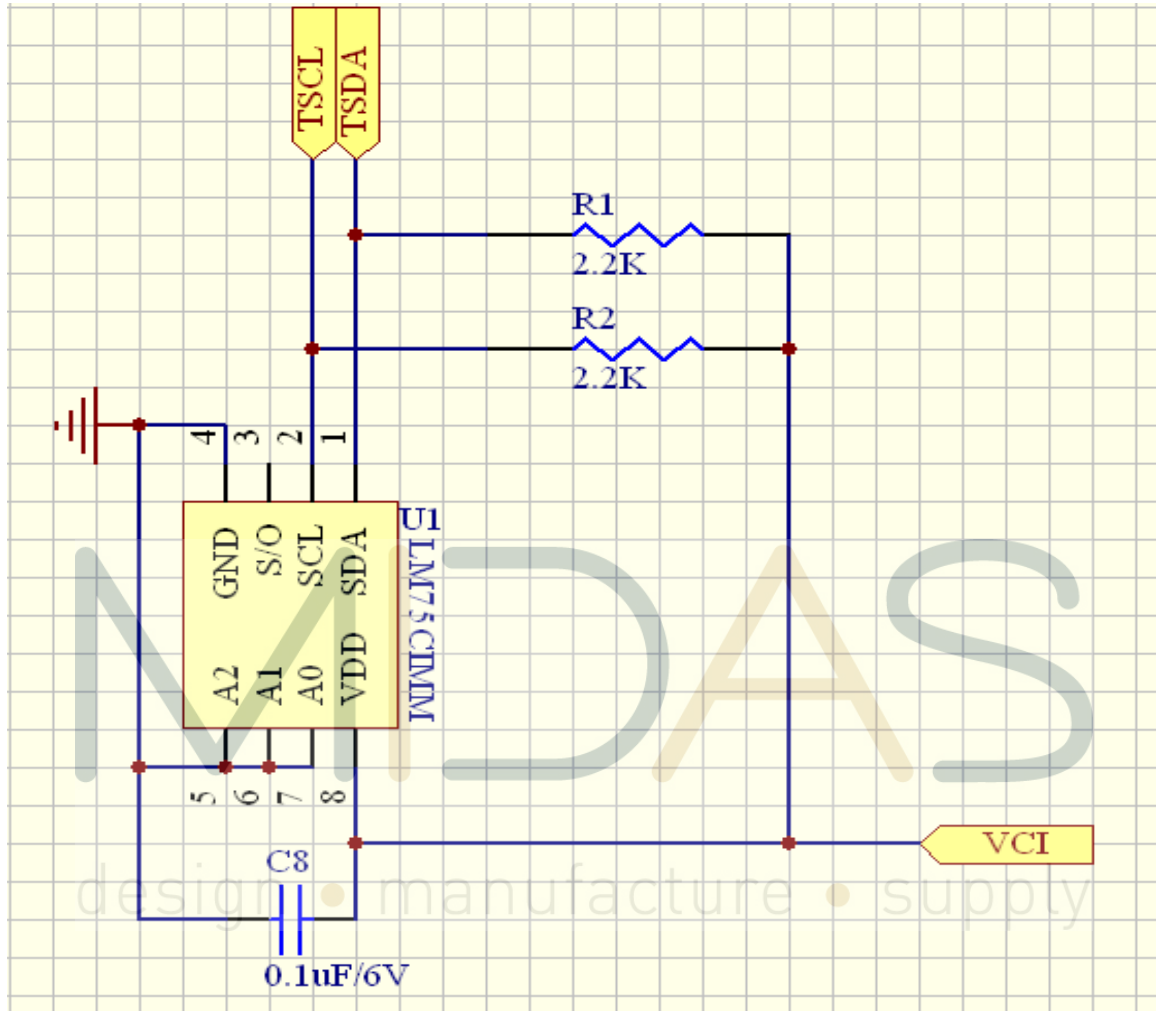


Figure . 12-3



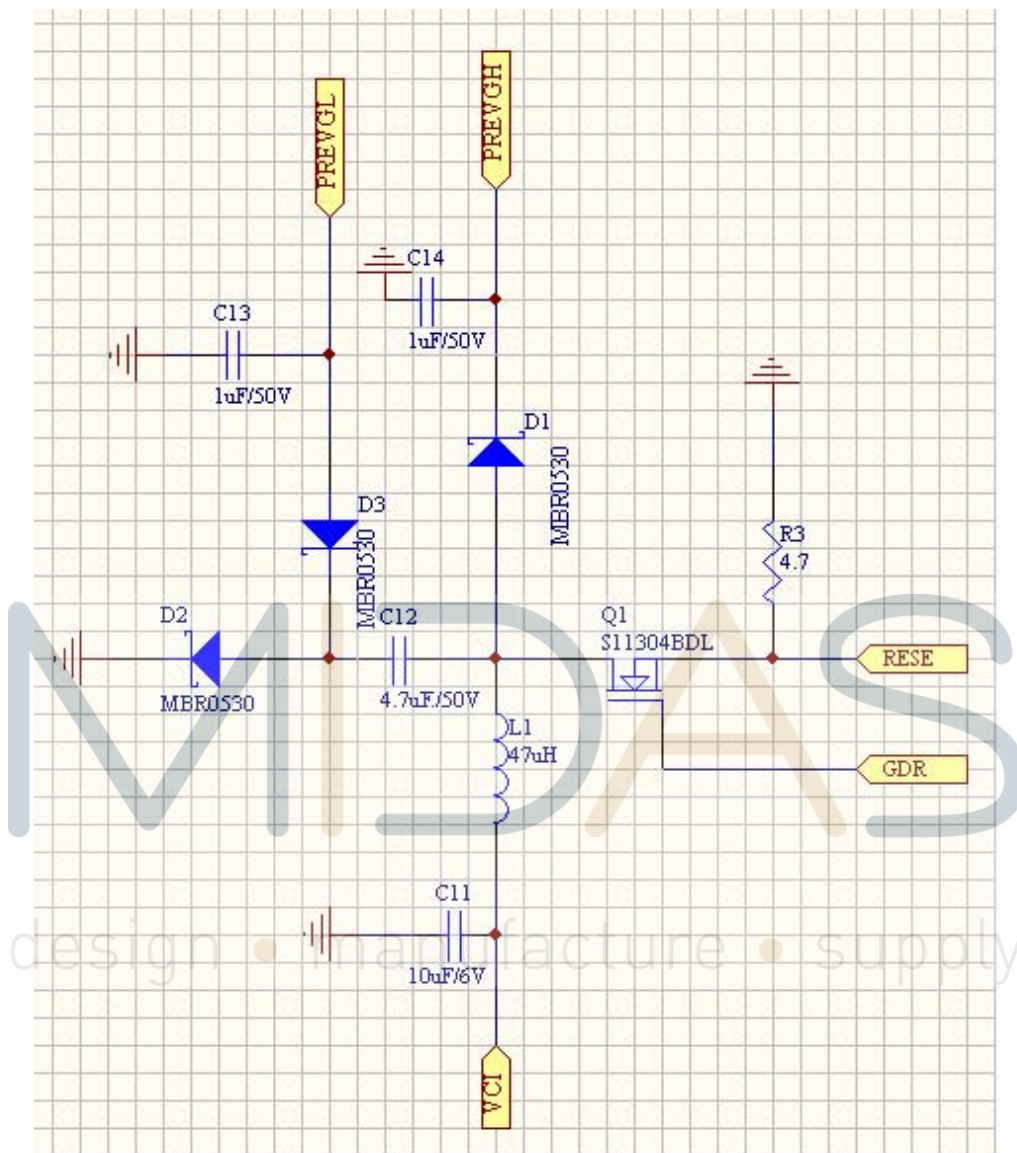
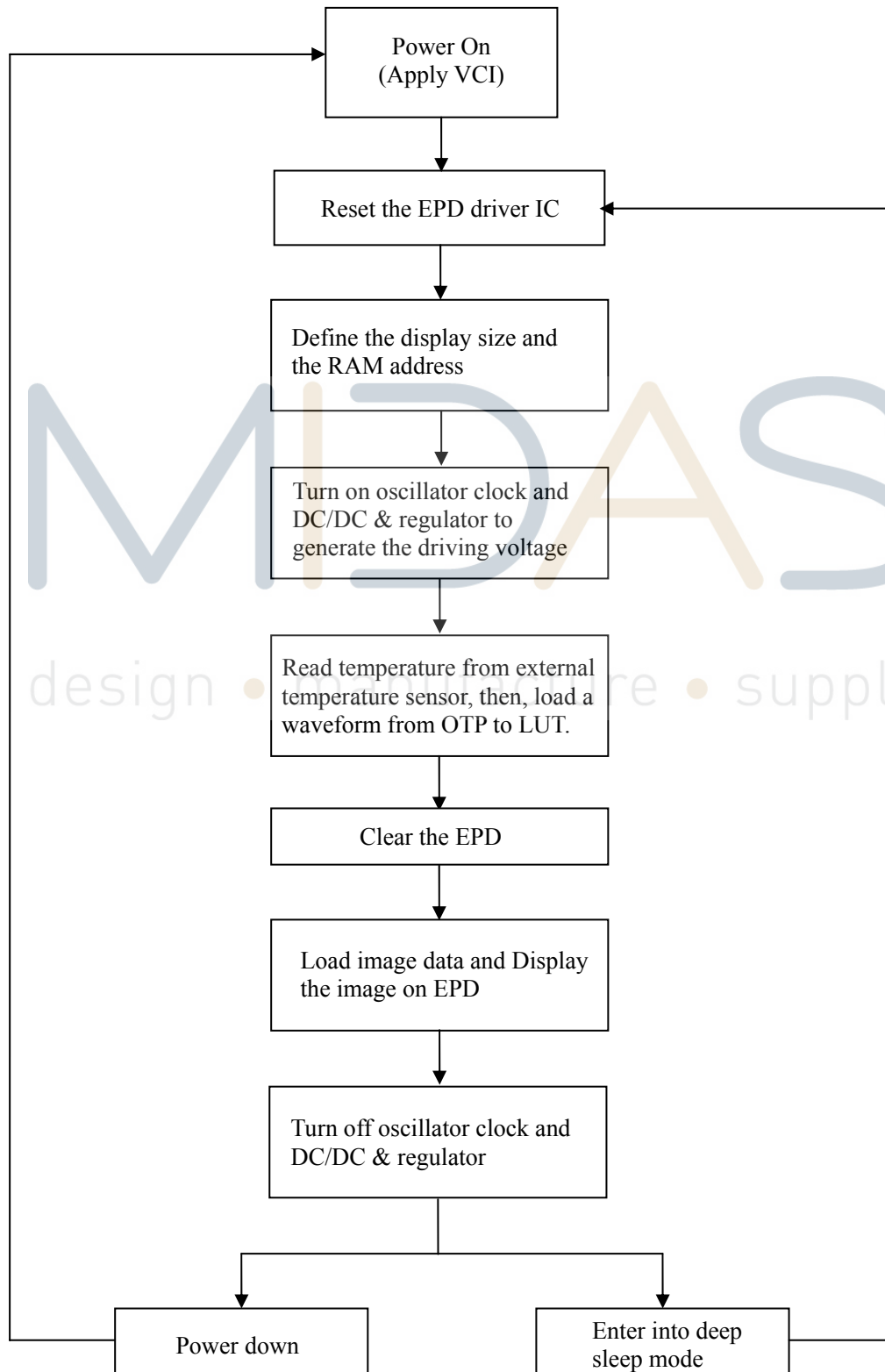


Figure . 12-4

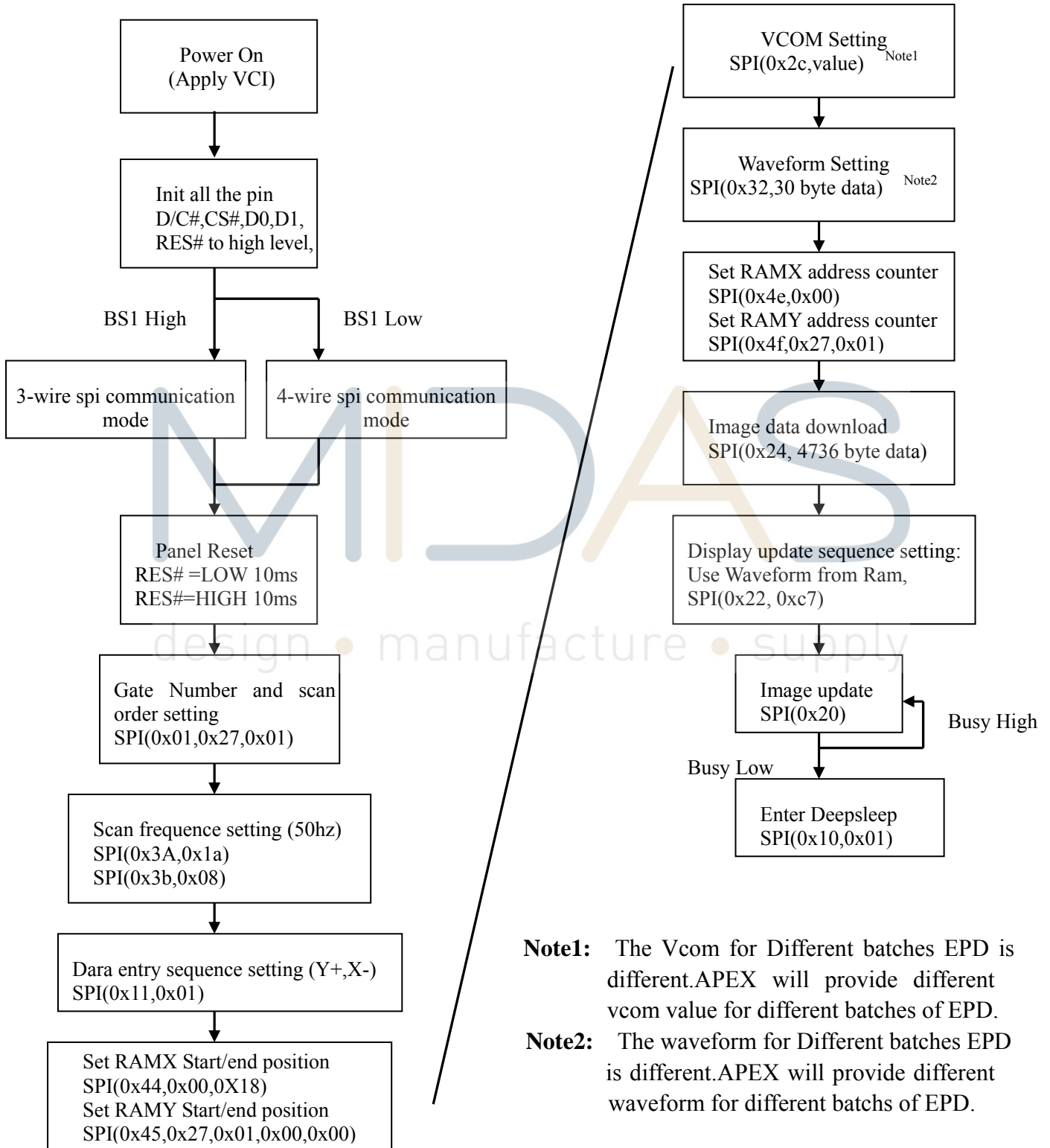


## 13 Typical Operating Sequence

### 13.1 Normal Operation Flow



## 13.2 Reference Program Code



## 14 Optical characteristics

### 14.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYPE	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 9-1
Gn	2Grey Level	-	-	$DS+(WS-DS) \times n(m-1)$	-	L*	-
CR	Contrast Ratio	indoor	-	10	-	-	-
T <sub>update</sub>	Update time	25°C	-	680ms	-	ms	-
Panel's life		0°C~50°C		1000000 times or 5 years			Note 9-2

WS : White state, DS : Dark state

Gray state from Dark to White : DS、 WS

m : 2

Note 9-1 : Luminance meter : Eye – One Pro Spectrophotometer

Note 9-2 : When work in temperature below 0 degree or above 50 degree , we do not recommend because the panel's life will not be guaranteed



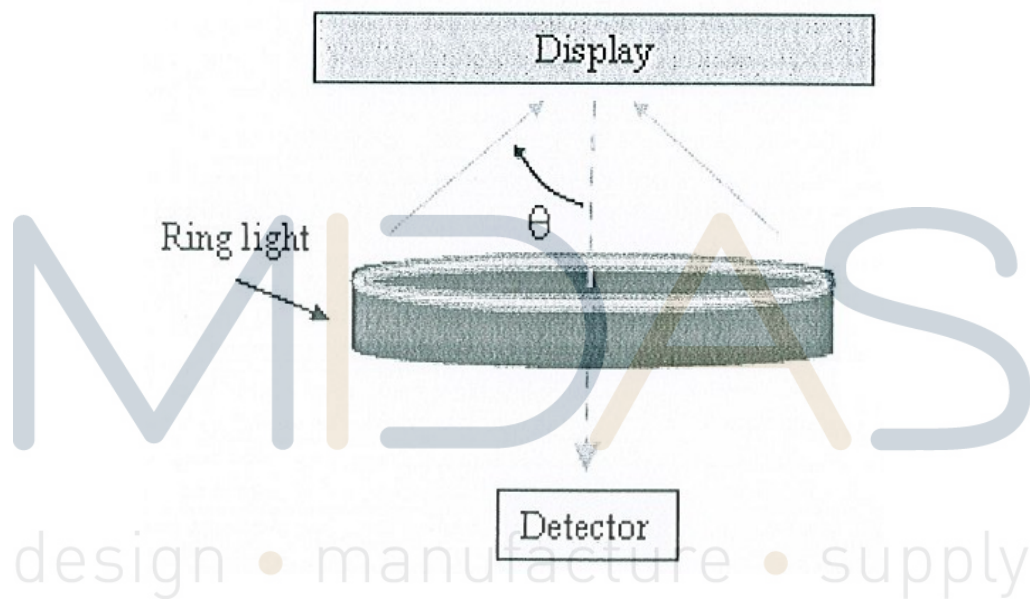


## 14.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd) :

R1: white reflectance      Rd: dark reflectance

$$CR = R1/Rd$$

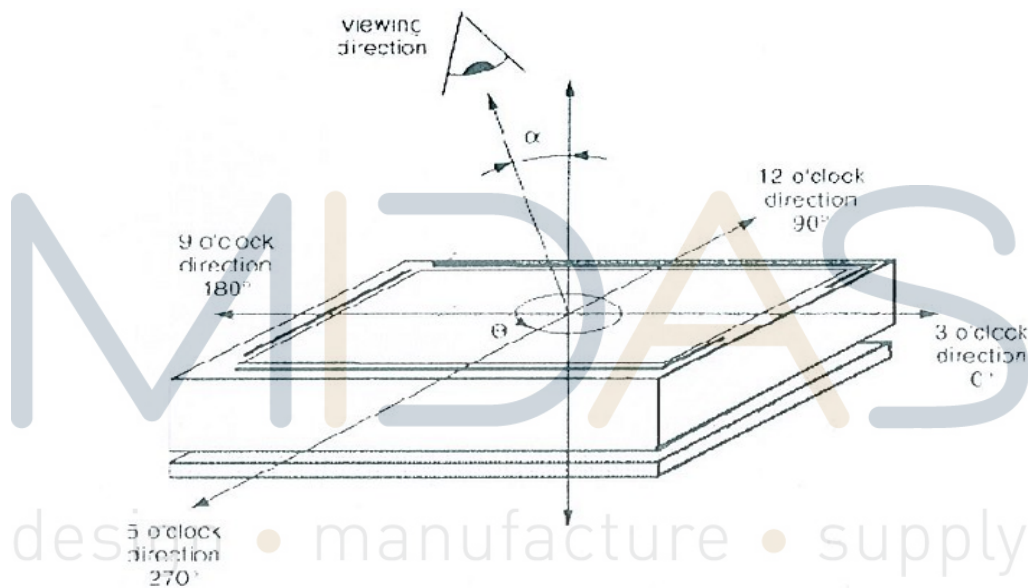


### 14.3 Reflection Ratio

The reflection ratio is expressed as :

$$R = \text{Reflectance Factor white board} \times (L_{\text{center}} / L_{\text{white board}})$$

$L_{\text{center}}$  is the luminance measured at center in a white area ( $R=G=B=1$ ) .  $L_{\text{white board}}$  is the luminance of a standard white board . Both are measured with equivalent illumination source . The viewing angle shall be no more than 2 degrees .



### 15.4 Bi-stability

1. The value of Contrast ratio in different time as follows:

Bi-stability	Result
250 hours	CR >8
500 hours	CR >8
750 hours	CR >7.5
1000 hours	CR >7



## 15 HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

<b>WARNING</b>
The display glass may break when it is dropped or bumped on a hard surface . Handle with care. Should the display break, do not touch the electrophoretic material . In case of contact with electrophoretic material , wash with water and soap.

<b>CAUTION</b>
The display module should not be exposed to harmful gases , such as acid and alkali gases , which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components . The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

<b>Data sheet status</b>	
Product specification	The data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied . Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given , it is advisory and dose not form part of the specification.	

<b>Product Environmental certification</b>
ROHS



## 16 Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = 50°C, 30% for 240 hrs	IEC 60 068-2-2Bp	
2	Low-Temperature Operation	T = 0°C for 240 hrs	IEC 60 068-2-2Ab	
3	High-Temperature Storage	T = +70°C, 40% for 240 hrs Test in white pattern	IEC 60 068-2-2Bp	
4	Low-Temperature Storage	T = -25°C for 240 hrs Test in white pattern	IEC 60 068-2-2Ab	
5	High Temperature, High-Humidity Operation	T=+40°C, RH=90%for168hrs	IEC 60 068-2-3CA	
6	High Temperature, High-Humidity Storage	T=+60°C, RH=80%for240hrs Test in white pattern	IEC 60 068-2-3CA	
7	Temperature Cycle	[-20°C 30mins]→ [+60°C 30mins] ,50cycles Test in white pattern	IEC 60 068-2-14NB	

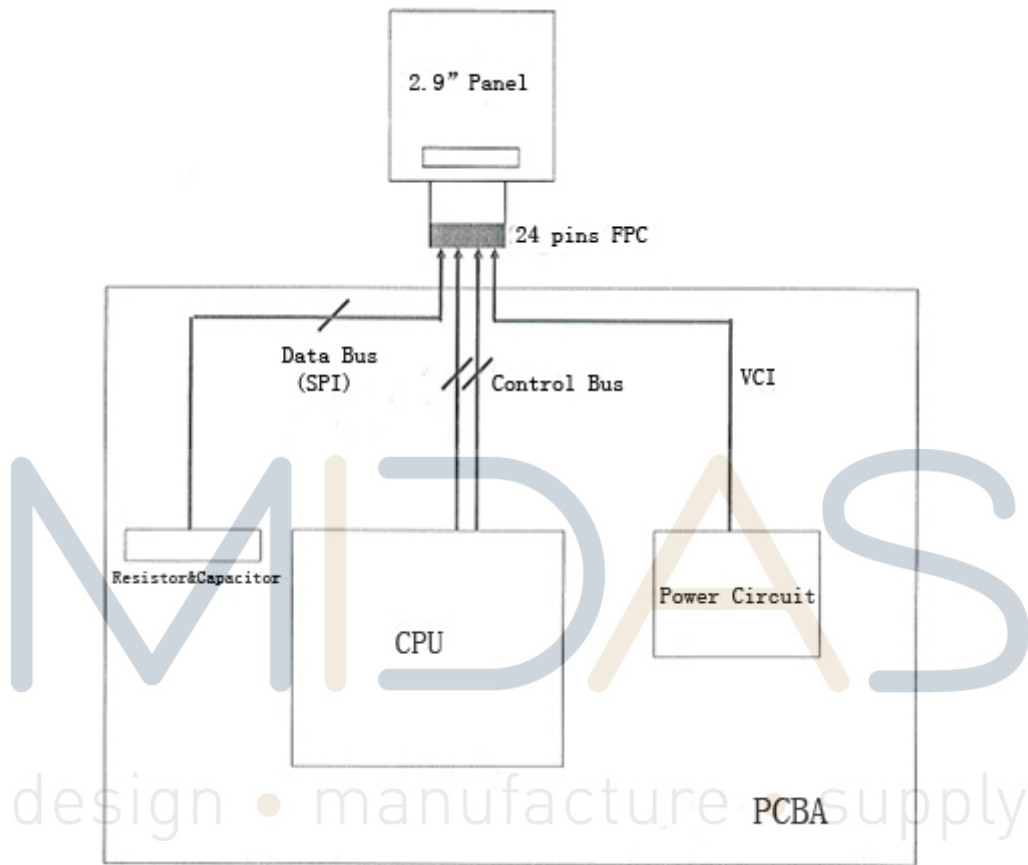
Actual EMC level to be measured on customer application.

Note : The protective film must be removed before temperature test.

design • manufacture • supply



## 17 Block Diagram



## 18 Point and line standard

### Shipment Inseption Standard

Equipment: Electrical test fixture, Point gauge

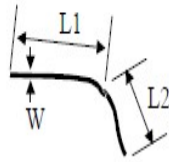
Outlinedimension:

36.7(H)×79.0(V) ×1.05(D)

Unit: mm

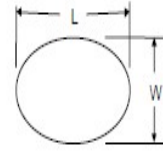
Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
		19℃~25℃	40%~55%RH	700~1000Lux	200~400 mm	35Sec
appearance standard	Defet type	Inspection	Standard		Part-A	
	dead/ switch point (point overproof)	Electric Display	D≤0.25mm		Ignore	
			0.25 mm < D ≤ 0.4 mm		N≤4	
			D > 0.4 mm		Not Allow	
	2.line (no switch)	Electric Display	L≤0.5mm, to point to determine			
			L≤4W, to point to determine			
	3.line (Switching line)	Electric Display	Ignore in gray scale viewing In Blak&white viewing Follow Non-Switching Criteria			
	4.Display unwork	Electric Display	Not Allow			
	5.Display error	Electric Display	Not Allow			
	6. warping	Vsual	T<0.5mm, Ignore;			
	7.Protector hurt	Vsual	L≤2mm, W≤0.05mm, Ignore;			
			0.05mm < W ≤ 01mm, L≤4mm, N≤2			
			L > 4 mm, W > 0.1 mm, Not Allow;			
8.PS Bubble	Vsual	D≤0.2mm, Ignore;				
		0.2mm≤D<0.35mm & N≤2				
		D>0.35 mm, Not Allow;				
9.Packing	Vsual	cannot be dirty and breakdown;must be marked and identified				
Remark	1. Cannot be defect&failure cause by appearence defect;					
	2. Cannot be larger size cause by appearence defect;					





$$L = L1 + L2$$

Line Defect



$$D = (L + W) / 2$$

Spot Defect

L=long W=wide D=point size

# MIDAS

design • manufacture • supply

