Layout Considerations for Pulse Ethernet Magnetics and Ethernet Connector Modules

Introduction

Pulse Electronics' Networking BU offers a broad line of networking and telecommunication products, including our Ethernet magnetics and Ethernet connector modules (which incorporate the Ethernet magnetic into the connector). Both of these product categories include components optimized for use in 100BASE-TX, 1000BASE-T and 2.5/5/10GBASE-T systems, including PoE, Extended Temperature, and high isolation applications.

Our Ethernet magnetics are RoHS compliant, qualified at major PHY suppliers, and optimized for all major LAN transceivers. All of them provide electrical circuit isolation that meets IEEE 802.3, while maintaining the high standard of signal integrity needed for the most demanding applications. Our Ethernet connector modules are designed and manufactured to meet or exceed IEEE 802.3 standards.

We developed this document to help our customers using these Ethernet products when laying out printed circuit boards (PCBs) intended to interface with an Ethernet network. It includes recommendations on PCB layout to reduce EMI and maintain signal integrity. For additional board layout assistance or specific design guidelines, contact the supplier of the PHY you have chosen.

Best Practices for PCB Design

Many factors go into laying out a PCB efficiently. Complexity, board space, and the number and types of devices required will often dictate routing and placement strategies.

Component Placement Guidelines

Component placement can affect signal quality, emissions, and component operating temperature. When performing a board layout, the CAD tool must not be used to route the differential pairs automatically without intervention. In most cases, the differential pairs must be routed manually. The following guidelines offer direction on optimizing the PCB design process:

- Minimize potential problems directly related to EMI, which could cause the system to fail to meet applicable government test specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.
- Optimize the distance between the Ethernet magnetic and the RJ45 connector. It should be kept to less than 25 mm (approx. 1 inch). Refer to Figure 1 for guidance on placement of these components.

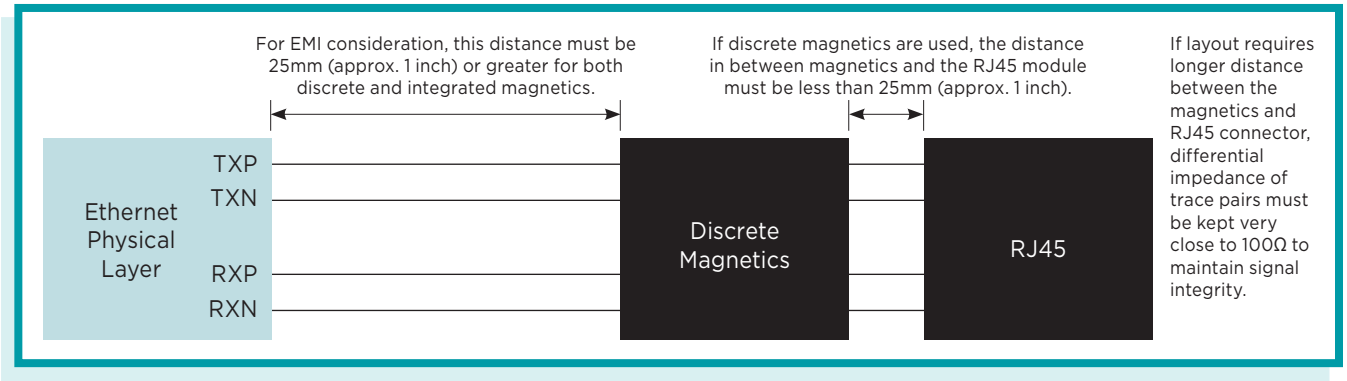

Figure 1. Pulse Ethernet Magnetic and RJ45 Placement

Note: This document is for reference only; please contact your PHY/IC supplier for specific board layout recommendations.

- Isolate the PHY from the Ethernet magnetic; the distance between them needs to be 25 mm (approx. 1 inch) or greater. Among PHY vendors, this rule is considered good design practice for EMI considerations.
- Keep the PHY device and the differential transmit pairs at least 25 mm (approx. 1 inch) from the edge of the PCB, up to the Ethernet magnetic. If using an Ethernet connector module, which incorporates the magnetic, the differential pairs should be routed to the back of the connector module, away from the board edge.
- Minimizing the amount of space needed for the Ethernet LAN interface is important because other interfaces will compete for physical space on a motherboard near the Ethernet connector module. Ethernet LAN circuits need to be located as close to the connector as possible.
- Refer to Figure 2 for some basic placement distance guidelines. Although it shows two differential pairs, it can be generalized for 1000BASE-T to 10GBASE-T systems with four analog pairs. The ideal placement for the Ethernet silicon would be approximately one inch behind the Ethernet magnetic. This figure also illustrates the need to keep the LAN silicon away from the board edge and the magnetics module for best EMI performance.

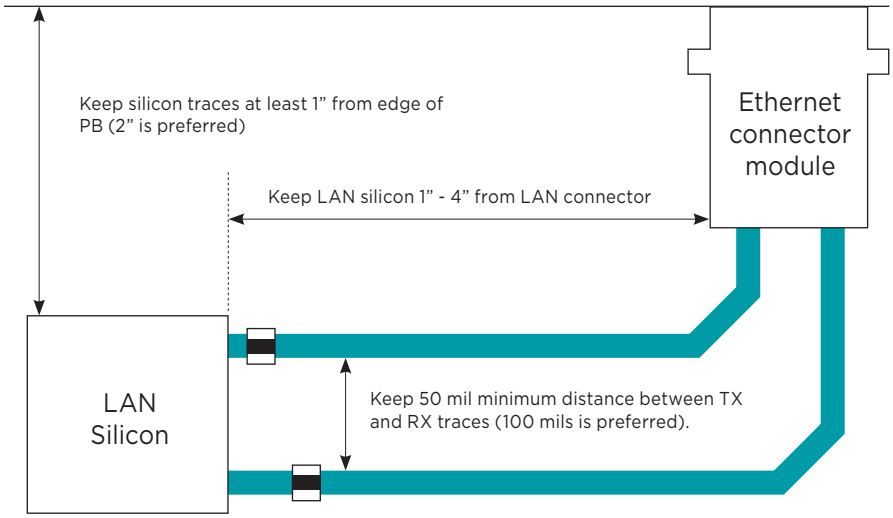

Figure 2. General Placement Distances

Trace Length and Symmetry

- Critical signal traces should be kept as short as possible to decrease the likelihood of any effects from other signals with high-frequency noise, including noise carried on power and ground planes. Keeping the traces as short as possible also helps reduce capacitive loading.
- Differential pairs should be routed to be as short and symmetrical as possible. The overall length of differential pairs should be less than four inches as measured from the controller across the Ethernet magnetic to the connector.
- The lengths of the differential traces (within each pair) should be equal to within 50 mils (1.25 mm) and as symmetrical as possible. Asymmetrical and unequal length traces in the differential pairs contribute to common mode noise.
- To reduce crosstalk interference on signals between pairs, the distance between unlike differential pairs must be more than 50 mils (1.25 mm). This rule also applies to differential pairs from other transceiver circuits on the same board.

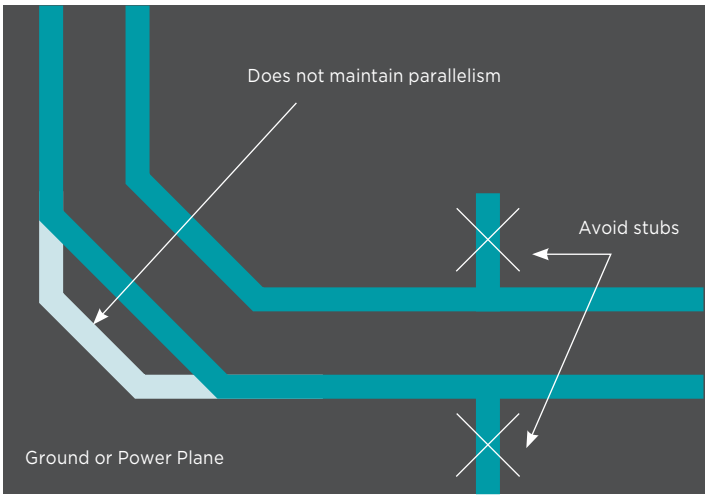

Figure 3. Differential Signal Pair – Stubs

- Stubs should be avoided on all signal traces, especially the differential signal pairs. See Figure 3.

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- Within the pairs (for example, TD+ and TD-) the trace lengths should be run parallel to each other and matched in length. Matched lengths minimize delay differences, avoiding an increase in common mode noise and increased EMI.
- Signal traces should not be run such that they cross a plane split. See Figure 4. A signal crossing a plane split may cause unpredictable return path currents and would likely impact signal quality as well, potentially creating EMI problems.
- Media Dependent Interface (MDI) signal traces should have 50 Ω to ground or 100 Ω differential controlled impedance.

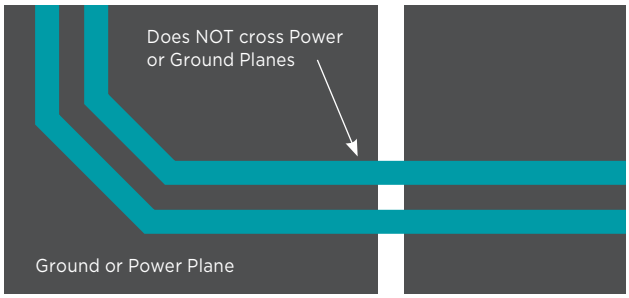

Figure 4. Differential Signal Pair-Plane Crossing

Differential Pair Trace Routing

To minimize the effects of crosstalk and propagation delays on sections of the board on which high-speed signals are routed, follow these trace routing guidelines:

- Place digital signals far away from the analog traces to help maintain signal integrity. A good rule of thumb to follow is that no digital signal should be located within 300 mils (7.5 mm) of the differential pairs.
- If digital signals on other board layers cannot be separated by a ground plane, they should be routed at right angles with respect to the differential pairs.
- Although ganged Ethernet connector modules are allowed, the signals for each circuit must also be carefully separated.
- Keep maximum separation within differential pairs to 10 mils.
- Ideally, there should be no crossover or via on the signal paths. Route an entire trace pair on a single layer if possible. Vias present impedance discontinuities and should be minimized; at most, use two vias per trace. For high-speed signals, keep the number of corners and vias to a minimum. If a 90° bend is required, use two 45° bends instead, as illustrated in Figure 5.
- Route traces away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.

Figure 5. Trace Routing

- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. As a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.
- Do not route differential pairs over splits in the associated reference plane.
- Place differential termination components as close as possible to the LAN silicon.

Signal Trace Geometry

- The key factors in controlling trace EMI radiation are the trace length and the ratio of trace width to trace height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1: 1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane.
- Each pair of signals should have a differential impedance of 100 Ω $\pm$ 15%. If a particular tool cannot design differential traces, it is permissible to specify 55 Ω to 65 Ω single-ended traces as long as the spacing between the two traces is minimized. As an example, consider a differential trace pair on Layer I that is 8 mils (0.2 mm) wide and 2 mils (0.05 mm) thick, with a spacing of 8 mils (0.2 mm). If the fiberglass layer is 8 mils (0.2 mm) thick with a dielectric constant, E^R, of 4.7, the calculated single-ended impedance would be approximately 61 Ω and the calculated differential impedance would be approximately 100 Ω.
- It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to 10 Ω, when the traces within a pair are closer than 30 mils (edge-to-edge).

Power and Ground Planes

Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return. These practices will significantly reduce EMI radiation. The following guidelines help reduce circuit inductance in both backplanes and motherboards.

- Route traces over a continuous plane with no interruptions. Do not route over a split power or ground plane. If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.

- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems.
- Connect all ground vias to every ground plane and every power via to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This will minimize the loop area.
- Avoid fast rise and fall times as much as possible. Signals with fast rise and fall times contain many high-frequency harmonics, which can radiate EMI.
- Split ground planes beneath magnetic modules. The RJ45 connector side of the magnetic module should have chassis ground beneath it.

Ground Planes Under the Ethernet Magnetic

There should be no ground planes beneath a discrete LAN magnetics package in order to minimize any possible coupling between components that are relatively close to the surface of the PCB (as illustrated in Figure 6). For integrated connector modules, the chassis ground plane should run under the component to connect with the shield of the connector (as shown in Figure 7). Within the connector module, all magnetic components are far enough away from the PCB to prevent any unwanted coupling of signals.

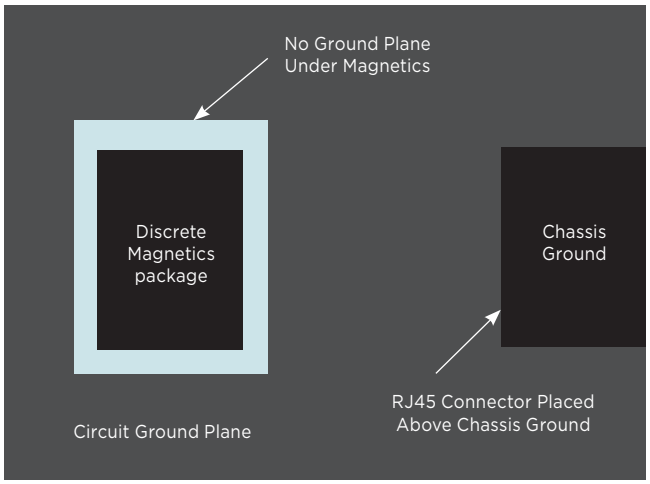

Figure 6. No Ground Planes Beneath Discrete Magnetics

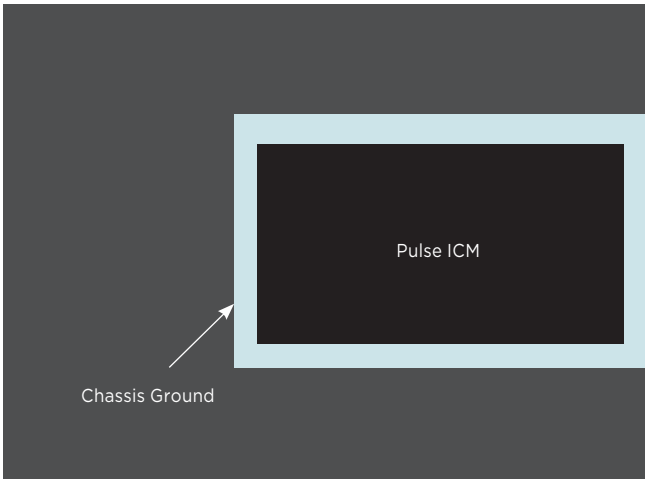

Figure 7. The Chassis Ground Plane Should Run Beneath the Integrated Connector Module (ICM).

Troubleshooting Common Physical Layout Issues

Check for these common physical layer design and layout mistakes in LAN on motherboard designs.

1. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
2. Lack of symmetry between the two traces within a differential pair. Asymmetry can create common-mode noise and distort the waveforms. For each component and via that one trace encounters, the other trace should encounter the same component or via at the same distance from the Ethernet silicon.
3. Excessive distance between the Ethernet silicon and the Ethernet magnetic. Long traces on FR-4 fiberglass epoxy substrate will attenuate the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are longer than four inches.
4. Routing any other trace parallel to and close to one of the differential traces. If crosstalk gets onto the receive channel, it will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive EMI emissions and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inches from the differential traces.
5. Routing one pair of differential traces too close to another pair of differential traces. After exiting the Ethernet silicon, the trace pairs should be kept 0.3 inches or more away from the other trace pairs. The only possible exceptions are in the vicinities where the traces enter or exit the Ethernet magnetic, the RJ45 connector, and the Ethernet silicon.
6. Re-use of an out-of-date physical layer schematic in an Ethernet silicon design. The terminations and decoupling can be different from one PHY to another.

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7. Incorrect differential trace impedances. It is important to have ~100 Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two, but this does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close to each other, the edge coupling can lower the effective differential impedance by 5 Ω to 20 Ω. Short traces will have fewer problems if the differential impedance is slightly off target.

Layout Issues and Configurations Specific to 1000BASE-T to 10GBASE-T Four-Pair Ethernet Applications

Termination Plane and Chassis Ground

In 1000BASE-T, 2.5GBASE-T, 5GBASE-T, and 10GBASE-T systems, the main design elements are the transceiver (PHY), the Ethernet magnetic and the RJ45 connector. In many cases, the Ethernet magnetic and RJ45 connector can be replaced with an Ethernet connector module. Because the transmission line medium extends onto the printed circuit board, special attention must be paid to layout and routing of the differential signal pairs.

Printed circuit boards for 1000BASE-T, 2.5GBASE-T, 5GBASE-T, and 10GBASE-T designs often have six or more layers. In these designs, it is common practice to terminate center tap Ethernet magnetic connections to ground as a path for low frequency noise. Depending on the overall shielding and grounding design, the specific ground used for this purpose can vary. We recommend the use of a dedicated termination plane, with the center tap leads connected to the termination plane through 75 Ω resistors.

The termination plane is typically fabricated in Layer I, with a matching chassis ground plane underneath as illustrated in Figure 8. The clearance between the termination plane and any traces should be at least 50 mils (1.25 mm) to prevent arcing during high voltage tests. The termination plane and chassis ground layer combination has some capacitance, which can be augmented by adding a discrete 1500 pF capacitor.

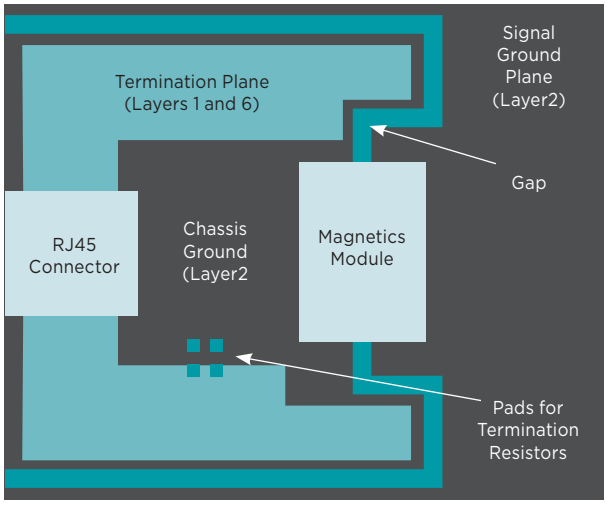

Figure 8. Termination Plane and Chassis Ground

The Ethernet connector module also contains the termination plane, 75 Ω termination resistors and a 1000 pF to 1500 pF capacitor. If integrated components are going to be used, their internal design needs to be evaluated carefully. The electrical parameters, EMI, and high voltage test results should be equivalent to, or better than, the characteristics of a discrete design.

Additional capacitors are required to interconnect chassis ground and signal ground. The suggested technique is to use several different capacitor values (for example, two 1000 pF, one 4.7 mF, and one 10 µF). Depending on available board space, one set of capacitors should be placed on each side of the Ethernet magnetic. Modifications to this interconnection scheme are possible.

In general, no ground plane should extend under the TX and RX differential pairs, under the Ethernet magnetic, or under the RJ45 jack. In cases where common mode capacitors are used for EMI suppression, a ground plane may be located under the TX and RX signals; however, the plane must not extend beyond the capacitors. When designing 4-layer boards, the ground plane should exist on layer 4, assuming the differential pair is routed on layer 1. On 2-layer boards, the ground plane can be located on layer 2, the layer adjacent to the TX and RX signal pairs. Under no circumstances should a ground plane exist under the Ethernet magnetic, the RJ45 connector, or in between the Ethernet magnetic and RJ45 connector. See Figure 9.

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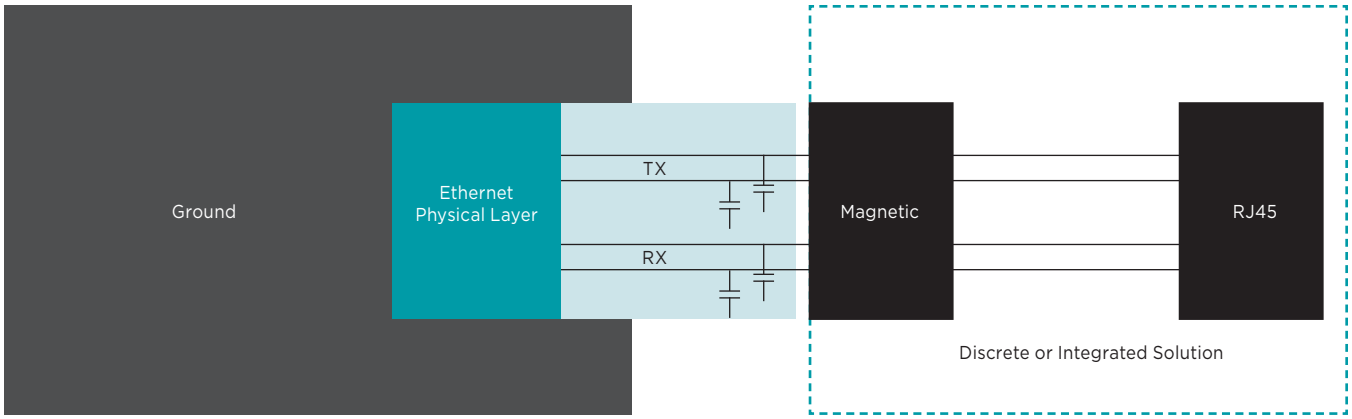

Figure 9. Ground Planes

Layout Issues and Configurations Specific to Power over Ethernet (PoE) Applications

Isolation and Termination

According to the IEEE 802.3af and the IEEE802.3at standards, certain isolation requirements need to be met in all PoE equipment. In addition, EMI limitations should be considered, as specified in the FCC and European EN regulations.

PoE Best Practices

- Layering ground planes is advisable. Route connector/discrete module ground pins to chassis/analog ground if possible. Keep signal traces from PHY to connector/discrete module as short as possible. If traces exceed 3-4 inches, pay close attention to line impedance imbalance.
- Using Bob Smith Termination (BST - 75 Ω resistors and high voltage cap to chassis ground) to terminate cable side center taps is advisable for best EMI performance (included in most connector solutions). Consult the PHY manufacturer's application notes for further layout considerations.
- To maintain 1500Vrms isolation between two adjacent layers of a NEMA FR-4 multi-layer PCB, a minimum of 15 mils isolation thickness is recommended. This provides a safe margin for hi-pot requirements.
- Take special care when routing the ground and power signals lines.

PoE Application Circuits

Figure 10 and Figure 11 illustrate 100BASE-TX and 1000BASE-T, 2.5GBASE-T, 5GBASE-T, and 10GBASE-T PoE application

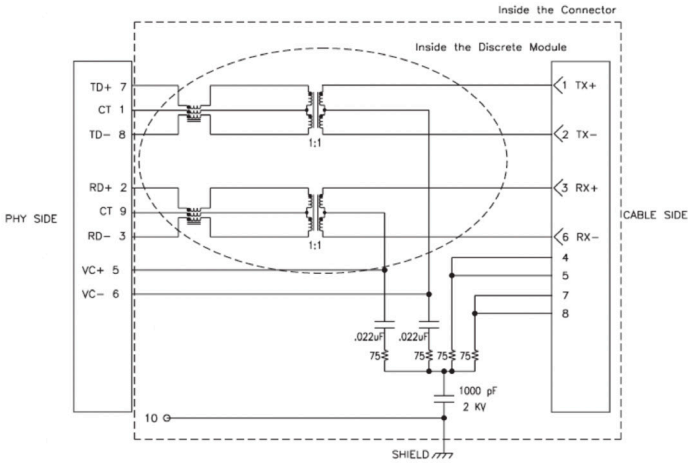

Figure 10. 100BASE-TX PoE Application Circuit

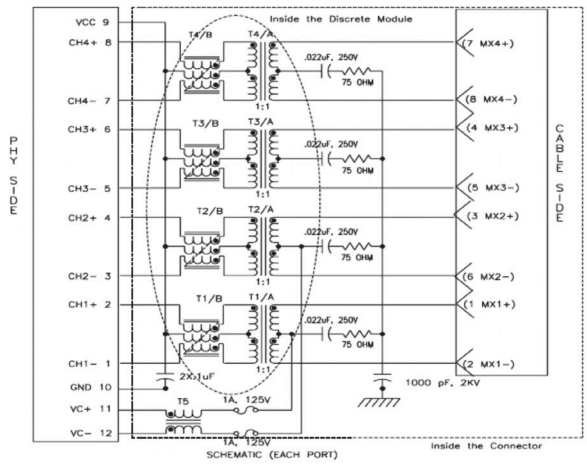

Figure 11. 1000BASE-T, 2.5GBASE-T, 5GBASE-T, and 10GBASE-T PoE Application Circuit

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