

# Development Kit S7G2 (DK-S7G2)

Quick Start Guide

Renesas Synergy™ Platform  
Synergy Tools & Kits  
Kits: DK-S7G2

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## General Precautions

### 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

### 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

### 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

### 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

### 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

### 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

### 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

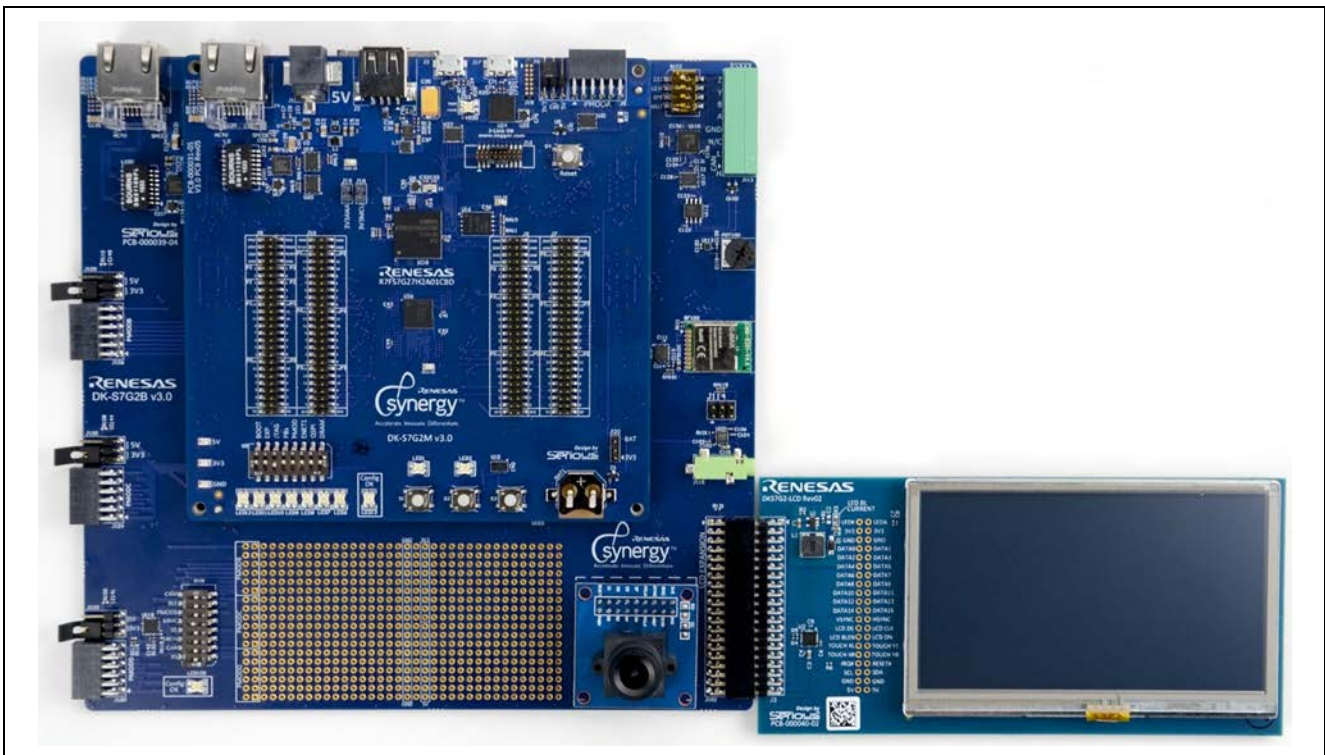
### 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

### 1. In the box

The following components are included in the Renesas Synergy™ Development Kit (DK-S7G2):

- DK-S7G2 Main Board
- DK-S7G2 Breakout Board (DK-S7G2B)
- Detachable 4.3-inch resistive-touch WQVGA (480 x 272) TFT LCD panel (DK-43TFTLCD)
- Detachable CMOS VGA camera module
- One USB Type A to Micro-B cable
- One Ethernet cable
- Multi-region 5V power supply
- Quick Start Guide

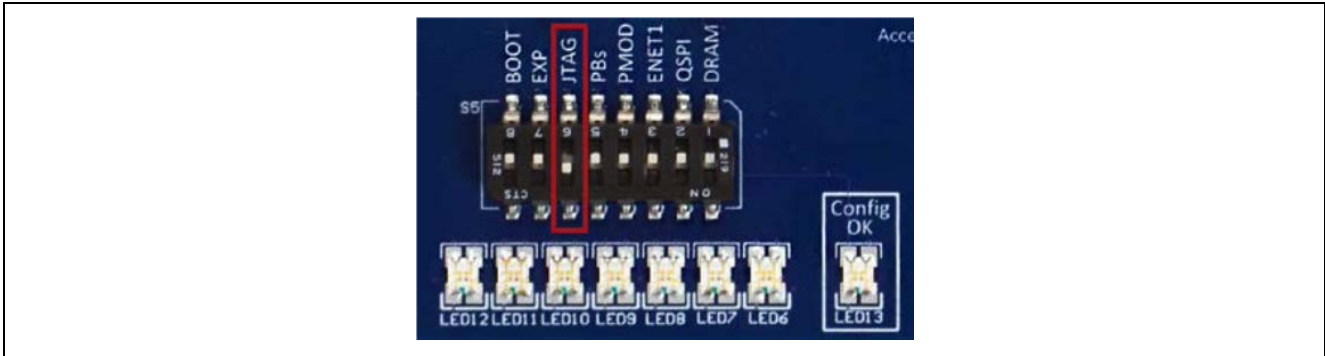


## 2. Overview

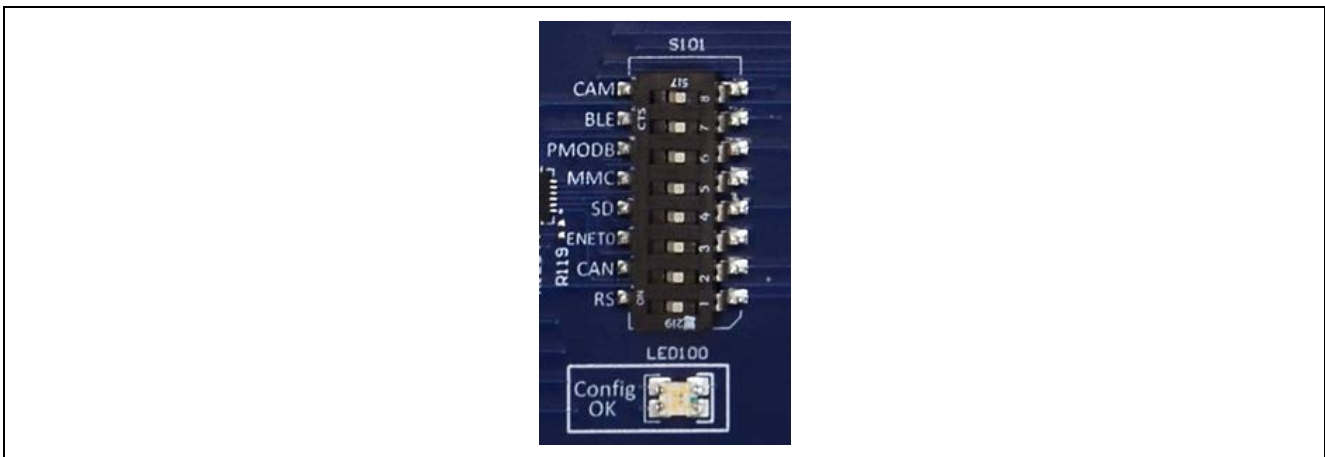
This Synergy Development Kit and its associated development tools provide the user with a platform to develop products with the Synergy Microcontrollers S7 Series. The Quick Start Guide walks the user through using the Out-of-Box Demo.

## 3. Connecting the board components

1. Set the JTAG DIP switch 6 on S5 to ON (toward the LEDs).

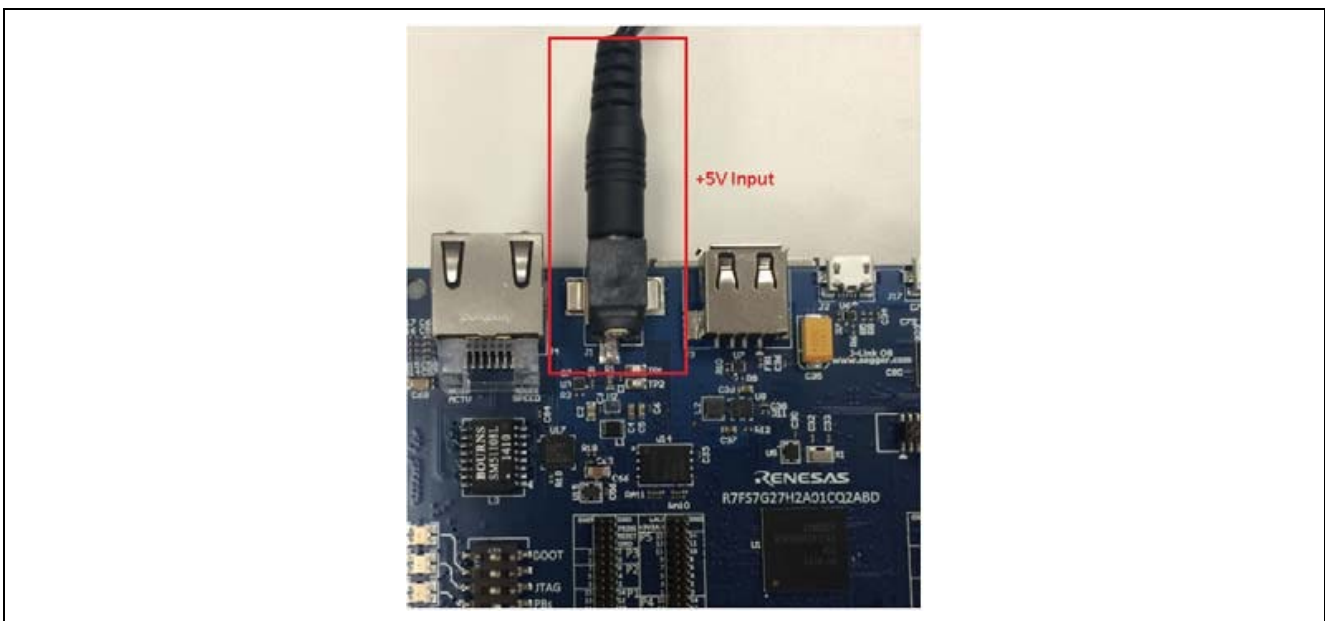


2. Verify all the S101 DIP switches on the Breakout Board are set to OFF.

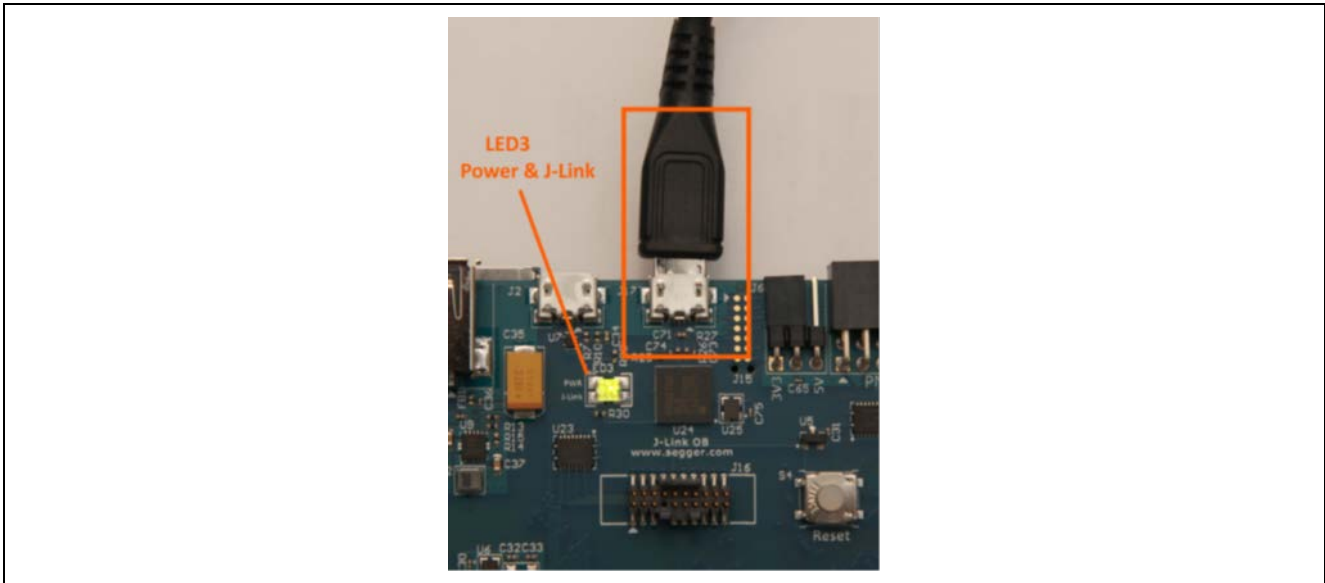


3. Using the power supply provided with the DK-S7G2, apply power through the 5V barrel connector (J1) on the Main Board. LED3 turns Green with a flashing-Red below it.

The solid-Green/flashing-Red LED3 indicates the kit cannot communicate with the PC on the debug port.



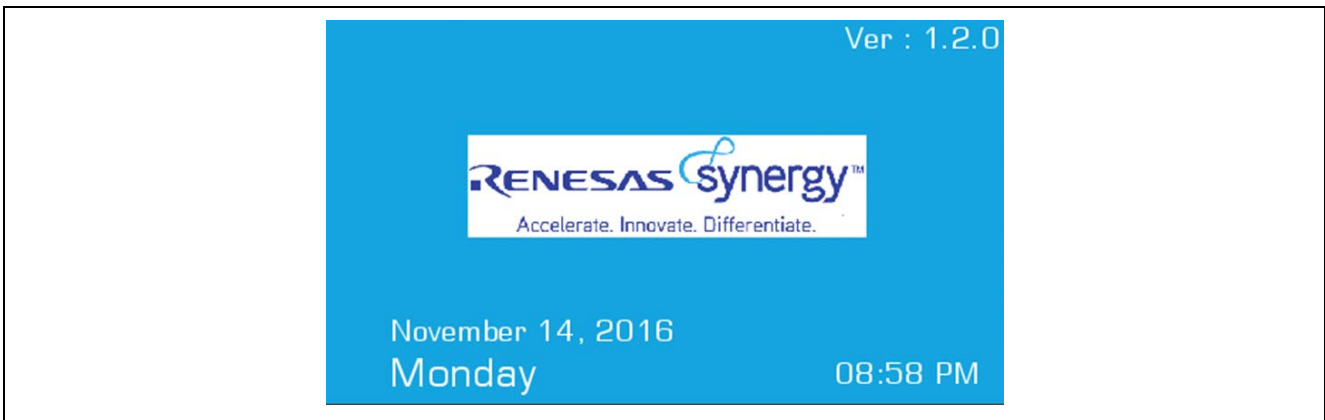
4. Connect the USB cable provided with the DK-S7G2 J-Link OB (J17) on the Main Board.



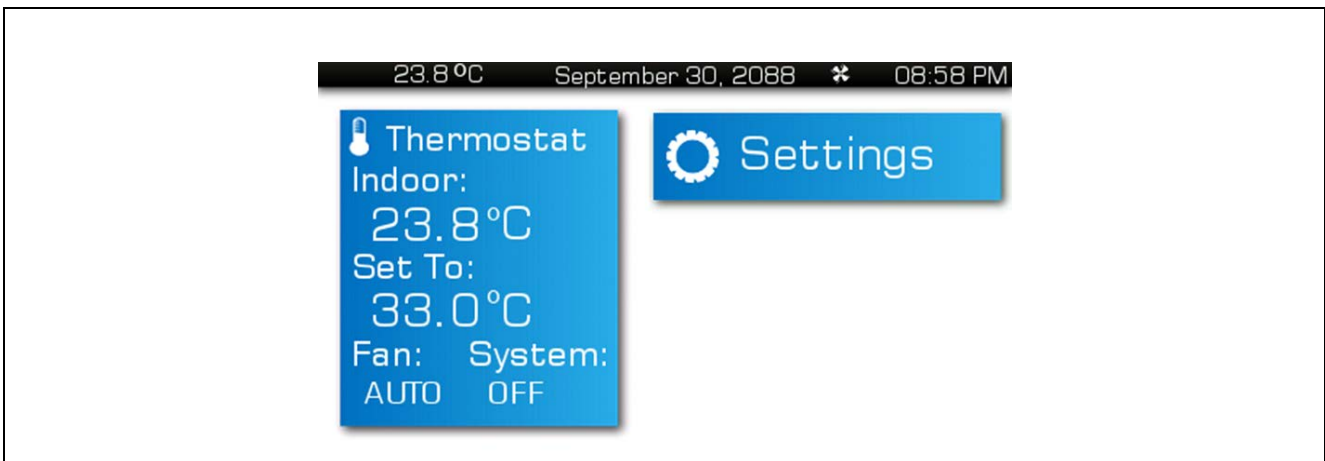
5. Connect the other end of the USB cable to a USB port of the PC. LED3 now turns solid-Green to indicate a good PC connection.

#### 4. Running the Out-of-Box Demo

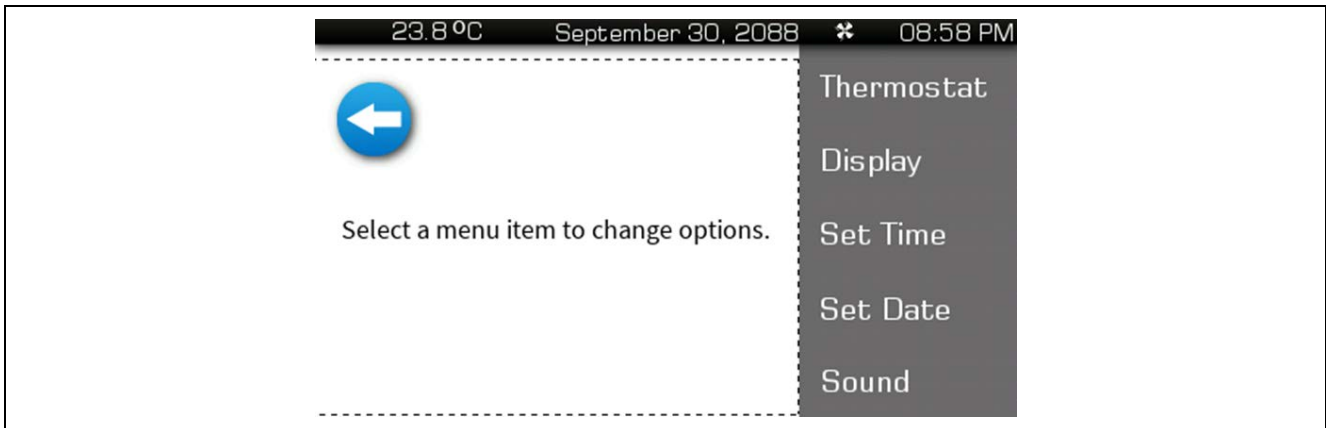
1. During initialization, the S7G2 turns the LEDs it can control Red and Green. S7G2 turns on and off the Red LEDs inside the Ethernet connectors to verify those work. At the end of initialization, LED1 and LED2 turn off and the Configuration LEDs, LED6 to LED12, turn Green.
2. A splash screen displays on the LCD showing the date and time. Press anywhere on the splash screen to go into the **Thermostat Demo**.



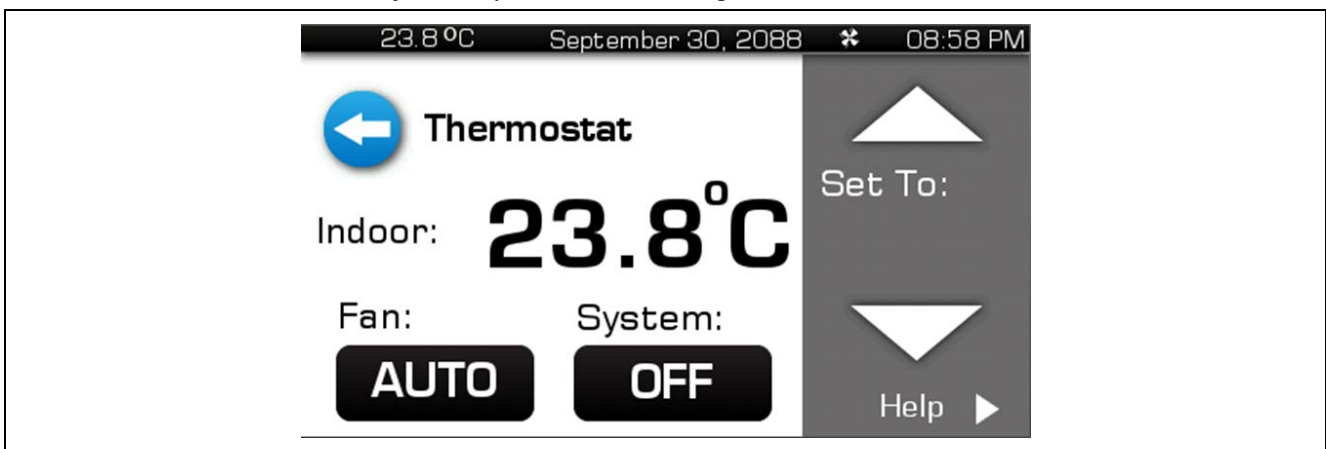
3. Press **Settings** on the top right.



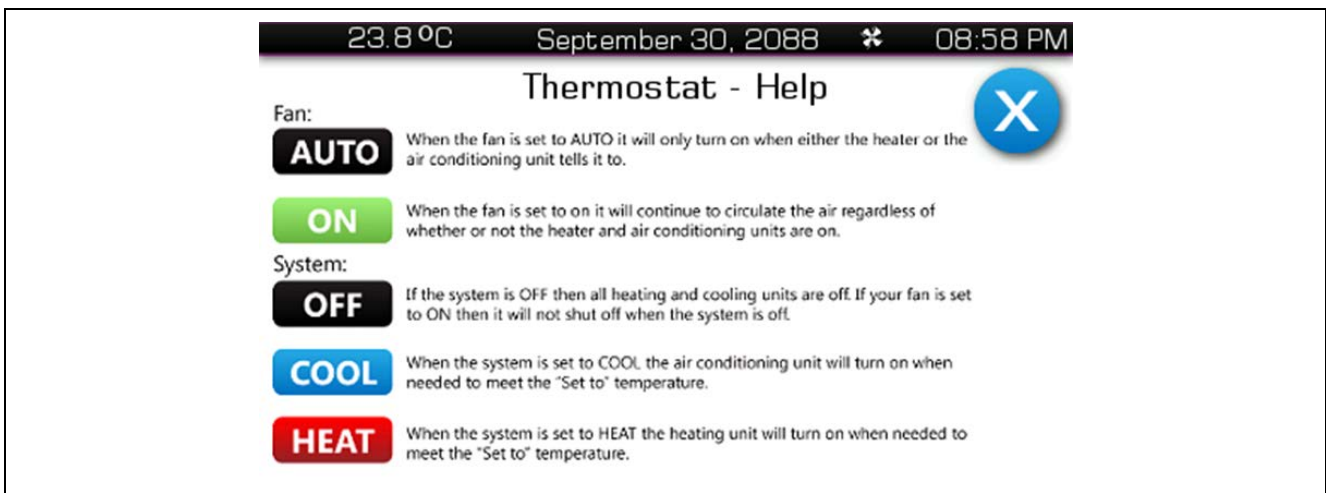
- Go to Units to adjust the demo for these settings: **Display, Set Time, Set Date, and Sound.**



- Click on the left side of the Thermostat main screen to enter the Thermostat control menu. With the Control menu, adjust the System, Fan, and Temperature.



Press the **Help** button to show the detailed Help screen.



## 5. Next steps

1. Visit the [DK-S7G2 kit page](http://www.renesassynergy.com/kits/dk-s7g2) for more information (<http://www.renesassynergy.com/kits/dk-s7g2> )
2. Visit the [tools section of the Synergy Explorer](http://synergyexplorer.renesas.com) site to learn more about development tools & utilities (<http://synergyexplorer.renesas.com>)
3. Visit the [Synergy Gallery](https://synergygallery.renesas.com) to download development tools & utilities (<https://synergygallery.renesas.com>).
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## Orderable Part Number

The part number for the DK-S7G2 is YSDKS7G2E31.

## Website and Support

Support: <https://synergygallery.renesas.com/support>

Technical Contact Details:

- America: [https://renesas.zendesk.com/anonymous\\_requests/new](https://renesas.zendesk.com/anonymous_requests/new)
- Europe: <https://www.renesas.com/en-eu/support/contact.html>
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## FCC Compliance

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

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## Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Oct 9, 2015	–	Initial release
1.01	May 2, 2017	All	Fixed terminologies

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