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APPLICATION NOTE 6042

## PMBUS PROTOCOLS FOR CONTROLLING AND MONITORING THE MAX20743/MAX20730 SWITCHING REGULATORS

Abstract: The MAX20743/MAX20730 fully integrated switching regulators include a serial bus (PMBus) that supports advanced regulator monitoring and control capabilities. This application note covers the serial interface protocols used for controlling and monitoring the ICS.

### MAX20734 PMBus Interface Overview

The MAX20734 fully integrated switching regulator includes a serial bus (PMBus™) that supports advanced regulator monitoring and control capabilities. This application note covers the MAX20734 silicon that reports F as the revision through the PMBus manufacturing revision command. The PMBus interface supports a subset of the PMBus 1.2 and SMBus 2.0 specifications. More information about these specifications can be found at [www.pmbus.org](http://www.pmbus.org) and [www.smbus.org](http://www.smbus.org). The following PMBus features are supported:

- Static PMBus address programming with external resistors
- Compliant with high-power SMBus DC specification
- Support PMBus protocols
- Write byte/word
- Read byte/word
- Send byte
- Block read
- Packet error checking mechanism support
- SMBALERT# signal

### Monitoring Functions

The following monitoring functions are available through the MAX20734 PMBus interface:

- Various fault status
- Parameters programmed using R\_SEL configuration resistors
- Input voltage
- Output voltage
- Junction temperature
- Output current

### Control Functions

- Overtemperature fault thresholds
- Output current fault threshold
- Output voltage command
- Output voltage minimum and maximum thresholds
- Operation: On and off configuration
- Regulation to power-good delay timing
- Soft-start timing
- Frequency
- Overcurrent protection mode
- Internal gain values
- Output voltage command ramping rate

### MAX20734 PMBus Protocol

#### Write/Read Format

The MAX20734 PMBus interface supports single-byte, dual-byte (word) register read/write, block read, as well as send byte protocols. Table 1 to Table 6 show the format used for all supported operations. Note that packet error checking can be used on any transaction. Table 7 shows the MAX20734 PMBus command codes. A 0x0h written to the WRITE\_PROTECT register (Reg\_10h) disables the write-protect feature and 0x20h turns on the write protect to all registers except the OPERATION and VOUT\_COMMAND registers.

Table 1. Read Byte Format

# of bits	1	7	1	1	8	1	1	7	1	1	8	1	1
	S	PMBus Address	W	S-ACK	Command	S-ACK	S	PMBus Address	R	M-ACK	Data Byte	M-NACK	P

Table 2. Write Byte Format

# of bits	1	7	1	1	8	1	8	1	1
	S	PMBus Address	W	S-ACK	Command	S-ACK	Data Byte	S-ACK	P

Table 3. Read Word Format

# of bits	1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
	S	PMBus Address	W	S-ACK	Command	S-ACK	S	PMBus Address	R	S-ACK	Data Byte Low	M-ACK	Data Byte High	M-NACK	P

Table 4. Write Word Format

# of bits	1	7	1	1	8	1	8	1	8	1	1
	S	PMBus Address	W	S-ACK	Command	S-ACK	Data Byte Low	S-ACK	Data Byte High	S-ACK	P

Table 5. Send Byte Format

# of bits	1	7	1	1	8	1	1
	S	PMBus Address	W	S-ACK	Command	S-ACK	P

Table 6. Block Read Format

# of bits	1	7	1	1	8	1	1	7	1	1	8	1	1
	S	PMBus Address	W	S-ACK	Command	S-ACK	S	PMBus Address	R	S-ACK	Byte Count = N	M-ACK	
					8	1	8	1	8	1	8	1	1
					Data Byte 1	M-ACK	Data Byte 2	M-ACK	...	Data Byte N	M-NACK	P	

### Tables 1 To 6 Legend

S	START condition: Clock and data lines initially high. Data transitions low while clock is high. Clock transitions low.
P	STOP condition: Clock and data lines initially low. Clock transitions high while data is low. Data transitions high.
R	Read bit (logic-high)
W	Write bit (logic-low)
Command	Relevant MAX20734 PMBus register
S-ACK	Slave acknowledge
M-ACK	Master acknowledge
M-NACK	Master no-acknowledge

- Note 1.** Packet error check (PEC) can be used in conjunction with these commands.  
**Note 2.** The PEC is a CRC-8 error checking byte, calculated on all the message bytes.  
**Note 3.** The OEN signal does not need to be high to communicate over the PMBus interface.

Table 7. MAX20734 PMBus Command Codes

Command Code	Dec	Command Name	Type	Size	Default	Low Byte	High Byte							
01h	1	OPERATION	RW	1	00h	OE_INT	0	0	0	0	0	0	0	0
02h	2	ON_OFF_CONFIG	RO	1	1Fh	0	0	0	1	1	1	1	1	
03h	3	CLEAR_FAULTS	WO	0										
10h	16	WRITE_PROTECT	RW	1	20h									
1Bh	27	SMBALERT_MASK	RW	2	N/A	ALERT-MASK [7:0]						ALERT-MASK[15:8]		
20h	32	VOUT_MODE	RO	1	17h	0	0	0	1	0	1	1	1	
21h	33	VOUT_COMMAND	RW	2	C_SELA					VDAC[7:0]	0	0	0	0
24h	36	VOUT_MAX	RW	2	0280h					VMAX[7:0]	0	0	0	0
78h	120	STATUS_BYTE	RO	1	00h	BUSY	OFF#	VOUT_OV_FAULT	IOUT_OC_FAULT	VIN_UV_FAULT	TEMP	CML	N/A	
79h	121	STATUS_WORD	RO	2	0000h	BUSY	OFF#	VOUT_OV_FAULT	IOUT_OC_FAULT	VIN_UV_FAULT	TEMP	CML	N/A	
7Ah	122	STATUS_VOUT	RO	1	00h	OVP_FLT	0	0	UVP_FLT	VOUTMA_X_FLT	0	0	0	

7Bh	123	STATUS_IOUT	RO	1	00h	OCF_FLT	0	0	0	0	0	0	0	0	0	0	0	0
7Ch	124	STATUS_INPUT	RO	1	00h	RSVD	0	0	FUVLO_FLT	FUVLO_FLT	0	0	0	0	0	0	0	0
7Dh	125	STATUS_TEMPERATURE	RO	1	00h	OTP_FLT	0	0	0	0	0	0	0	0	0	0	0	0
7Eh	126	STATUS_CML	RO	1	00h	INVALID/ UNSUPPORTED CMD	INVALID/ UNSUPPORTED DATA	INCORRECT PEC	0	0	0	0	0	0	0	0	0	OTHER COMM FAULT
80h	128	STATUS_MFR_SPECIFIC	RO	1	00h	VOUTMIN_FLT	SEALR_FLT	RADC_FLT	AUVLO_FLT	BOOST-FAULT	VXSHORT _FLT	VSN_ VSP_ FLT	LDO_OFF					
88h	136	READ_VIN	RO	2	N/A				VINADC_AVE[7:0]				0	0	0	0	0	VINADC_AVE[9:8]
8Bh	139	READ_VOUT	RO	2	N/A				VADC_AVE[7:0]				0	0	0	0	0	VADC_AVE[9:8]
8Ch	140	READ_IOUT	RO	2	N/A				IADC_AVE[7:0]				0	0	0	0	0	IADC_AVE[9:8]
8Dh	141	READ_TEMPERATURE_1	RO	2	N/A				TADC_AVE[7:0]				0	0	0	0	0	TADC_AVE[9:8]
99h	152	MFR_ID	BLK	5	N/A				ASCII "MAXIM"(HEX CODES 56h, 4Ch,n54h, 52h)									
9Bh	155	MFR_REVISION	BLK	1	N/A													ASCII "F" (HEX CODE 31h)
D1h	209	MFR_VOUT_MIN	RW	2	0133h				VMIN[7:0]				0	0	0	0	0	VMIN[9:8]
D2h	210	MFR_DEVSET1	RW	2	2061h	0			OCF[1:0]		FSW[2:0]		TSTAT[1:0]	0	RGAIN[1:0]	OTP[1:0]	0	VBOOT[1:0]
D3h	211	MFR_DEVSET2	RW	2	03A6h		VRATE[1:0]	HICCUP_EN	RSVD	RSVD	RSVD	SFT_START[1:0]	0	0	0	0	0	IMAX[2:0]

RW = Read Write, RO = Read Only, WO = Write Only, BLK = Block Read. VBOOT[1:0] values in MFR\_DEVSET1 are programmed by the external capacitor (C\_SELA ) and equal to binary value 00b, here representing  $V_{BOOT} = 0.65V$ .

#### Configuring the MAX20734 Address

The MAX20734 PMBus address is set through R\_SELA. Eight unique addresses are possible, as shown in Table 8.

Table 8. MAX20734 PMBus Address Byte

PMBus ADDRESS (PMAD)	CONSTANT/VARIABLE
(6)(MSB)	Constant = 1
(5)	Constant = 0
(4)	Constant = 1
(3)	Constant = 0
(2)	R_SELA_bit2
(1)	R_SELA_bit1
(0)	R_SELA_bit0

#### Status Reporting

The MAX20734 supports the status registers shown in Figure 1. The CLEAR\_FAULTS command is used to clear any fault bits that have been set, and clear the device's SMALERT pin output. The CLEAR\_FAULTS command does not cause a unit that has been latched off for a fault condition to restart. To restart after a latched fault, power must be cycled. If the fault is still present after power is cycled, the fault bit is set again.

The STATUS\_BYTE contains the most important faults and warnings. The STATUS\_WORD contains two bytes of information. The low byte of the STATUS\_WORD is the same as the STATUS\_BYTE, and the high byte contains additional information about the status of the device.

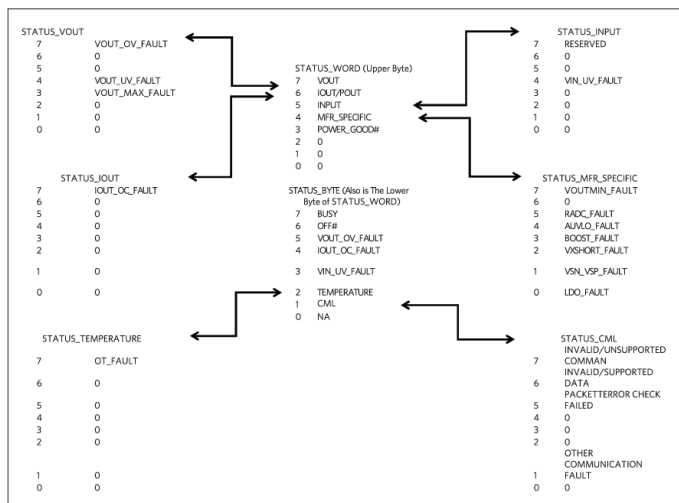


Figure 1. Summary of Status registers.

Table 9. STATUS\_WORD

BYTE	BIT NUMBER	STATUS BIT NAME	MEANING
Low	7	BUSY	A fault is asserted because the device was busy and unable to respond.
	6	OFF#	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.

	5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
	4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
	3	VIN_UV_FAULT	An input undervoltage fault has occurred.
	2	TEMPERATURE	A temperature fault has occurred.
	1	CML	A communications, memory, or logic fault has occurred.
	0	N/A	N/A
High	7	VOUT	An output voltage fault has occurred.
	6	IOUT/POUT	An output current fault has occurred.
	5	INPUT	An input voltage, input current, or input power fault has occurred.
	4	MFR_SPECIFIC	A manufacturer specific fault or warning has occurred.
	3	POWER_GOOD#	If this bit is set, power is not good.
	2	N/A	N/A
	1	N/A	N/A
	0	N/A	N/A

### Control

#### Operation/On and Off Configuration

The OPERATION command is used to turn on (0x80h) and turn off (0x0h) with OE pin low, as determined by the ON\_OFF\_CONFIG, which is fixed at 0x1Fh.

#### Output Voltage Control

The following registers are used for output voltage-related configuration settings. All the formats are in linear mode with N = -9, which is indicated in the V<sub>OUT</sub> Mode register (Reg\_20h) value of 0x17h. The output voltage command (Reg\_21h) and other output voltage related commands are a 2-bit unsigned variable. The output voltage formulas follow:

$$\frac{V_{OUT}}{V} = \text{REG\_21h (BITS 15:0)} \times 2^{N-9} \quad (\text{Eq. 1})$$

$$\frac{V_{OUTMAX}}{V} = \text{REG\_24h (BITS 15:0)} \times 2^{N-9} \quad (\text{Eq. 2})$$

$$\frac{V_{OUTMIN}}{V} = \text{REG\_D1h (BITS 15:0)} \times 2^{N-9} \quad (\text{Eq. 3})$$

#### Configuration Registers

The PGMA and PGMB configuration resistors and capacitors are used to configure PMBus address, soft-start timing, boot voltage overcurrent protection limit, internal gain setting, and frequency. There are two PMBus registers, MFR\_DEVSET1 and MFR\_DEVSET2, that can be used to check and override these settings. The other system parameters that can be changed by these two configuration registers include regulation to power-good delay timing, overtemperature protection limit, output voltage command ramping rate, and overcurrent protection mode. The override parameters revert back to default values once power is cycled.

MFR\_DEVSET2 (Reg\_D3h) is used to program the soft-start timing as shown in Table 11.

Table 10. PGMA (R\_SELA)

NO.	R (k )	SS TIME (ms)	SLAVE ADDRESS (1010_XXXX)
1	1.78	3	PMBus Slave Address 1010 000b
3	4.02	3	PMBus Slave Address 1010 010b
4	6.04	3	PMBus Slave Address 1010 011b
5	9.09	3	PMBus Slave Address 1010 100b
6	13.3	3	PMBus Slave Address 1010 101b
7	20	3	PMBus Slave Address 1010 110b
8	30.9	3	PMBus Slave Address 1010 111b
9	46.4	1.5	PMBus Slave Address 1010 000b
10	71.5	1.5	PMBus Slave Address 1010 001b
11	107	1.5	PMBus Slave Address 1010 010b
12	162	1.5	PMBus SlaveAddress 1010 011b

Table 11. Soft-Start Timing

SFT-START[1:0]	SOFT-START TIME (ms)
00b	0.75
01b	1.5
10b	3
11b	6

MFR\_DEVSET1 (Reg\_D2h (bits 9:8)) is used to read the boot voltage as shown in Table 12.

Table 12. Boot Voltage

V <sub>BOOT</sub> [1:0]	V <sub>BOOT</sub> VOLTAGE (V)
00b	0.6484
01b	0.8984
10b	1.0
11b	N/A

#### Other System Parameters

##### Overcurrent Protections

Overcurrent protection MFR\_DEVSET1 (Reg\_D2h (bits 6:5)) is used to set the positive and negative overcurrent inception and clamp level as shown in Table 13.

Table 13. OCP Settings

OCP[1:0]	OCP SETTING
00b	Setting 0
01b	Setting 1
10b	Setting 2
11b	Setting 3

##### Temperature Control

MFR\_DEVSET1 (Reg\_D2h (bits 12:11)) is used to program the overtemperature trigger level as shown in Table 14.

Table 14. Overtemperature Shutdown Limit

OTP[1:0]	OVERTEMPERATURE (°C)
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00b	150
01b	130
10b	N/A
11b	N/A

#### Internal Gain Setting

MFR\_DEVSET1 (Reg\_D2h) is used to program the internal gain setting as shown in Table 15.

Table 15. Internal Gain Setting

R_GAIN[1:0]	R_GAIN (m )
00b	0.8
01b	3.2
10b	1.6
11b	6.4

#### Boot Voltage to Output Voltage Command Ramp Rate

MFR\_DEVSET2 (Reg\_D3h (bits 7:6)) is used to program the boot voltage to output voltage command ramp rate as shown in Table 16.

Table 16. Output Voltage Ramping Rate

V_RATE[1:0]	V_RATE (mV/μs)
00b	4
01b	2
10b	1
11b	N/A

#### Frequency

MFR\_DEVSET1 (Reg\_D2h (bits 4:2)) is used to program the switching frequency as shown in Table 17.

Table 17. Frequency Register

FSW[2:0]	FREQUENCY (kHz)
000b	400
001b	500
010b/011b	600
100b	700
101b	800
110b/111b	900

#### Regulation to Power-Good Delay Timing

MFR\_DEVSET1 (Reg\_D2h) is used to program the tSTAT time as shown in Table 18.

Table 18. tSTAT Register

TSTAT [1:0]	tSTAT TIME (μs)
00b	2000
01b	125
10b	62.5
11b	32

#### Output Current Overcurrent Mode

MFR\_DEVSET2 (Reg\_D3h) is used to program the output current overcurrent mode as shown in Table 19.

Table 19. Overcurrent Protection Mode

CODE (BINARY)	OCF MODE
0b	Constant current
1b	Hiccup

#### Read Telemetry

The MAX20734 provides reporting of junction temperature, output current, input voltage, and voltage at the sense pins. With direct feedback, the voltage at the sense pins equals  $V_{OUT}$ . With a divider in the feedback, the voltage at the sense pins is scaled by the divide ratio.

#### Read Output Current

Read  $I_{OUT}$  returns the output current in amperes. The data is in PMBus DIRECT format, with R = -1, and m and b as defined below.

$$READ I_{OUT} = \frac{(REG\ 8Ch\ (BITS\ 15:0) \times 10^{R-b})}{m} + a \times (T_1-50)(AMPS) \quad (Eq. 4)$$

where: m = 111 - 3.4 × D  
b = 3461 - 114 × D  
D =  $V_{OUT}/V_{IN}$   
a = 0.13  
T<sub>J</sub> = junction temperature reading in °C

#### Read Temperature

Read temperature returns the junction temperature in °C. The data is in PMBus DIRECT format with m = 21, b = 5887, and R = -1.

$$READ TEMP = \frac{(REG\ 8Dh\ (BITS\ 15:0) \times 10^{R-b})}{m} \quad (°C) \quad (Eq. 5)$$

#### Read Output Voltage

Read  $V_{OUT}$  returns the output voltage in volts. The data is in PMBus LINEAR format, with N = -9.

$$READ V_{OUT} = REG\_8Bh\ (BITS\ 9:0) \times 2^N\ (VOLTS) \quad (Eq. 6)$$

#### Read Input Voltage

Read  $V_{IN}$  returns the input voltage in volts. The data is in PMBus DIRECT format with m = 3592, b = 0, and R = -2.

$$READ I_{IN} = \frac{(REG\ 88h\ [BITS\ 10:0] \times 10^{R-b})}{m} \quad (VOLTS) \quad (Eq. 7)$$

#### ARA READ/PMBus Alert

The MAX20734 supports the alert response address (ARA) protocol as described in the SMBus 2.0 Specification. Refer to the SMBus 2.0 Specification Appendix A for more details.

#### PMBus Alert Pin

The MAX20734 SMBALERT pin supports the SMBALERT# signal described in the SMBus 2.0 specification. The fault conditions that assert the alert line low are as follows:

- Any bits different from 0 and not masked by SMBALERT\_MASK command pull low SMALERT pin in STATUS\_CML.
- Any bits different from 0 and not masked by SMBALERT\_MASK command pull low SMALERT pin in STATUS\_VOUT.
- Any bits different from 0 and not masked by SMBALERT\_MASK command pull low SMALERT pin in STATUS\_IOUT.
- Any bits different from 0 and not masked by SMBALERT\_MASK command pull low SMALERT pin in STATUS\_TEMPERATURE.
- Any bits different from 0 and not masked by SMBALERT\_MASK command pull low SMALERT pin in STATUS\_MFR\_SPECIFIC.
- Any bits different from 0 and not masked by SMBALERT\_MASK command pull low SMALERT pin in STATUS\_INPUT.
- PMBus message lasts longer than expected.

SMBALERT\_MASK is used to prevent a warning or fault condition from asserting the SMALERT pin. The command format (write word) used to block a status bit or bits from causing the SMALERT pin to be asserted is shown in **Table 20**. The bits in the mask byte align with the bits in the corresponding status register.

**Table 20. SMBALERT\_MASK Command Packet Format**

# of bits	1	7	1	1	8	1	8	1	8	1	1
	S	PMBus Address	W	ACK	SMBALERT_MASK Command Code	ACK	Status_x Command Code	ACK	Mask Byte	ACK	P

The two ways to release the SMALERT pin are as follows:

- CLEAR\_FAULTS command
- ARA (refer to SMBus Specification 2.0)

Related Parts	
MAX20730	Integrated, Step-Down Switching Regulator with PMBus
MAX20743	Integrated, Step-Down Switching Regulator with PMBus

**More Information**

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