# FDBL9403L-F085

# Single N-Channel Power MOSFET

## 40 V, 240 A, 0.72 mΩ

**Features**

- Small Footprint (TOLL) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low $Q_G$ and Capacitance to Minimize Driver Losses
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | 40 | V |
| Gate−to−Source Voltage | | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3) | Steady State | $T_C$ = 25°C | $I_D$ | 240 | A |
| Power Dissipation $R_{\theta JC}$ (Note 1) | Steady State | $T_C$ = 25°C | $P_D$ | 357.1 | W |
| | | $T_C$ = 100°C | | 178.6 | |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3) | Steady State | $T_C$ = 25°C | $I_D$ | 53.3 | A |
| | | $T_C$ = 100°C | | 37.7 | |
| Power Dissipation $R_{\theta JA}$ (Notes 1, 2) | Steady State | $T_C$ = 25°C | $P_D$ | 3.5 | W |
| | | $T_C$ = 100°C | | 1.7 | |
| Pulsed Drain Current | $T_C$ = 25°C, $t_p$ = 10 μs | | $I_{DM}$ | 2113 | A |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | −55 to +175 | °C |
| Source Current (Body Diode) | | | $I_S$ | 100 | A |
| Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 79 A, L = 0.2 mH) | | | $E_{AS}$ | 624 | mJ |
| Lead Temperature for Soldering Purposes (1/8″ from case for 10 s) | | | $T_L$ | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted. Current is limited by bondwire configuration.
2. Surface−mounted on FR4 board using a 650 $mm^2$, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

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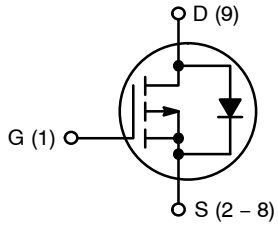
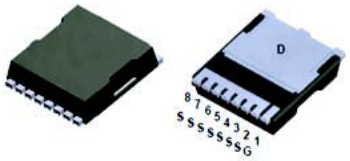
| $V_{(BR)DSS}$ | $R_{DS(ON)}$ MAX | $I_D$ MAX |
|---|---|---|
| 40 V | 0.72 mΩ @ 10 V | 80 A |
| | 0.98 mΩ @ 4.5 V | |

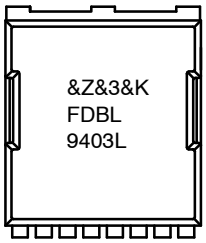



**N-CHANNEL MOSFET**




**H−PSOF8L**
**CASE 100CU**

**MARKING DIAGRAM**




| | |
|---|---|
| &Z | = Assembly Plant Code |
| &3 | = Numeric Date Code |
| &K | = Lot Code |
| FDBL9403L | = Specific Device Code |

**ORDERING INFORMATION**

See detailed ordering and shipping information on page 7 of this data sheet.

**Table 1. THERMAL CHARACTERISTICS**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Junction−to−Case − Steady State | 0.42 | °C/W |
| $R_{\theta JA}$ | Junction−to−Ambient − Steady State (Note 4) | 43 | |

4. Surface−mounted on FR4 board using a 650 $mm^2$, 2 oz. Cu pad.

**Table 2. ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 40 | – | – | V |
| $V_{(BR)DSS}/T_J$ | Drain-to-Source Breakdown Voltage Temperature Coefficienct | | – | 22.5 | – | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 40 V, $V_{GS}$ = 0 V, $T_J$ = 25°C<br>$V_{DS}$ = 40 V, $V_{GS}$ = 0 V, $T_J$ = 175°C | –<br>– | –<br>– | 1<br>1 | μA<br>mA |
| $I_{GSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | – | – | ±100 | nA |
| **ON CHARACTERISTICS** (Note 5) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 1 | 1.75 | 3 | V |
| $V_{GS(th)}/T_J$ | Threshold Temperature Coefficient | | – | −5.6 | – | mV/°C |
| $R_{DS(on)}$ | Drain−to−Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 80 A | – | 0.59 | 0.72 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 40 A | – | 0.76 | 0.98 | |
| **CHARGES, CAPACITANCES & GATE RESISTANCE** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$ = 0 V, f = 1 MHz, $V_{DS}$ = 20 V | – | 14100 | – | pF |
| $C_{oss}$ | Output Capacitance | | – | 4070 | – | |
| $C_{rss}$ | Reverse Transfer Capacitance | | – | 300 | – | |
| $R_g$ | Gate Resistance | $V_{GS}$ = 0.5 V, f = 1 MHz | – | 3.3 | – | Ω |
| $Q_{g(tot)}$ | Total Gate Charge | $V_{GS}$ = 4.5 V, $V_{DS}$ = 32 V, $I_D$ = 80 A | – | 97 | – | nC |
| | | $V_{GS}$ = 10 V, $V_{DS}$ = 32 V, $I_D$ = 80 A | – | 203 | – | |
| $Q_{g(th)}$ | Threshold Gate Charge | $V_{GS}$ = 0 V to 1 V | – | 13 | – | |
| $Q_{gs}$ | Gate−to−Source Gate Charge | $V_{DD}$ = 32 V, $I_D$ = 80 A | – | 40 | – | |
| $Q_{gd}$ | Gate−to−Drain “Miller” Charge | | – | 27 | – | |
| $V_{GP}$ | Plateau Voltage | | – | 3 | – | V |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 20 V, $I_D$ = 80 A,<br>$V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | – | 21 | – | ns |
| $t_r$ | Turn-On Rise Time | | – | 42 | – | |
| $t_{d(off)}$ | Turn-Off Delay Time | | – | 288 | – | |
| $t_f$ | Turn-Off Fall Time | | – | 101 | – | |
| **DRAIN-SOURCE DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Source−to−Drain Diode Voltage | $I_{SD}$ = 80 A, $V_{GS}$ = 0 V | – | 0.79 | 1.25 | V |
| | | $I_{SD}$ = 40 A, $V_{GS}$ = 0 V | – | 0.75 | 1.2 | |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0 V, $dI_{SD}/dt$ = 100 A/μs, $I_S$ = 80 A | – | 96 | – | ns |
| $t_a$ | Charge Time | | – | 46 | – | |
| $t_b$ | Discharge Time | | – | 50 | – | |
| $Q_{rr}$ | Reverse Recovery Charge | | – | 130 | – | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

## TYPICAL CHARACTERISTICS

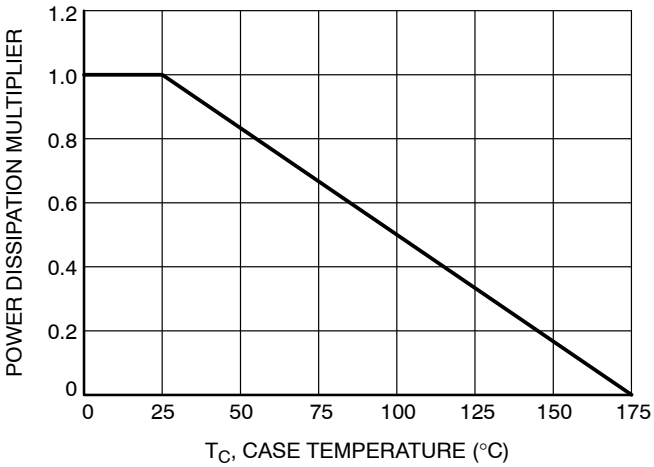



**Figure 1. Normalized Power Dissipation vs. Case Temperature**

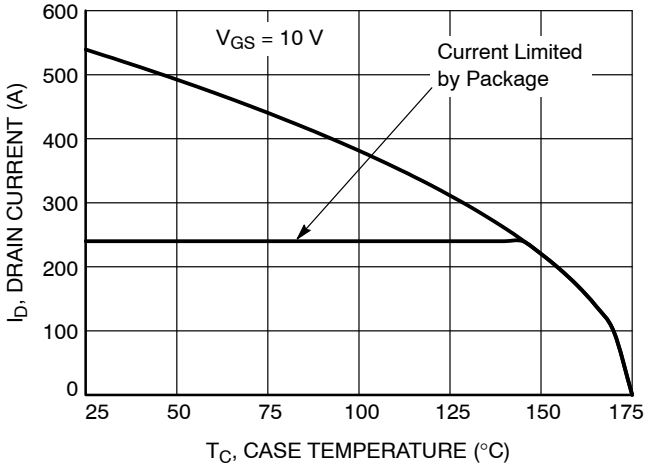



**Figure 2. Maximum Continuous Drain Current vs. Case Temperature**

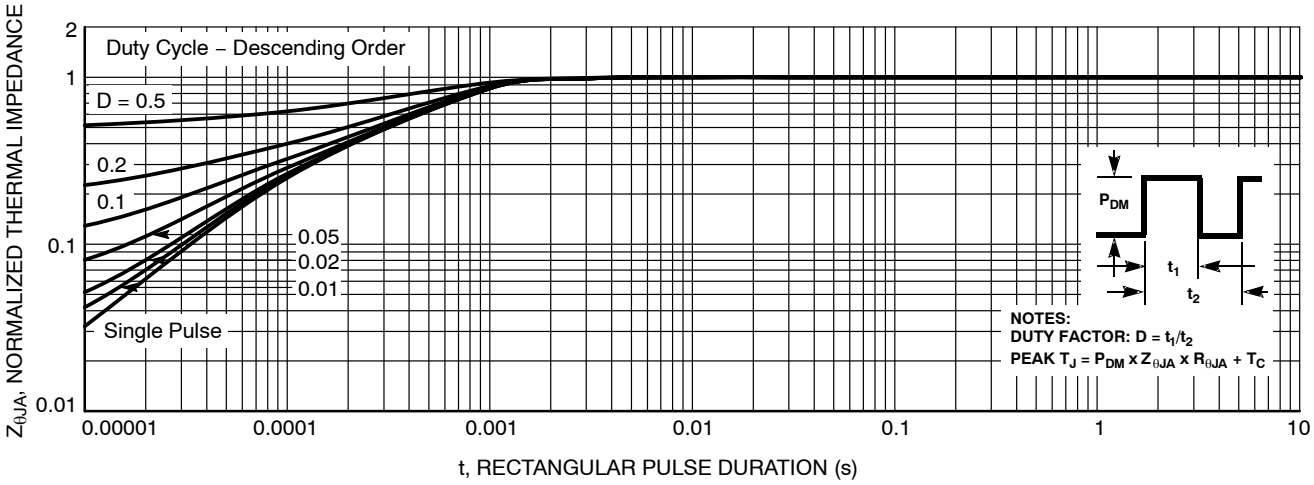



**Figure 3. Normalized Maximum Transient Thermal Impedance**

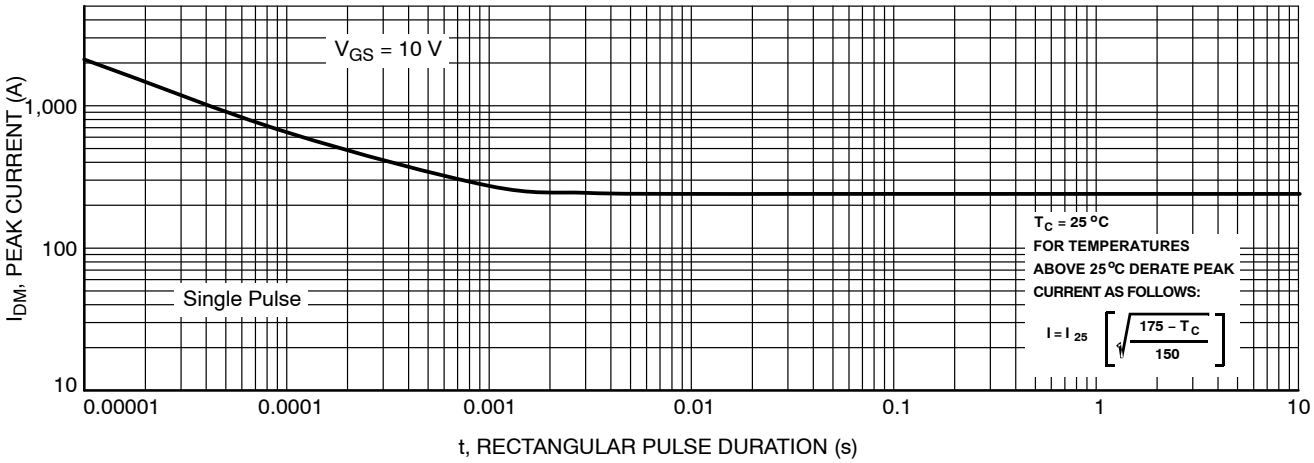



**Figure 4. Peak Current Capability**

## TYPICAL CHARACTERISTICS

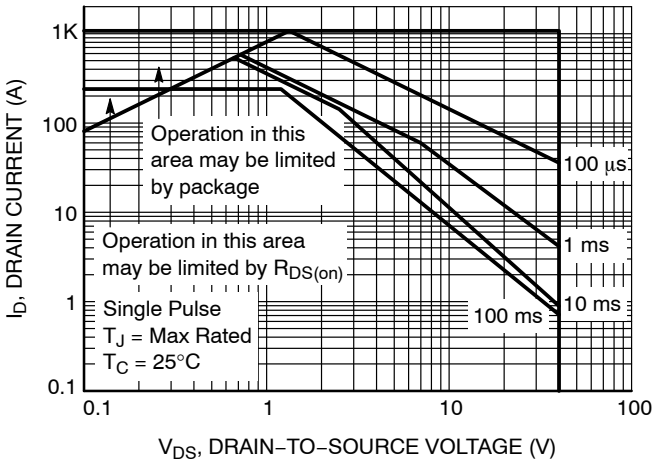



**Figure 5. Forward Bias Safe Operating Area**

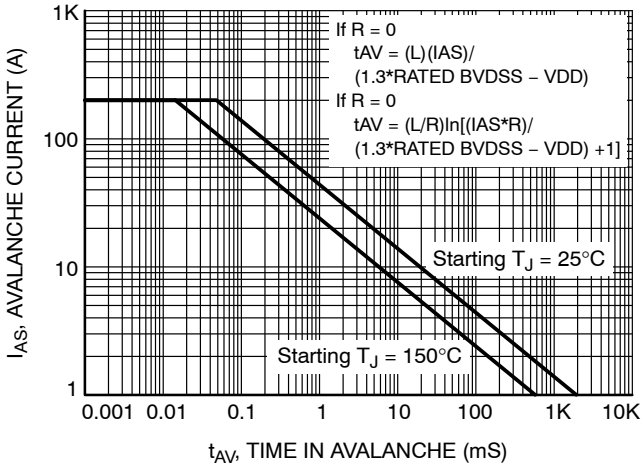



**Figure 6. Unclamped Inductive Switching Capability**

Note: Refer to ON Semiconductor Application Notes AN7514 and AN7515

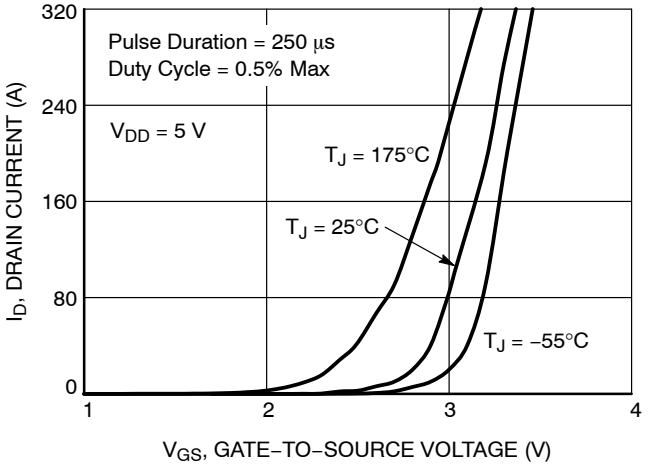



**Figure 7. Transfer Characteristics**

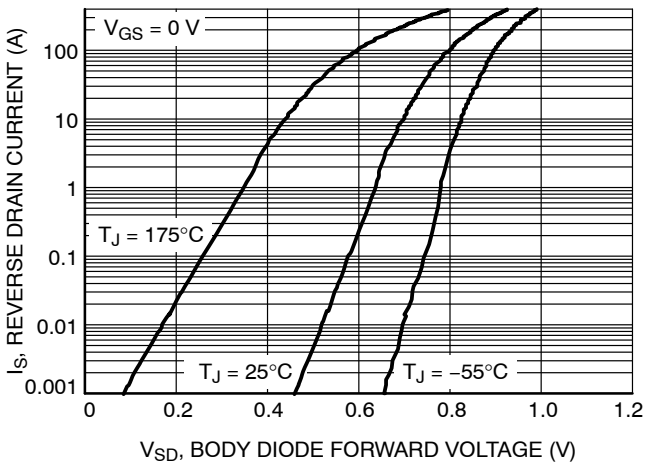



**Figure 8. Forward Diode Characteristics**

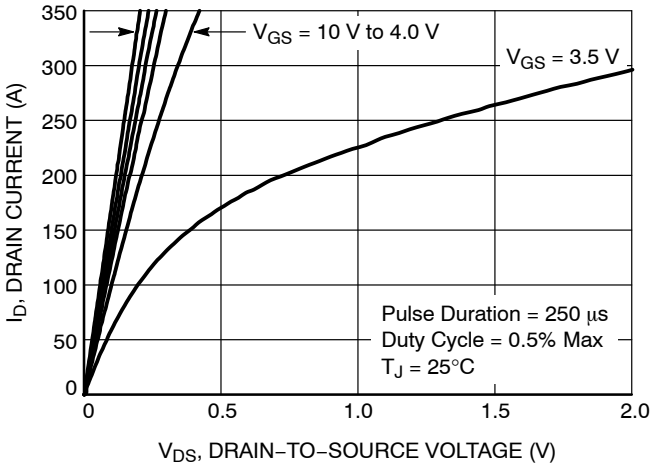



**Figure 9. Saturation Characteristics**

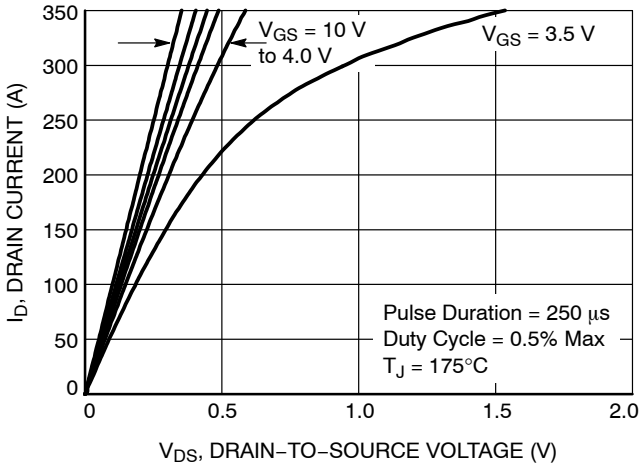



**Figure 10. Saturation Characteristics**

## TYPICAL CHARACTERISTICS

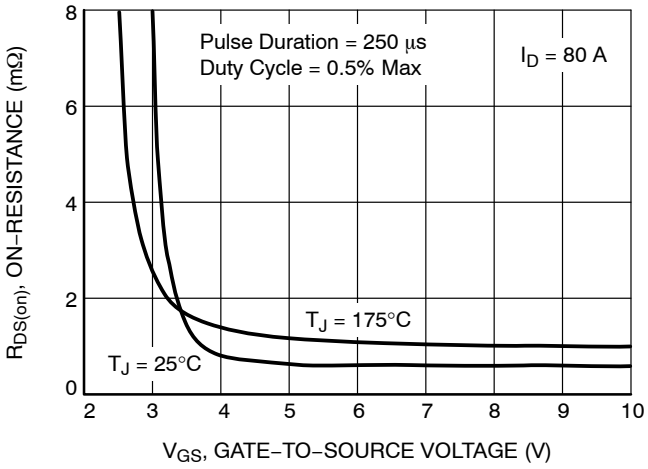



**Figure 11. $R_{DS(on)}$ vs. Gate Voltage**

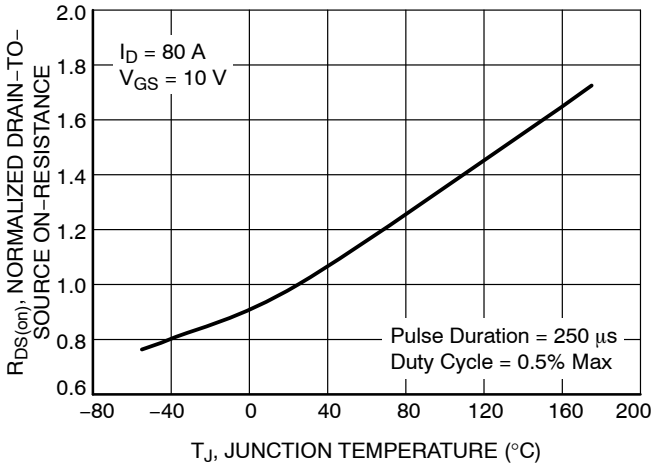



**Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature**

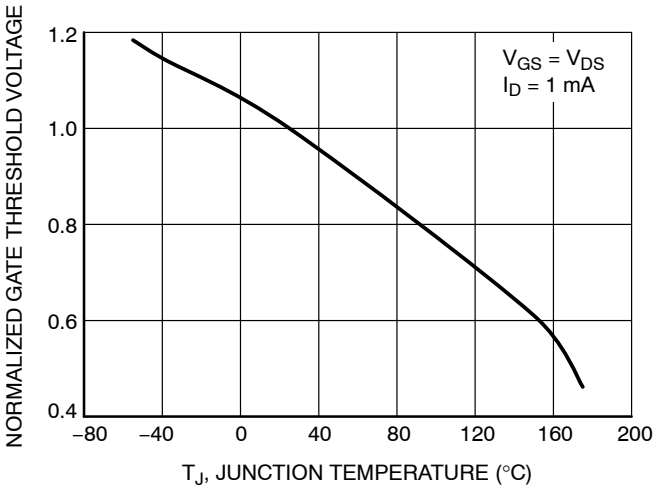



**Figure 13. Normalized Gate Threshold Voltage vs. Temperature**

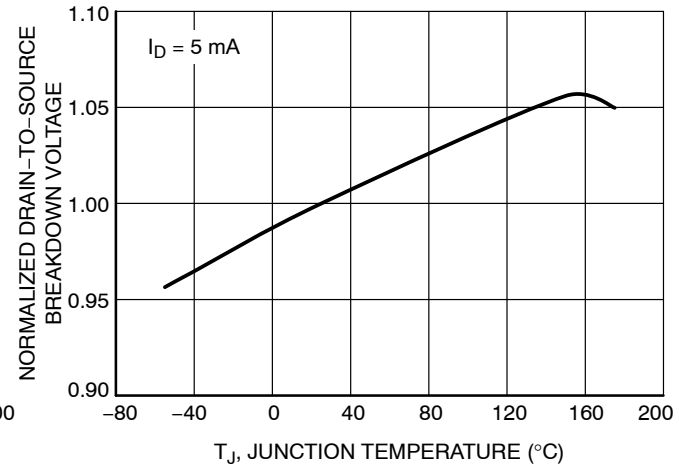



**Figure 14. Normalized Drain−to−Source Breakdown Voltage vs. Junction Temperature**

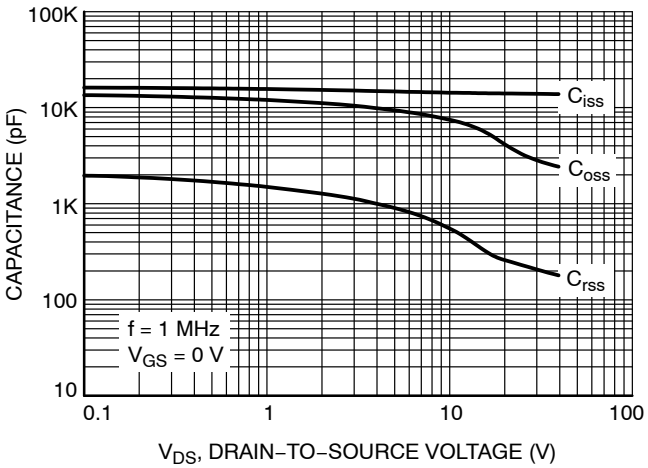



**Figure 15. Capacitance vs. Drain−to−Source Voltage**

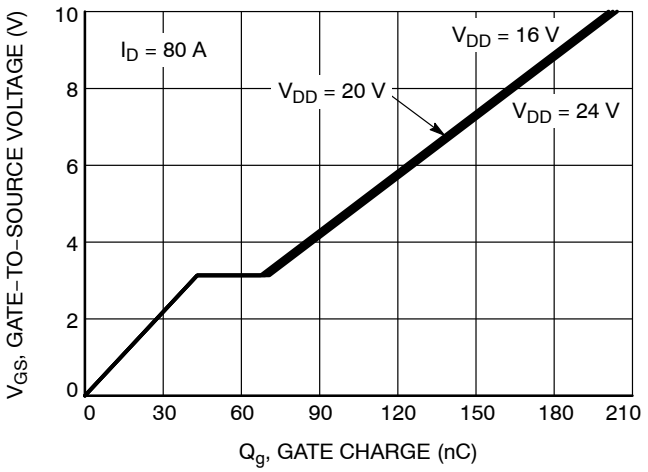
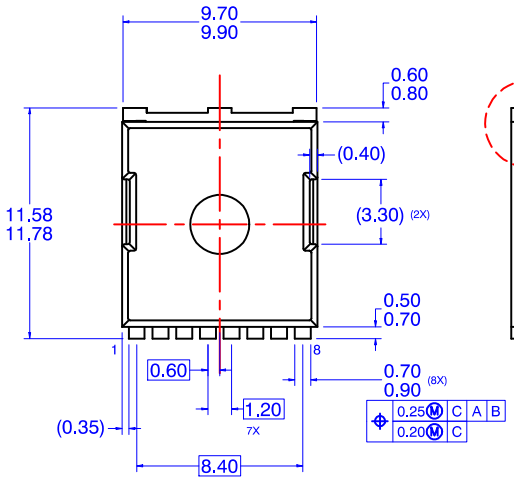


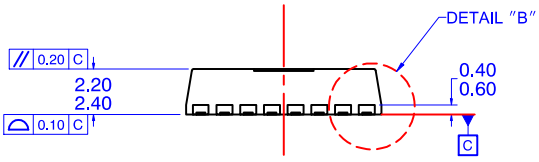

**Figure 16. Gate Charge vs. Gate−to−Source Voltage**

## PACKAGE DIMENSIONS

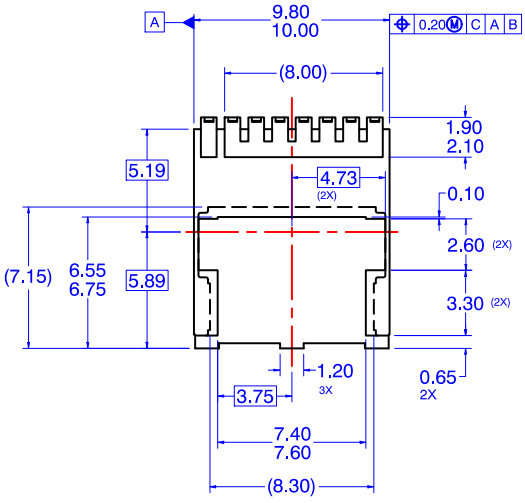
**H−PSOF8L 11.68x9.80**
CASE 100CU
ISSUE O



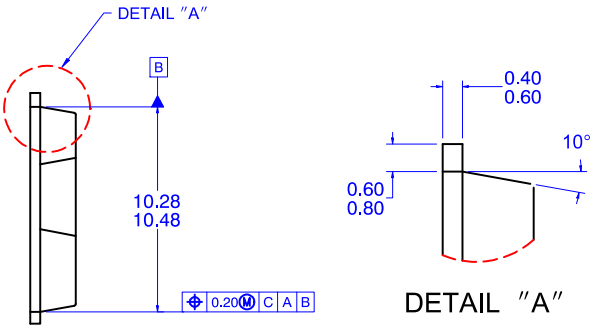

TOP VIEW



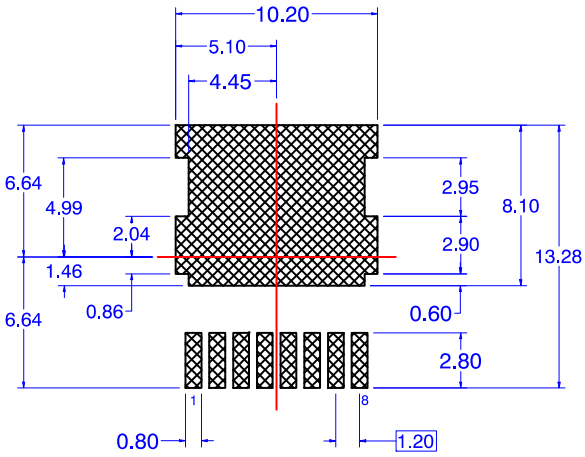

SIDE VIEW



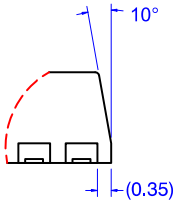

BOTTOM VIEW




DETAIL "A"




LAND PATTERN
RECOMMENDATION




DETAIL "B"

NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A, DATED NOVEMBER 2009.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.

D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

## PACKAGE MARKING AND ORDERING INFORMATION

| Device | Marking | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FDBL9403L−F085 | FDBL9403L | H−PSOF8L<br>(Pb-Free / Halogen Free) | 13″ | 24 mm | 2000 Units |



## PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT**:
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