DPAK

D(2, TAB)

G(1)

S(3)

NG1D2TS3Z

Features

Order code	V$_{DS}$ @ T$_{Jmax}$	R$_{DS(on)}$ max.	I$_D$
STD12N60DM2AG	650 V	0.440 Ω	10 A

- AEC-Q101 qualified
- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high-voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast-recovery diode series. It offers very low recovery charge (Q$_{rr}$) and time (t$_{rr}$) combined with low R$_{DS(on)}$, rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Product status
STD12N60DM2AG

Product summary	
Order code	STD12N60DM2AG
Marking	12N60DM2
Package	DPAK
Packing	Tape and reel

DS12209 - **Rev 3** - **June 2018**
For further information contact your local STMicroelectronics sales office.

www.st.com

1   Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_{case} = 25 °C	10	A
	Drain current (continuous) at T_{case} = 100 °C	6.3	
I_{DM} [1]	Drain current (pulsed)	25	A
P_{TOT}	Total dissipation at T_{case} = 25 °C	110	W
dv/dt[2]	Peak diode recovery voltage slope	50	V/ns
dv/dt[3]	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

1. *Pulse width is limited by safe operating area.*

2. *$I_{SD} \leq 10$ A, di/dt= 800 A/μs; V_{DS} peak < $V_{(BR)DSS}$, V_{DD} = 400 V*

3. *$V_{DS} \leq 480$ V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.14	°C/W
$R_{thj-pcb}$ [1]	Thermal resistance junction-pcb	50	

1. *When mounted on 1 inch² FR-4 board, 2oz Cu.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR} [1]	Avalanche current, repetitive or not repetitive	2	A
E_{AS} [2]	Single pulse avalanche energy	250	mJ

1. *pulse width limited by T_{jmax}*

2. *starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.*

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1.5	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_{case} = 125 °C[1]			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 5 A		0.380	0.440	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	614	-	pF
C_{oss}	Output capacitance		-	32	-	
C_{rss}	Reverse transfer capacitance		-	3.7	-	
$C_{oss\ eq.}$ [1]	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	57	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	7	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 10 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	14.5	-	nC
Q_{gs}	Gate-source charge		-	3.8	-	
Q_{gd}	Gate-drain charge		-	6.2	-	

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	15	-	ns
t_r	Rise time		-	8	-	
$t_{d(off)}$	Turn-off delay time		-	30	-	
t_f	Fall time		-	9.5	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		10	A
I_{SDM} [1]	Source-drain current (pulsed)		-		25	A
V_{SD} [2]	Forward on voltage	$V_{GS} = 0$ V, $I_{SD} = 10$ A	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 10$ A, di/dt = 100 A/µs, $V_{DD} = 60$ V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	70		ns
Q_{rr}	Reverse recovery charge		-	210		nC
I_{RRM}	Reverse recovery current		-	5.9		A
t_{rr}	Reverse recovery time	$I_{SD} = 10$ A, di/dt = 100 A/µs, $V_{DD} = 60$ V, $T_j = 150$ °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	110		ns
Q_{rr}	Reverse recovery charge		-	460		nC
I_{RRM}	Reverse recovery current		-	8.1		A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm250$ µA, $I_D = 0$ A	±30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area
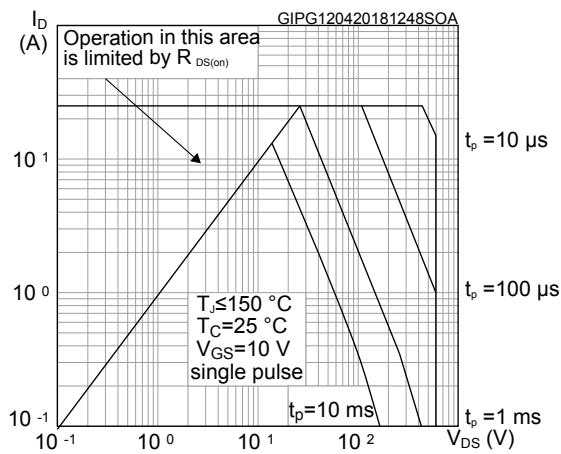

**Figure 2. Thermal impedance**
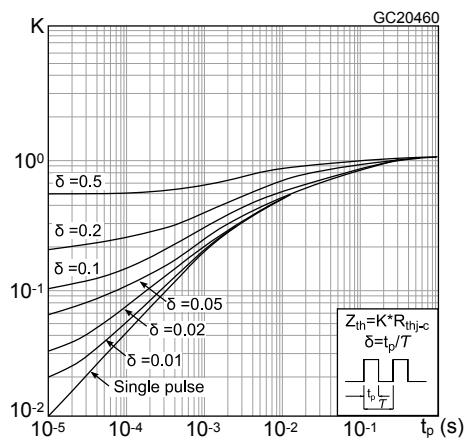
**Figure 3. Output characteristics**
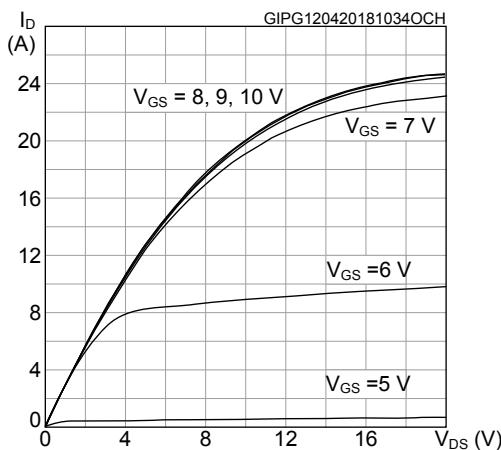
Figure 4. Transfer characteristics
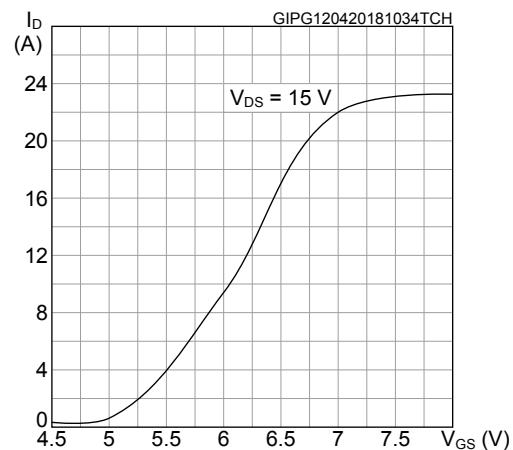
Figure 5. Gate charge vs gate-source voltage

GIPG120420181035QVG

V_{DS}

V_{DD} = 480 V
I_D = 10 A

Q_g

Q_{gs} Q_{gd}
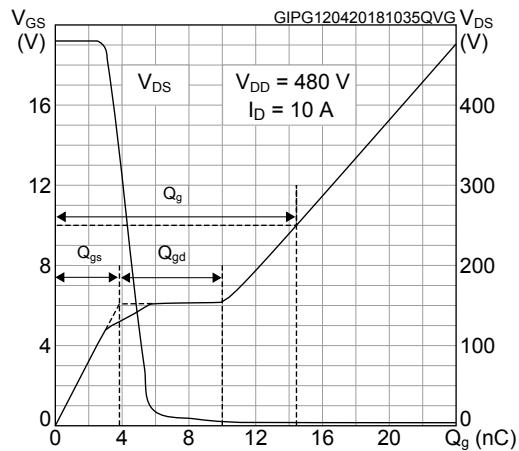
Figure 6. Static drain-source on-resistance

GIPG120420181043RID

V_{GS} = 10 V
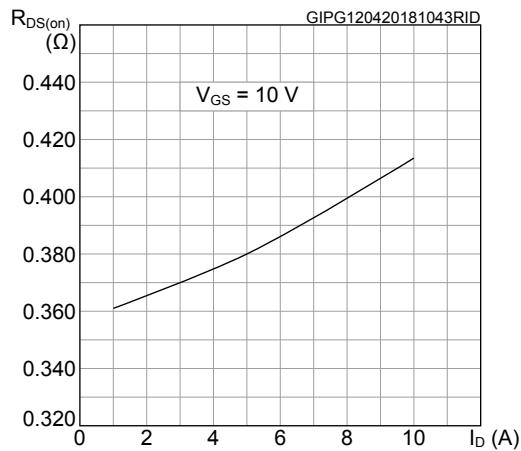
Figure 7. Capacitance variations

IGIPG120420181145CVR

C_{ISS}

C_{OSS}

C_{RSS}

f = 1 MHz
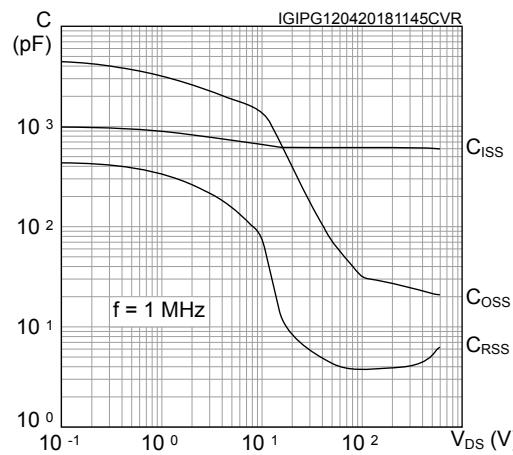
Figure 8. Normalized gate threshold voltage vs temperature

GIPG120420181044VTH

I_D=250 µA
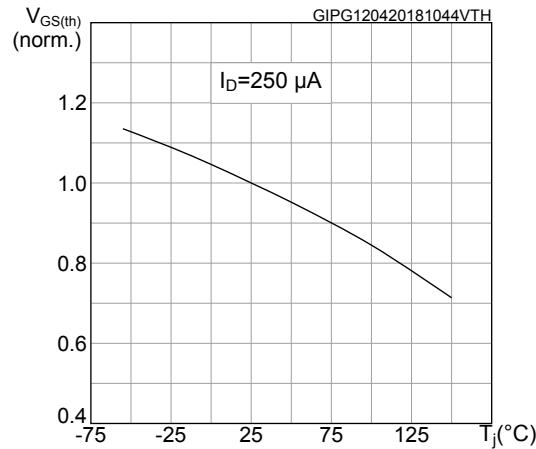
Figure 9. Normalized on-resistance vs temperature

GIPG120420181045RON

V_{GS} = 10 V
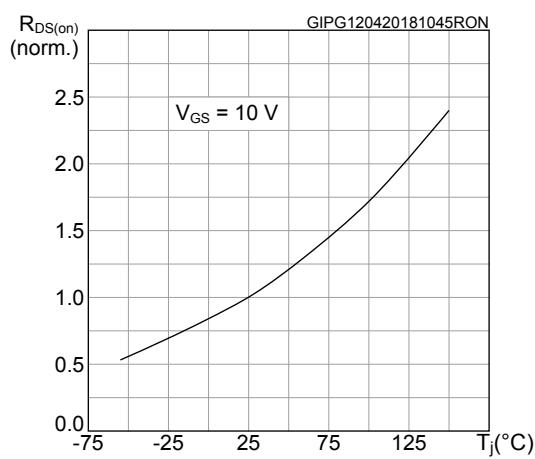
Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

GIPG120420181045BDV

I_D = 1 mA
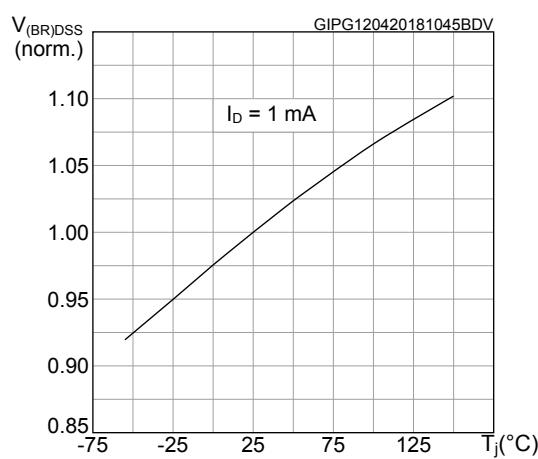
Figure 11. **Output capacitance stored energy**
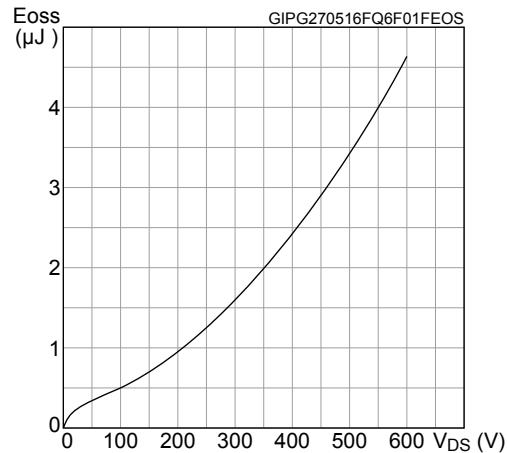
Figure 12. **Source-drain diode forward characteristics**
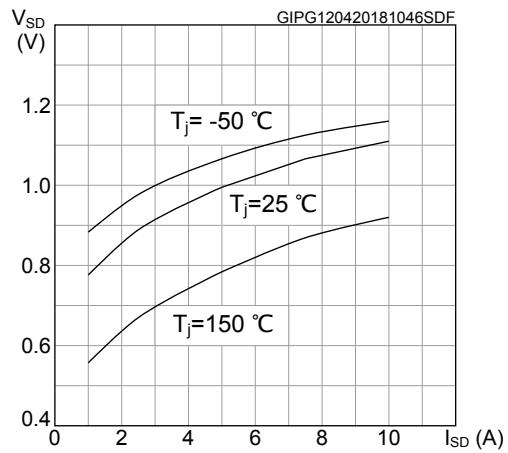
3 Test circuits

Figure 13. Test circuit for resistive load switching times
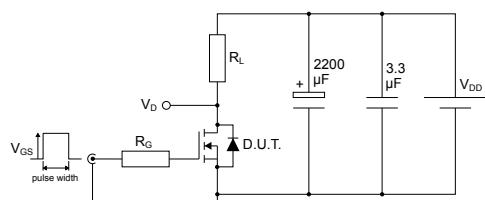
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**Figure 14. Test circuit for gate charge behavior**
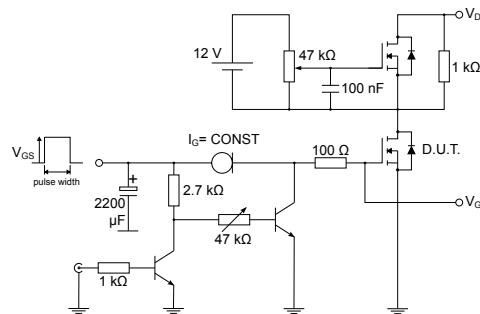
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**Figure 15. Test circuit for inductive load switching and diode recovery times**
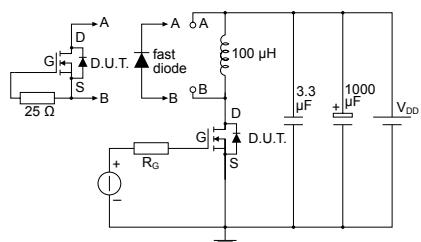
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Figure 16. Unclamped inductive load test circuit
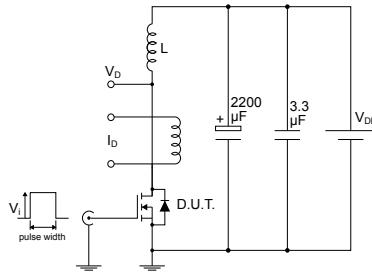
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Figure 17. Unclamped inductive waveform
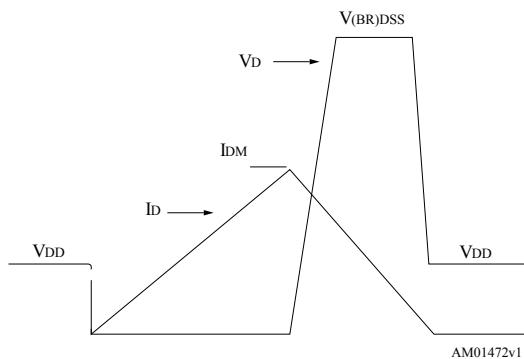
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Figure 18. Switching time waveform
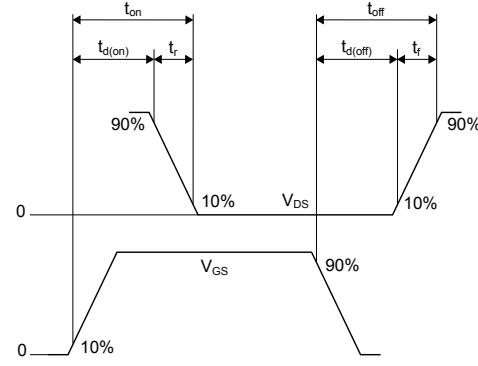
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK®
packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions
and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK package information

**Figure 19. DPAK (TO-252) type A2 package outline**
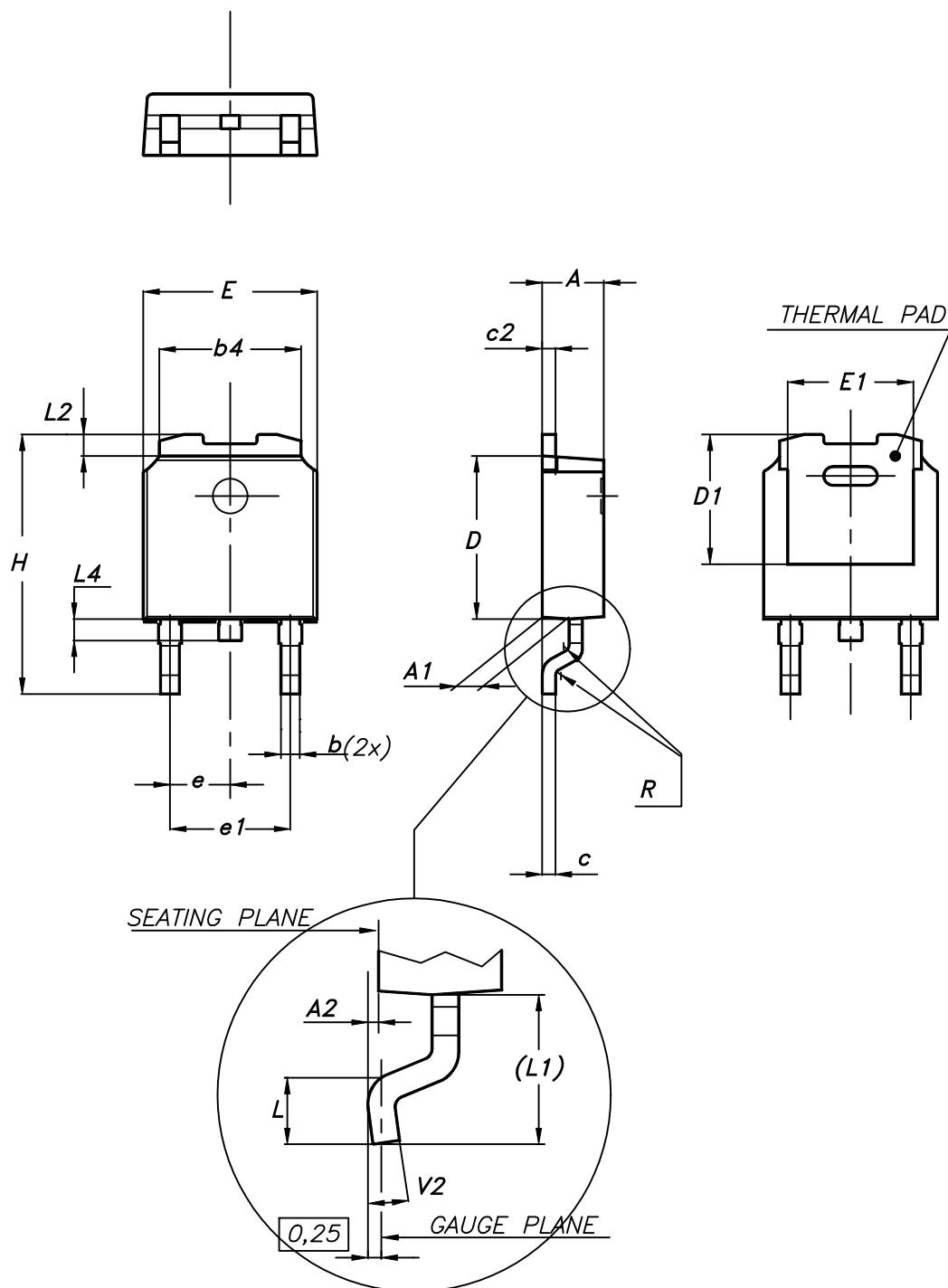
0068772_type-A2_rev25

Table 9. DPAK (TO-252) type A2 mechanical data

| Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 20. DPAK (TO-252) recommended footprint (dimensions are in mm)
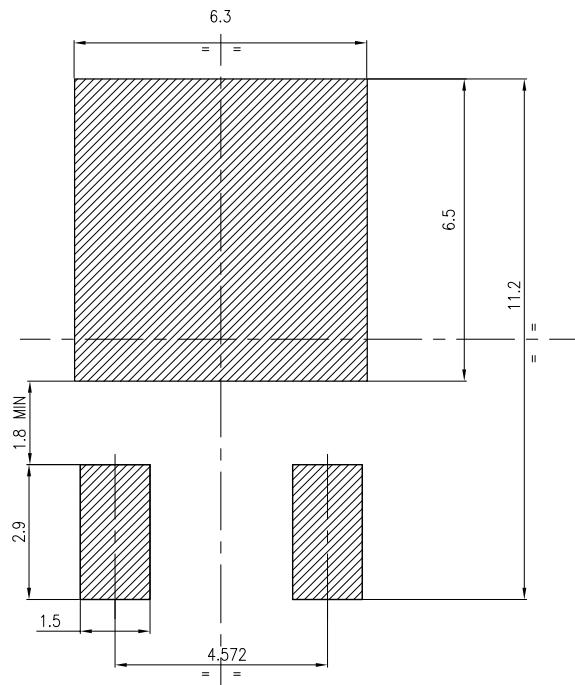
FP_0068772_25

4.2 DPAK packing information

Figure 21. DPAK (TO-252) tape outline

10 pitches cumulative
tolerance on tape +/- 0.2 mm

Top cover tape

For machine ref. only
including draft and
radii concentric around B0

User direction of feed
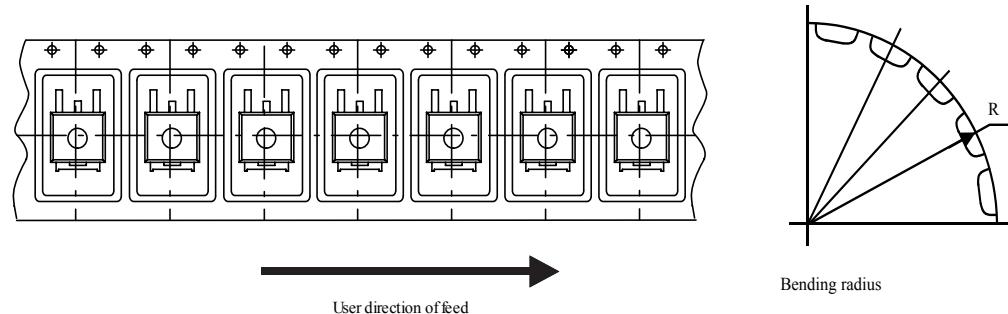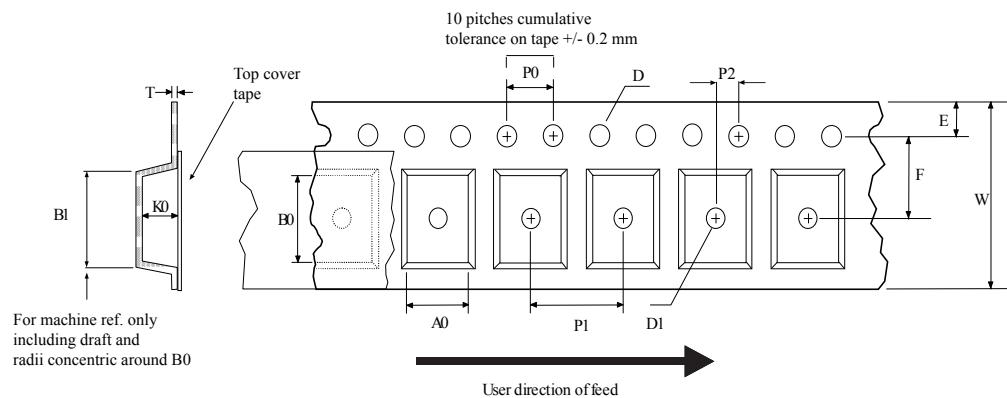
Bending radius

AM08852v1

Figure 22. DPAK (TO-252) reel outline
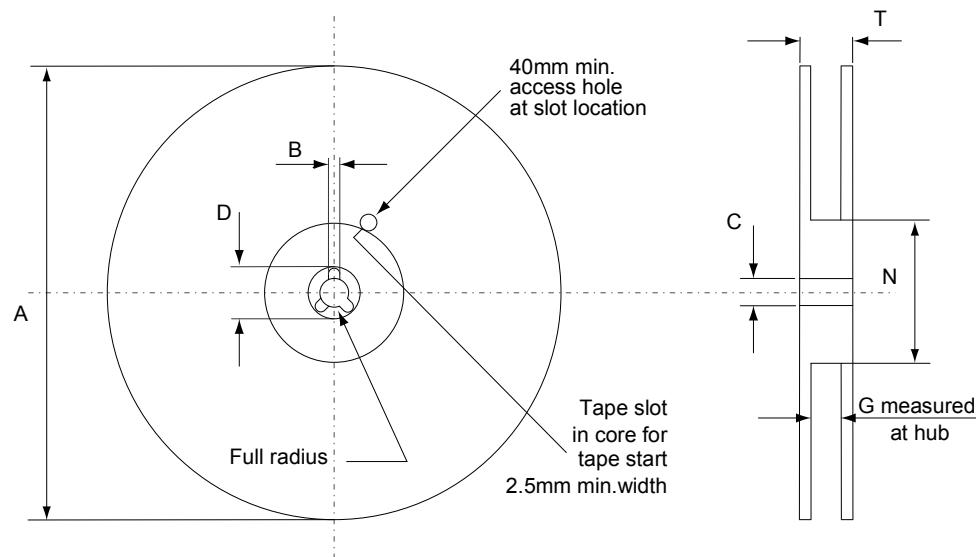
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Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 11. Document revision history

Date	Revision	Changes
23-Jun-2017	1	First release.
16-Apr-2018	2	Removed maturity status indication from cover page. The document status is production data. Modified features table on cover page. Modified *Table 1. Absolute maximum ratings*, *Table 3. Avalanche characteristics*, *Table 4. Static*, *Table 5. Dynamic*, *Table 6. Switching times* and *Table 7. Source-drain diode*. Updated *Section 2.1 Electrical characteristics (curves)*. Minor text changes.
27-Jun-2018	3	Updated Section 4 Package information.

Contents

IMPORTANT NOTICE – PLEASE READ CAREFULLY