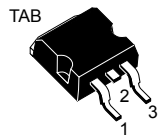
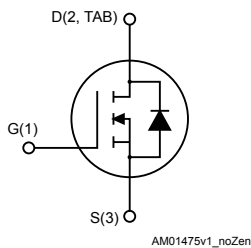


## N-channel 300 V, 53 A, 0.037 $\Omega$ typ., MDmesh™ M5 Power MOSFET in a D<sup>2</sup>PAK package


 D<sup>2</sup>PAK


### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STB45N30M5	300 V	0.040 $\Omega$	53 A

- Extremely low R<sub>DS(on)</sub>
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET based on the MDmesh™ M5 innovative vertical process technology combined with the well-known PowerMESH™ horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

#### Product status link

[STB45N30M5](#)

#### Product summary

<b>Order code</b>	STB45N30M5
<b>Marking</b>	45N30M5
<b>Package</b>	D <sup>2</sup> PAK
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$	53	A
	Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$	34	
$I_{DM}^{(1)}$	Drain current (pulsed)	212	A
$P_{TOT}$	Total dissipation at $T_{case} = 25\text{ }^\circ\text{C}$	250	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature range		

1. Pulse width is limited by safe operating area.

2.  $I_{SD} \leq 53\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS\text{ peak}} < V_{(BR)DSS}$ ,  $V_{DD} = 240\text{ V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.5	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	30	

1. When mounted on an 1-inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_j\text{ max}$ )	16	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	550	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified

**Table 4. On-/off-states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	300			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 300\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 300\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$			100	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 26.5\text{ A}$		0.037	0.040	$\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	4240	-	pF
$C_{oss}$	Output capacitance		-	205	-	pF
$C_{riss}$	Reverse transfer capacitance		-	9.5	-	pF
$C_{o(tr)}^{(1)}$	Time-related equivalent capacitance	$V_{DS} = 0\text{ to }240\text{ V}$ , $V_{GS} = 0\text{ V}$	-	373	-	pF
$C_{o(er)}^{(2)}$	Energy-related equivalent capacitance		-	202	-	pF
$R_G$	Gate input resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	1.4	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 240\text{ V}$ , $I_D = 24\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	95	-	nC
$Q_{gs}$	Gate-source charge		-	23	-	nC
$Q_{gd}$	Gate-drain charge		-	37	-	nC

1.  $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

2.  $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	$V_{DD} = 240\text{ V}$ , $I_D = 32\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times and Figure 19. Switching time waveform)	-	66	-	ns
$t_{r(v)}$	Voltage rise time		-	15	-	ns
$t_{f(i)}$	Current fall time		-	24	-	ns
$t_{c(off)}$	Crossing time		-	22.5	-	ns

**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		53	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		212	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 53 \text{ A}$ , $V_{GS} = 0 \text{ V}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 48 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 60 \text{ V}$	-	223		ns
$Q_{rr}$	Reverse recovery charge		-	2.5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	23		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 48 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 60 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$	-	280		ns
$Q_{rr}$	Reverse recovery charge		-	3.9		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	28	

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

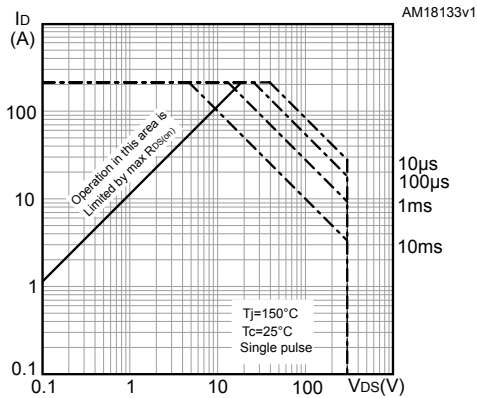


Figure 2. Thermal impedance

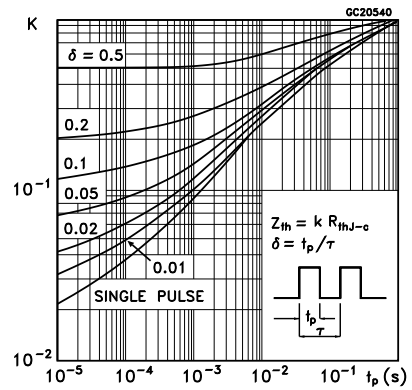


Figure 3. Output characteristics

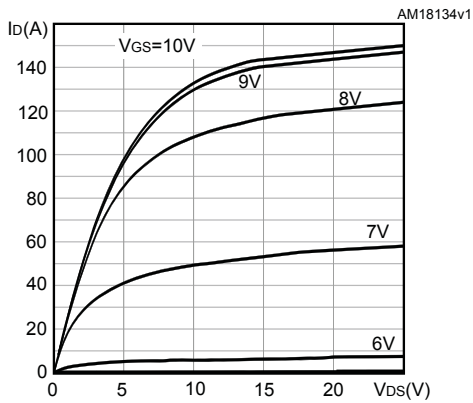


Figure 4. Transfer characteristics

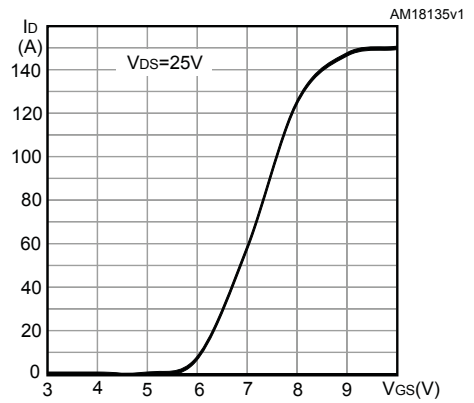


Figure 5. Gate charge vs gate-source voltage

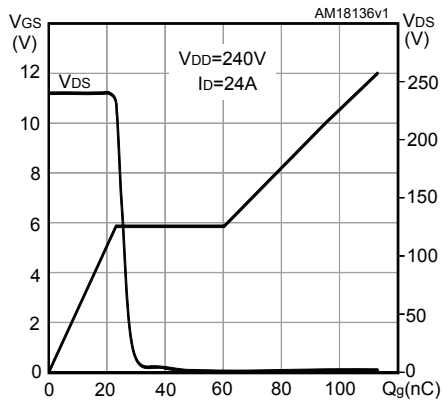
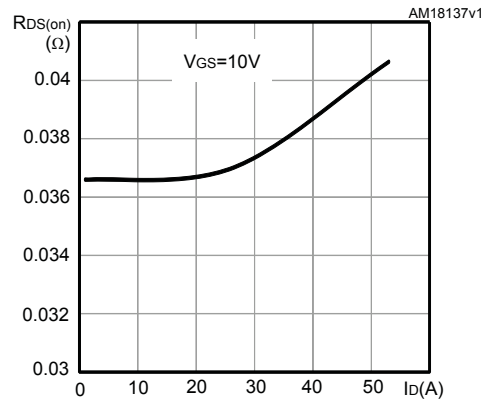
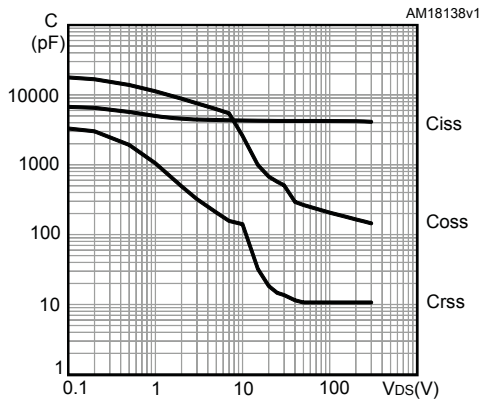


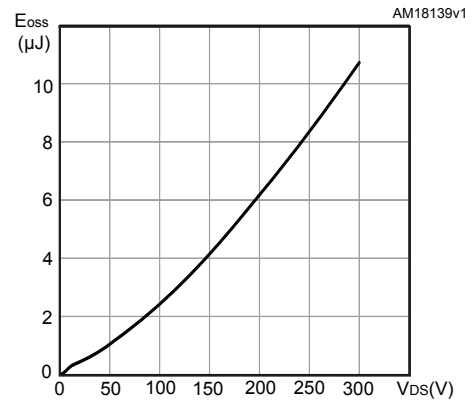
Figure 6. Static drain-source on-resistance



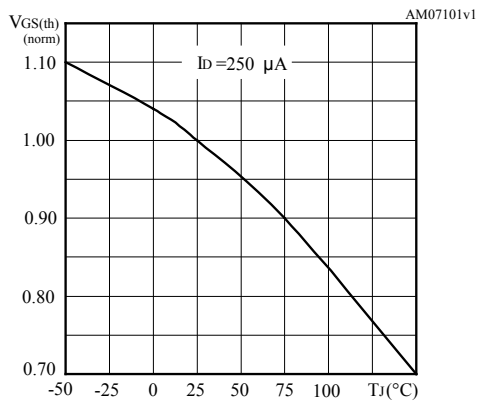
**Figure 7. Capacitance variations**



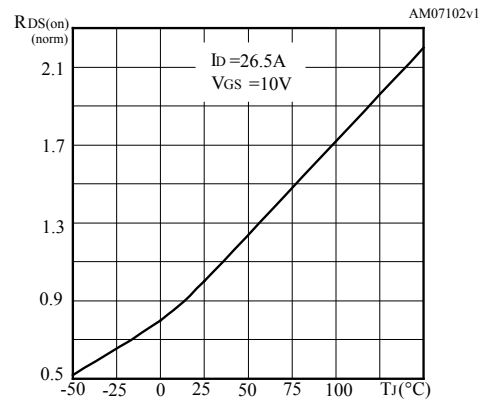
**Figure 8. Output capacitance stored energy**



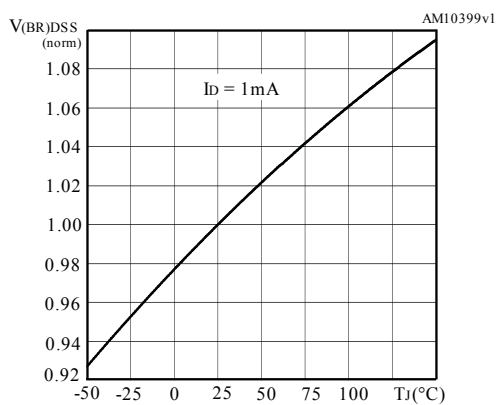
**Figure 9. Normalized gate threshold voltage vs temperature**



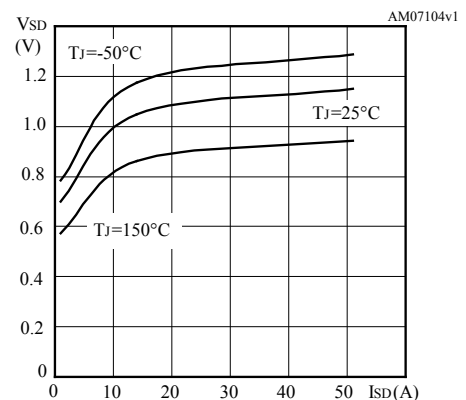
**Figure 10. Normalized on-resistance vs temperature**



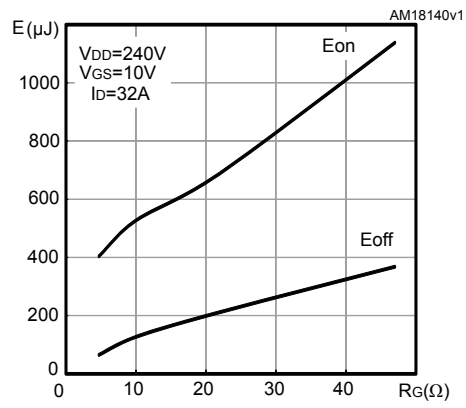
**Figure 11. Normalized V<sub>(BR)DSS</sub> vs temperature**



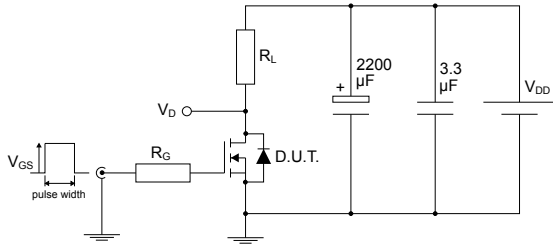
**Figure 12. Source-drain diode forward characteristics**



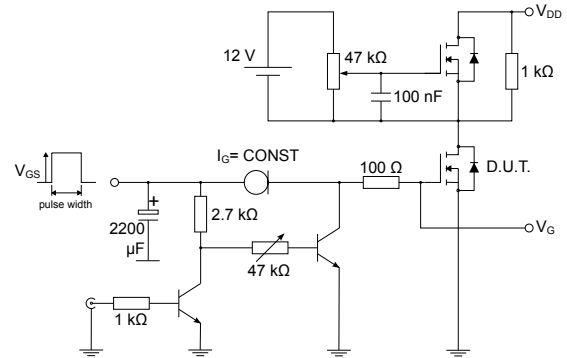
**Figure 13. Switching energy vs gate resistance**



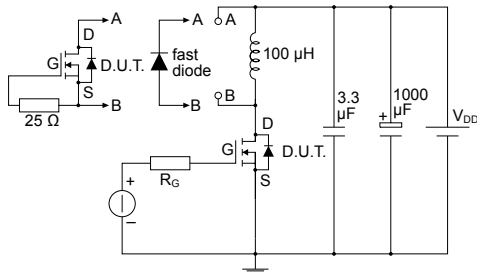
### 3 Test circuits

**Figure 14. Test circuit for resistive load switching times**


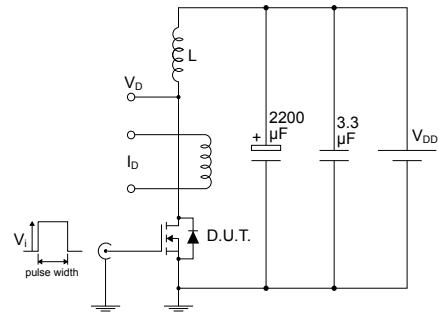
AM01488v1

**Figure 15. Test circuit for gate charge behavior**


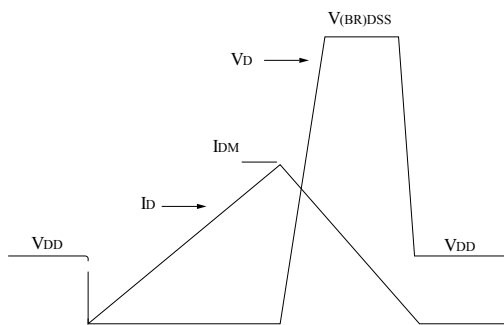
AM01469v1

**Figure 16. Test circuit for inductive load switching and diode recovery times**


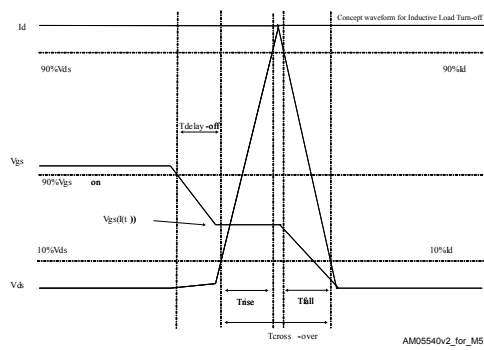
AM01470v1

**Figure 17. Unclamped inductive load test circuit**


AM01471v1

**Figure 18. Unclamped inductive waveform**


AM01472v1

**Figure 19. Switching time waveform**


AM05540v2\_for\_M5

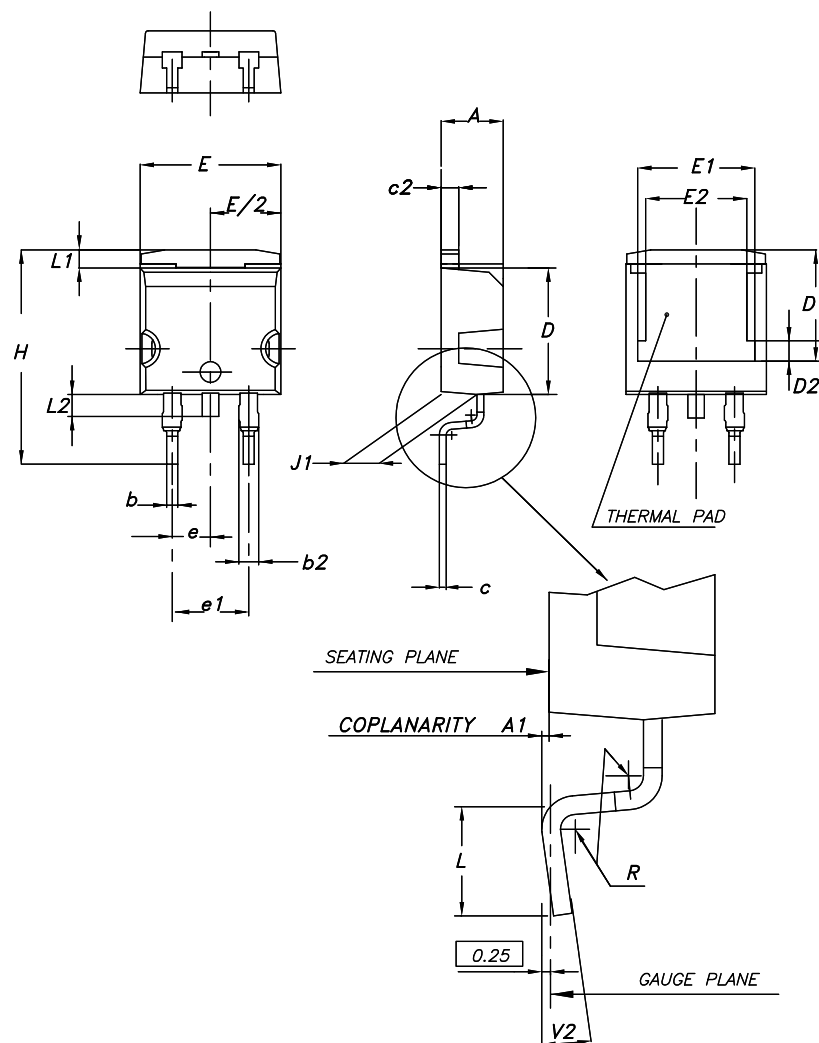


## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 D<sup>2</sup>PAK (TO-263) type A2 package information

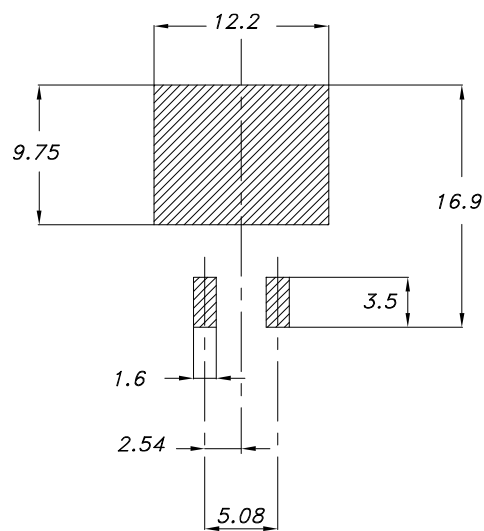
Figure 20. D<sup>2</sup>PAK (TO-263) type A2 package outline



0079457\_A2\_24

**Table 8. D<sup>2</sup>PAK (TO-263) type A2 package mechanical data**

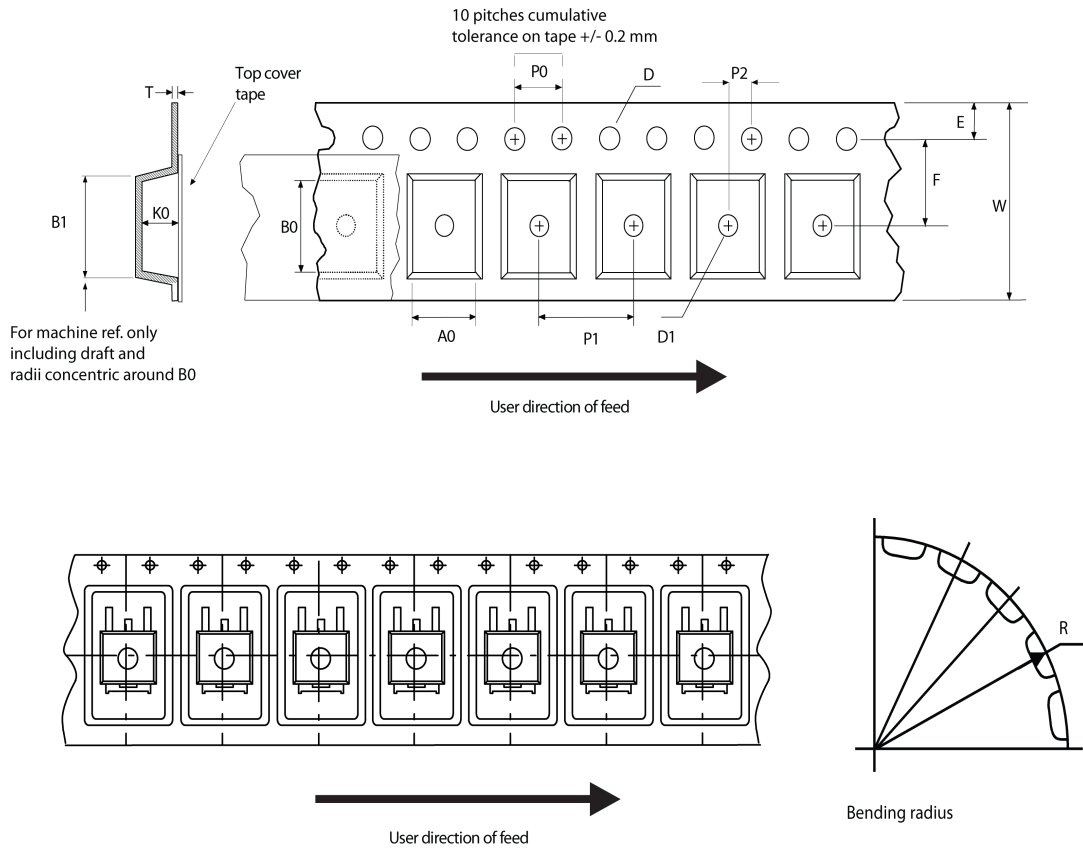
Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.70	8.90	9.10
E2	7.30	7.50	7.70
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

**Figure 21. D<sup>2</sup>PAK (TO-263) recommended footprint (dimensions are in mm)**


Footprint

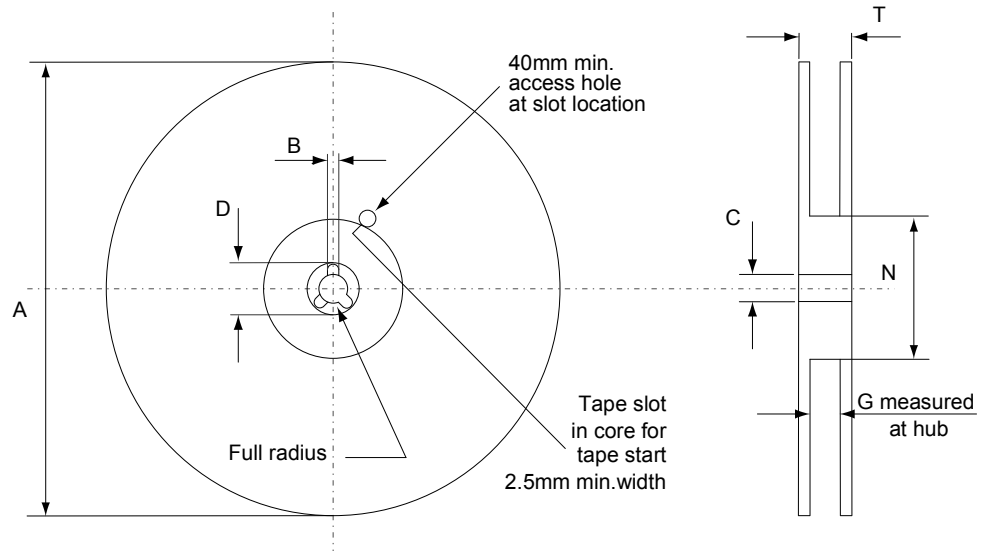
## 4.2 D<sup>2</sup>PAK packing information

Figure 22. D<sup>2</sup>PAK tape outline



AM08852v1

**Figure 23. D<sup>2</sup>PAK reel outline**



AM06038v1

**Table 9. D<sup>2</sup>PAK tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

## Revision history

**Table 10. Document revision history**

Date	Version	Changes
16-May-2018	1	Initial release

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