Single-input Voltage, 30 A Buck Regulators with PVID

OptiMOS™ IPOL IR38265

FEATURES

- Internal LDO allows single 16 V operation
- Output Voltage Range: 0.5V to 0.875*PVin
- 0.5% accurate Reference Voltage
- Enhanced line/load regulation with Feedforward
- Frequency programmable by I2C up to 1.5 MHz
- Enable input with Voltage Monitoring Capability
- Remote Sense Amplifier with True Differential Voltage Sensing
- 3 pins (PVID) to program output voltage
- Fast mode I2C interface for programming, sequencing and margining output voltage, and for monitoring input voltage, output voltage, output current and temperature.
- I2C configurable fault thresholds for input UVLO, output OVP, OCP and thermal shutdown.
- Thermally compensated pulse-by-pulse current limit and Hiccup Mode Over Current Protection
- Dedicated output voltage sensing for power good indication and overvoltage protection which remains active even when Enable is low.
- Enhanced Pre-Bias Start up
- Integrated MOSFET drivers and Bootstrap diode
- Operating junction temp: -40°C<Tj<125°C
- Thermal Shut Down
- Post Package trimmed rising edge dead-time
- I2C Programmable Power Good Output
- Small Size 5 mm x 7 mm PQFN
- Pb-Free (RoHS Compliant)
- External resistor allows setting up to 16 PMBus™ addresses

DESCRIPTION

This family of OptiMOS™ IPOL devices offers easy-to-use, fully integrated and highly efficient DC/DC regulators with PVID and I2C interface. The on-chip PWM controller and co-packaged low duty cycle optimized MOSFETs make these devices a space-efficient solution, providing accurate power delivery for low output voltage and high current applications that require a parallel VID interface.

These versatile devices offer programmability of switching frequency, output voltage, and fault/warning thresholds and fault responses while operating over a wide input range. Thus, they offer flexibility as well as system level security in event of fault conditions.

The switching frequency is programmable from 150 kHz to 1.5 MHz for an optimum solution.

The on-chip sensors and ADC along with the PVID and I2C interfaces make it easy to monitor and report input voltage, output voltage, output current and temperature.

APPLICATIONS

- Intel® VR13 and VR12.5 based systems
- Servers and High End Desktop CPU VRs for non-core applications
- Telecom and storage applications

BASIC APPLICATION

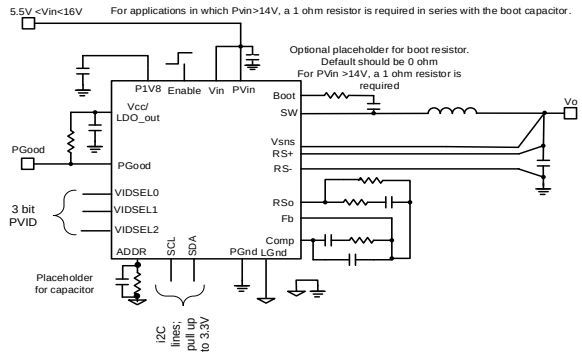


Figure 1: Typical application circuit

PIN DIAGRAM

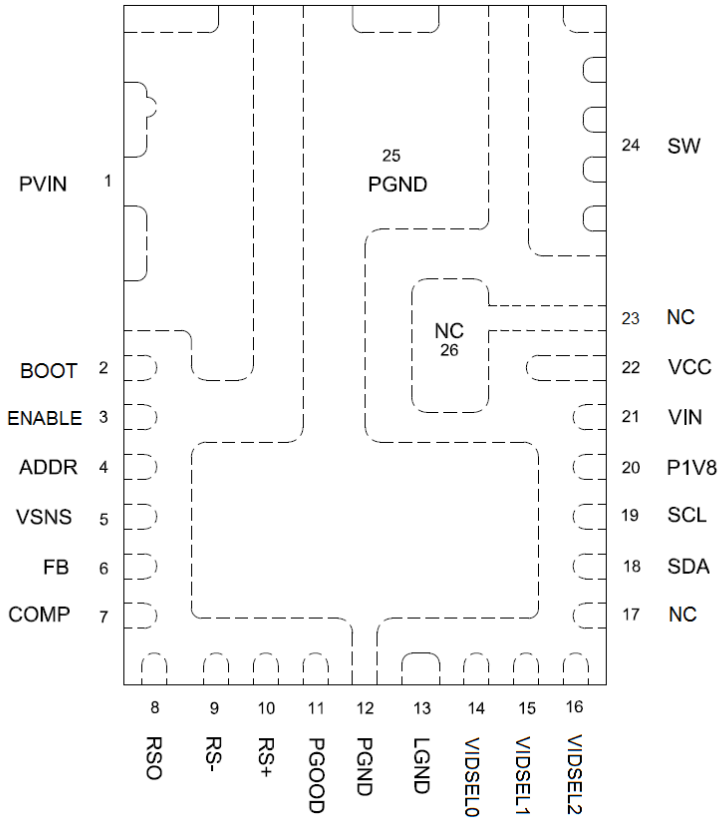


Figure 2: IR38265 Package Top View
5mm X 7mm PQFN

ORDERING INFORMATION

Package	Tape and Reel Qty	Part Number	Description
PQFN	4000	IR38265MTRPbF	30A Buck Regulator with PVID and I2C for PVNN

FUNCTIONAL BLOCK DIAGRAM

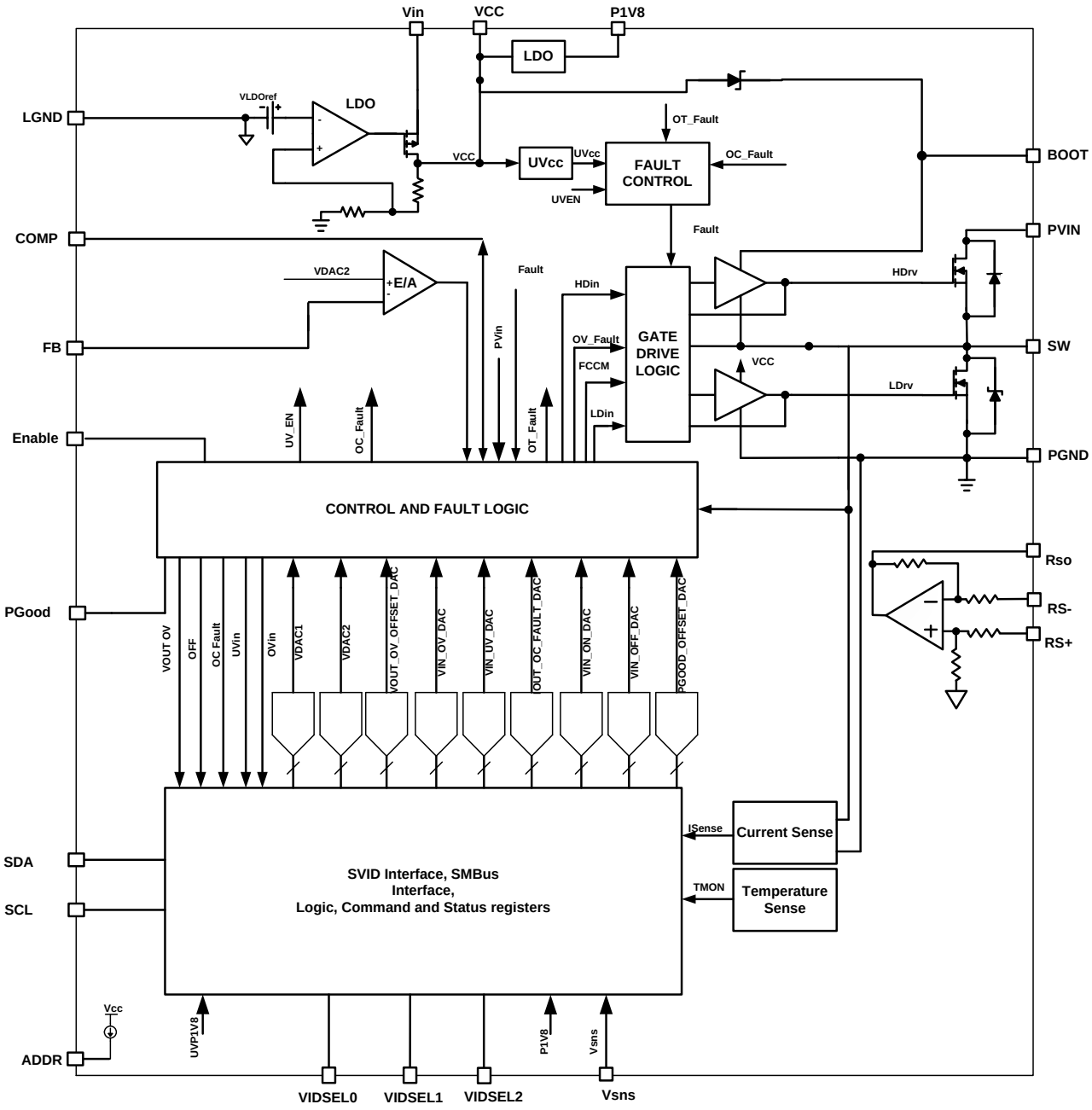


Figure 3: Simplified Block Diagram for IR38265

PIN DESCRIPTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1	PVIN	Input voltage for power stage. Bypass capacitors between PVin and PGND should be connected very close to this pin and PGND. Typical applications use four 22 uF input capacitors and a low ESR, low ESL 0.1uF decoupling capacitor in a 0603/0402 case size. A 3.3nF capacitor may also be used in parallel with these input capacitors to reduce ringing on the Sw node.
2	Boot	Supply voltage for high side driver. A 0.1uF capacitor should be connected from this pin to the Sw pin. It is recommended to provide a placement for a 0 ohm resistor in series with the capacitor. For applications in which PVin>14V, a 1 ohm resistor is required in series with boot capacitor.
3	ENABLE	Enable pin to turn on and off the IC.
4	ADDR	A resistor should be connected from this pin to LGnd to set the I2C address offset for the device. It is recommended to provide a placement for a 10 nF capacitor in parallel with the offset resistor.
5	Vsns	Sense pin for OVP and PGood. Typically connected to a local Vout capacitor at the output of the inductor.
6	FB	Inverting input to the error amplifier. This pin is connected directly to the output of the regulator or to the output of the remote sense amplifier, via resistor divider to set the output voltage and provide feedback to the error amplifier.
7	COMP	Output of error amplifier. An external resistor and capacitor network is typically connected from this pin to FB to provide loop compensation.
8	RSo	Remote Sense Amplifier Output. When the remote sense amplifier is used, this is connected to the feedback compensation network.
9	RS-	Remote Sense Amplifier input. Connect to ground at the load.
10	RS+	Remote Sense Amplifier input. Connect to output at the load.
11	PGood	Power Good status pin. Output is open drain. Connect a pull up resistor from this pin to VCC. If the power good voltage before VCC UVLO needs to be limited to < 500 mV, use a 49.9K pullup, otherwise a 4.99K pullup will suffice.
12,25	PGND	Power ground. This pin should be connected to the system's power ground plane. Bypass capacitors between PVin and PGND should be connected very close to PVIN pin (pin 1) and this pin.
13	LGND	Signal ground for internal reference and control circuitry. This should be connected to the PGnd plane at a quiet location using a single point connection.
14	VIDSEL0	Used to select VID voltage registers. This is the LSB of the 3 bit PVID code that is internally decoded to select the register containing the target voltage. Only connect to Vcc via a 4.99KΩ resistor and do not use a direct connection. Do not exceed 6V.
15	VIDSEL1	Used to select VID voltage registers. Only connect to Vcc via a 4.99KΩ resistor and do not use a direct connection. Do not exceed 6V.
16	VIDSEL2	Used to select VID voltage registers. This is the MSB of the 3 bit PVID code that is internally decoded to select the register containing the target voltage. Only connect to Vcc via a 4.99KΩ resistor and do not use a direct connection. Do not exceed 6V.
17	NC	NC
18	SDA	I2C data serial input/output line. This should be pulled up to 3.3V-5V with a 1K-5K resistor

PIN #	PIN NAME	PIN DESCRIPTION
19	SCL	I2C clock line. This should be pulled up to 3.3V-5V with a 1K-5K resistor
20	P1V8	This is the supply for the digital circuits; bypass with a 10uF capacitor to PGnd. A 2.2uF capacitor is valid however a 10uF capacitor is recommended.
21	Vin	Input Voltage for LDO. A 1 uF capacitor is placed from this pin to PGnd. If the internal bias LDO is used, tie this pin to PVin. If an external bias voltage (typically 5V) is available for Vcc, tie the Vin pin to Vcc.
22	VCC	Bias Voltage for IC and driver section, output of LDO. Add 10 uF bypass cap from this pin to PGnd.
23,26	NC	NC
24	SW	Switch node. This pin is connected to the output inductor.

ABSOLUTE MAXIMUM RATINGS

Stresses beyond these listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

PVin, Vin	-0.3V to 25V
VCC	-0.3V to 6V
P1V8	-0.3V to 2 V
SW	-0.3V to 25V (DC), -4V to 25V (AC, 100ns)
BOOT	-0.3V to 31V
BOOT to SW	-0.3V to 6V (DC) (Note 1), -0.3V to 6.5V (AC, 100ns)
PGD, other Input/output pins	-0.3V to 6V (Note 1)
PGND to GND, RS- to GND	-0.3V to + 0.3V
THERMAL INFORMATION	
Junction to ambient thermal resistance θ_{JA}	11.1 C/W (Note 2)
Junction to board thermal resistance θ_{JB}	4.16 C/W (Note 3)
Junction to case top thermal resistance $\theta_{JC(top)}$	18.9 C/W (Note 4)
Junction to case top thermal parameter $\Psi_{JT\ (top)}$	0.32 C/W (Note 2)
Storage Temperature Range	-55°C to 150°C
Junction Temperature Range	-40°C to 150°C

(Voltages referenced to GND unless otherwise specified)

Note 1: Must not exceed 6V.
Note 2: Value obtained via thermal simulation under natural convention on a PVNN, IR38263 demo board. 10 layer, 7” x 5.5”x0.072” PCB with 1.5 oz copper at the top and bottom layer. Inner layers 2, 3, 8 and 9 have 1 oz copper and layers 4,5,6,7 have 2 oz copper. Ta = 25C was used for the simulation.
Note 3: PCB from note 2 and package is considered in thermal simulation with Ta=25 ^{0}C. Pin 12 is considered.
Note 4: Only package is considered. Simulation is used with a cold plate that fixes top of package at Ta=25 ^{0}C.

ELECTRICAL SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

SYMBOL	DEFINITION	MIN	MAX	UNITS
PVin	Input Bus Voltage	1.5	16*	V
Vin	LDO supply voltage	5.3	16	
VCC	LDO output/Bias supply voltage	4.5	5.5	
Boot to SW	High Side driver gate voltage	4.5	5.5	
VO	Output Voltage	0.5	$0.875*PV_{in}$	
I_O	Output Current	0	30	A
Fs	Switching Frequency	150	1500	kHz
T_J	Junction Temperature	-40	125	°C

* SW Node must not exceed 25V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
MOSFET $R_{ds(on)}$						
Top Switch	Rds(on)_Top	$V_{Boot} – V_{SW}$ = 5V, I_D = 30A, Tj = 25°C		2.2		mΩ
Bottom Switch	Rds(on)_Bot	Vcc =5V, I_D = 30A, Tj = 25°C		0.78		
Reference Voltage						
Accuracy $0^0C<Tj<85^0C$		1.25V<V_{FB}<2.555V VOUT_SCALE_LOOP=1;	-1		+1	%
		0.75V<V_{FB}<1.25V VOUT_SCALE_LOOP=1;	-0.75		+0.75	
		0.45V<V_{FB}<0.75V VOUT_SCALE_LOOP=1;	-0.5		+0.5	%
Accuracy $-40^0C<Tj<125^0C$		1.25V<V_{FB}<2.555V VOUT_SCALE_LOOP=1;	-1.6		+1.6	%
		0.75V<V_{FB}<1.25V VOUT_SCALE_LOOP=1;	-1.0		+1.0	%
		0.45V<V_{FB}<0.75V VOUT_SCALE_LOOP=1;	-2.0		+2.0	%
Supply Current						
PVin range (using external Vcc=5V)				1.5-16		V
Vin range (using internal LDO)		Fsw=600kHz		5.3-16		V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
		Fsw=1.5MHz		5.5-16		
Vin range (when Vin=Vcc)			4.5	5.0	5.5	V
V_{in} Supply Current (Standby) (internal Vcc)	$I_{in(Standby)}$	Enable low, No Switching, Vin=16V, low power mode enabled		2.7	4	mA
V_{in} Supply Current (Dyn)(internal Vcc)	$I_{in(Dyn)}$	Enable high, Fs = 600kHz, Vin=16V		39	50	mA
VCC Supply Current (Standby)(external Vcc)	$I_{cc(Standby)}$	Enable low, No Switching, Vcc=5.5V, low power mode enabled		2.7	5	mA
VCC Supply Current (Dyn)(external Vcc)	$I_{cc(Dyn)}$	Enable high, Fs = 600kHz, Vcc=5.5V		39	50	mA
Under Voltage Lockout						
VCC – Start – Threshold	VCC_UVLO_Start	VCC Rising Trip Level	4.0	4.2	4.4	V
VCC – Stop – Threshold	VCC_UVLO_Stop	VCC Falling Trip Level	3.7	3.9	4.1	
Enable – Start – Threshold	Enable_UVLO_Start	Supply ramping up	0.55	0.6	0.65	V
Enable – Stop – Threshold	Enable_UVLO_Stop	Supply ramping down	0.35	0.4	0.45	
Enable leakage current	Ien	Enable=5.5V			1	µA
Oscillator						
Ramp Amplitude	Vramp	PVin=5V, D=Dmax, Note 2		0.71		Vp-p
		PVin=12V, D=Dmax, Note 2		1.84		
		PVin=16V,D=Dmax, Note 2		2.46		
Ramp Offset	Ramp (os)	Note 2		0.22		V
Min Pulse Width	Dmin (ctrl)	Note 2		35	50	ns
Fixed Off Time		Note 2 Fs=1.5MHz		100	150	ns
Max Duty Cycle	Dmax	Fs=400kHz	86	87.5	89	%
Error Amplifier						
Input Bias Current	IFb(E/A)		-0.5		+0.5	µA
Sink Current	Isink(E/A)		0.6	1.1	1.8	mA
Source Current	Isource(E/A)		8	13	25	mA
Slew Rate	SR	Note 2	7	12	20	V/µs
Gain-Bandwidth Product	GBWP	Note 2	20	30	40	MHz
DC Gain	Gain	Note 2	100	110	120	dB
Maximum Voltage	Vmax(E/A)		2.8	3.9	4.3	V
Minimum Voltage	Vmin(E/A)				100	mV

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Remote Sense Differential Amplifier						
Unity Gain Bandwidth	BW_RS	Note 2	3	6.4		MHz
DC Gain	Gain_RS	Note 2		110		dB
Offset Voltage	Offset_RS	0.5V<RS+<2.555V, 4kOhm load $27^0C<Tj<85^0C$	-1.6	0	1.6	mV
		0.5V<RS+<2.555V, 4kOhm load $-40^0C<Tj<125^0C$	-3		3	
Source Current	Isource_RS	V_RSO=1.5V, V_RSP=4V	11		16	mA
Sink Current	Isink_RS		0.4	1	2	mA
Slew Rate	Slew_RS	Note 2, Cload = 100pF	2	4	8	V/µs
RS+ input impedance	Rin_RS+		36	55	74	Kohm
RS- input impedance	Rin_RS-	Note 2	36	55	74	Kohm
Maximum Voltage	Vmax_RS	V(VCC) – V(RS+)	0.5	1	1.5	V
Minimum Voltage	Min_RS			4	20	mV
Bootstrap Diode						
Forward Voltage		I(Boot) = 40mA	150	300	450	mV
Switch Node						
SW Leakage Current	Isw	SW = 0V, Enable = 0V			1	µA
	Isw_En	SW=0; Enable= 2V		18		
Internal Regulator (VCC/LDO)						
Output Voltage	VCC	Vin(min) = 5.5V, Io=0mA, Cload = 10uF	4.8	5.15	5.4	V
		Vin(min) = 5.5V, Io=70mA, Cload = 10uF	4.5	4.99	5.2	
VCC dropout	VCC_drop	Io=0-70mA, Cload = 10uF, Vin=5.1V			0.7	V
Short Circuit Current	Ishort			110		mA
Internal Regulator (P1V8)						
Output Voltage	P1V8	Vin(min) = 4.5V, Io = 0-1mA, Cload = 2.2uF	1.795	1.83	1.905	V
1.8V UVLO Start	P1V8_UVLO_Start	1.8V Rising Trip Level	1.66	1.72	1.78	V
1.8V UVLO Stop	P1V8_UVLO_Stop	1.8V Falling Trip Level	1.59	1.63	1.68	V
Adaptive On time Mode						
Zero-crossing comparator threshold	ZC_Vth		-4	-1	2	mV
Zero-crossing comparator delay	ZC_Tdly			8/Fs		s

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
FAULTS						
Power Good						
Power Good High Threshold Rising Delay	TPDLY	Vsns rising, Vsns > Power_Good_High		0		ms
Power Good Low Threshold Falling delay	VPG_low_Dly	Vsns falling, Vsns < Power_Good_Low	150	175	200	µs
PGood Voltage Low	PG (voltage)	I_{PGood} = -5mA			0.5	V
Over Voltage Protection (OVP)						
OVP Trip Threshold	OVP (trip)	Vsns rising, VOUT_SCALE_LOOP=1, Vout=0.5V	0.57	0.605	0.63	V
OVP comparator Hysteresis	OVP (hyst)	Vsns falling, VOUT_SCALE_LOOP=1, Vout=0.5V	20	30	40	mV
OVP Fault Prop Delay	OVP (delay)	Vsns rising, Vsns-OVP(trip)>200 mV		200		ns
Over-Current Protection						
OC Trip Current	I_{TRIP}	OC limit=40, VCC = 5.05V, T_j=25^{0}C	36	40	44	A
		OC limit=16A, VCC = 5.05V, T_j=25^{0}C	12.5	16	19.5	A
OCset Current Temperature coefficient	OCSET(temp)	-40^{0}C to 125^{0}C, VCC=5.05V, Note 2		5900		ppm/°C
Hiccup blanking time	Tblk_Hiccup	Note 2		20		ms
Thermal Shutdown						
Thermal Shutdown		Note 2		145		°C
Hysteresis		Note 2		25		°C
Input Over-Voltage Protection						
PVin overvoltage threshold	$PVin_{OV}$		22	23.7	25	V
PVin overvoltage Hysteresis	$PVin_{ov\ hyst}$			2.4		V
MONITORING AND REPORTING						
Bus Speed[1]				100	400	kHz
Iout & Vout filter				78		Hz
Iout & Vout Update rate				31.25		kHz
Vin & Temperature filter				78		Hz
Vin & Temperature update rate				31.25		kHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage Reporting						
Resolution	N_{Vout}	Note 2		1/256		V
Lowest reported Vout	Vomon_low	Vsns=0V		0		V
Highest reported Vout	Vomon_high	VOUT_SCALE_LOOP=1, Vsns=3.3V		3.3		V
		VOUT_SCALE_LOOP=0.5, Vsns=3.3V		6.6		V
		VOUT_SCALE_LOOP=0.25, Vsns=3.3V		13.2		V
		VOUT_SCALE_LOOP=0.125 , Vsns=3.3V		26.4		V
Vout reporting accuracy		0^0C to 85^0C, 4.5V<Vcc<5.5V, 1V<Vsns≤ 1.5V VOUT_SCALE_LOOP=1		+/- 0.6		%
		0^0C to 85^0C, 4.5V<Vcc<5.5V, Vsns> 1.5V VOUT_SCALE_LOOP=1		+/-1		
		0^0C to 125^0C, 4.5V<Vcc<5.5V, Vsns>0.9V VOUT_SCALE_LOOP=1		+/- 1.5		
		0^0C to 125^0C, 4.5V<Vcc<5.5V, 0.5V<Vsns<0.9V VOUT_SCALE_LOOP=1		+/-3		
Iout Reporting						
Resolution	N_{Iout}	Note 2		0.0625		A
Iout (digital) monitoring Range	Iout_dig		0		40	A
Iout_dig Accuracy	I	0^0C to 125^0C, 4.5V<Vcc<5.5V, 5A < Iout <30A		+/-5		%
Temperature Reporting						
Resolution	N_{Tmon}	Note 2		1		°C
Temperature Monitoring Range	Tmon_dig		-40		150	°C
Thermal shutdown hysteresis		Note 2		25		°C
Input Voltage Reporting						
Resolution	N_{PVin}	Note 2		1/32		V
Monitoring Range	PMBVinmon		0		21	V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Monitoring accuracy		0^0C to 85^0C, 4.5V<Vcc<5.5V, PVin>10V	-1.5		1.5	%
		-40^0C to 125^0C, 4.5V<Vcc<5.5V, PVin>14V	-1.5		1.5	
		-40^0C to 125^0C, 4.5V<Vcc<5.5V, 7V<PVin<14V	-4		4	
I2C Interface Timing Specifications						
I2C Operating frequency	F_{SMB}				400	kHz
Bus Free time between Start and Stop condition	T_{BUF}		1.3			µs
Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	$T_{HD:STA}$		0.6			µs
Repeated start condition setup time	$T_{SU:STA}$		0.6			µs
Stop condition setup time	$T_{SU:STO}$		0.6			µs
Data Rising Threshold			1.339		1.766	V
Data Falling Threshold			1.048		1.495	V
Clock Rising Threshold			1.339		1.766	V
Clock Falling Threshold			1.048		1.499	V
Data Rising Threshold LVT			0.7		0.9	V
Data Falling Threshold LVT			0.45		0.65	V
Clock Rising Threshold LVT			0.7		0.9	V
Clock Falling Threshold LVT			0.45		0.65	V
Data Hold Time	$T_{HD:DAT}$		300		900	ns
Data Setup Time	$T_{SU:DAT}$		100			ns
Data pulldown resistance			8	11	16	Ω
Clock low time out	$T_{TIMEOUT}$		25		35	ms
Clock low period	T_{LOW}		1.3			µs
Clock High Period	T_{HIGH}		0.6		50	µs
Digital Inputs – Low Vth Type 2 (VIDSELx)						

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input High Voltage			0.65	-	-	V
Input Low Voltage			-	-	0.45	V
Hysteresis			-	95	-	mV
Input Leakage Current		Vpad = 0 to 2V	-	-	±1	µA

Notes

2. Guaranteed by design but not tested in production
3. Guaranteed by statistical correlation, but not tested in production

TYPICAL APPLICATION DIAGRAMS

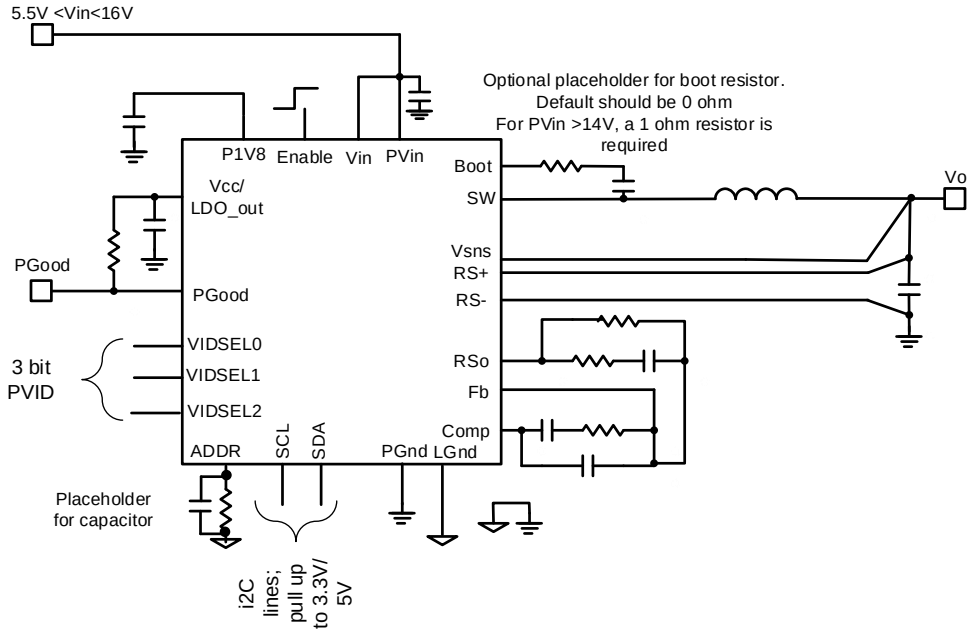


Figure 4: Using the internal LDO, Vo < 2.555V

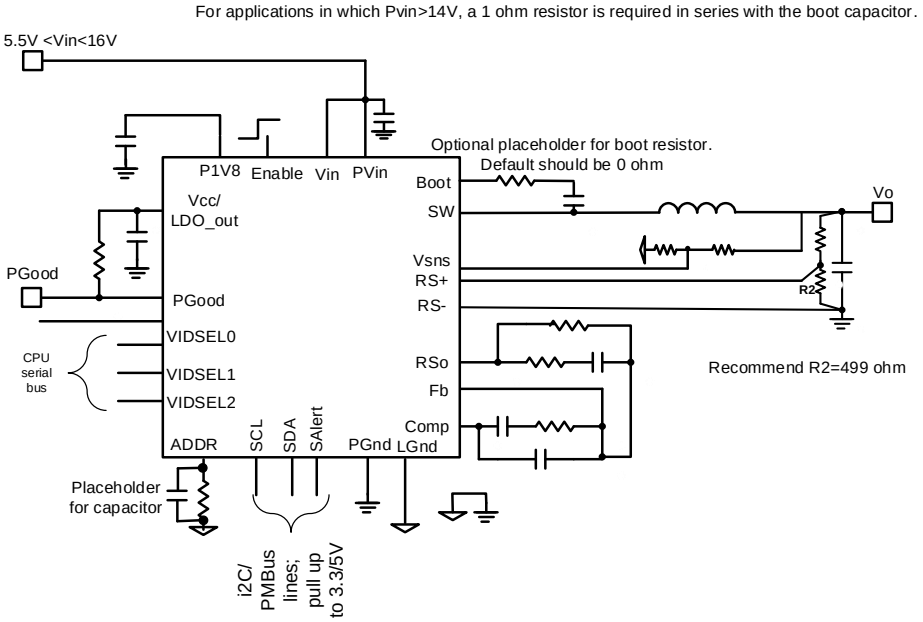


Figure 5: Using the internal LDO, Vo > 2.555V

TYPICAL APPLICATION DIAGRAMS

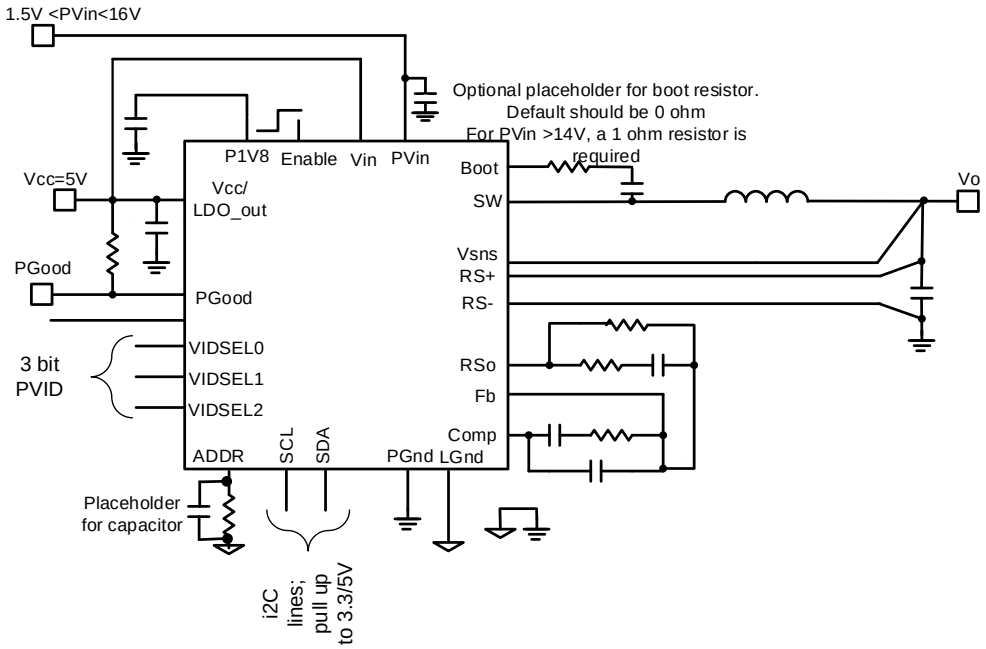


Figure 6: Using external Vcc, Vo<2.555V

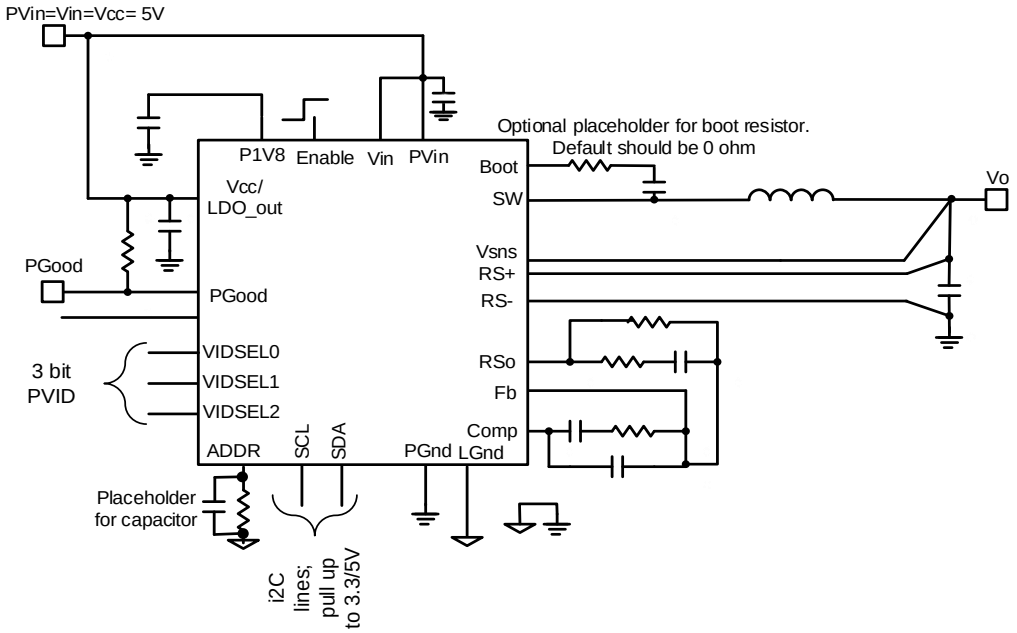
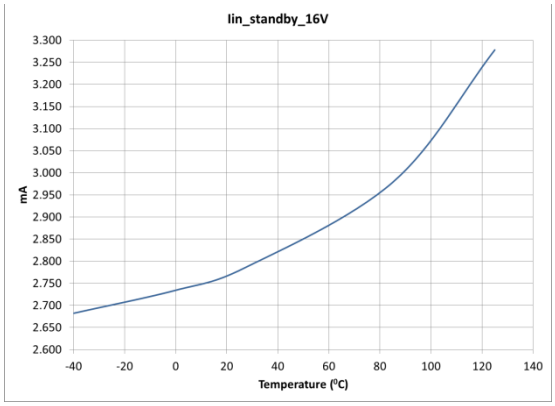
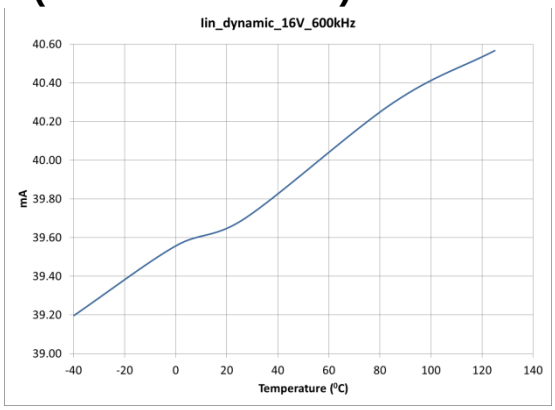
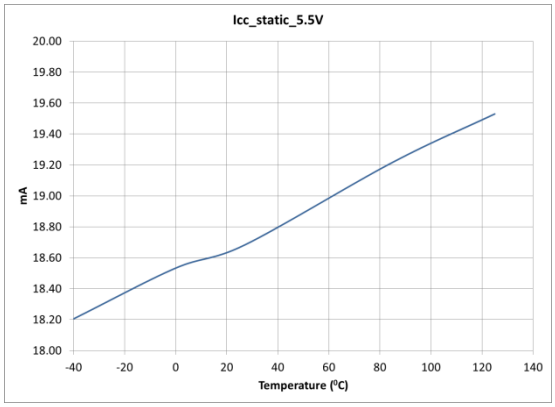


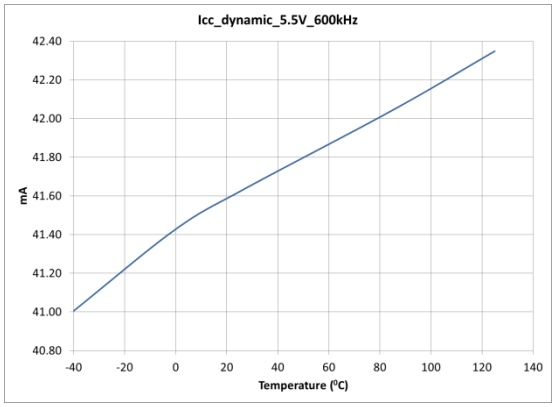
Figure 7: Single 5V application, Vo<2.555V

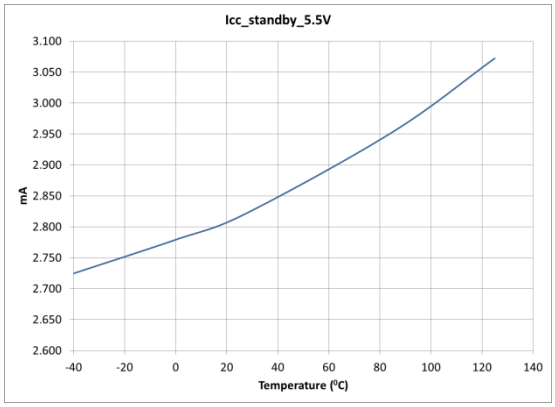
TYPICAL OPERATING CHARACTERISTICS (-40°C TO +125°C)

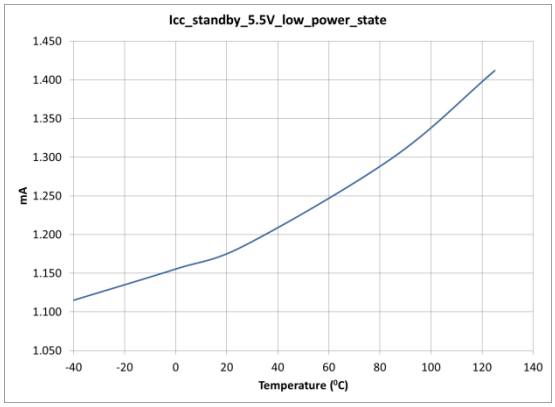




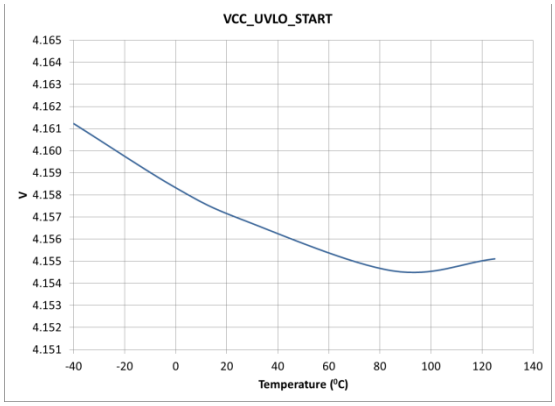


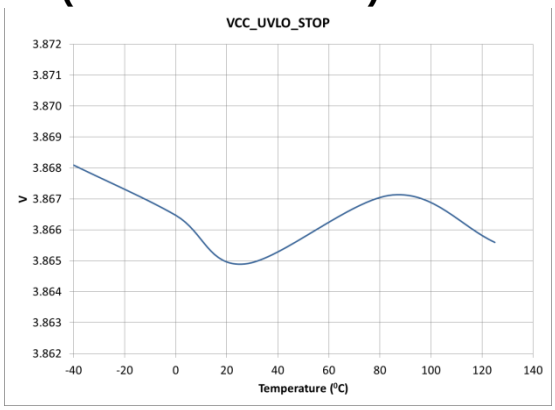


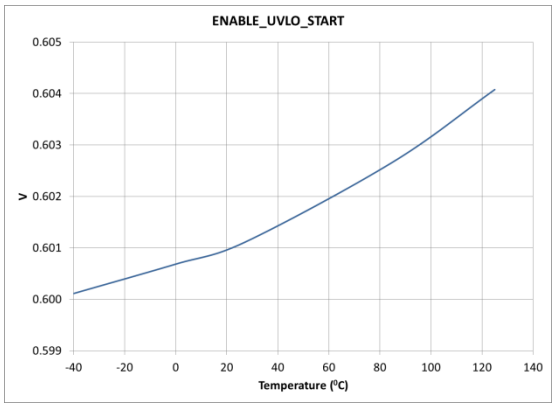


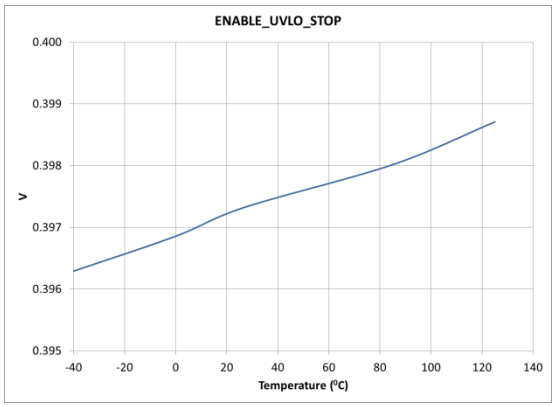


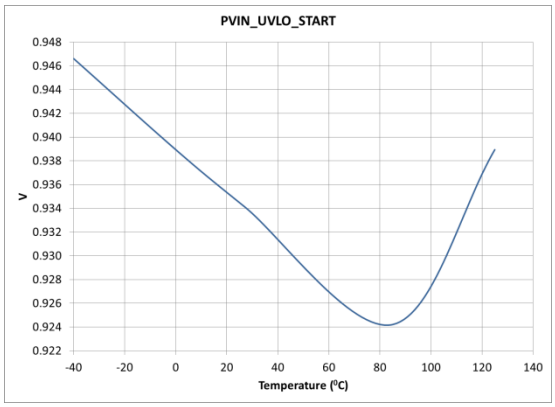
TYPICAL OPERATING CHARACTERISTICS (-40°C TO +125°C)

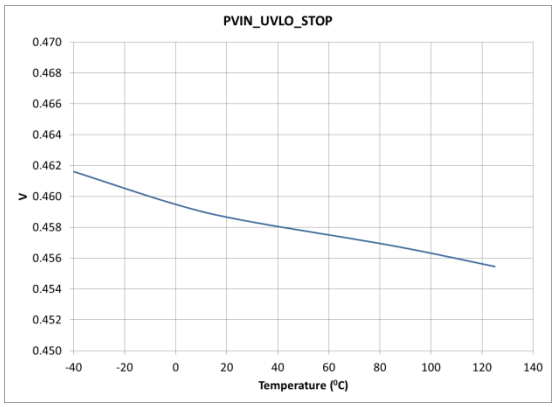




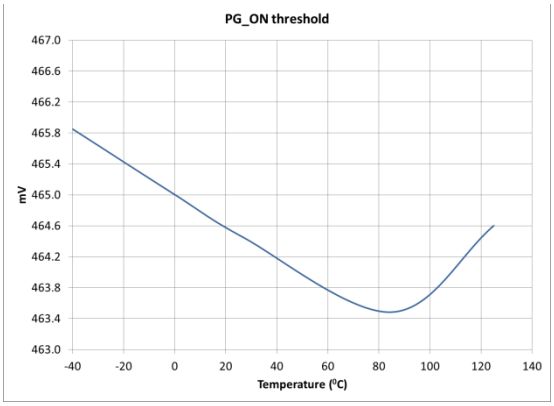


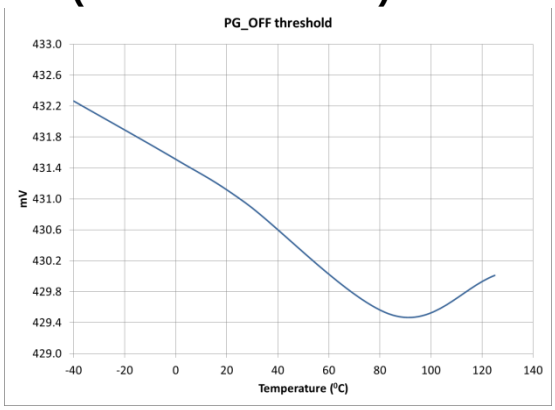


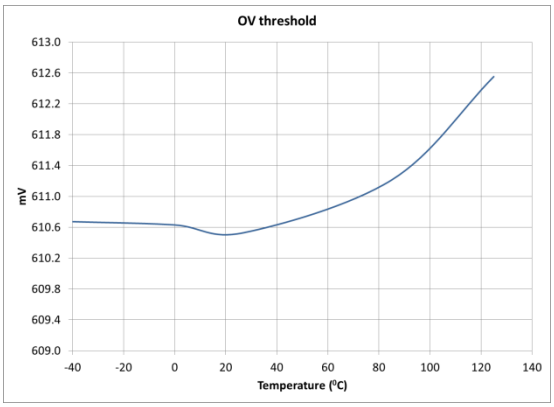


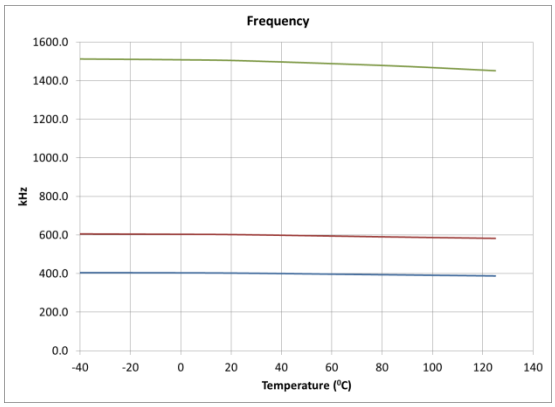


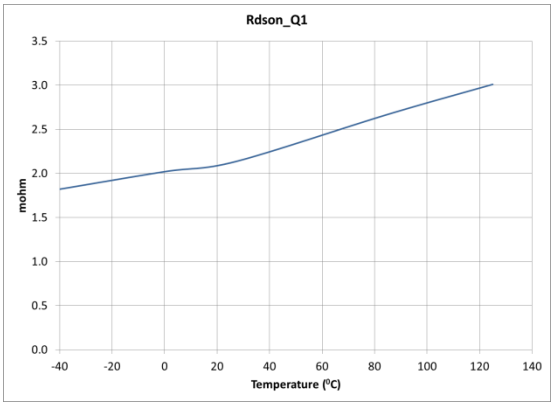
TYPICAL OPERATING CHARACTERISTICS (-40°C TO +125°C)

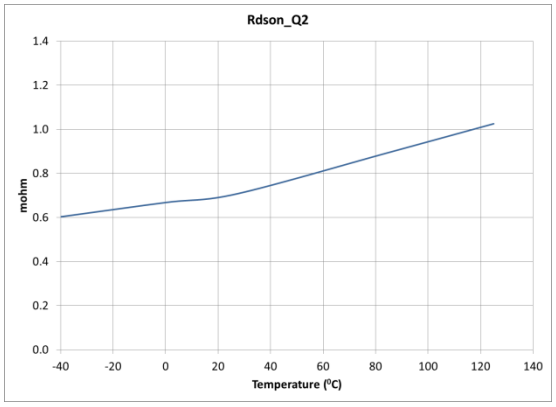




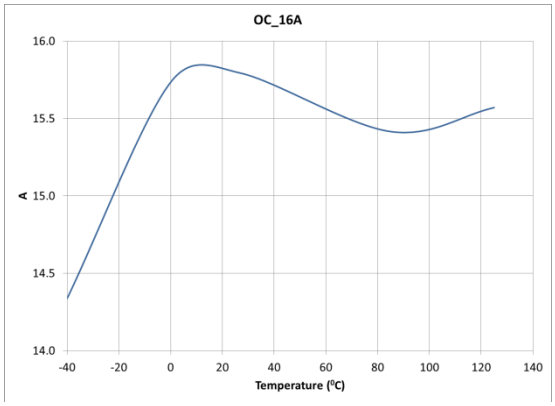


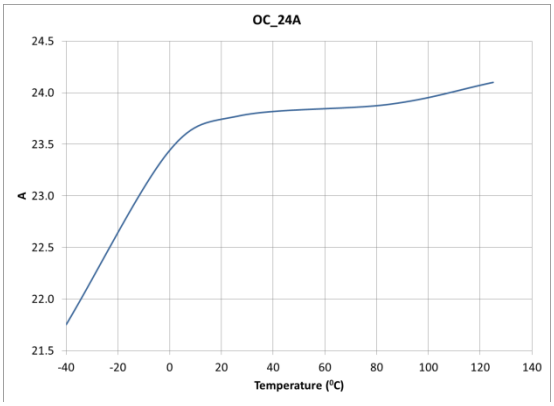


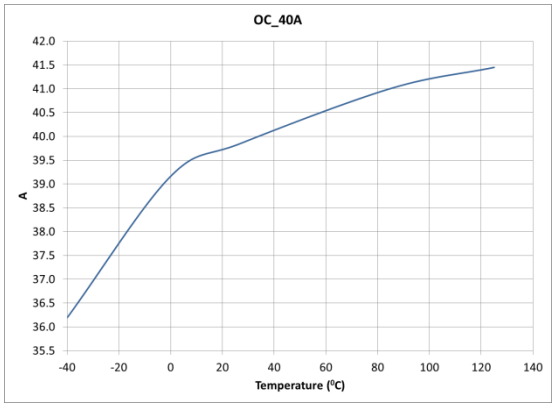




TYPICAL OPERATING CHARACTERISTICS (-40°C TO +125°C)



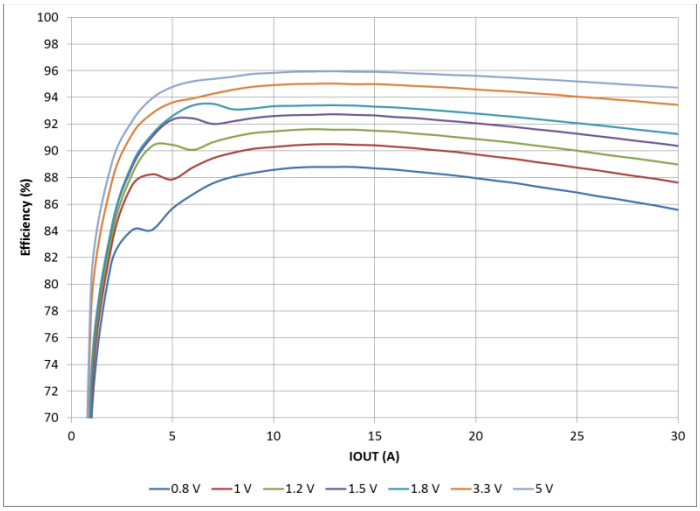


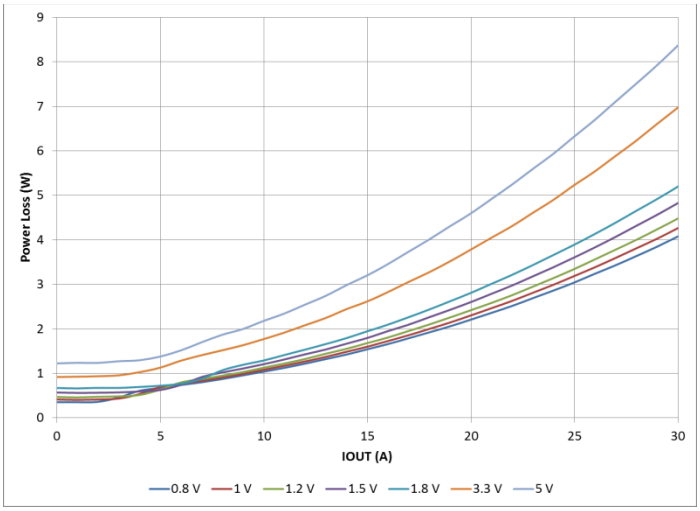


TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = Vin = 12V, VCC = 5V, Io=0-30A, Fs= 600kHz, Room Temperature, No Air Flow. Note that the losses of the inductor, input and output capacitors are also considered in the efficiency and power loss curves. The table below shows the indicator used for each of the output voltages in the efficiency measurement.

VOUT (V)	LOUT (uH)	P/N	DCR (mΩ)
0.8	0.15	HCB178380D-151 (Delta)	0.15
1	0.15	HCB138380D-151 (Delta)	0.15
1.2	0.15	HCB138380D-151 (Delta)	0.15
1.5	0.15	HCB138380D-151 (Delta)	0.15
1.8	0.15	HCB138380D-101 (Delta)	0.15
3.3	0.32	FP1308R3-R32-R (Cooper)	0.32
5	0.32	FP1308R3-R32-R (Cooper)	0.32

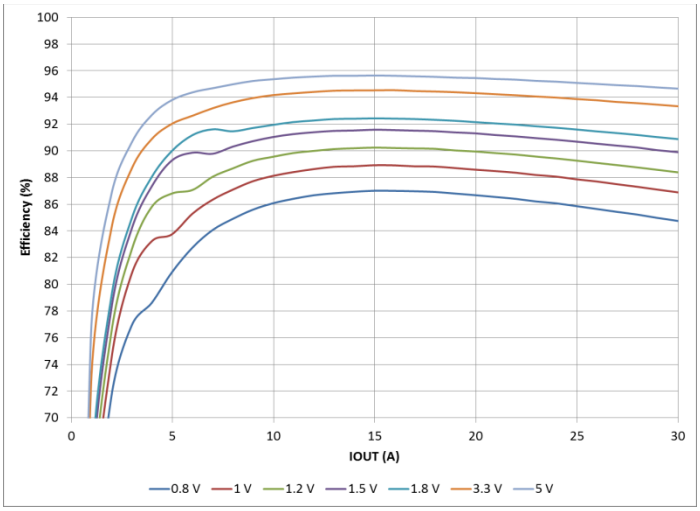


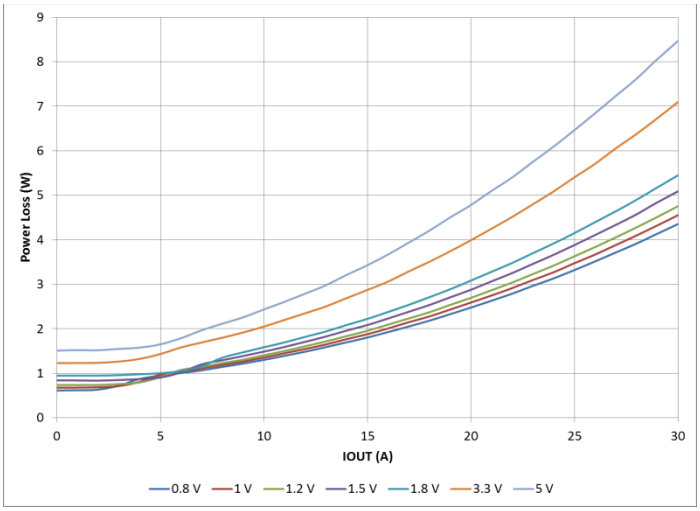


TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = Vin = 12V, Internal LDO, Io=0-30A, Fs= 600kHz, Room Temperature, No Air Flow. Note that the losses of the inductor, input and output capacitors are also considered in the efficiency and power loss curves. The table below shows the indicator used for each of the output voltages in the efficiency measurement.

VOUT (V)	LOUT (uH)	P/N	DCR (mΩ)
0.8	0.15	HCB178380D-151 (Delta)	0.15
1	0.15	HCB138380D-151 (Delta)	0.15
1.2	0.15	HCB138380D-151 (Delta)	0.15
1.5	0.15	HCB138380D-151 (Delta)	0.15
1.8	0.15	HCB138380D-101 (Delta)	0.15
3.3	0.32	FP1308R3-R32-R (Cooper)	0.32
5	0.32	FP1308R3-R32-R (Cooper)	0.32

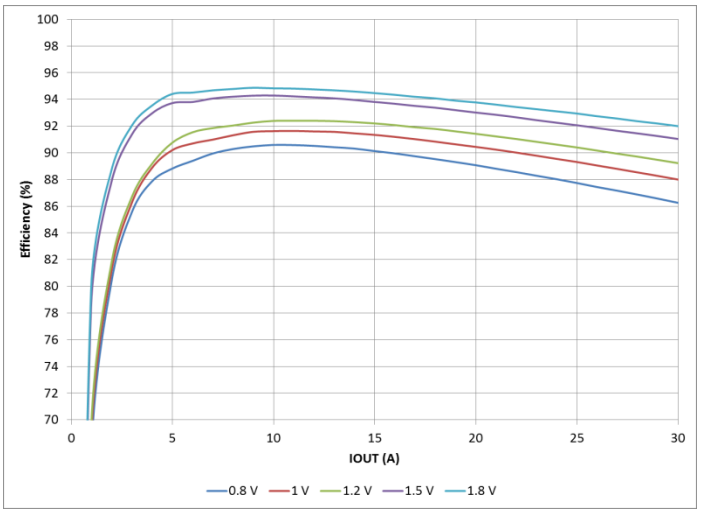


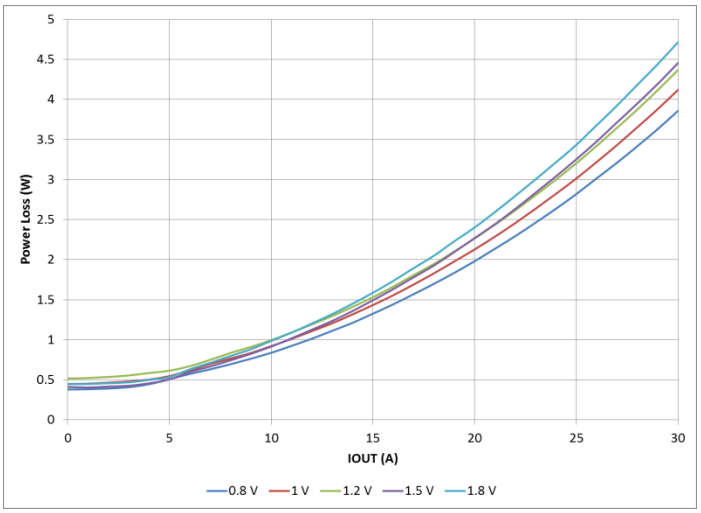


TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = Vin = VCC = 5V, Io=0-30A, Fs= 600kHz, Room Temperature, No Air Flow. Note that the losses of the inductor, input and output capacitors are also considered in the efficiency and power loss curves. The table below shows the indicator used for each of the output voltages in the efficiency measurement.

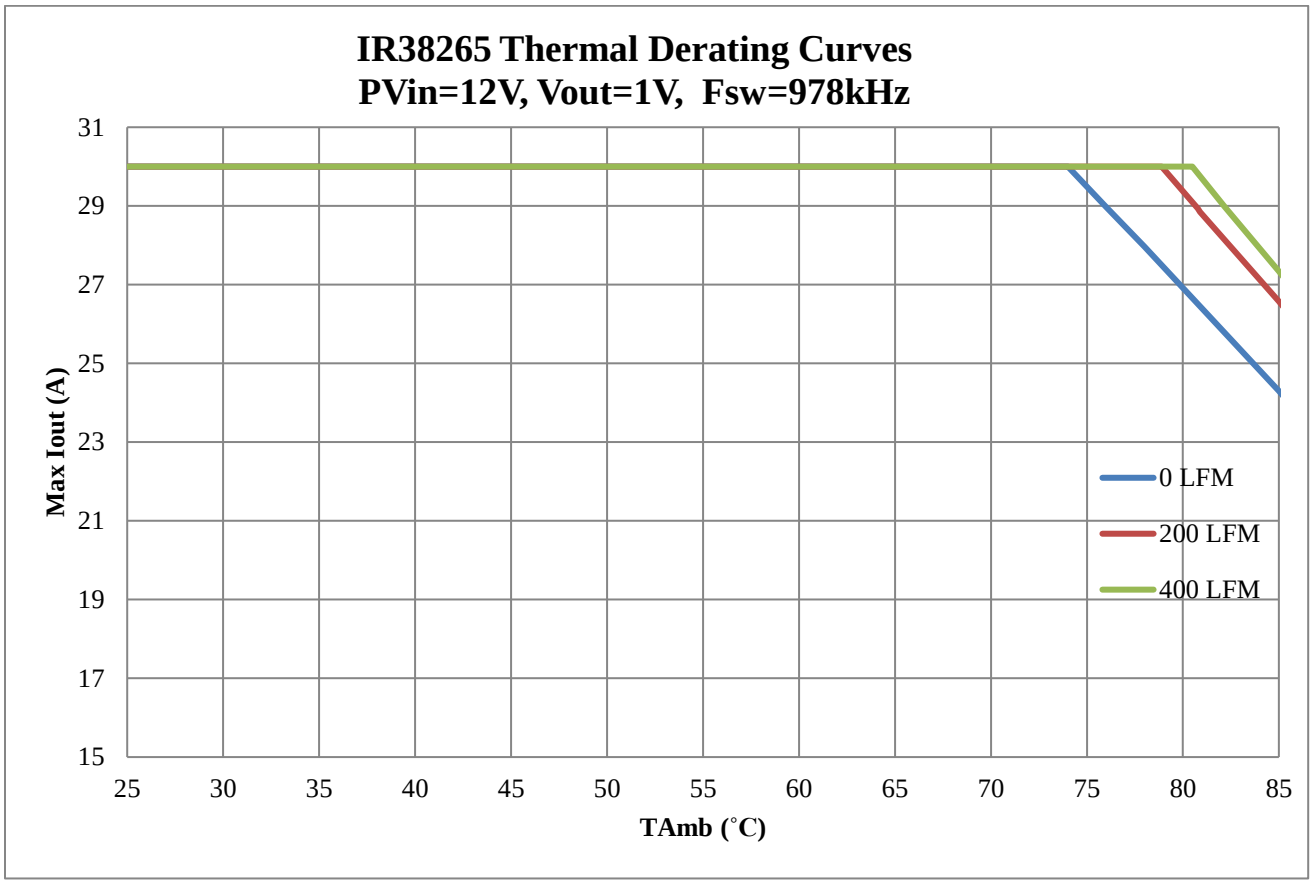
VOUT (V)	LOUT (uH)	P/N	DCR (mΩ)
0.8	0.1	HCB138380D-101 (Delta)	0.15
1	0.1	HCB138380D-101 (Delta)	0.15
1.2	0.15	HCB138380D-101 (Delta)	0.15
1.5	0.15	HCB138380D-151 (Delta)	0.15
1.8	0.15	HCB138380D-151 (Delta)	0.15





THERMAL DERATING CURVES

The measurements were done on an evaluation kit demo board. The PCB is 7.0” x 5.5” x 0.072” with 10-layers, FR4 material and 2 oz. copper. The conditions used were, PVin = Vin = 12V, Internal LDO, Io=30A, Fs= 978kHz.



THEORY OF OPERATION

DESCRIPTION

The IR38265 is a 30A rated synchronous buck converter that supports II2C communication. This device also has 3 pins that function as a parallel VID interface that can be used to set the output voltage to one of eight pre-programmed settings. They use an externally compensated fast, analog, PWM voltage mode control scheme to provide good noise immunity as well as fast dynamic response in a wide variety of applications. At the same time, the digital communication interfaces allow complete configurability of output setting and fault functions, as well as telemetry.

The switching frequency is programmable from 150 kHz to 1500 kHz and provides the capability of optimizing the design in terms of size and performance. Recommend 500 kHz or higher frequencies.

This device provides precisely regulated output voltages from 0.5V to 0.875*PVin programmed via two external resistors or through the communication interfaces. They operate with an internal bias supply (LDO), typically 5.2V. This allows operation with a single supply. The output of this LDO is brought out at the Vcc pin and must be bypassed to the system power ground with a 10 uF decoupling capacitor. The Vcc pin may also be connected to the Vin pin, and an external Vcc supply between 4.5V and 5.5V may be used, allowing an extended operating bus voltage (PVin) range from 1.5V to 16V.

The device utilizes the on-resistance of the low side MOSFET (synchronous MOSFET) as current sense element. This method enhances the converter's efficiency and reduces cost by eliminating the need for external current sense resistor.

The IR38265 includes two low $R_{ds(on)}$ MOSFETs using Infineon's OptiMOS™ technology. These are specifically designed for low duty cycle, high efficiency applications.

DEVICE POWER-UP AND INITIALIZATION

During the power-up sequence, when Vin is brought up, the internal LDO converts it to a regulated 5.2V at Vcc. There is another LDO which further converts this down to 1.8V to supply the internal digital circuitry. An under-voltage lockout circuit monitors the voltage of VCC pin and the P1V8 pin, and holds the Power-on-reset (POR) low until these voltages exceed their thresholds and the internal 48 MHz oscillator is stable. When the device comes out of reset, it initializes a multiple times programmable (MTP) memory load cycle, where the contents of the MTP are loaded into the working registers. Once the registers are loaded from MTP, the designer can use the I2C interface to re-configure the various parameters to suit the specific VR design requirements if desired, irrespective of the status of Enable.

The typical default configuration utilizes the internal LDO to supply the VCC rail when PVin is brought up. For this configuration power conversion is enabled only when the Enable pin voltage exceeds its under-voltage threshold, the PVin bus voltage exceeds its under-voltage threshold, the contents of the MTP have been fully loaded into the working registers and the device address has been read. The initialization sequence is shown in Figure 8. Another common default configuration uses an external power supply for the VCC rail. While in this configuration it is recommended to ensure the VCC rail reaches its target voltage prior the enable signal goes high.

Additional options are available to enable the device power conversion through software and these options may be configured to override the default by using the I2C interface.

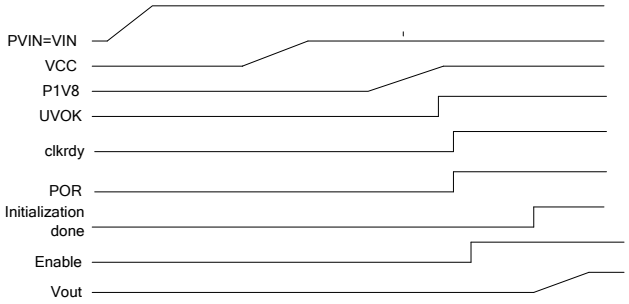


Figure 8: Initialization sequence showing PVin, Vin, Vcc, 1.8V, Enable and Vout signals as well as the internal logic signals

I2C COMMUNICATION

The IR38265 has two 7-bit registers that are used to set the base I2C address, as shown below in Table 1.

Table 1: Registers used to set device base address

Register	Description
I2C_address[6:0]	The chip I2C address. An address of 0 will disable I2C communication.

In addition, a resistor may be connected between the ADDR and LGND pins to set an offset from the default preconfigured I2C address (0x10) in the MTP. Up to 16 different offsets can be set, allowing 16 devices with unique addresses in a single system. This offset, and hence, the device address, is read by the internal 10 bit ADC during the initialization sequence.

Table 2 below provides the resistor values needed to set the 16 offsets from the base address.

Table 2 : Address offset vs. External Resistor(R_{ADDR})

ADDR Resistor (Ohm)	Address Offset
499	+0
1050	+1
1540	+2
2050	+3
2610	+4
3240	+5
3830	+6
4530	+7
5230	+8

6040	+9
6980	+10
7870	+11
8870	+12
9760	+13
10700	+14
>11800	+15

The device will then respond to I2C commands sent to this address. There is also a register bit *I2C_disable_addr_offset* that may be set in order to instruct the device to ignore the resistor offset. If this bit is set, the device will always respond to commands sent to the base address.

MODES FOR SETTING OUTPUT VOLTAGES

The IR38265 uses the VIDSEL0, VIDSEL1 and VIDSEL2 lines to set the output voltage. The VIDSELx lines select an MTP register which holds a VID value that sets the output voltage. The MTP registers are programmable via I2C. Note that the same VID value can result in different voltages depending on which VID table, 5mV or 10mV has been selected. Table 3 shows how the VIDSELx lines are used to select the register containing the target value. It is worth noting that the VIDSEL lines may be driven with logic gates or with Open drain devices. When driven by open drain devices, a pullup resistor of 4.99K must be used. When driven by logic gates, a resistor of 4.99K is required in series with the pin. The VID tables for 5mV and 10mV VID steps are shown in the tables 4 and 5 below.

Table 3: Mapping the VIDSEL lines to MTP registers

VIDSEL2	VIDSEL1	VIDSEL0	Selects MTP register address
0	0	0	77h
0	0	1	78h
0	1	0	79h
0	1	1	7Ah
1	0	0	7Bh
1	0	1	7Ch
1	1	0	7Dh
1	1	1	7Eh

Table 4: Intel 5mV VID table

VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)
FF	1.52	C5	1.23	91	0.97	57	0.68	2F	0.48
FE	1.515	C4	1.225	90	0.965	56	0.675	2E	0.475
FD	1.51	C3	1.22	8F	0.96	55	0.67	2D	0.47
FC	1.505	C2	1.215	8E	0.955	54	0.665	2C	0.465
FB	1.5	C1	1.21	8D	0.95	53	0.66	2B	0.46
FA	1.495	C0	1.205	8C	0.945	52	0.655	2A	0.455
F9	1.49	BF	1.2	8B	0.94	51	0.65	29	0.45
F8	1.485	BE	1.195	8A	0.935	50	0.645	28	0.445
F7	1.48	BD	1.19	89	0.93	4F	0.64	27	0.44
F6	1.475	BC	1.185	88	0.925	4E	0.635	26	0.435
F5	1.47	BB	1.18	87	0.92	4D	0.63	25	0.43
F4	1.465	BA	1.175	86	0.915	4C	0.625	24	0.425
F3	1.46	B9	1.17	85	0.91	4B	0.62	23	0.42
F2	1.455	B8	1.165	84	0.905	4A	0.615	22	0.415
F1	1.45	B7	1.16	83	0.9	49	0.61	21	0.41
F0	1.445	B6	1.155	82	0.895	48	0.605	20	0.405
EF	1.44	BB	1.18	81	0.89	47	0.6	1F	0.4
EE	1.435	BA	1.175	80	0.885	58	0.685	1E	N/A
ED	1.43	B9	1.17	7F	0.88	57	0.68	1D	N/A
EC	1.425	B8	1.165	7E	0.875	56	0.675	1C	N/A
EB	1.42	B7	1.16	7D	0.87	55	0.67	1B	N/A
EA	1.415	B6	1.155	7C	0.865	54	0.665	1A	N/A
E9	1.41	B5	1.15	7B	0.86	53	0.66	19	N/A
E8	1.405	B4	1.145	7A	0.855	52	0.655	18	N/A
E7	1.4	B3	1.14	79	0.85	51	0.65	17	N/A
E6	1.395	B2	1.135	78	0.845	50	0.645	16	N/A
E5	1.39	B1	1.13	77	0.84	4F	0.64	15	N/A
E4	1.385	B0	1.125	76	0.835	4E	0.635	14	N/A
E3	1.38	AF	1.12	75	0.83	4D	0.63	13	N/A
E2	1.375	AE	1.115	74	0.825	4C	0.625	12	N/A
E1	1.37	AD	1.11	73	0.82	4B	0.62	11	N/A
E0	1.365	AC	1.105	72	0.815	4A	0.615	10	N/A
DF	1.36	AB	1.1	71	0.81	49	0.61	F	N/A
DE	1.355	AA	1.095	70	0.805	48	0.605	E	N/A
DD	1.35	A9	1.09	6F	0.8	47	0.6	D	N/A
DC	1.345	A8	1.085	6E	0.795	46	0.595	C	N/A
DB	1.34	A7	1.08	6D	0.79	45	0.59	B	N/A
DA	1.335	A6	1.075	6C	0.785	44	0.585	A	N/A
D9	1.33	A5	1.07	6B	0.78	43	0.58	9	N/A
D8	1.325	A4	1.065	6A	0.775	42	0.575	8	N/A
D7	1.32	A3	1.06	69	0.77	41	0.57	7	N/A
D6	1.315	A2	1.055	68	0.765	40	0.565	6	N/A
D5	1.31	A1	1.05	67	0.76	3F	0.56	5	N/A
D4	1.305	A0	1.045	66	0.755	3E	0.555	4	N/A
D3	1.3	9F	1.04	65	0.75	3D	0.55	3	N/A
D2	1.295	9E	1.035	64	0.745	3C	0.545	2	N/A
D1	1.29	9D	1.03	63	0.74	3B	0.54	1	N/A
D0	1.285	9C	1.025	62	0.735	3A	0.535	0	0
CF	1.28	9B	1.02	61	0.73	39	0.53		
CE	1.275	9A	1.015	60	0.725	38	0.525		
CD	1.27	99	1.01	5F	0.72	37	0.52		
CC	1.265	98	1.005	5E	0.715	36	0.515		
CB	1.26	97	1	5D	0.71	35	0.51		
CA	1.255	96	0.995	5C	0.705	34	0.505		
C9	1.25	95	0.99	5B	0.7	33	0.5		
C8	1.245	94	0.985	5A	0.695	32	0.495		
C7	1.24	93	0.98	59	0.69	31	0.49		
C6	1.235	92	0.975	58	0.685	30	0.485		

Table 4: Intel 10mV VID table

VID (HEX)	VOLTAGE (V)	VID (HEX)	VOLTAGE (V)	VID (HEX)	VOLTAGE (V)	VID (HEX)	VOLTAGE (V)	VID (HEX)	VOLTAGE (V)
FF	3.04	C5	2.46	8B	1.88	51	1.30	17	0.72
FE	3.03	C4	2.45	8A	1.87	50	1.29	16	0.71
FD	3.02	C3	2.44	89	1.86	4F	1.28	15	0.70
FC	3.01	C2	2.43	88	1.85	4E	1.27	14	0.69
FB	3.00	C1	2.42	87	1.84	4D	1.26	13	0.68
FA	2.99	C0	2.41	86	1.83	4C	1.25	12	0.67
F9	2.98	BF	2.40	85	1.82	4B	1.24	11	0.66
F8	2.97	BE	2.39	84	1.81	4A	1.23	10	0.65
F7	2.96	BD	2.38	83	1.80	49	1.22	F	0.64
F6	2.95	BC	2.37	82	1.79	48	1.21	E	0.63
F5	2.94	BB	2.36	81	1.78	47	1.20	D	0.62
F4	2.93	BA	2.35	80	1.77	46	1.19	C	0.61
F3	2.92	B9	2.34	7F	1.76	45	1.18	B	0.60
F2	2.91	B8	2.33	7E	1.75	44	1.17	A	0.59
F1	2.90	B7	2.32	7D	1.74	43	1.16	9	0.58
F0	2.89	B6	2.31	7C	1.73	42	1.15	8	0.57
EF	2.88	B5	2.30	7B	1.72	41	1.14	7	0.56
EE	2.87	B4	2.29	7A	1.71	40	1.13	6	0.55
ED	2.86	B3	2.28	79	1.70	3F	1.12	5	0.54
EC	2.85	B2	2.27	78	1.69	3E	1.11	4	0.53
EB	2.84	B1	2.26	77	1.68	3D	1.10	3	0.52
EA	2.83	B0	2.25	76	1.67	3C	1.09	2	0.51
E9	2.82	AF	2.24	75	1.66	3B	1.08	1	0.50
E8	2.81	AE	2.23	74	1.65	3A	1.07		
E7	2.80	AD	2.22	73	1.64	39	1.06		
E6	2.79	AC	2.21	72	1.63	38	1.05		
E5	2.78	AB	2.20	71	1.62	37	1.04		
E4	2.77	AA	2.19	70	1.61	36	1.03		
E3	2.76	A9	2.18	6F	1.60	35	1.02		
E2	2.75	A8	2.17	6E	1.59	34	1.01		
E1	2.74	A7	2.16	6D	1.58	33	1.00		
E0	2.73	A6	2.15	6C	1.57	32	0.99		
DF	2.72	A5	2.14	6B	1.56	31	0.98		
DE	2.71	A4	2.13	6A	1.55	30	0.97		
DD	2.70	A3	2.12	69	1.54	2F	0.96		
DC	2.69	A2	2.11	68	1.53	2E	0.95		
DB	2.68	A1	2.10	67	1.52	2D	0.94		
DA	2.67	A0	2.09	66	1.51	2C	0.93		
D9	2.66	9F	2.08	65	1.50	2B	0.92		
D8	2.65	9E	2.07	64	1.49	2A	0.91		
D7	2.64	9D	2.06	63	1.48	29	0.90		
D6	2.63	9C	2.05	62	1.47	28	0.89		
D5	2.62	9B	2.04	61	1.46	27	0.88		
D4	2.61	9A	2.03	60	1.45	26	0.87		
D3	2.60	99	2.02	5F	1.44	25	0.86		
D2	2.59	98	2.01	5E	1.43	24	0.85		
D1	2.58	97	2.00	5D	1.42	23	0.84		
D0	2.57	96	1.99	5C	1.41	22	0.83		
CF	2.56	95	1.98	5B	1.40	21	0.82		
CE	2.55	94	1.97	5A	1.39	20	0.81		
CD	2.54	93	1.96	59	1.38	1F	0.80		
CC	2.53	92	1.95	58	1.37	1E	0.79		
CB	2.52	91	1.94	57	1.36	1D	0.78		
CA	2.51	90	1.93	56	1.35	1C	0.77		
C9	2.50	8F	1.92	55	1.34	1B	0.76		
C8	2.49	8E	1.91	54	1.33	1A	0.75		
C7	2.48	8D	1.90	53	1.32	19	0.74		
C6	2.47	8C	1.89	52	1.31	18	0.73		

BUS VOLTAGE UVLO

If the input to the Enable pin is derived from the bus voltage by a suitably programmed resistive divider, it can be ensured that the device does not turn on until the bus voltage reaches the desired level as shown in Figure 9. Only after the bus voltage reaches or exceeds this level and voltage at the Enable pin exceeds its threshold (typically 0.6V) will the device be enabled. Therefore, in addition to being logic input pin to enable the converter, the Enable feature, with its precise threshold, also allows the user to override the default under-Voltage Lockout for the bus voltage (PVin). This is desirable particularly for high output voltage applications, where we might want the device to be disabled at least until PVin exceeds the desired output voltage level. Alternatively, the default 8 V PVin UVLO threshold may be reconfigured/overridden using the corresponding registers. It should be noted that the input voltage is also fed to an ADC through a 21:1 internal resistive divider. However, the digitized input voltage is used only for the purposes of reporting the input voltage through a 8-bit register *v12_supply [7:0].* It has no impact on the bus voltage UVLO, input overvoltage faults and input undervoltage warnings, all of which are implemented by using analog comparators to compare the input voltage to the corresponding thresholds programmed into the I2C registers. The bus voltage reading as reported by *v12_supply* has no effect on the input feedforward function either.

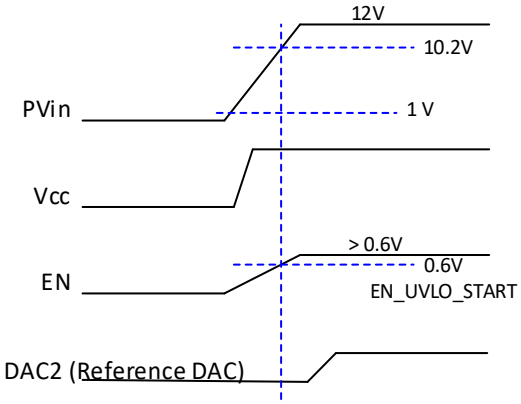


Figure 9: Normal Start up, device turns on when the bus voltage reaches 10.2V. A resistor divider is used at EN pin from PVin to turn on the device at 10.2V.

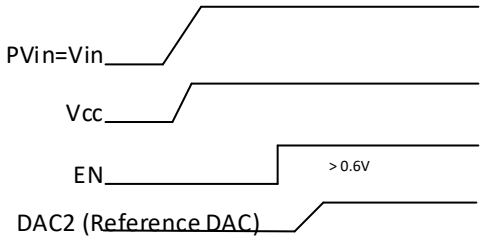


Figure 10: Recommended startup for Normal operation

Figure 10 shows the recommended startup sequence for the normal operation of the device, when Enable is used as logic input.

PRE-BIAS STARTUP

The IR38265 can start up into a pre-charged output, which prevents oscillation and disturbances of the output voltage.

The output starts in asynchronous fashion and keeps the synchronous MOSFET (Sync FET) off until the first gate signal for control MOSFET (Ctrl FET) is generated. Figure 11 shows a typical Pre-Bias condition at start up. The sync FET always starts with a narrow pulse width (12.5% of a switching period) and gradually increases its duty cycle with a step of 12.5%, with 16 cycles at each step, until it reaches the steady state value. Figure 12 shows the series of 16x8 startup pulses.

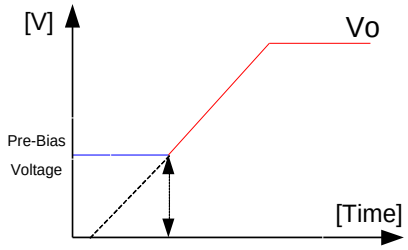


Figure 11: Pre-Bias startup

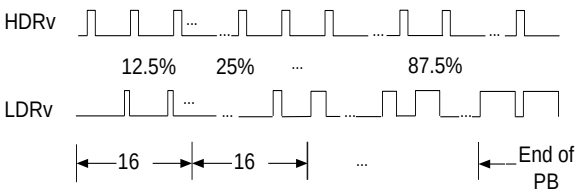


Figure 12: Pre-Bias startup pulses

SOFT-START (REFERENCE DAC RAMP)

An internal soft starting DAC controls the output voltage rise and limit the current surge at the start-up. To ensure correct start-up, the DAC sequence initiates only after power conversion is enabled when the Enable pin voltage exceeds its undervoltage threshold, the PVin bus voltage exceeds its undervoltage threshold and the contents of the MTP have been fully loaded into the working registers. Figure 13 shows the waveforms during soft start. The output voltage rises with a slew rate of 0.625 mv/us.

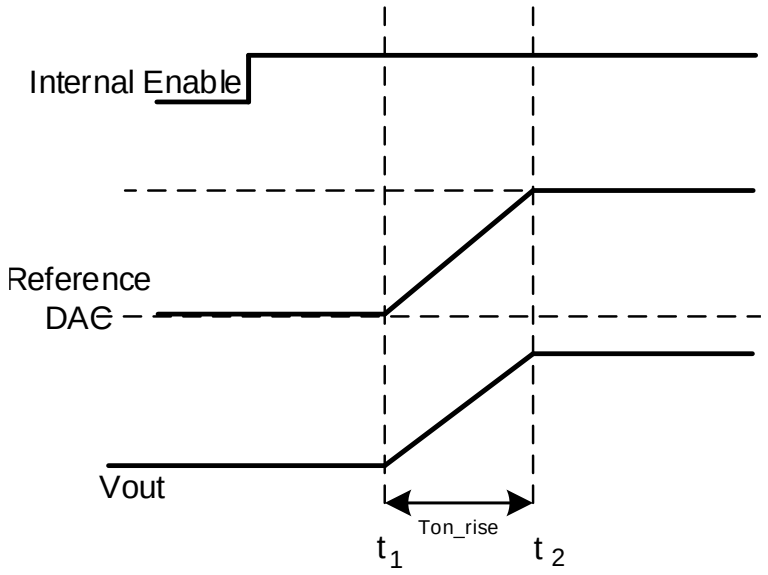


Figure 13: DAC2 (VREF) Soft start

During the startup sequence the over-current protection (OCP) and over-voltage protection (OVP) are active to protect the device against any short circuit or over voltage condition.

OPERATING FREQUENCY

Using the corresponding I2C registers, the switching frequency may be programmed between 150 kHz and 1.5 MHz. For best telemetry accuracy, it is recommended that the following switching frequencies be avoided: 250 kHz, 300 kHz, 400 kHz, 500 kHz, 600 kHz, 750 kHz, 800 kHz, 1 MHz, 1.2 MHz and 1.5 MHz. Instead, Infineon suggests using the following values 251 kHz, 302 kHz, 403 kHz, 505 kHz, 607 kHz, 762 kHz, 813 kHz, 978 kHz, 1171 kHz and 1454 kHz respectively.

SHUTDOWN

In the default configuration, the device can be shutdown by pulling the Enable pin below its 0.4V threshold. During shutdown the high side and the low side drivers are turned off. By default, the device exhibits an immediate shutdown with no delay and no soft stop.

Part may also be configured to allow a soft or controlled turned off. If the soft-stop option is used, the output voltage slews down at 0.625 mV/us.

CURRENT SENSING, TELEMETRY AND OVER CURRENT PROTECTION

Current sensing for both, telemetry as well as overcurrent protection is done by sensing the voltage across the sync FET RDson. This method enhances the converter's efficiency, reduces cost by eliminating a current sense resistor and any minimizes sensitivity to layout related noise issues. A novel, patented scheme allows reconstruction of the average inductor current from the voltage sensed across the Sync FET Rdson. It should be noted here that it is this reconstructed average inductor current that is digitized by the ADC and used for output current reporting as well as for overcurrent warning, the threshold for which may be set using the I2C commands. The current information can be read back through the 8-bit register *output_current_byte,* which reports the current in 1/4 A resolution.

The Over current (OC) fault protection circuit also uses the voltage sensed across the $R_{DS(on)}$ of the Synchronous MOSFET; however, the protection mechanism relies on a fast comparator to compare the sensed signal to the overcurrent threshold and does not depend on the ADC or reported current. The current limit scheme uses an internal temperature compensated current source that has the same temperature coefficient as the $R_{DS(on)}$ of the Synchronous MOSFET. As a result, the over-current trip threshold remains almost constant over temperature.

Over Current Protection circuitry senses the inductor current flowing through the Synchronous FET closer to the valley point. The OCP circuit samples this current for 75 ns typically after the rising edge of the PWM set pulse which is an internal signal that has a width of 12.5% of the switching period. The PWM pulse that turns on the high side FET starts at the falling edge of the PWM set pulse. This makes valley current sense more robust as current is sensed close to the bottom of the inductor downward slope where transient and switching noise is low. This helps to prevent false tripping due to noise and transients.

The actual DC output current limit point will be greater than the valley point by an amount equal to approximately half of the peak to peak inductor ripple current. The current limit point will be a function of the inductor value, input voltage, output voltage and the frequency of operation. On equation 1, I_{Limit} is the value set when configuring the 38265 OCP value. The user should account for the inductor ripple to obtain the actual DC output current limit.

$$I_{OCP} = I_{LIMIT} + \frac{\Delta i}{2} \qquad (1)$$

I_{OCP} = DC current limit hiccup point
I_{LIMIT} = Current Limit Valley Point
Δi = Inductor ripple current

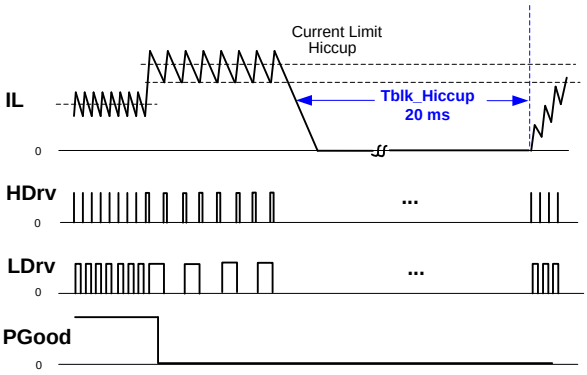


Figure 14: Timing Diagram for Current Limit Hiccup

In the default configuration, if the overcurrent detection trips the OCP comparator for a total of 8 cycles, the device goes into a hiccup mode. The hiccup is performed by de-asserting the internal Enable signal to the analog and power conversion circuitry and holding it low for 20 ms.

Following this, the OCP signal resets and the converter recovers. After every hiccup cycle, the converter stays in this mode until the overload or short circuit is removed. This behavior is shown in Figure 14.

It should be noted that on some units, a false OCP maybe experienced during device start-up due to noise. The part will ride through this false OCP due to the pulse by pulse current limiting feature and successfully ramp to the correct output voltage.

Note that the user can reprogram the default overcurrent threshold using I2C. It is recommended that the overcurrent threshold be programmed to at least 16A for good accuracy. While these devices will still offer overcurrent protection for thresholds programmed lower than these recommended values, the thresholds will not be as accurate.

Also, there is a register than can be reprogrammed using I2C to configure the part to respond to an overcurrent fault in one of two ways

1) Pulse by pulse current limiting for a programmed number of 8 switching cycles followed by a latched shutdown.
2) Pulse by pulse current limiting for a programmed number 8 switching cycles followed by hiccup. This is the default explained above.

The pulse-by-pulse or constant current limiting mechanism is briefly explained below.

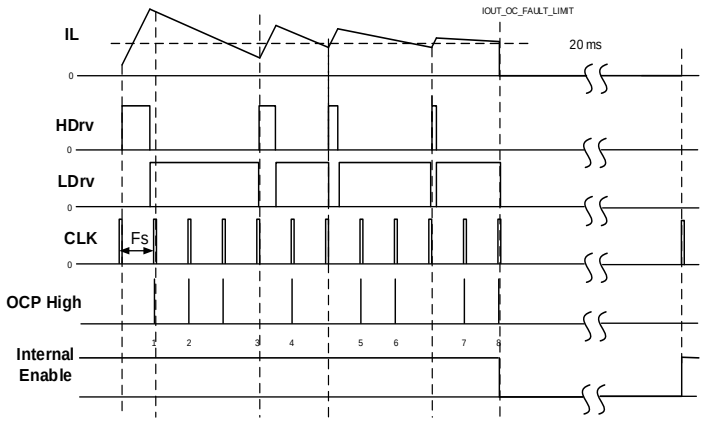


Figure 15: Pulse by pulse current limiting for 8 cycles, followed by hiccup.

In Figure 15 above, with the overcurrent response set to pulse-by-pulse current limiting for 8 cycles followed by hiccup, the converter is operating at D<0.125 when the overcurrent condition occurs. In such a case, no duty cycle limiting is applied.

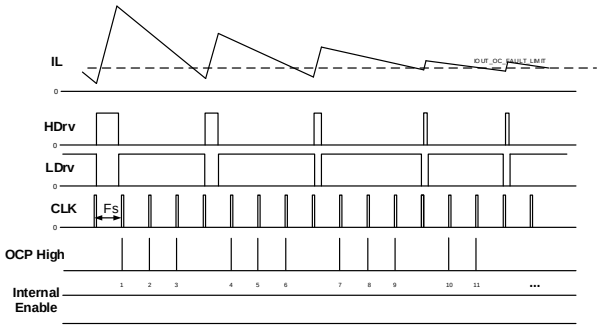


Figure 16: Constant current limiting.

Figure 16 depicts a case where the overcurrent condition happens when the converter is operating at D>0.5 and the overcurrent response has been set to Constant current operation through pulse by pulse current limiting. In such a case, after 3 consecutive overcurrent cycles are recognized, the pulse width is dropped such that D=0.5 and then after 3 more consecutive OCP cycles, to 0.25 and then finally to 0.125 at which it keeps running until the total OCP count reaches the programmed maximum following which the part enters hiccup mode. Conversely, when the overcurrent condition disappears, the pulse width is restored to its nominal value gradually, by a similar mechanism in reverse; every sequence of 4 consecutive cycles in which the current is below the overcurrent threshold doubles the duty cycle, so that D goes from 0.125 to 0.25, then to 0.5 and finally to its nominal value.

DIE TEMPERATURE SENSING, TELEMETRY AND THERMAL SHUTDOWN

On die temperature sensing is used for accurate temperature reporting and over temperature detection. The temperature may be read back through the 8-bit register *temp_byte,* which reports the die temperature in 1^0C resolution, offset by 40^0C. Thus, the temperature is given by temp_*byte* $+40^0$C.

The trip threshold is set by default to 125°C. The default over temperature response of the device is to inhibit power conversion while the fault is present, followed by automatic restart after the fault condition is cleared. Hence, in the default configuration, when trip threshold is exceeded, the internal Enable signal to the power conversion circuitry is de-asserted, turning off both MOSFETs.

Automatic restart is initiated when the sensed temperature drops within the operating range. There is a 25°C hysteresis in the thermal shutdown threshold.

The default overtemperature threshold as well as overtemperature response may be re-configured or overridden using the corresponding MTP registers. The devices support three types of responses to an over-temperature fault:

1) Ignore
2) Inhibit when over temperature condition exists and auto-restart when over temperature condition disappears
3) Latched shutdown.

REMOTE VOLTAGE SENSING

True differential remote sensing in the feedback loop is critical to high current applications where the output voltage across the load may differ from the output voltage measured locally across an output capacitor at the output inductor, and to applications that require die voltage sensing.

The RS+ and RS- pins form the inputs to a remote sense differential amplifier with high speed, low input offset and low input bias current, which ensure accurate voltage sensing and fast transient response in such applications.

The input range for the differential amplifier is limited to 1.5V below the VCC rail. Therefore, for applications in which the output voltage is more than 3V, it is recommended to use local sensing, or if remote sensing is a must, then the voltage between the RS+ and RS-pins must be divided down to less than 3V using a resistive voltage divider. It's recommended that the divider be placed at the input of the remote sense amplifier and that a low impedance such as 499 Ω be used between the RS+ and RS- nodes. A typical schematic for this setup is shown on Figure 5. Please note, however, that this modifies the open loop transfer function and requires a change in the compensation network to optimally stabilize the loop.

FEED-FORWARD

Feed-Forward (F.F.) is an important feature, because it can keep the converter stable and preserve its load transient performance when PVin varies over a wide range. The PWM ramp amplitude (Vramp) is proportionally changed with PVin to maintain PVin/Vramp almost constant throughout PVin variation range (as shown in Figure 17). Thus, the control loop bandwidth and phase margin can be maintained constant. Feed-forward function can also minimize impact on output voltage from fast PVin change. The feedforward is disabled for PVin<4.7V. Hence, for PVin<4.7V, a re-calculation of control loop parameters is needed for re-compensation.

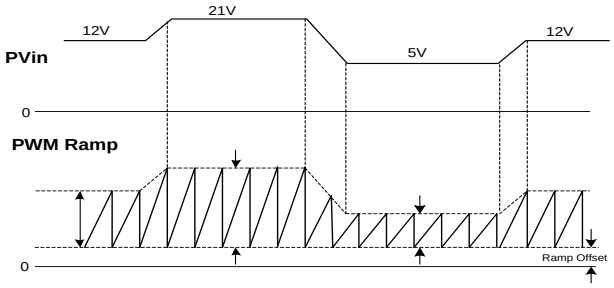


Figure 17: Timing Diagram for Feed-Forward (F.F.) Function

LIGHT LOAD EFFICIENCY ENHANCEMENT (AOT)

These devices implement a diode emulation scheme with Adaptive On Time control or AOT to improve light load efficiency. It is based on a COT (Constant On Time) control scheme with some novel advancements that make the on-time during diode emulation adaptive and dependent upon the pulse width in constant frequency operation. This allows the scheme to be combined with a PWM scheme, while providing relatively smooth transition between the two modes of operation. In other words, the switching regulator can operate in AOT mode at light loads and automatically switch to PWM at medium and heavy loads and vice versa. Therefore, the regulator will benefit from the high efficiency of the AOT mode at light loads, and from the constant frequency and fast transient response of the PWM at medium to heavy loads.

A register bit *mfr_fccm* bit can be used to enable AOT operation at light load.

Shortly after the reference voltage has finished ramping up, an internal circuit which is called the “calibration circuit” starts operation. It samples the Comp voltage (output of the error amplifier), digitizes it and stores it in a register. There is a DAC which converts the value of this register to an analog voltage which is equal to the sampled Comp voltage. At this time, the regulator is ready to enter AOT mode if the load condition is appropriate. If the load is so low that the inductor current becomes negative before the next SW pulse, the operation can be switched to AOT mode. The condition to enter AOT is the occurrence of 8 consecutive inductor current zero crossings in eight consecutive switching cycles. If this happens, operation is switched to AOT mode as shown in Figure 18Figure 18. The inductor current is sensed using the RDS_ON of the Sync-FET and no direct inductor current measuring is required. In AOT mode, just like COT operation, pulses with constant width are generated and diode emulation is utilized. This means that a pulse is generated and LDrv is held on until the inductor current becomes zero. Then both HDrv and LDrv remain off until the voltage of the sense pin comes down and reaches the reference voltage. At this moment the next pulse is generated. The sense pin is connected to the output voltage by a resistor divider which has the same ratio as the voltage divider which is connected to the feedback pin (Fb).

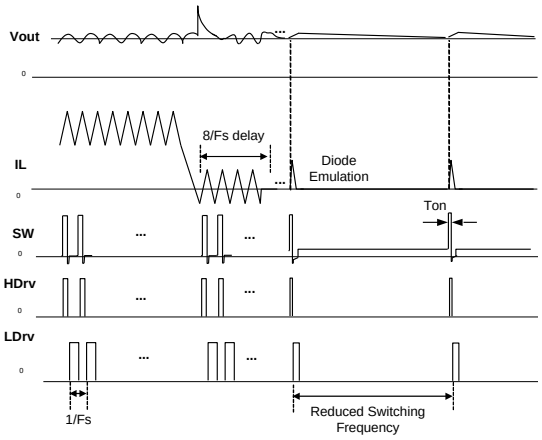


Figure 18: Timing Diagram for Reduced Switching Frequency and Diode Emulation in Light Load Condition (AOT mode)

When the load increases beyond a certain value, the control is switched back to PWM through either of the following two mechanisms:

1) If due to the increase in load, the output voltage drops to 95% of the reference voltage.
2) If Vsense remains below the reference voltage for 3 consecutive inductor current zero-cross events

It is worth mentioning that in AOT mode, when Vsense comes down to reference voltage level, a new pulse in generated only if the inductor current is already zero. If at this time the inductor current (sensed on the Sync-FET) is still positive, the new pulse generation is postponed till the current decays to zero. The second condition mentioned above usually happens when the load is gradually increased.

It should be noted that in tracking mode, AOT operation is disabled and the device can only operate in continuous conduction mode even at light loads.

AOT is disabled during output voltage transitions. It is enabled only after reference voltage finishes its ramp (up or down) and the calibration circuit has sampled and held the new Comp voltage.

In general, AOT operation is more jittery and noisier than FCCM operation, where the switching frequency may vary from cycle to cycle, giving increased Vout ripple and noisier, inconsistent telemetry. Therefore, it is recommended to use FCCM mode of operation as far as possible.

OUTPUT VOLTAGE SENSING, TELEMETRY AND FAULTS

In the IR38265, the voltage sense and regulation circuits are decoupled, enabling ease of testing as well as redundancy. In order to do this, the device uses the sense voltage at the dedicated Vsns pin for output voltage reporting (in 1/64 V resolution, using 2 registers: *output_voltage_msb [2:0]* and *output_voltage_lsb [7:0])* as well as for power good detection and output overvoltage protection.

Power good detection and output overvoltage detection rely on fast analog comparator circuits, whereas overvoltage warnings as well as undervoltage faults and warnings rely on comparing the digitized Vsns to the corresponding thresholds programmed in the MTP. The thresholds are reprogrammable using I2C.

Power Good Output

Power Good is asserted when the output voltage is within the tolerance band of the target voltage set in the register selected by the VIDSELx pins. Following this, the Power Good signal remains asserted irrespective of any output voltage transitions and is de-asserted only in the event of a fault that shuts down power conversion.

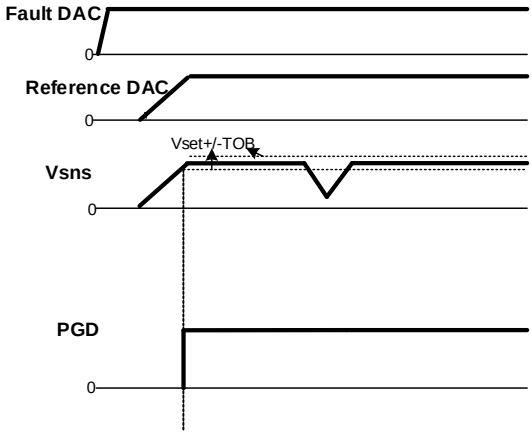


Figure 19: Power Good in PVID mode, Vboot >0 V

Over-Voltage Protection (OVP)

Over-voltage protection is achieved by comparing sense pin voltage Vsns to a configurable overvoltage threshold.

The OVP threshold may be reprogrammed to within 655 mV of the output voltage (for output voltages lower than 2.555V, without any resistive divider on the Fb pin), using I2C. For an OVP threshold programmed to be more than 655 mV greater than the output voltage, the effective OV threshold ceases to be an absolute value and instead tracks the output voltage with a 655 mV offset.

When Vsns exceeds the over voltage threshold, an over voltage trip signal asserts after 200ns (typ.) delay. The default response is that the high side drive signal HDrv is latched off immediately and PGood flags are set low. The low side drive signal is kept on until the Vsns voltage drops below the threshold. HDrv remains latched off until a reset is performed by cycling either Vcc or Enable or the OPERATION command. In addition to the default response

described above, I2C can be used to configure the device such that Vout overvoltage faults are ignored and the converter remains enabled..

Vsns voltage is set by an external resistive voltage divider connected to the output. This divider ratio must match the divider used on the feedback pin or on the RS+ pin.

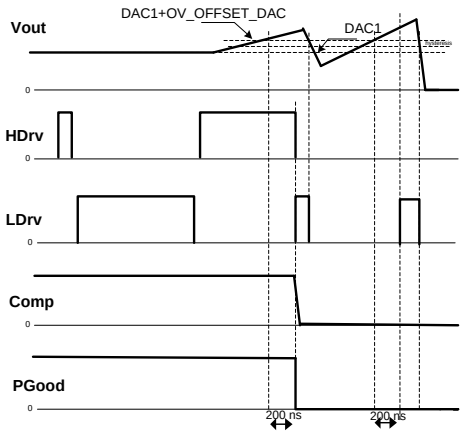


Figure 20: Timing Diagram for OVP in non-tracking mode

MINIMUM ON TIME CONSIDERATIONS

The minimum ON time is the shortest amount of time for Ctrl FET to be reliably turned on. This is a very critical parameter for low duty cycle, high frequency applications. In the conventional approach, when the error amplifier output is near the bottom of the ramp waveform with which it is compared to generate the PWM output, propagation delays can be high enough to cause pulse skipping, and hence limit the minimum pulse width that can be realized. Moreover, in the conventional approach, the bottom of the ramp often presents a high gain region to the error amplifier output, making the modulator more susceptible to noise and requiring the use of lower control loop bandwidth to prevent noise, jitter and pulse skipping.

Infineon has developed a proprietary scheme to improve and enhance the minimum pulse width which minimizes these delays and hence, allows stable operation with pulse-widths as small as 35ns. At the same time, this scheme also has greater noise immunity, thus allowing stable, jitter free operation down to very low pulse widths even with a high control loop bandwidth, thus reducing the required output capacitance.

Any design or application using these devices must ensure operation with a pulse width that is higher than the minimum on-time and at least 50 ns of on-time is recommended in the application. This is necessary for the circuit to operate without jitter and pulse-skipping, which can cause high inductor current ripple and high output voltage ripple.

$$t_{on} = \frac{D}{F_s} = \frac{V_{out}}{PV_{in} \times F_s} \qquad (2)$$

In any application that uses these devices, the following condition must be satisfied:

$$t_{on(\min)} \le t_{on} \quad (3)$$

$$t_{on(\min)} \le \frac{V_{out}}{PV_{in} \times F_s} \quad (4)$$

$$\therefore PV_{in} \times F_s \le \frac{V_{out}}{t_{on(\min)}} \quad (5)$$

The minimum output voltage is limited by the reference voltage and hence $V_{out(min)}$ = 0.5V. Therefore, for $V_{out(min)}$ = 0.5V,

$$\therefore PV_{in} \times F_s \le \frac{V_{out}}{t_{on(\min)}} \quad (6)$$

$$\therefore PV_{in} \times F_s \le \frac{0.5V}{50ns} \le 10\ \text{V/}\mu s$$

Therefore, at the maximum recommended input voltage 16V and minimum output voltage, the converter should be designed at a switching frequency that does not exceed 625 kHz. Conversely, for operation at the maximum recommended operating frequency (1.5 MHz) and minimum output voltage (0.5V), the input voltage (PVin) should not exceed 6.67 V, otherwise pulse skipping may happen.

MAXIMUM DUTY RATIO

An upper limit on the operating duty ratio is imposed by the larger of a) A fixed off time (dominant at high switching frequencies) b) blanking provided by the PWMSet or clock pulse, which has a pulse width that is 1/8 of the switching period. The latter mechanism is dominant at lower switching frequencies (typically below 1.25 MHz). This upper limit ensures that the Sync FET turns on for a long enough duration to allow recharging the bootstrap capacitor and also allows current sensing. Figure 21 shows a plot of the maximum duty ratio vs. the switching frequency with built in input voltage feed forward mechanism.

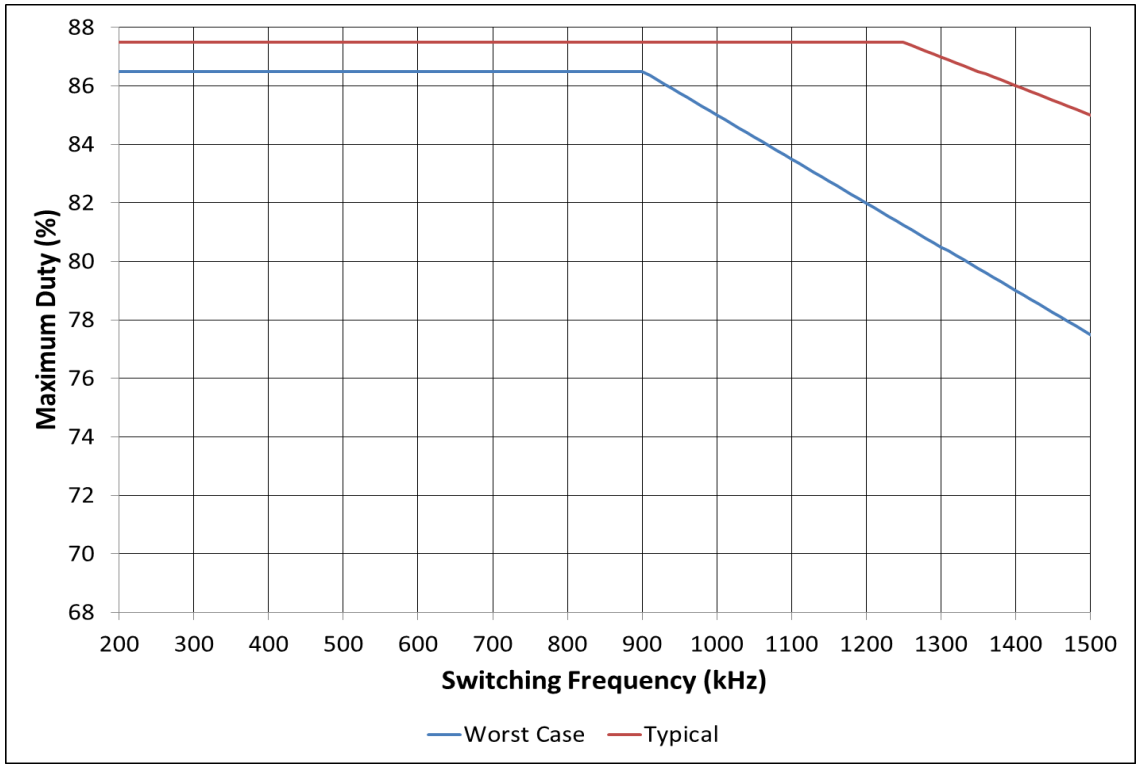


Figure 21: Maximum duty cycle vs. switching frequency

BOOTSTRAP CAPACITOR

To drive the Control FET, it is necessary to supply a gate voltage at least 4V greater than the voltage at the SW pin, which is connected to the source of the Control FET. This is achieved by using a bootstrap configuration, which comprises the internal bootstrap diode and an external bootstrap capacitor (C1). Typically a 0.1uF capacitor is used. A layout placement for a 0 ohm resistor in series with the capacitor is also recommended. For PVin> 14V, a 1 ohm series resistor is required. The operation of the circuit is as follows: When the sync FET is turned on, the capacitor node connected to SW is pulled down to ground. The capacitor charges towards V_{cc} through the internal bootstrap diode (Figure 22), which has a forward voltage drop V_D. The voltage V_c across the bootstrap capacitor C1 is approximately given as:

$$V_c \cong V_{cc} - V_D \qquad (7)$$

When the control FET turns on in the next cycle, the capacitor node connected to SW rises to the bus voltage PVin. However, if the value of C1 is appropriately chosen, the voltage Vc across C1 remains approximately unchanged and the voltage at the Boot pin becomes:

$$V_{Boot} \cong PV_{in} + V_{cc} - V_D \qquad (8)$$

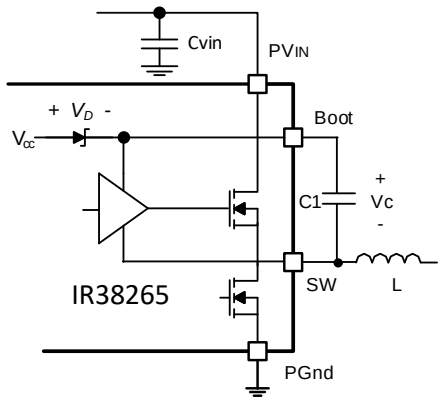


Figure 22: Bootstrap circuit to generate high side drive voltage

LOOP COMPENSATION

Feedback loop compensation is achieved using standard Type III techniques and the compensation values can be easily calculated using Infineon's design tool. The design tool can also be used to predict the control bandwidth and phase margin for the loop for any set of user defined compensation component values. For a theoretical understanding of the calculations used, please refer to Infineon's Application Note AN-1162 "Compensator Design Procedure for Buck Converter with Voltage-Mode Error-Amplifier".

DYNAMIC VID COMPENSATION

This family of devices uses an analog control scheme with voltage mode control. In this scheme, the compensator acts on the Vout signal and not just on the error signal. For load and line transients, with a steady and unchanging reference voltage, this has the same dynamic characteristics as for a compensator that acts on only the error signal. However, for reference voltage changes, as in the case of Dynamic VID, the dynamics are altered. A proprietary dynamic VID compensation scheme allows the dynamic VID response to be tuned optimally to the feedback compensator values. Once properly optimized, the output voltage will follow the DAC more closely during a positive dynamic VID, irrespective of whether the new voltage is commanded by using I2C or by using the 3 VIDSELx pins to select a different register and target voltage. Infineon's design tool will allow the user to quickly and conveniently calculate the dynamic VID compensation parameters for optimal dynamic VID response.

LAYOUT RECOMMENDATIONS

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Make the connections for the power components in the top layer with wide, copper filled areas or polygons. In general, it is desirable to make proper use of power planes and polygons for power distribution and heat dissipation.

The input capacitors, inductor, output capacitors and the device should be as close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place the input capacitor directly at the PVin pin of IR38x6x.

Power vias should be at least 20/10 mil and a good rule of thumb is to design at 2A/via.

The feedback part of the system should be kept away from the inductor and other noise sources.

The critical bypass components such as capacitors for Vin, VCC and 1.8V should be close to their respective pins. It is important to place the feedback components including feedback resistors and compensation components close to Fb and Comp pins.

In a multilayer PCB use one layer as a power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control functions. These two grounds must be connected together on the PC board layout at a single point. It is recommended to place all the compensation parts over the analog ground plane in top layer.

The Power QFN is a thermally enhanced package. Based on thermal performance it is recommended to use at least a 6-layers PCB. To effectively remove heat from the device the exposed pad should be connected to the ground plane using vias.

IR38265 has 3 pins, SCL, SDA and SALERT# that are used for I2C communication. It is recommended that the traces used for these communication lines be at least 10 mils wide with spacing between the SCL and SDA traces that is at least 2-3 times the trace width.

I2C PROTOCOLS

All registers may be accessed using I2C protocols. I2C allows the use of a simple format whereas PMBus provides error checking capability. Figure 23 shows the I2C format employed by IC.

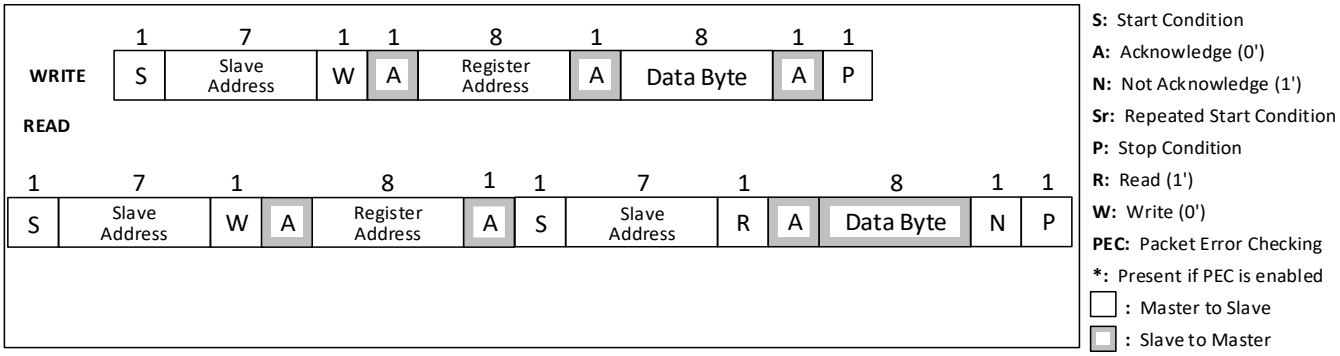
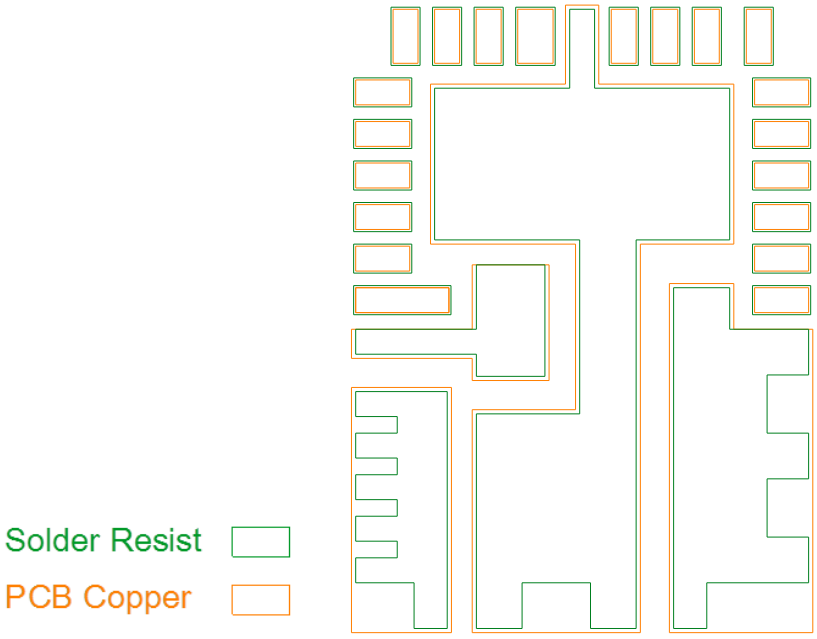
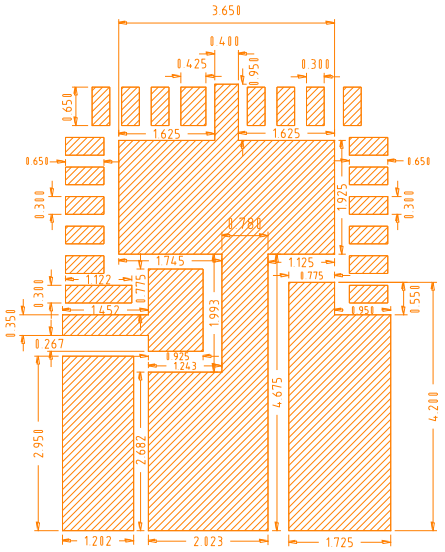


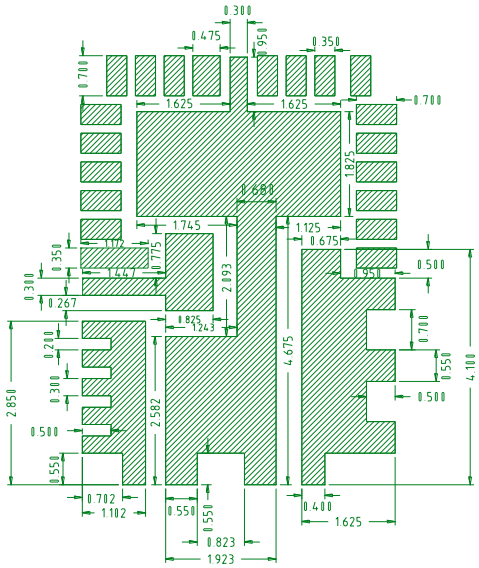
Figure 23: I2C Format

PCB PADS AND COMPONENT

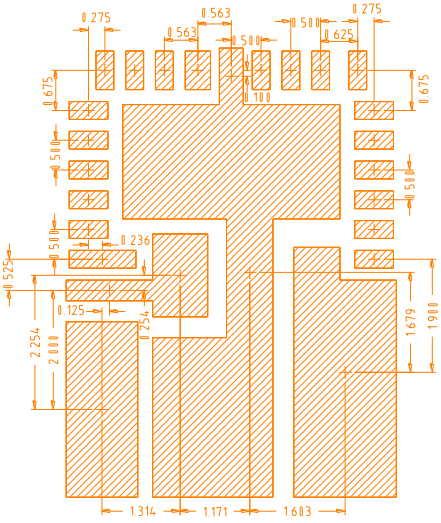


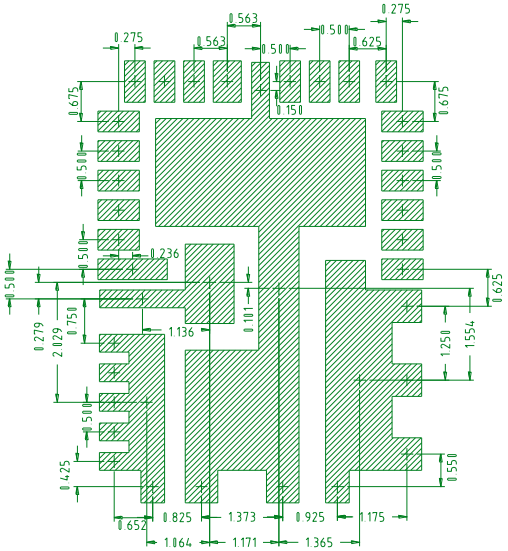
PCB COPPER AND SOLDER RESIST (PAD SIZES)



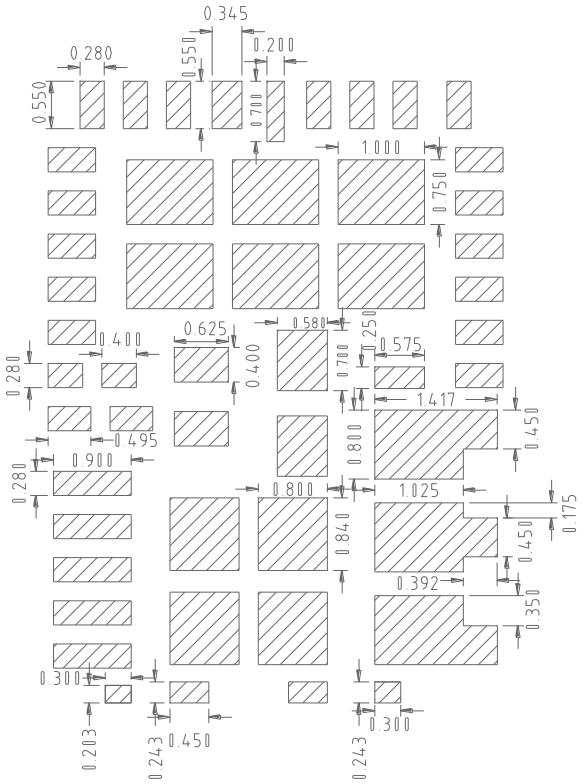


PCB COPPER AND SOLDER RESIST (PAD SPACING)

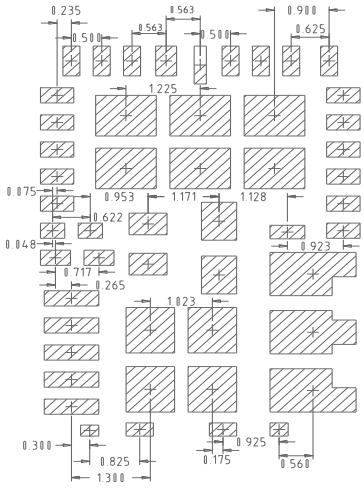


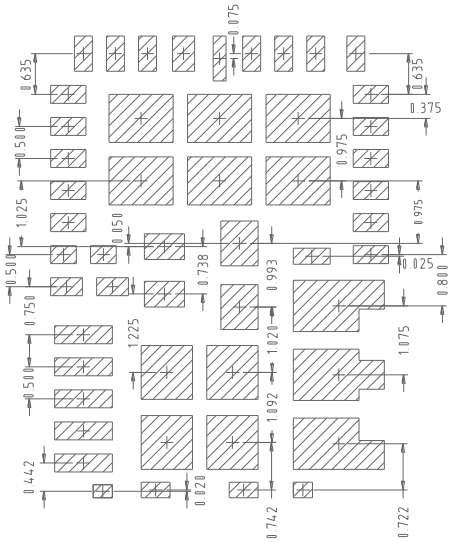


SOLDER PASTE STENCIL (PAD SIZES)

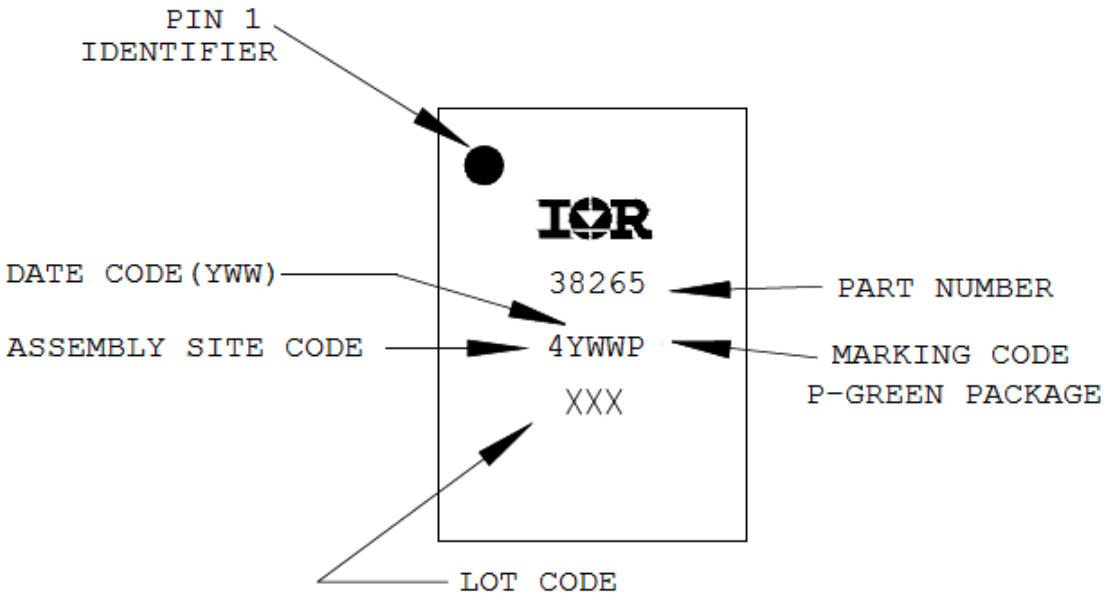


SOLDER PASTE STENCIL (PAD SPACING)

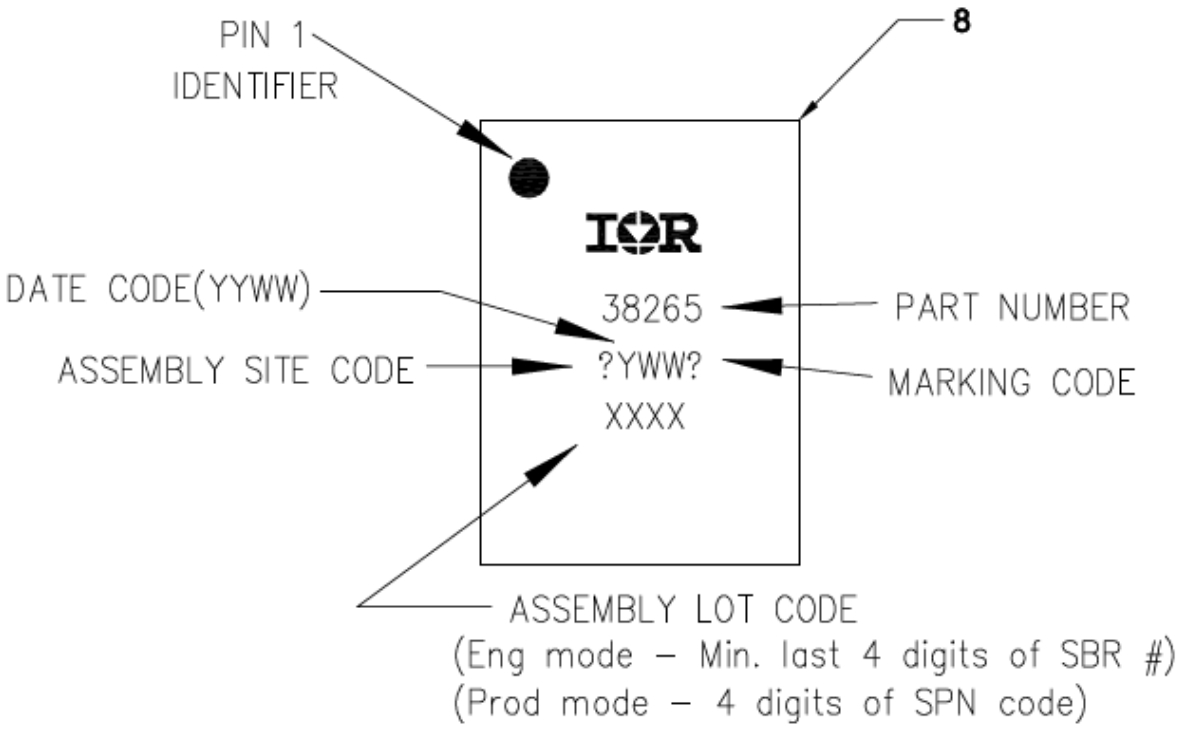




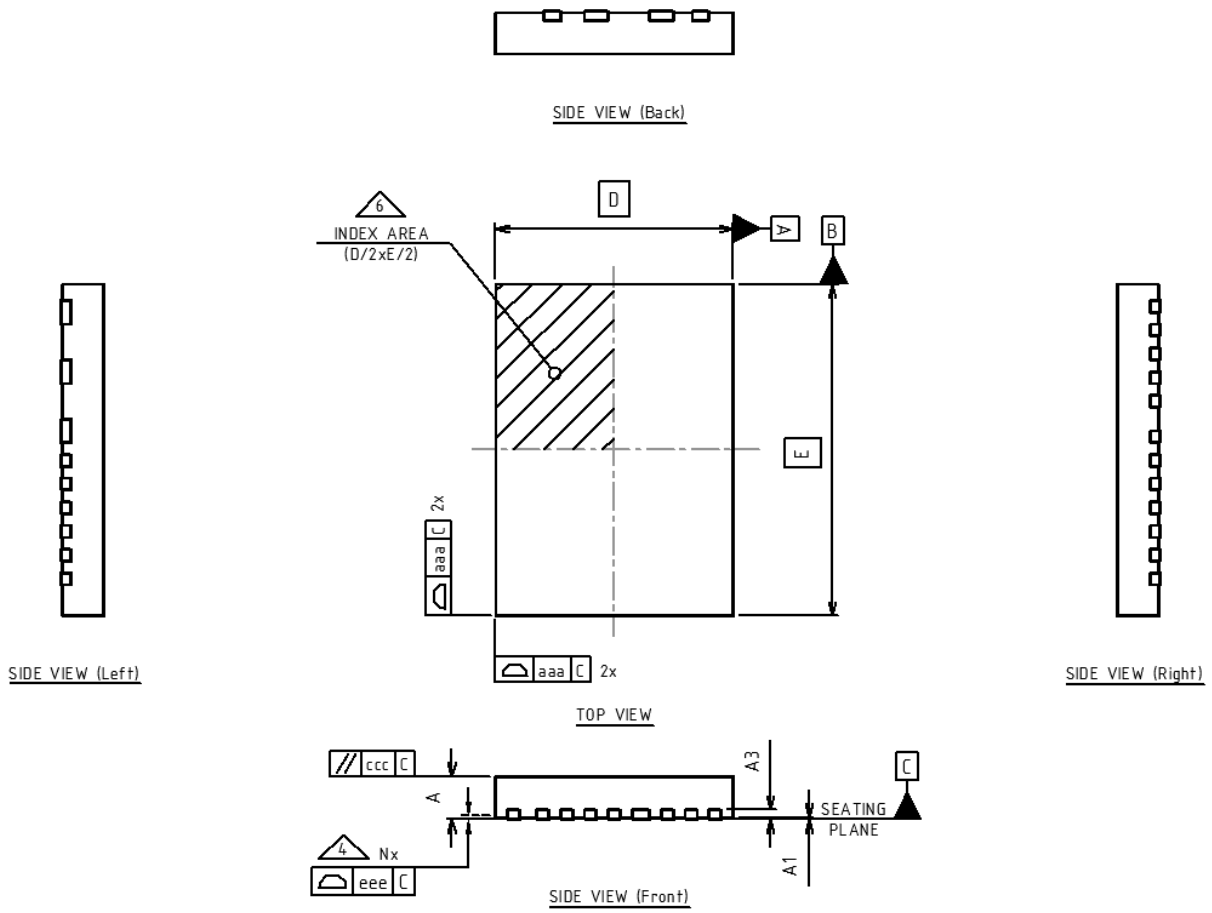
MARKING INFORMATION FOR FINAL PRODUCTION

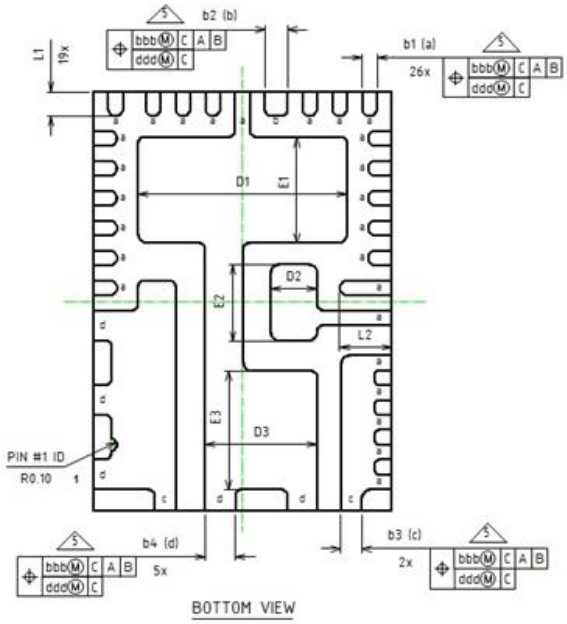


MARKING INFORMATION FOR EARLY PRODUCTION

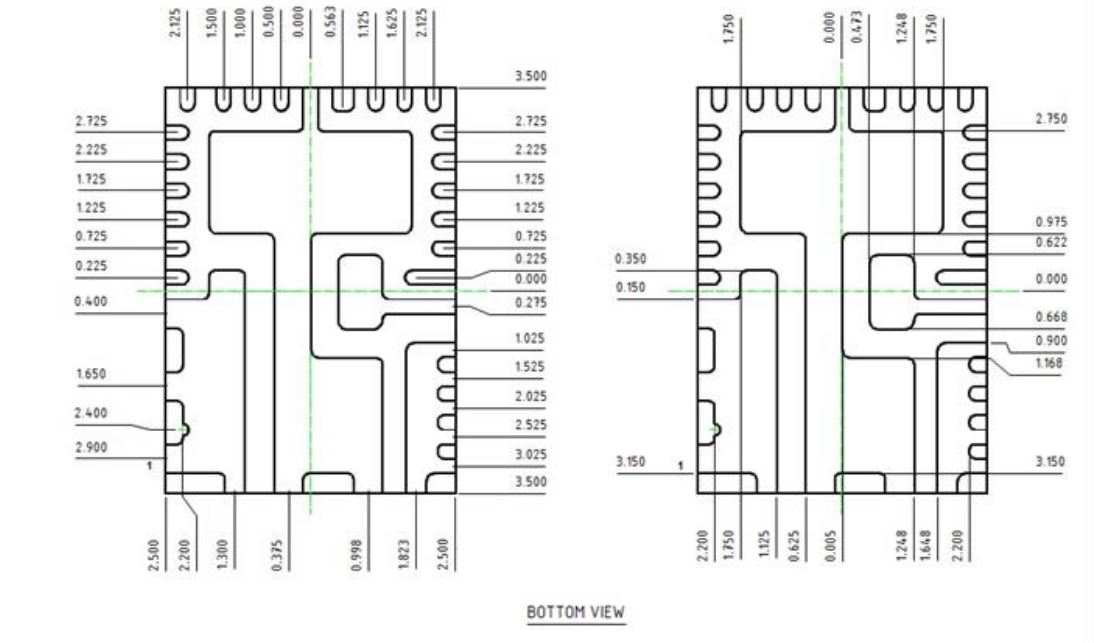


PACKAGE INFORMATION





Dimension Table				
Thickness / Symbol	V			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
A3	---	0.20 Ref	---	
b1	0.20	0.25	0.30	5
b2	0.325	0.375	0.425	5
b3	0.30	0.35	0.40	5
b4	0.45	0.50	0.55	5
D	5.00 BSC			
E	7.00 BSC			
D1	3.35	3.50	3.60	
E1	1.625	1.775	1.875	
D2	0.625	0.775	0.875	
E2	1.14	1.29	1.39	
D3	1.723	1.873	1.973	
E3	1.832	1.982	2.082	
L1	0.30	0.40	0.50	
L2	0.772	0.872	0.972	
aaa	0.05			
bbb	0.10			
ccc	0.10			
ddd	0.05			
eee	0.08			
N	34			3
NOTES	1, 2			
LF PART NO.	443297			



ENVIRONMENTAL QUALIFICATIONS

Qualification Level		Industrial	
Moisture Sensitivity Level		5mm x 7mm PQFN	MSL 2 260C
ESD	Machine Model (JESD22-A115A)	JEDEC Class A	
	Human Body Model (JESD22-A114F)	JEDEC Class 1C	
	Charged Device Model (JESD22-C101F)	JEDEC Class 3	
RoHS Compliant		Yes (with Exemption 7a)	

† Qualification standards can be found at International Rectifier web site: http://www.irf.com

REVISION HISTORY

0.0	12/8/2014	Initial Release			
0.1	12/8/2014	Changed current rating from 20A to 30A			
0.2	4/14/2015	Added packaging info, new POD, PMBus commands, combined IR38263 and IR38265 datasheets			
0.3	3/28/2016	Added SM_ALERT pin info and updated POD to show NC for IR38265 and SALERT for IR38263			
0.4	7/14/2016	Separate ds for IR38263. Added theory of operation. PVin rating=16V Changed from SupIRBuck to OptiMOS™ IPOL brand:RB Changed max duty chart to reflect 200 kHz to 1.5MHz range Changed min time calculation Change IOUT_OC_FAULT_LIMIT range in PMBus table Added Manhattan SVID IDs for IC_DEVICE_ID Added small section on dynamic VID and prefilter (called dynamic vid compensation just like the MP parts) Truncated Vboot table at 0.4V Removed min max spec for Rdson			
1.0	12/9/2016	added OCP curves, OCP spec, typical operating curves, efficiency curves, note discouraging AOT; added note about using a 4.99K pullup.			
1.1	1/13/2017	Changed from Concept to Preliminary			
3.0	3/9/2017	For DR3, added layout guidelines, removed Preliminary and added marking diagrams, added description of layout circuit			
3.1	3/20/2017	changed 1.8V LDO regulation current to 1 mA, updated stencil drawings			
3.2	5/8/2017	Added requirement of 1 ohm series resistor for PVin>14V			
3.3	12/12/2017	Added recommendation to use 10uF bypass capacitor at P1V8 pin. Added note about using a 4.99K resistor for the VIDSEL pins section. Updated OCP and other functionality descriptions.			

3.4	9/6/2018	Updated package marking information on IC. Added thermal derating curves.			

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