MGM13S 是 Silicon Labs 首款适用于 802.15.4 Mesh 和多协议网络的 SiP 模块解决方案，支持 Bluetooth 5.0 LE（包括 2 Mbps, 1 Mbps 和编码 LE PHY）。

基于 EFR32MG13 Mighty Gecko SoC 的 MGM13S 采用 6.5 mm × 6.5 mm 封装尺寸，可提供强大的 RF 性能、低能耗、各种 MCU 外围设备、适用于各个地区和国家的监管测试证书，以及简化的开发体验。结合同样由 Silicon Labs 提供的认证软件堆栈和强大的工具，MGM13S 可以最大程度地减少为产品增加 Zigbee、Thread、Bluetooth 5.0 LE 或多协议连接相关的区域要求、工程工作和开发成本，从而缩短产品上市时间。

MGM13S 面向广泛的应用，包括：
- IoT 多协议端节点设备和网关
- 联网家庭
- 照明
- 健康和保健
- 测量
- 建筑自动化及安全

主要特点
- Zigbee、Thread、BLE 或多协议连接
- 天线或 RF 引脚版本
- TX 功率高达 +18 dBm
- 在 1 Mbps 时, dBm BLE RX 灵敏度为 -94.1
- -101.5 dBm 802.15.4 RX 灵敏度
- 32 位 ARM® Cortex®-M4 内核为 38.4 MHz
- 512/64 kB 闪存/RAM 记忆体
- 强化的安全功能
- 广泛的 MCU 外围设备选择
- 集成直流转换器
- 32 个 GPIO 引脚
- 6.5 mm × 6.5 mm × 1.4 mm
1. 功能列表

MGM13S 重要功能如下所列。

- **支持的协议**
  - Zigbee
  - Thread
  - Bluetooth 5.0 LE
  - 多协议

- **无线片上系统**
  - 2.4 GHz 无线电
  - TX 功率高达 +18 dBm
  - 高性能 32 位 38.4 MHz ARM Cortex®-M4，带有 DSP 指令和浮点运算单元，可高效处理信号
  - 512 kB 闪存程序存储器
  - 64 kB RAM 数据存储器
  - 嵌入追踪宏单元 (ETM)，可实现高级调试
  - 集成直流转换器

- **卓越的接收器性能**
  - 在 250 kbps DSSS-OQPSK 时，具备 -101.5 dBm 灵敏度 (1% PER)
  - 在 125 kbit/s GFSK 时，具备 -102.1 dBm 灵敏度 (0.1% BER)
  - 在 500 kbit/s GFSK 时，具备 -97.9 dBm 灵敏度 (0.1% BER)
  - 在 1 Mbit/s GFSK 时，具备 -90.2 dBm 灵敏度 (0.1% BER)

- **低能耗**
  - 在 250 kbps O-QPSK DSSS 时，RX 电流为 10.4 mA
  - 在 1 Mbps GFSK 时，RX 电流为 9.7 mA
  - 在 0 dBm 输出功率下，TX 电流为 8.9 mA
  - 在活动模式 (EM0) 下，运行功耗为 69 μA/MHz
  - 在 EM2 深度睡眠模式下 (保留 64 kB RAM，RTCC 从 LFXO 中运行) 下，电流为 1.4 μA
  - 在 EM2 深度睡眠模式下 (保留 16 kB RAM，RTCC 从 LFRCO 中运行) 下，电流为 1.3 μA
  - 无线模块唤醒，带有信号强度检测、前导模式检测、帧检测和超时
  - 监控认证
    - FCC
    - CE
    - IC/ISEDIC
    - MIC/Telec

- **运行范围宽**
  - 1.8 V 至 3.8 V 单电源
  - -40 °C 至 +85 °C

- **尺寸**
  - 6.5 mm × 6.5 mm × 1.4 mm

- **互联网安全支持**
  -通用 CRC
  - 真随机数生成器 (TRNG)
  - 2 倍硬件加密加速，支持 AES 128/256、SHA-1、SHA-2（SHA-224 和 SHA-256）以及 ECC

- **广泛的 MCU 外围设备选择**
  - 12 位 1 Msps SAR 模拟数字转换器 (ADC)
  - 2 个模拟比较器 (ACMP)
  - 2 个数字模拟电压转换器 (VDAC)
  - 3 个运算放大器 (Opamp)
  - 数字模拟电流转换器 (IDAC)
  - 低功耗传感器接口 (LESENSE)
  - 多通道电容式感应接口 (CSEN)
  - 32 个连接至模拟信道 (APORT) 的引脚，可供多个模拟外围设备共用
  - 32 个通用 I/O 引脚，带有输出状态保留和异步中断功能
  - 8 信道 DMA 控制器
  - 12 信道外围设备反射系统 (PRS)
  - 2 个 16 位定时器/计数器
  - 3 个或 4 个比较/捕获/PWM 通道
  - 1 个 32 位定时器/计数器
  - 3 个比较/捕获/PWM 通道
  - 32 位实时计数器和日历
  - 16 位低能耗定时器，用于生成波形
  - 32 位超低能耗定时器/计数器，可从任何能源模式定期唤醒
  - 16 位可异步运行的脉冲计数器
  - 2 个看门狗定时器
  - 3 个通用同步/异步接收器/发射器（UART/SPI/智能卡 (ISO 7816)/IrDA/FS）
  - 低能耗 UART (LEUART™)
  - 2 个 I²C 接口，带有 SMBus 支持和 E3 停止模式下的地址识别功能
## 2. Ordering Information

### Table 2.1. Ordering Information

<table>
<thead>
<tr>
<th>Ordering Code</th>
<th>Protocol Stack</th>
<th>Max TX Power</th>
<th>Antenna</th>
<th>Flash (kB)</th>
<th>RAM (kB)</th>
<th>GPIO</th>
<th>Packaging</th>
</tr>
</thead>
<tbody>
<tr>
<td>MGM13S12F512GA-V2</td>
<td>Bluetooth LE, Zigbee, Thread</td>
<td>18 dBm</td>
<td>Built-in</td>
<td>512</td>
<td>64</td>
<td>32</td>
<td>Cut Tape</td>
</tr>
<tr>
<td>MGM13S12F512GA-V2R</td>
<td>Bluetooth LE, Zigbee, Thread</td>
<td>18 dBm</td>
<td>Built-in</td>
<td>512</td>
<td>64</td>
<td>32</td>
<td>Reel</td>
</tr>
<tr>
<td>MGM13S12F512GN-V2</td>
<td>Bluetooth LE, Zigbee, Thread</td>
<td>18 dBm</td>
<td>RF pin</td>
<td>512</td>
<td>64</td>
<td>32</td>
<td>Cut Tape</td>
</tr>
<tr>
<td>MGM13S12F512GN-V2R</td>
<td>Bluetooth LE, Zigbee, Thread</td>
<td>18 dBm</td>
<td>RF pin</td>
<td>512</td>
<td>64</td>
<td>32</td>
<td>Reel</td>
</tr>
<tr>
<td>MGM13S02F512GA-V2</td>
<td>Bluetooth LE, Zigbee, Thread</td>
<td>10 dBm</td>
<td>Built-in</td>
<td>512</td>
<td>64</td>
<td>32</td>
<td>Cut Tape</td>
</tr>
<tr>
<td>MGM13S02F512GA-V2R</td>
<td>Bluetooth LE, Zigbee, Thread</td>
<td>10 dBm</td>
<td>Built-in</td>
<td>512</td>
<td>64</td>
<td>32</td>
<td>Reel</td>
</tr>
<tr>
<td>MGM13S02F512GN-V2</td>
<td>Bluetooth LE, Zigbee, Thread</td>
<td>10 dBm</td>
<td>RF pin</td>
<td>512</td>
<td>64</td>
<td>32</td>
<td>Cut Tape</td>
</tr>
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<td>RF pin</td>
<td>512</td>
<td>64</td>
<td>32</td>
<td>Reel</td>
</tr>
</tbody>
</table>

End-product manufacturers must verify that the module is configured to meet regulatory limits for each region in accordance with the formal certification test reports.

Devices are not pre-programmed with a firmware image.
# Table of Contents

1. Feature List .......................................................... 2

2. Ordering Information .................................................. 3

3. System Overview ....................................................... 7
   3.1 Introduction ......................................................... 7
   3.2 Radio ................................................................. 7
      3.2.1 Antenna Interface ........................................... 7
      3.2.2 RFSENSE ...................................................... 8
      3.2.3 Packet and State Trace ..................................... 8
      3.2.4 Random Number Generator .................................. 8
   3.3 Power ............................................................... 9
      3.3.1 Energy Management Unit (EMU) .......................... 10
      3.3.2 DC-DC Converter ............................................ 10
      3.3.3 Power Domains .............................................. 10
   3.4 General Purpose Input/Output (GPIO) ........................... 10
   3.5 Clocking ............................................................ 10
      3.5.1 Clock Management Unit (CMU) .......................... 10
      3.5.2 Internal Oscillators and Crystal ....................... 11
   3.6 Counters/Timers and PWM ....................................... 11
      3.6.1 Timer/Counter (TIMER) ..................................... 11
      3.6.2 Wide Timer/Counter (WTIMER) .......................... 11
      3.6.3 Real Time Counter and Calendar (RTCC) .................... 11
      3.6.4 Low Energy Timer (LETIMER) ........................... 11
      3.6.5 Ultra Low Power Wake-up Timer (CRYOTIMER) .......... 11
      3.6.6 Pulse Counter (PCNT) ...................................... 11
      3.6.7 Watchdog Timer (WDOG) ................................... 12
   3.7 Communications and Other Digital Peripherals ................ 12
      3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) .......... 12
      3.7.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART) ............ 12
      3.7.3 Inter-Integrated Circuit Interface (I\textsuperscript{2}C) ...................... 12
      3.7.4 Peripheral Reflex System (PRS) .......................... 12
      3.7.5 Low Energy Sensor Interface (LESENSE) .................. 12
   3.8 Security Features .................................................. 12
      3.8.1 GPCR (General Purpose Cyclic Redundancy Check) .......... 12
      3.8.2 Crypto Accelerator (CRYPTO) ............................ 13
      3.8.3 True Random Number Generator (TRNG) .................. 13
      3.8.4 Security Management Unit (SMU) ........................ 13
   3.9 Analog ............................................................. 13
      3.9.1 Analog Port (APORT) ....................................... 13
      3.9.2 Analog Comparator (ACMP) ................................ 13
      3.9.3 Analog to Digital Converter (ADC) ........................ 13
      3.9.4 Capacitive Sense (CSEN) .................................. 13
      3.9.5 Digital to Analog Current Converter (IDAC) .............. 14
3.9.6 Digital to Analog Converter (VDAC) ........................................... 14
3.9.7 Operational Amplifiers .......................................................... 14
3.10 Reset Management Unit (RMU) .................................................. 14
3.11 Core and Memory ........................................................................ 14
  3.11.1 Processor Core ....................................................................... 14
  3.11.2 Memory System Controller (MSC) ......................................... 14
  3.11.3 Linked Direct Memory Access Controller (LDMA) ...................... 14
3.12 Memory Map ................................................................................ 15
3.13 Configuration Summary .............................................................. 16

4. Electrical Specifications ................................................................. 17
  4.1 Electrical Characteristics ............................................................ 17
    4.1.1 Absolute Maximum Ratings ............................................... 18
    4.1.2 Operating Conditions .......................................................... 19
    4.1.3 DC-DC Converter ............................................................... 20
    4.1.4 Current Consumption ........................................................ 22
    4.1.5 Wake Up Times ................................................................... 28
    4.1.6 Brown Out Detector (BOD) ................................................. 28
    4.1.7 Frequency Synthesizer ......................................................... 29
    4.1.8 2.4 GHz RF Transceiver Characteristics ............................. 30
    4.1.9 Oscillators .......................................................................... 41
    4.1.10 Flash Memory Characteristics .......................................... 44
    4.1.11 General-Purpose I/O (GPIO) ............................................. 45
    4.1.12 Voltage Monitor (VMON) ................................................... 46
    4.1.13 Analog to Digital Converter (ADC) .................................... 47
    4.1.14 Analog Comparator (ACMP) .............................................. 49
    4.1.15 Digital to Analog Converter (VDAC) .................................. 52
    4.1.16 Current Digital to Analog Converter (IDAC) ......................... 55
    4.1.17 Capacitive Sense (CSEN) ................................................... 57
    4.1.18 Operational Amplifier (OPAMP) ........................................ 59
    4.1.19 Pulse Counter (PCNT) ....................................................... 62
    4.1.20 Analog Port (APORT) ....................................................... 62
    4.1.21 I2C ................................................................................. 63
    4.1.22 USART SPI ...................................................................... 66

5. Typical Connection Diagrams ......................................................... 68
  5.1 Typical MGM13S Connections .................................................... 68

6. Layout Guidelines ............................................................................ 70
  6.1 Layout Guidelines ....................................................................... 70
  6.2 Effect of PCB Width .................................................................... 71
  6.3 Effect of Plastic and Metal Materials ........................................... 72
  6.4 Effects of Human Body ................................................................ 72
  6.5 2D Radiation Pattern Plots .......................................................... 73

7. Pin Definitions .................................................................................. 75
  7.1 MGM13S Device Pinout ............................................................. 75
7.2  GPIO Functionality Table .............................................. .77
7.3  Alternate Functionality Overview ...................................... .89
7.4  Analog Port (APORT) Client Maps ................................... .101

8.  Package Specifications .................................................. 110
   8.1 MGM13S Package Dimensions ....................................... .110
   8.2 MGM13S Recommended PCB Land Pattern .......................... .113
   8.3 MGM13S Package Marking ............................................. .117

9.  Soldering Recommendations ............................................ 118
   9.1 Soldering Recommendations .......................................... .118

10. Certifications ............................................................ 119
   10.1 Qualified Antenna Types ............................................. .119
   10.2 Bluetooth ............................................................... .119
   10.3 CE ....................................................................... .119
   10.4 FCC .................................................................... .120
   10.5 ISED Canada .......................................................... .121
   10.6 Japan ................................................................. .123

11. Revision History .......................................................... 124
3. System Overview

3.1 Introduction

The MGM13S product family combines an energy-friendly MCU with a highly integrated radio transceiver and a high performance, ultra-robust antenna. The devices are well suited for any battery operated application, as well as other systems where ultra-small size, reliable high performance RF, low-power consumption and easy application development are key requirements. This section gives a short introduction to the full radio and MCU system.

A detailed block diagram of the MGM13S module is shown in the figure below.

![MGM13S Block Diagram](image)

**Figure 3.1. MGM13S Block Diagram**

3.2 Radio

The Mighty Gecko family features a highly configurable radio transceiver supporting a wide range of wireless protocols.

3.2.1 Antenna Interface

The MGM13S has two antenna solution variants. One of them is a high-performance integrated chip antenna (MGM13SxxFxxxxA) and the other is a 50 Ohm matched RF pin to attach an external antenna to the module (MGM13SxxFxxxxN).

<table>
<thead>
<tr>
<th>Table 3.1. Antenna Efficiency and Peak Gain</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Parameter</strong></td>
</tr>
<tr>
<td>Efficiency</td>
</tr>
<tr>
<td>Peak gain</td>
</tr>
</tbody>
</table>

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3.2.2 RFSENSE

The RFSENSE block generates a system wakeup interrupt upon detection of wideband RF energy at the antenna interface, providing true RF wakeup capabilities from low energy modes including EM2, EM3 and EM4.

RFSENSE triggers on a relatively strong RF signal and is available in the lowest energy modes, allowing exceptionally low energy consumption. RFSENSE does not demodulate or otherwise qualify the received signal, but software may respond to the wakeup event by enabling normal RF reception.

Various strategies for optimizing power consumption and system response time in presence of false alarms may be employed using available timer peripherals.

3.2.3 Packet and State Trace

The MGM13S Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

• Non-intrusive trace of transmit data, receive data and state information
• Data observability on a single-pin UART data output, or on a two-pin SPI data output
• Configurable data output bitrate / baudrate
• Multiplexed transmitted data, received data and state / meta information in a single serial data stream

3.2.4 Random Number Generator

The Frame Controller (FRC) implements a random number generator that uses entropy gathered from noise in the RF receive chain. The data is suitable for use in cryptographic applications.

Output from the random number generator can be used either directly or as a seed or entropy source for software-based random number generator algorithms such as Fortuna.
3.3 Power

The MGM13S has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An integrated DC-DC buck regulator is utilized to further reduce the current consumption. Figure 3.2 Power Supply Configuration for MGM13S02xxx Devices on page 9 and Figure 3.3 Power Supply Configuration for MGM13S12xxx Devices on page 9 show how the external and internal supplies of the module are connected for different part numbers.

Figure 3.2. Power Supply Configuration for MGM13S02xxx Devices

Figure 3.3. Power Supply Configuration for MGM13S12xxx Devices
3.3.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the dc-dc regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.3.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3. Patented RF noise mitigation allows operation of the DC-DC converter without degrading sensitivity of radio components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.3.3 Power Domains

The MGM13S has two peripheral power domains for operation in EM2 and EM3. If all of the peripherals in a peripheral power domain are configured as unused, the power domain for that group will be powered off in the low-power mode, reducing the overall current consumption of the device.

### Table 3.2. Peripheral Power Subdomains

<table>
<thead>
<tr>
<th>Peripheral Power Domain 1</th>
<th>Peripheral Power Domain 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACMP0</td>
<td>ACMP1</td>
</tr>
<tr>
<td>PCNT0</td>
<td>CSEN</td>
</tr>
<tr>
<td>ADC0</td>
<td>VDAC0</td>
</tr>
<tr>
<td>LETIMER0</td>
<td>LEUART0</td>
</tr>
<tr>
<td>LESENSE</td>
<td>I2C0</td>
</tr>
<tr>
<td>APORT</td>
<td>I2C1</td>
</tr>
<tr>
<td>-</td>
<td>IDAC</td>
</tr>
</tbody>
</table>

3.4 General Purpose Input/Output (GPIO)

MGM13S has up to 32 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.5 Clocking

3.5.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the MGM13S. Individual enabling and disabling of clocks to all peripherals is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.
3.5.2 Internal Oscillators and Crystal

The MGM13S fully integrates two crystal oscillators, four RC oscillators, and a 38.4 MHz crystal.

- The high-frequency crystal oscillator (HFXO) and integrated 38.4 MHz crystal provide a precise timing reference for the MCU and radio.
- The low-frequency crystal oscillator (LFXO) provides an accurate timing reference for low energy modes and the real-time-clock circuits.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range.
- An integrated auxiliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire Viewer port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) for low power operation where high accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.6 Counters/Timers and PWM

3.6.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.6.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER_0 only.

3.6.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. When receiving frames, the RTCC value can be used for timestamping. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

A secondary RTC is used by the RF protocol stack for event scheduling, leaving the primary RTCC block available exclusively for application software.

3.6.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.6.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.
3.6.6 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The peripheral may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.6.7 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.7 Communications and Other Digital Peripherals

3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O interface. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I^2S

3.7.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUARTTM provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.7.3 Inter-Integrated Circuit Interface (I^2C)

The I^2C interface enables communication between the MCU and a serial I^2C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C peripheral allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.7.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripherals without software involvement. Peripherals producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals, which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.7.5 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSETM is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

3.8 Security Features

3.8.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC block implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.
3.8.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. EFR32 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO1 block is tightly linked to the Radio Buffer Controller (BUFC) enabling fast and efficient autonomous cipher operations on data buffer content. It allows fast processing of GCM (AES), ECC and SHA with little CPU intervention.

CRYPTO also provides trigger signals for DMA read and write operations.

3.8.3 True Random Number Generator (TRNG)

The TRNG is a non-deterministic random number generator based on a full hardware solution. The TRNG is validated with NIST800-22 and AIS-31 test suites as well as being suitable for FIPS 140-2 certification (for the purposes of cryptographic key generation).

3.8.4 Security Management Unit (SMU)

The Security Management Unit (SMU) allows software to set up fine-grained security for peripheral access, which is not possible in the Memory Protection Unit (MPU). Peripherals may be secured by hardware on an individual basis, such that only privileged accesses to the peripheral's register interface will be allowed. When an access fault occurs, the SMU reports the specific peripheral involved and can optionally generate an interrupt.

3.9 Analog

3.9.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog peripherals on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.9.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.9.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.9.4 Capacitive Sense (CSEN)

The CSEN peripheral is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such as switches and sliders. The CSEN peripheral uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The peripheral can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.
3.9.5 Digital to Analog Current Converter (IDAC)

The IDAC can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05 µA and 64 µA with several ranges consisting of various step sizes.

3.9.6 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per single-ended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.9.7 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC peripheral or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

3.10 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the MGM13S. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.11 Core and Memory

3.11.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

• ARM Cortex-M4 RISC processor achieving 1.25 Dhrystone MIPS/MHz
• Memory Protection Unit (MPU) supporting up to 8 memory segments
• Up to 512 kB flash program memory
• Up to 64 kB RAM data memory
• Configuration and event handling of all peripherals
• 2-pin Serial-Wire debug interface

3.11.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.11.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.
3.12 Memory Map

The MGM13S memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

![Memory Map Diagram]

Figure 3.4. MGM13S Memory Map — Core Peripherals and Code Space
3.13 Configuration Summary

Many peripherals on the MGM13S are available in multiple instances. However, certain USART, TIMER and WTIMER instances implement only a subset of the full features for that peripheral type. The table below describes the specific features available on these peripheral instances. All remaining peripherals support full configuration.

### Table 3.3. Configuration Summary

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Configuration</th>
<th>Pin Connections</th>
</tr>
</thead>
<tbody>
<tr>
<td>USART0</td>
<td>IrDA SmartCard</td>
<td>US0_TX, US0_RX, US0_CLK, US0_CS</td>
</tr>
<tr>
<td>USART1</td>
<td>IrDA I²S SmartCard</td>
<td>US1_TX, US1_RX, US1_CLK, US1_CS</td>
</tr>
<tr>
<td>TIMER0</td>
<td>with DTI</td>
<td>TIM0_CC[2:0], TIM0_CDTI[2:0]</td>
</tr>
<tr>
<td>TIMER1</td>
<td>-</td>
<td>TIM1_CC[3:0]</td>
</tr>
<tr>
<td>WTIMER0</td>
<td>with DTI</td>
<td>WTIM0_CC[2:0], WTIM0_CDTI[2:0]</td>
</tr>
</tbody>
</table>
4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on $T_{\text{AMB}}=25{}^\circ\text{C}$ and $V_{DD}=3.3\text{ V}$, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a $50\ \Omega$ antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

The MGM13S module is powered primarily from the VBATT supply pin. GPIO are powered from the IOVDD supply pin. There are also several internal supply rails mentioned in the electrical specifications, whose connections vary based on transmit power configuration. Refer to 3.3 Power for the relationship between the module’s external supply pins and the internal voltage supply rails.

Refer to for more details about operational supply and temperature limits.
### 4.1.1 Absolute Maximum Ratings

Stress levels beyond those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions beyond those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at [http://www.silabs.com/support/quality/pages/default.aspx](http://www.silabs.com/support/quality/pages/default.aspx).

#### Table 4.1. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage temperature range</td>
<td>$T_{STG}$</td>
<td></td>
<td>-40</td>
<td></td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td>Voltage on any supply pin</td>
<td>$V_{DDMAX}$</td>
<td></td>
<td>-0.3</td>
<td></td>
<td>3.8</td>
<td>V</td>
</tr>
<tr>
<td>Voltage ramp rate on any supply pin</td>
<td>$V_{DDRAMP MAX}$</td>
<td></td>
<td></td>
<td></td>
<td>1 V / µs</td>
<td></td>
</tr>
<tr>
<td>DC voltage on any GPIO pin</td>
<td>$V_{DIGPIN}$</td>
<td>5V tolerant GPIO pins(^1)(^2)(^3)</td>
<td>-0.3</td>
<td></td>
<td>Min of 5.25 and IOVDD +2</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Standard GPIO pins</td>
<td>-0.3</td>
<td></td>
<td>IOVDD+0.3</td>
<td>V</td>
</tr>
<tr>
<td>Maximum RF level at input</td>
<td>$P_{RFMAX2G4}$</td>
<td></td>
<td></td>
<td></td>
<td>10</td>
<td>dBm</td>
</tr>
<tr>
<td>Total current into supply pins</td>
<td>$I_{VDDMAX}$</td>
<td>Source</td>
<td></td>
<td></td>
<td>200</td>
<td>mA</td>
</tr>
<tr>
<td>Total current into VSS ground lines</td>
<td>$I_{VSSMAX}$</td>
<td>Sink</td>
<td></td>
<td></td>
<td>200</td>
<td>mA</td>
</tr>
<tr>
<td>Current per I/O pin</td>
<td>$I_{IOMAX}$</td>
<td>Sink</td>
<td></td>
<td></td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Source</td>
<td></td>
<td></td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td>Current for all I/O pins</td>
<td>$I_{IOALLMAX}$</td>
<td>Sink</td>
<td></td>
<td></td>
<td>200</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Source</td>
<td></td>
<td></td>
<td>200</td>
<td>mA</td>
</tr>
<tr>
<td>Junction temperature</td>
<td>$T_J$</td>
<td></td>
<td>-40</td>
<td></td>
<td>105</td>
<td>°C</td>
</tr>
</tbody>
</table>

**Note:**

1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = IOVDD.
2. Valid for IOVDD in valid operating range or when IOVDD is undriven (high-Z). If IOVDD is connected to a low-impedance source below the valid operating range (e.g. IOVDD shorted to VSS), the pin voltage maximum is IOVDD + 0.3 V, to avoid exceeding the maximum IO current specifications.
3. To operate above the IOVDD supply rail, over-voltage tolerance must be enabled according to the GPIO_Px_OVTDIS register. Pins with over-voltage tolerance disabled have the same limits as Standard GPIO.
4.1.2 Operating Conditions

The following subsections define the operating conditions for the module.

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating ambient temperature range</td>
<td>$T_A$</td>
<td>-G temperature grade</td>
<td>-40</td>
<td>25</td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td>VBATT operating supply voltage$^1$</td>
<td>$V_{VBATT}$</td>
<td>DCDC in regulation</td>
<td>2.4</td>
<td>3.3</td>
<td>3.8</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCDC in bypass 50mA load</td>
<td>1.8</td>
<td>3.3</td>
<td>3.8</td>
<td>V</td>
</tr>
<tr>
<td>VBATT current</td>
<td>$I_{VBATT}$</td>
<td>DCDC in bypass, $T \leq 85 , ^\circ C$</td>
<td>—</td>
<td>—</td>
<td>200</td>
<td>mA</td>
</tr>
<tr>
<td>HFCORECLK frequency</td>
<td>$f_{CORE}$</td>
<td>VSCALE2, MODE = WS1</td>
<td>—</td>
<td>—</td>
<td>40</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VSCALE0, MODE = WS0</td>
<td>—</td>
<td>—</td>
<td>20</td>
<td>MHz</td>
</tr>
<tr>
<td>HFCLK frequency</td>
<td>$f_{HFCLK}$</td>
<td>VSCALE2</td>
<td>—</td>
<td>—</td>
<td>40</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VSCALE0</td>
<td>—</td>
<td>—</td>
<td>20</td>
<td>MHz</td>
</tr>
</tbody>
</table>

Note:
1. The minimum voltage required in bypass mode is calculated using $R_{BYP}$ from the DCDC specification table. Requirements for other loads can be calculated as $V_{VBATT\_min} + I_{LOAD} \times R_{BYP\_max}$. 

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Electrical Specifications

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4.1.3 DC-DC Converter

Test conditions: $V_{\text{DCDC}_I}=3.3\ V$, $V_{\text{DCDC}_O}=1.8\ V$, $I_{\text{DCDC}_{\text{LOAD}}}=50\ mA$, Heavy Drive configuration, $F_{\text{DCDC}_{\text{LN}}}=7\ MHz$, unless otherwise indicated.

**Table 4.3. DC-DC Converter**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>$V_{\text{DCDC}_I}$</td>
<td>Bypass mode, $I_{\text{DCDC}_{\text{LOAD}}} = 50\ mA$</td>
<td>1.8</td>
<td>—</td>
<td>$V_{\text{VREGVDD}_\text{MAX}}$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low noise (LN) mode, 1.8 V output, $I_{\text{DCDC}_{\text{LOAD}}} = 100\ mA$, or</td>
<td>2.4</td>
<td>—</td>
<td>$V_{\text{VREGVDD}_\text{MAX}}$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low power (LP) mode, 1.8 V output, $I_{\text{DCDC}_{\text{LOAD}}} = 10\ mA$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output voltage programmable range$^1$</td>
<td>$V_{\text{DCDC}_O}$</td>
<td></td>
<td>1.8</td>
<td>—</td>
<td>$V_{\text{VREGVDD}}$</td>
<td>V</td>
</tr>
<tr>
<td>Regulation DC accuracy</td>
<td>$\text{ACC}_{\text{DC}}$</td>
<td>Low Noise (LN) mode, 1.8 V target output</td>
<td>1.7</td>
<td>—</td>
<td>1.9</td>
<td>V</td>
</tr>
<tr>
<td>Regulation window$^2$</td>
<td>$\text{WIN}_{\text{REG}}$</td>
<td>Low Power (LP) mode, LPCMPBIASEMxx$^3 = 0$, 1.8 V target output, $I_{\text{DCDC}_{\text{LOAD}}} \leq 75\ \mu\text{A}$</td>
<td>1.63</td>
<td>—</td>
<td>2.2</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low Power (LP) mode, LPCMPBIASEMxx$^3 = 3$, 1.8 V target output, $I_{\text{DCDC}_{\text{LOAD}}} \leq 10\ mA$</td>
<td>1.63</td>
<td>—</td>
<td>2.1</td>
<td>V</td>
</tr>
<tr>
<td>Steady-state output ripple</td>
<td>$V_R$</td>
<td>Radio disabled</td>
<td>—</td>
<td>3</td>
<td>—</td>
<td>mVpp</td>
</tr>
<tr>
<td>Output voltage under/overshoot</td>
<td>$V_{\text{OV}}$</td>
<td>CCM Mode ($\text{LNFORCECCM}^3 = 1$), Load changes between 0 mA and 100 mA</td>
<td>—</td>
<td>25</td>
<td>60</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCM Mode ($\text{LNFORCECCM}^3 = 0$), Load changes between 0 mA and 10 mA</td>
<td>—</td>
<td>45</td>
<td>90</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Overshoot during LP to LN CCM/DCM mode transitions compared to DC level in LN mode</td>
<td>—</td>
<td>200</td>
<td>—</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Undershoot during BYP/LP to LN CCM ($\text{LNFORCECCM}^3 = 1$) mode transitions compared to DC level in LN mode</td>
<td>—</td>
<td>40</td>
<td>—</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Undershoot during BYP/LP to LN DCM ($\text{LNFORCECCM}^3 = 0$) mode transitions compared to DC level in LN mode</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>mV</td>
</tr>
<tr>
<td>DC line regulation</td>
<td>$V_{\text{REG}}$</td>
<td>Input changes between $V_{\text{VREGVDD}_\text{MAX}}$ and 2.4 V</td>
<td>—</td>
<td>0.1</td>
<td>—</td>
<td>%</td>
</tr>
<tr>
<td>DC load regulation</td>
<td>$I_{\text{REG}}$</td>
<td>Load changes between 0 mA and 100 mA in CCM mode</td>
<td>—</td>
<td>0.1</td>
<td>—</td>
<td>%</td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Test Condition</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Unit</td>
</tr>
<tr>
<td>--------------------</td>
<td>------------</td>
<td>-----------------------------------------------------</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>------</td>
</tr>
<tr>
<td>Max load current</td>
<td>$I_{LOAD_MAX}$</td>
<td>Low noise (LN) mode, Medium or Heavy Drive(^4)</td>
<td></td>
<td></td>
<td>80</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low noise (LN) mode, Light Drive(^4)</td>
<td></td>
<td></td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low power (LP) mode, LPCMPBIASEM(x)^3 = 0</td>
<td></td>
<td></td>
<td>75</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low power (LP) mode, LPCMPBIASEM(x)^3 = 3</td>
<td></td>
<td></td>
<td>10</td>
<td>mA</td>
</tr>
</tbody>
</table>

**Note:**

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, $V_{VREGVDD}$.
2. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits.
3. LPCMPBIASEM\(x\) refers to either LPCMPBIASEM234H in the EMU_DCDCMISCCTRL register or LPCMPBIASEM01 in the EMU_DCDCLOEM01CFG register, depending on the energy mode.
4. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.
4.1.4 Current Consumption

4.1.4.1 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VBATT = 3.3 V. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T = 25 °C.

### Table 4.4. Current Consumption 3.3 V using DC-DC Converter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise DCM mode</td>
<td>$I_{\text{ACTIVE_DCM}}$</td>
<td>38.4 MHz crystal, CPU running while loop from flash</td>
<td>—</td>
<td>87</td>
<td>—</td>
<td>µA/MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>38 MHz HFRCO, CPU running Prime from flash</td>
<td>—</td>
<td>69</td>
<td>—</td>
<td>µA/MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>38 MHz HFRCO, CPU running while loop from flash</td>
<td>—</td>
<td>70</td>
<td>—</td>
<td>µA/MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>38 MHz HFRCO, CPU running CoreMark from flash</td>
<td>—</td>
<td>82</td>
<td>—</td>
<td>µA/MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>26 MHz HFRCO, CPU running while loop from flash</td>
<td>—</td>
<td>76</td>
<td>—</td>
<td>µA/MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 MHz HFRCO, CPU running while loop from flash</td>
<td>—</td>
<td>615</td>
<td>—</td>
<td>µA/MHz</td>
</tr>
<tr>
<td>Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise CCM mode</td>
<td>$I_{\text{ACTIVE_CCM}}$</td>
<td>38.4 MHz crystal, CPU running while loop from flash</td>
<td>—</td>
<td>97</td>
<td>—</td>
<td>µA/MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>38 MHz HFRCO, CPU running Prime from flash</td>
<td>—</td>
<td>80</td>
<td>—</td>
<td>µA/MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>38 MHz HFRCO, CPU running while loop from flash</td>
<td>—</td>
<td>81</td>
<td>—</td>
<td>µA/MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>38 MHz HFRCO, CPU running CoreMark from flash</td>
<td>—</td>
<td>92</td>
<td>—</td>
<td>µA/MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>26 MHz HFRCO, CPU running while loop from flash</td>
<td>—</td>
<td>94</td>
<td>—</td>
<td>µA/MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 MHz HFRCO, CPU running while loop from flash</td>
<td>—</td>
<td>1145</td>
<td>—</td>
<td>µA/MHz</td>
</tr>
<tr>
<td>Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode</td>
<td>$I_{\text{ACTIVE_CCM_VS}}$</td>
<td>19 MHz HFRCO, CPU running while loop from flash</td>
<td>—</td>
<td>101</td>
<td>—</td>
<td>µA/MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 MHz HFRCO, CPU running while loop from flash</td>
<td>—</td>
<td>1124</td>
<td>—</td>
<td>µA/MHz</td>
</tr>
<tr>
<td>Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode</td>
<td>$I_{\text{EM1_DCM}}$</td>
<td>38.4 MHz crystal</td>
<td>—</td>
<td>56</td>
<td>—</td>
<td>µA/MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>38 MHz HFRCO</td>
<td>—</td>
<td>39</td>
<td>—</td>
<td>µA/MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>26 MHz HFRCO</td>
<td>—</td>
<td>46</td>
<td>—</td>
<td>µA/MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 MHz HFRCO</td>
<td>—</td>
<td>588</td>
<td>—</td>
<td>µA/MHz</td>
</tr>
<tr>
<td>Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise DCM mode</td>
<td>$I_{\text{EM1_DCM_VS}}$</td>
<td>19 MHz HFRCO</td>
<td>—</td>
<td>50</td>
<td>—</td>
<td>µA/MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 MHz HFRCO</td>
<td>—</td>
<td>572</td>
<td>—</td>
<td>µA/MHz</td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Test Condition</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Unit</td>
</tr>
<tr>
<td>---------------------------------------------------------------------------</td>
<td>----------</td>
<td>---------------------------------------------------------------------------------</td>
<td>-----</td>
<td>------</td>
<td>------</td>
<td>------</td>
</tr>
<tr>
<td>Current consumption in EM2 mode, with voltage scaling enabled, DCDC in LP mode</td>
<td>IEM2_VS</td>
<td>Full 64 kB RAM retention and RTCC running from LFXO</td>
<td></td>
<td>1.4</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Full 64 kB RAM retention and RTCC running from LFRCO</td>
<td></td>
<td>1.5</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 bank RAM retention and RTCC running from LFRCO&lt;sup&gt;5&lt;/sup&gt;</td>
<td></td>
<td>1.3</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Current consumption in EM3 mode, with voltage scaling enabled</td>
<td>IEM3_VS</td>
<td>Full 64 kB RAM retention and CRYOTIMER running from ULFRCO</td>
<td></td>
<td>1.14</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Current consumption in EM4H mode, with voltage scaling enabled</td>
<td>IEM4H_VS</td>
<td>128 byte RAM retention, RTCC running from LFXO</td>
<td></td>
<td>0.75</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>128 byte RAM retention, CRYOTIMER running from ULFRCO</td>
<td></td>
<td>0.44</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>128 byte RAM retention, no RTCC</td>
<td></td>
<td>0.42</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Current consumption in EM4S mode</td>
<td>IEM4S</td>
<td>No RAM retention, no RTCC</td>
<td></td>
<td>0.07</td>
<td></td>
<td>µA</td>
</tr>
</tbody>
</table>

**Note:**

1. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD.
2. CMU_HFXOCTRL_LOWPOWER=0.
3. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD.
4. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPCMPBIASEM234H=0, LPCLIMILIM-SEL=1, ANASW=DVDD.
5. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1
4.1.4.2 Current Consumption 1.8 V (DC-DC Converter in Bypass Mode)

Unless otherwise indicated, typical conditions are: VBATT = 1.8 V, T = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T = 25 °C.

Table 4.5. Current Consumption 1.8 V (DC-DC Converter in Bypass Mode)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current consumption in EM0 mode with all peripherals disabled</td>
<td>( I_{ACTIVE} )</td>
<td>38.4 MHz crystal, CPU running while loop from flash(^1)</td>
<td>—</td>
<td>128</td>
<td>—</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>38 MHz HFRCO, CPU running Prime from flash</td>
<td>—</td>
<td>97</td>
<td>—</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>38 MHz HFRCO, CPU running while loop from flash</td>
<td>—</td>
<td>98</td>
<td>—</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>38 MHz HFRCO, CPU running CoreMark from flash</td>
<td>—</td>
<td>119</td>
<td>—</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>26 MHz HFRCO, CPU running while loop from flash</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 MHz HFRCO, CPU running while loop from flash</td>
<td>—</td>
<td>243</td>
<td>—</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td>Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled</td>
<td>( I_{ACTIVE_VS} )</td>
<td>19 MHz HFRCO, CPU running while loop from flash</td>
<td>—</td>
<td>86</td>
<td>—</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 MHz HFRCO, CPU running while loop from flash</td>
<td>—</td>
<td>206</td>
<td>—</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td>Current consumption in EM1 mode with all peripherals disabled</td>
<td>( I_{EM1} )</td>
<td>38.4 MHz crystal(^1)</td>
<td>—</td>
<td>76</td>
<td>—</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>38 MHz HFRCO</td>
<td>—</td>
<td>47</td>
<td>—</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>26 MHz HFRCO</td>
<td>—</td>
<td>48</td>
<td>—</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 MHz HFRCO</td>
<td>—</td>
<td>191</td>
<td>—</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td>Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled</td>
<td>( I_{EM1_VS} )</td>
<td>19 MHz HFRCO</td>
<td>—</td>
<td>43</td>
<td>—</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 MHz HFRCO</td>
<td>—</td>
<td>163</td>
<td>—</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td>Current consumption in EM2 mode, with voltage scaling enabled</td>
<td>( I_{EM2_VS} )</td>
<td>Full 64 kB RAM retention and RTCC running from LFXO</td>
<td>—</td>
<td>1.8</td>
<td>—</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Full 64 kB RAM retention and RTCC running from LFRCO</td>
<td>—</td>
<td>2.0</td>
<td>—</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 bank (16 kB) RAM retention and RTCC running from LFRCO</td>
<td>—</td>
<td>1.6</td>
<td>—</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Current consumption in EM3 mode, with voltage scaling enabled</td>
<td>( I_{EM3_VS} )</td>
<td>Full 64 kB RAM retention and CRYOTIMER running from ULFRCO</td>
<td>—</td>
<td>1.43</td>
<td>—</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Current consumption in EM4H mode, with voltage scaling enabled</td>
<td>( I_{EM4H_VS} )</td>
<td>128 byte RAM retention, RTCC running from LFXO</td>
<td>—</td>
<td>0.83</td>
<td>—</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>128 byte RAM retention, CRYOTIMER running from ULFRCO</td>
<td>—</td>
<td>0.37</td>
<td>—</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>128 byte RAM retention, no RTCC</td>
<td>—</td>
<td>0.36</td>
<td>—</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Current consumption in EM4S mode</td>
<td>( I_{EM4S} )</td>
<td>no RAM retention, no RTCC</td>
<td>—</td>
<td>0.05</td>
<td>—</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Test Condition</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Unit</td>
</tr>
<tr>
<td>----------</td>
<td>--------</td>
<td>----------------</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>------</td>
</tr>
</tbody>
</table>

**Note:**
1. CMU_HFXOCTRL_LOWPOWER=0.
2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1
4.1.4.3 Current Consumption 3.3 V (DC-DC Converter in Bypass Mode)

Unless otherwise indicated, typical conditions are: VBATT = 3.3 V, T = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T = 25 °C.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current consumption in EM0 mode with all peripherals disabled</td>
<td>( I_{ACTIVE} )</td>
<td>38.4 MHz crystal, CPU running while loop from flash</td>
<td>—</td>
<td>128</td>
<td>—</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>38 MHz HFRCO, CPU running Prime from flash</td>
<td>—</td>
<td>97</td>
<td>—</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>38 MHz HFRCO, CPU running while loop from flash</td>
<td>—</td>
<td>98</td>
<td>107</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>38 MHz HFRCO, CPU running CoreMark from flash</td>
<td>—</td>
<td>119</td>
<td>—</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>26 MHz HFRCO, CPU running while loop from flash</td>
<td>—</td>
<td>100</td>
<td>109</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 MHz HFRCO, CPU running while loop from flash</td>
<td>—</td>
<td>246</td>
<td>430</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td>Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled</td>
<td>( I_{ACTIVE_{VS}} )</td>
<td>19 MHz HFRCO, CPU running while loop from flash</td>
<td>—</td>
<td>86</td>
<td>—</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 MHz HFRCO, CPU running while loop from flash</td>
<td>—</td>
<td>209</td>
<td>—</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td>Current consumption in EM1 mode with all peripherals disabled</td>
<td>( I_{EM1} )</td>
<td>38.4 MHz crystal</td>
<td>—</td>
<td>76</td>
<td>—</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>38 MHz HFRCO</td>
<td>—</td>
<td>47</td>
<td>51</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>26 MHz HFRCO</td>
<td>—</td>
<td>49</td>
<td>55</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 MHz HFRCO</td>
<td>—</td>
<td>195</td>
<td>374</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td>Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled</td>
<td>( I_{EM1_{VS}} )</td>
<td>19 MHz HFRCO</td>
<td>—</td>
<td>43</td>
<td>—</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 MHz HFRCO</td>
<td>—</td>
<td>167</td>
<td>—</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td>Current consumption in EM2 mode, with voltage scaling enabled</td>
<td>( I_{EM2_{VS}} )</td>
<td>Full 64 kB RAM retention and RTCC running from LFXO</td>
<td>—</td>
<td>1.9</td>
<td>—</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Full 64 kB RAM retention and RTCC running from LFRCO</td>
<td>—</td>
<td>2.2</td>
<td>—</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 bank (16 kB) RAM retention and RTCC running from LFRCO</td>
<td>—</td>
<td>1.9</td>
<td>3.3</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Current consumption in EM3 mode, with voltage scaling enabled</td>
<td>( I_{EM3_{VS}} )</td>
<td>Full 64 kB RAM retention and CRYOTIMER running from ULFRCO</td>
<td>—</td>
<td>1.53</td>
<td>3.0</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Current consumption in EM4H mode, with voltage scaling enabled</td>
<td>( I_{EM4H_{VS}} )</td>
<td>128 byte RAM retention, RTCC running from LFXO</td>
<td>—</td>
<td>0.93</td>
<td>—</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>128 byte RAM retention, CRYOTIMER running from ULFRCO</td>
<td>—</td>
<td>0.45</td>
<td>—</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>128 byte RAM retention, no RTCC</td>
<td>—</td>
<td>0.44</td>
<td>0.9</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Current consumption in EM4S mode</td>
<td>( I_{EM4S} )</td>
<td>No RAM retention, no RTCC</td>
<td>—</td>
<td>0.04</td>
<td>0.18</td>
<td>( \mu A )</td>
</tr>
</tbody>
</table>
4.1.4.4 Current Consumption Using Radio

Unless otherwise indicated, typical conditions are: \( VBATT = 3.3 \) V, \( T = 25 \) °C. DC-DC on. Minimum and maximum values in this table represent the worst conditions across process variation at \( T = 25 \) °C.

### Table 4.7. Current Consumption Using Radio

<table>
<thead>
<tr>
<th>Parameter Description</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current consumption in receive mode, active packet reception (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), ( T \leq 85 ) °C</td>
<td>( I_{RX_ACTIVE} )</td>
<td>125 kbit/s, 2GFSK, ( F = 2.4 ) GHz, Radio clock prescaled by 4</td>
<td></td>
<td>9.4</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500 kbit/s, 2GFSK, ( F = 2.4 ) GHz, Radio clock prescaled by 4</td>
<td></td>
<td>9.4</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Mbit/s, 2GFSK, ( F = 2.4 ) GHz, Radio clock prescaled by 4</td>
<td></td>
<td>9.7</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2 Mbit/s, 2GFSK, ( F = 2.4 ) GHz, Radio clock prescaled by 4</td>
<td></td>
<td>10.5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>802.15.4 receiving frame, ( F = 2.4 ) GHz, Radio clock prescaled by 3</td>
<td></td>
<td>10.4</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Current consumption in receive mode, listening for packet (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), ( T \leq 85 ) °C</td>
<td>( I_{RX_LISTEN} )</td>
<td>125 kbit/s, 2GFSK, ( F = 2.4 ) GHz, No radio clock prescaling</td>
<td></td>
<td>10.4</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500 kbit/s, 2GFSK, ( F = 2.4 ) GHz, No radio clock prescaling</td>
<td></td>
<td>10.4</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Mbit/s, 2GFSK, ( F = 2.4 ) GHz, No radio clock prescaling</td>
<td></td>
<td>10.7</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2 Mbit/s, 2GFSK, ( F = 2.4 ) GHz, No radio clock prescaling</td>
<td></td>
<td>11.5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>802.15.4, ( F = 2.4 ) GHz, No radio clock prescaling</td>
<td></td>
<td>12.0</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Current consumption in transmit mode (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), ( T \leq 85 ) °C</td>
<td>( I_{TX} )</td>
<td>( F = 2.4 ) GHz, CW, 0 dBm output power, Radio clock prescaled by 3</td>
<td></td>
<td>8.9</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( F = 2.4 ) GHz, CW, 0 dBm output power, Radio clock prescaled by 1</td>
<td></td>
<td>9.7</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( F = 2.4 ) GHz, CW, 10 dBm output power</td>
<td></td>
<td>34.7</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( F = 2.4 ) GHz, CW, 18 dBm output power, PAVDD connected directly to external 3.3V supply</td>
<td></td>
<td>122.7</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

**Note:**
1. \( \text{CMU\_HFXOCTRL\_LOWPOWER} = 0 \).
2. \( \text{CMU\_LFRCOCTRL\_ENVREF} = 1, \text{CMU\_LFRCOCTRL\_VREFUPDATE} = 1 \).
### 4.1.5 Wake Up Times

#### Table 4.8. Wake Up Times

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wake up time from EM1</td>
<td>$t_{\text{EM1_WU}}$</td>
<td></td>
<td></td>
<td>3</td>
<td></td>
<td>AHB Clocks</td>
</tr>
<tr>
<td>Wake up from EM2</td>
<td>$t_{\text{EM2_WU}}$</td>
<td>Code execution from flash</td>
<td></td>
<td>10.9</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Code execution from RAM</td>
<td></td>
<td>3.8</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Wake up from EM3</td>
<td>$t_{\text{EM3_WU}}$</td>
<td>Code execution from flash</td>
<td></td>
<td>10.9</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Code execution from RAM</td>
<td></td>
<td>3.8</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Wake up from EM4H$^1$</td>
<td>$t_{\text{EM4H_WU}}$</td>
<td>Executing from flash</td>
<td></td>
<td>90</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Wake up from EM4S$^1$</td>
<td>$t_{\text{EM4S_WU}}$</td>
<td>Executing from flash</td>
<td></td>
<td>300</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Time from release of reset source to first instruction execution</td>
<td>$t_{\text{RESET}}$</td>
<td>Soft Pin Reset released</td>
<td></td>
<td>51</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Any other reset released</td>
<td></td>
<td>358</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Power mode scaling time</td>
<td>$t_{\text{SCALE}}$</td>
<td>VSacle0 to VSacle2, HFCLK = 19 MHz$^3$</td>
<td></td>
<td>31.8</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VSacle2 to VSacle0, HFCLK = 19 MHz$^4$</td>
<td></td>
<td>4.3</td>
<td></td>
<td>µs</td>
</tr>
</tbody>
</table>

**Note:**
1. Time from wake up request until first instruction is executed. Wakeup results in device reset.
2. Scaling up from VSacle0 to VSacle2 requires approximately 30.3 µs + 28 HFCLKs.
3. VSacle0 to VSacle2 voltage change transitions occur at a rate of 10 mV/µs for approximately 20 µs. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 µF capacitor) to 70 mA (with a 2.7 µF capacitor).
4. Scaling down from VSacle2 to VSacle0 requires approximately 2.8 µs + 29 HFCLKs.

### 4.1.6 Brown Out Detector (BOD)

#### Table 4.9. Brown Out Detector (BOD)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVDD BOD threshold</td>
<td>$V_{\text{AVDDBOD}}$</td>
<td>AVDD rising</td>
<td></td>
<td>1.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AVDD falling (EM0/EM1)</td>
<td>1.62</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AVDD falling (EM2/EM3)</td>
<td>1.53</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>AVDD BOD hysteresis</td>
<td>$V_{\text{AVDDBOD_HYST}}$</td>
<td></td>
<td>20</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>AVDD BOD response time</td>
<td>$t_{\text{AVDDBOD_DELAY}}$</td>
<td>Supply drops at 0.1V/µs rate</td>
<td>2.4</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>EM4 BOD threshold</td>
<td>$V_{\text{EM4DBOD}}$</td>
<td>AVDD rising</td>
<td></td>
<td>1.7</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AVDD falling</td>
<td>1.45</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>EM4 BOD hysteresis</td>
<td>$V_{\text{EM4BOD_HYST}}$</td>
<td></td>
<td>25</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>EM4 BOD response time</td>
<td>$t_{\text{EM4BOD_DELAY}}$</td>
<td>Supply drops at 0.1V/µs rate</td>
<td>300</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
</tbody>
</table>
### 4.1.7 Frequency Synthesizer

#### Table 4.10. Frequency Synthesizer

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF synthesizer frequency range</td>
<td>f(_{\text{RANGE}})</td>
<td>2400 - 2483.5 MHz</td>
<td>2400</td>
<td>—</td>
<td>2483.5 MHz</td>
<td>MHz</td>
</tr>
<tr>
<td>LO tuning frequency resolution with 38.4 MHz crystal</td>
<td>f(_{\text{RES}})</td>
<td>2400 - 2483.5 MHz</td>
<td>—</td>
<td>—</td>
<td>73 Hz</td>
<td>Hz</td>
</tr>
<tr>
<td>Frequency deviation resolution with 38.4 MHz crystal</td>
<td>df(_{\text{RES}})</td>
<td>2400 - 2483.5 MHz</td>
<td>—</td>
<td>—</td>
<td>73 Hz</td>
<td>Hz</td>
</tr>
<tr>
<td>Maximum frequency deviation with 38.4 MHz crystal</td>
<td>df(_{\text{MAX}})</td>
<td>2400 - 2483.5 MHz</td>
<td>—</td>
<td>—</td>
<td>1677 kHz</td>
<td>kHz</td>
</tr>
</tbody>
</table>
4.1.8 2.4 GHz RF Transceiver Characteristics

4.1.8.1 RF Transmitter General Characteristics for 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VBATT = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.11. RF Transmitter General Characteristics for 2.4 GHz Band

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum TX power¹</td>
<td>POUTMAX</td>
<td>18 dBm-rated part numbers.</td>
<td>—</td>
<td>17.9</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10 dBm-rated part numbers</td>
<td>—</td>
<td>10.7</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td>Minimum active TX Power</td>
<td>POUTMIN</td>
<td>CW</td>
<td>-30</td>
<td>—</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td>Output power step size</td>
<td>POUTSTEP</td>
<td>-5 dBm&lt; Output power &lt; 0 dBm</td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 dBm&lt; output power &lt; POUTMAX</td>
<td>—</td>
<td>0.5</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Output power variation vs supply at POUTMAX</td>
<td>POUTVAR_V</td>
<td>1.8 V &lt; V&lt;sub&gt;VREGVDD&lt;/sub&gt; &lt; 3.3 V, PAVDD connected directly to external supply, for output power &gt; 10 dBm.</td>
<td>—</td>
<td>4.5</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.8 V &lt; V&lt;sub&gt;VREGVDD&lt;/sub&gt; &lt; 3.3 V, PAVDD connected directly to external supply, for output power = 10 dBm.</td>
<td>—</td>
<td>3.6</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.8 V &lt; V&lt;sub&gt;VREGVDD&lt;/sub&gt; &lt; 3.3 V using DC-DC converter</td>
<td>—</td>
<td>2.1</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Output power variation vs temperature at POUTMAX</td>
<td>POUTVAR_T</td>
<td>From -40 to +85 °C, PAVDD connected to DC-DC output</td>
<td>—</td>
<td>1.7</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>From -40 to +85 °C, PAVDD connected to external supply</td>
<td>—</td>
<td>1.7</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Output power variation vs RF frequency at POUTMAX</td>
<td>POUTVAR_F</td>
<td>Over RF tuning frequency range, PAVDD connected to external supply</td>
<td>—</td>
<td>0.3</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>RF tuning frequency range</td>
<td>FRANGE</td>
<td></td>
<td>2400</td>
<td>—</td>
<td>2483.5</td>
<td>MHz</td>
</tr>
</tbody>
</table>

Note:
1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.
### 4.1.8.2 RF Receiver General Characteristics for 2.4 GHz Band

Unless otherwise indicated, typical conditions are: \( T = 25 \, ^\circ\text{C} \), \( \text{VBATT} = 3.3 \, \text{V} \). DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

#### Table 4.12. RF Receiver General Characteristics for 2.4 GHz Band

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF tuning frequency range</td>
<td>( F_{\text{RANGE}} )</td>
<td></td>
<td>2400</td>
<td>—</td>
<td>2483.5</td>
<td>MHz</td>
</tr>
<tr>
<td>Receive mode maximum spurious emission</td>
<td>( \text{SPUR}_{\text{RX}} )</td>
<td>30 MHz to 1 GHz</td>
<td>—</td>
<td>-57</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 GHz to 12 GHz</td>
<td>—</td>
<td>-47</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td>Max spurious emissions during active receive mode, per FCC Part 15.109(a)</td>
<td>( \text{SPUR}_{\text{RX,FCC}} )</td>
<td>216 MHz to 960 MHz, Conducted Measurement</td>
<td>—</td>
<td>-55.2</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Above 960 MHz, Conducted Measurement</td>
<td>—</td>
<td>-47.2</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td>Level above which RFSENSE will trigger(^1)</td>
<td>( \text{RFSENSE}_{\text{TRIG}} )</td>
<td>CW at 2.45 GHz</td>
<td>—</td>
<td>-24</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td>Level below which RFSENSE will not trigger(^1)</td>
<td>( \text{RFSENSE}_{\text{THRES}} )</td>
<td>CW at 2.45 GHz</td>
<td>—</td>
<td>-50</td>
<td>—</td>
<td>dBm</td>
</tr>
</tbody>
</table>

**Note:**

1. RFSENSE performance is only valid from 0 to 85 \(^\circ\text{C}\). RFSENSE should be disabled outside this temperature range.
### 4.1.8.3 RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: \( T = 25 \, ^\circ \text{C}, \) \( \text{VBATT} = 3.3 \, \text{V}. \) DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

#### Table 4.13. RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max usable receiver input level, 1% PER</td>
<td>SAT</td>
<td>Signal is reference signal. Packet length is 20 octets.</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td>Sensitivity, 1% PER</td>
<td>SENS</td>
<td>Signal is reference signal. Packet length is 20 octets. Using DC-DC converter.</td>
<td>—</td>
<td>-101.5</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td>Co-channel interferer rejection, 1% PER</td>
<td>CCR</td>
<td>Desired signal 3 dB above sensitivity limit</td>
<td>—</td>
<td>-4.7</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>High-side adjacent channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level(^2)</td>
<td>ACR(_P1)</td>
<td>Interferer is reference signal at +1 channel-spacing.</td>
<td>—</td>
<td>40.2</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Interferer is filtered reference signal(^3) at +1 channel-spacing.</td>
<td>—</td>
<td>49.7</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Interferer is CW at +1 channel-spacing(^4).</td>
<td>—</td>
<td>55.6</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Low-side adjacent channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level(^2)</td>
<td>ACR(_M1)</td>
<td>Interferer is reference signal at -1 channel-spacing.</td>
<td>—</td>
<td>40.7</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Interferer is filtered reference signal(^3) at -1 channel-spacing.</td>
<td>—</td>
<td>49.3</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Interferer is CW at -1 channel-spacing.</td>
<td>—</td>
<td>57.9</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Alternate channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level(^2)</td>
<td>ACR(_2)</td>
<td>Interferer is reference signal at ±2 channel-spacing</td>
<td>—</td>
<td>52.0</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Interferer is filtered reference signal(^3) at ±2 channel-spacing</td>
<td>—</td>
<td>55.1</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Interferer is CW at ±2 channel-spacing</td>
<td>—</td>
<td>64.5</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Image rejection , 1% PER. Desired is reference signal at 3dB above reference sensitivity level(^2)</td>
<td>IR</td>
<td>Interferer is CW in image band(^4)</td>
<td>—</td>
<td>51.4</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Blocking rejection of all other channels. 1% PER. Desired is reference signal at 3dB above reference sensitivity level(^2). Interferer is reference signal</td>
<td>BLOCK</td>
<td>Interferer frequency &lt; Desired frequency - 3 channel-spacing</td>
<td>—</td>
<td>56.6</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Interferer frequency &gt; Desired frequency + 3 channel-spacing</td>
<td>—</td>
<td>57.8</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Blocking rejection of 802.11g signal centered at +12MHz or -13MHz(^5)</td>
<td>BLOCK(_{80211G})</td>
<td>Desired is reference signal at 6dB above reference sensitivity level(^2)</td>
<td>—</td>
<td>46.8</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Upper limit of input power range over which RSSI resolution is maintained</td>
<td>RSSI(_{\text{MAX}})</td>
<td>—</td>
<td>—</td>
<td>5</td>
<td>dBm</td>
<td></td>
</tr>
</tbody>
</table>
### Parameter Symbols and Test Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lower limit of input power range over which RSSI resolution is maintained</td>
<td>RSSMIN</td>
<td></td>
<td>-98</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>RSSI resolution</td>
<td>RSSRES</td>
<td>over RSSIMIN to RSSIMAX</td>
<td></td>
<td>0.3</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>RSSI accuracy in the linear region as defined by 802.15.4-2003</td>
<td>RSSLIN</td>
<td></td>
<td></td>
<td>6.0</td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

**Note:**
1. Reference signal is defined as O-QPSK DSSS per 802.15.4, Frequency range = 2400-2483.5 MHz, Symbol rate = 62.5 ksymbols/s.
2. Reference sensitivity level is -85 dBm.
3. Filter is characterized as a symmetric bandpass centered on the adjacent channel having a 3dB bandwidth of 4.6 MHz and stopband rejection better than 26 dB beyond 3.15 MHz from the adjacent carrier.
4. Due to low-IF frequency, there is some overlap of adjacent channel and image channel bands. Adjacent channel CW blocker tests place the Interferer center frequency at the Desired frequency ± 5 MHz on the channel raster, whereas the image rejection test places the CW interferer near the image frequency of the Desired signal carrier, regardless of the channel raster.
5. This is an IEEE 802.11b/g ERP-PBCC 22 MBit/s signal as defined by the IEEE 802.11 specification and IEEE 802.11g addendum.

### 4.1.8.4 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25°C, VBATT = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

#### Table 4.14. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 125 kbps Data Rate

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power spectral density limit</td>
<td>PSDLIMIT</td>
<td>Per FCC part 15.247 at 10 dBm</td>
<td></td>
<td></td>
<td>8</td>
<td>dBm/3kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Per FCC part 15.247 at 20 dBm&lt;sup&gt;1&lt;/sup&gt;</td>
<td></td>
<td></td>
<td>8</td>
<td>dBm/3kHz</td>
</tr>
<tr>
<td>Spurious emissions out-of-band, excluding harmonics captured in SPURHARM,FCC</td>
<td>SPURQOB,FCC</td>
<td>Per FCC part 15.205/15.209, Above 2.483 GHz or below 2.4 GHz; continuous transmission of CW carrier, Restricted Bands&lt;sup&gt;2,3&lt;/sup&gt;</td>
<td></td>
<td>-47</td>
<td></td>
<td>dBm</td>
</tr>
</tbody>
</table>

**Note:**
1. Output power limited to 14 dBm to ensure compliance with FCC specifications.
2. For 2476 MHz, 1.2 dB of power backoff is used to achieve this value.
3. For 2478 MHz, 5.8 dB of power backoff is used to achieve this value.
4.1.8.5 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VBATT = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.15. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 125 kbps Data Rate

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max usable receiver input level, 0.1% BER</td>
<td>SAT</td>
<td>Signal is reference signal. Packet length is 20 bytes.</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td>Sensitivity, 0.1% BER</td>
<td>SENS</td>
<td>Signal is reference signal. Using DC-DC converter.</td>
<td>—</td>
<td>-102.1</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>With non-ideal signals as specified in RF-PHY.TS.4.2.2, section 4.6.1.</td>
<td>—</td>
<td>-101.8</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td>N+1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -79 dBm</td>
<td>C/I_{1+}</td>
<td>Interferer is reference signal at +1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz</td>
<td>—</td>
<td>-14.0</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>N-1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -79 dBm</td>
<td>C/I_{1-}</td>
<td>Interferer is reference signal at -1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz</td>
<td>—</td>
<td>-13.6</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Selectivity to image frequency, 0.1% BER. Desired is reference signal at -79 dBm</td>
<td>C/I_{IM}</td>
<td>Interferer is reference signal at image frequency with 1 MHz precision</td>
<td>—</td>
<td>-51.6</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Selectivity to image frequency ± 1 MHz, 0.1% BER. Desired is reference signal at -79 dBm</td>
<td>C/I_{IM+1}</td>
<td>Interferer is reference signal at image frequency ± 1 MHz with 1 MHz precision</td>
<td>—</td>
<td>-55.5</td>
<td>—</td>
<td>dB</td>
</tr>
</tbody>
</table>

**Note:**
1. Reference signal is defined 2GFSK at -79 dBm, Modulation index = 0.5, BT = 0.5, Bit rate = 125 kbps, desired data = PRBS9; interferer data = PRBS15; frequency accuracy better than 1 ppm.
4.1.8.6 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VBATT = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.16. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 500 kbps Data Rate

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power spectral density limit</td>
<td>PSD\textsubscript{LIMIT}</td>
<td>Per FCC part 15.247 at 10 dBm</td>
<td>—</td>
<td>-9.8</td>
<td>—</td>
<td>dBm/3kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Per FCC part 15.247 at 20 dBm\textsuperscript{1}</td>
<td>—</td>
<td>—</td>
<td>8</td>
<td>dBm/3kHz</td>
</tr>
<tr>
<td>Spurious emissions out-of-band, excluding harmonics captured in SPUR\textsubscript{HARM,FCC}</td>
<td>SPUR\textsubscript{OOB,FCC}</td>
<td>Per FCC part 15.205/15.209, Above 2.483 GHz or below 2.4 GHz; continuous transmission of CW carrier, Restricted Bands\textsuperscript{2,3}</td>
<td>—</td>
<td>-47</td>
<td>—</td>
<td>dBm</td>
</tr>
</tbody>
</table>

Note:

1. Output power limited to 14 dBm to ensure compliance with FCC specifications.
2. For 2476 MHz, 1.2 dB of power backoff is used to achieve this value.
3. For 2478 MHz, 5.8 dB of power backoff is used to achieve this value.
4.1.8.7 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VBATT = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.17. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 500 kbps Data Rate

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max usable receiver input level, 0.1% BER</td>
<td>SAT</td>
<td>Signal is reference signal(^1). Packet length is 20 bytes.</td>
<td></td>
<td>10</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Sensitivity, 0.1% BER</td>
<td>SENS</td>
<td>Signal is reference signal(^1). Using DC-DC converter.</td>
<td></td>
<td>-97.9</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>With non-ideal signals as specified in RF-PHY.TS.4.2.2, section 4.6.1.</td>
<td></td>
<td>-97.0</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>N+1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -72 dBm</td>
<td>C/I(_{1+})</td>
<td>Interferer is reference signal at +1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz</td>
<td></td>
<td>-9.2</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>N-1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -72 dBm</td>
<td>C/I(_{1-})</td>
<td>Interferer is reference signal at -1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz</td>
<td></td>
<td>-9.0</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Alternate selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -72 dBm</td>
<td>C/I(_{2})</td>
<td>Interferer is reference signal at ± 2 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz</td>
<td></td>
<td>-46.5</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Selectivity to image frequency, 0.1% BER. Desired is reference signal at -72 dBm</td>
<td>C/I(_{IM})</td>
<td>Interferer is reference signal at image frequency with 1 MHz precision</td>
<td></td>
<td>-46.5</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Selectivity to image frequency ± 1 MHz, 0.1% BER. Desired is reference signal at -72 dBm</td>
<td>C/I(_{IM+1})</td>
<td>Interferer is reference signal at image frequency ± 1 MHz with 1 MHz precision</td>
<td></td>
<td>-50.7</td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

**Note:**
1. Reference signal is defined 2GFSK at -72 dBm, Modulation index = 0.5, BT = 0.5, Bit rate = 500 kbps, desired data = PRBS9; interferer data = PRBS15; frequency accuracy better than 1 ppm.
4.1.8.8 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VBATT = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.18. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 1 Mbps Data Rate

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>In-band spurious emissions, with allowed exceptions&lt;sup&gt;1&lt;/sup&gt;</td>
<td>SPUR&lt;sub&gt;INB&lt;/sub&gt;</td>
<td>At ± 2 MHz, 10 dBm</td>
<td>—</td>
<td>-39.7</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>At ± 3 MHz, 10 dBm</td>
<td>—</td>
<td>-43.6</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>At ± 2 MHz, 20 dBm</td>
<td>—</td>
<td>—</td>
<td>-20</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>At ± 3 MHz, 20 dBm</td>
<td>—</td>
<td>—</td>
<td>-30</td>
<td>dBm</td>
</tr>
<tr>
<td>Spurious emissions out-of-band, excluding harmonics captured in SPUR&lt;sub&gt;HARM,FCC&lt;/sub&gt;: Emissions taken at POUT&lt;sub&gt;MAX&lt;/sub&gt;, PAVDD connected to external 3.3 V supply</td>
<td>SPUR&lt;sub&gt;OOB,FCC&lt;/sub&gt;</td>
<td>Per FCC part 15.205/15.209, Above 2.483 GHz or below 2.4 GHz; continuous transmission of CW carrier, Restricted Bands&lt;sup&gt;2&lt;/sup&gt; 3</td>
<td>—</td>
<td>-47</td>
<td>—</td>
<td>dBm</td>
</tr>
</tbody>
</table>

Note:
1. Per Bluetooth Core_5.0, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.
2. For 2476 MHz, 1.5 dB of power backoff is used to achieve this value.
3. For 2478 MHz, 4.2 dB of power backoff is used to achieve this value.
4.1.8.9 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VBATT = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

Table 4.19. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 1 Mbps Data Rate

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max usable receiver input level, 0.1% BER</td>
<td>SAT</td>
<td>Signal is reference signal(^1). Packet length is 20 bytes.</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td>Sensitivity, 0.1% BER</td>
<td>SENS</td>
<td>Signal is reference signal(^1). Using DC-DC converter.</td>
<td>—</td>
<td>-94.1</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>With non-ideal signals as specified in RF-PHY.TS.4.2.2, section 4.6.1.</td>
<td>—</td>
<td>-93.8</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td>Signal to co-channel interferer, 0.1% BER</td>
<td>C/I(_{CC})</td>
<td>Desired signal 3 dB above reference sensitivity.</td>
<td>—</td>
<td>9.0</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>N+1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm</td>
<td>C/I(_{1+})</td>
<td>Interferer is reference signal at +1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz</td>
<td>—</td>
<td>-3.3</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>N-1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm</td>
<td>C/I(_{1-})</td>
<td>Interferer is reference signal at -1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz</td>
<td>—</td>
<td>-1.6</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Alternate selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm</td>
<td>C/I(_{2})</td>
<td>Interferer is reference signal at ± 2 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz</td>
<td>—</td>
<td>-42.0</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Alternate selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm</td>
<td>C/I(_{3})</td>
<td>Interferer is reference signal at ± 3 MHz offset. Desired frequency 2404 MHz ≤ Fc ≤ 2480 MHz</td>
<td>—</td>
<td>-46.4</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Selectivity to image frequency, 0.1% BER. Desired is reference signal at -67 dBm</td>
<td>C/I(_{IM})</td>
<td>Interferer is reference signal at image frequency with 1 MHz precision</td>
<td>—</td>
<td>-42.0</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Selectivity to image frequency ± 1 MHz, 0.1% BER. Desired is reference signal at -67 dBm</td>
<td>C/I(_{IM+1})</td>
<td>Interferer is reference signal at image frequency ± 1 MHz with 1 MHz precision</td>
<td>—</td>
<td>-47.1</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Intermodulation performance</td>
<td>IM</td>
<td>Per Core_4.1, Vol 6, Part A, Section 4.4 with n = 3</td>
<td>—</td>
<td>-18.4</td>
<td>—</td>
<td>dBm</td>
</tr>
</tbody>
</table>

Note:
1. Reference signal is defined 2GFSK at -67 dBm, Modulation index = 0.5, BT = 0.5, Bit rate = 1 Mbps, desired data = PRBS9; interferer data = PRBS15; frequency accuracy better than 1 ppm.
### 4.1.8.10 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VBATT = 3.3 V. DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

**Table 4.20. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 2 Mbps Data Rate**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>In-band spurious emissions, with allowed exceptions&lt;sup&gt;1&lt;/sup&gt;</td>
<td>SPUR&lt;sub&gt;INB&lt;/sub&gt;</td>
<td>At ± 4 MHz, 10 dBm</td>
<td>—</td>
<td>-38.2</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>At ± 6 MHz, 10 dBm</td>
<td>—</td>
<td>-41.1</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>At ± 4 MHz, 20 dBm</td>
<td>—</td>
<td>-30.1</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>At ± 6 MHz, 20 dBm</td>
<td>—</td>
<td>-31.4</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td>Spurious emissions out-of-band, excluding harmonics captured in SPUR&lt;sub&gt;HARM,FCC&lt;/sub&gt;: Emissions taken at POUT&lt;sub&gt;MAX&lt;/sub&gt;, PAVDD connected to external 3.3 V supply</td>
<td>SPUR&lt;sub&gt;OOB,FCC&lt;/sub&gt;</td>
<td>Per FCC part 15.205/15.209, Above 2.483 GHz or below 2.4 GHz; continuous transmission of CW carrier, Restricted Bands&lt;sup&gt;2 3 4 5&lt;/sup&gt;</td>
<td>—</td>
<td>-47</td>
<td>—</td>
<td>dBm</td>
</tr>
</tbody>
</table>

**Note:**

1. Per Bluetooth Core_5.0, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.
2. For 2472 MHz, 1.3 dB of power backoff is used to achieve this value.
3. For 2474 MHz, 3.8 dB of power backoff is used to achieve this value.
4. For 2476 MHz, 7 dB of power backoff is used to achieve this value.
5. For 2478 MHz, 11.2 dB of power backoff is used to achieve this value.
4.1.8.11  RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: \( T = 25 \, ^\circ\text{C}, \) \( \text{VBATT} = 3.3 \, \text{V}. \) DC-DC on. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Conducted measurement from the antenna feedpoint.

**Table 4.21. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 2 Mbps Data Rate**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max usable receiver input level, 0.1% BER</td>
<td>SAT</td>
<td>Signal is reference signal(^1). Packet length is 20 bytes.</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td>Sensitivity, 0.1% BER</td>
<td>SENS</td>
<td>Signal is reference signal(^1). Using DC-DC converter.</td>
<td>—</td>
<td>-90.2</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>With non-ideal signals as specified in RF-PHY.TS.4.2.2, section 4.6.1.</td>
<td>—</td>
<td>-89.9</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td>Signal to co-channel interferer, 0.1% BER</td>
<td>C/I(_\text{CC})</td>
<td>Desired signal 3 dB above reference sensitivity.</td>
<td>—</td>
<td>8.6</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>N+1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm</td>
<td>C/I(_\text{1+})</td>
<td>Interferer is reference signal at +2 MHz offset. Desired frequency 2402 MHz ≤ ( F_c ) ≤ 2480 MHz</td>
<td>—</td>
<td>-7.6</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>N-1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm</td>
<td>C/I(_\text{1-})</td>
<td>Interferer is reference signal at -2 MHz offset. Desired frequency 2402 MHz ≤ ( F_c ) ≤ 2480 MHz</td>
<td>—</td>
<td>-11.4</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Alternate selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm</td>
<td>C/I(_\text{2})</td>
<td>Interferer is reference signal at ± 4 MHz offset. Desired frequency 2402 MHz ≤ ( F_c ) ≤ 2480 MHz</td>
<td>—</td>
<td>-40.3</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Alternate selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm</td>
<td>C/I(_\text{3})</td>
<td>Interferer is reference signal at ± 6 MHz offset. Desired frequency 2404 MHz ≤ ( F_c ) ≤ 2480 MHz</td>
<td>—</td>
<td>-45.1</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Selectivity to image frequency, 0.1% BER. Desired is reference signal at -67 dBm</td>
<td>C/I(_\text{IM})</td>
<td>Interferer is reference signal at image frequency with 1 MHz precision</td>
<td>—</td>
<td>-7.6</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Selectivity to image frequency ± 2 MHz, 0.1% BER. Desired is reference signal at -67 dBm</td>
<td>C/I(_\text{IM+1})</td>
<td>Interferer is reference signal at image frequency ± 2 MHz with 2 MHz precision</td>
<td>—</td>
<td>-40.30</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Intermodulation performance</td>
<td>IM</td>
<td>Per Core_4.1, Vol 6, Part A, Section 4.4 with n = 3</td>
<td>—</td>
<td>-18.4</td>
<td>—</td>
<td>dBm</td>
</tr>
</tbody>
</table>

**Note:**
1. Reference signal is defined 2GFSK at -67 dBm, Modulation index = 0.5, \( BT = 0.5 \), Bit rate = 2 Mbps, desired data = PRBS9; interferer data = PRBS15; frequency accuracy better than 1 ppm.
4.1.9 Oscillators

4.1.9.1 Low-Frequency Crystal Oscillator (LFXO)

Table 4.22. Low-Frequency Crystal Oscillator (LFXO)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Crystal frequency</td>
<td>( f_{LFXO} )</td>
<td></td>
<td>—</td>
<td>32.768</td>
<td>—</td>
<td>kHz</td>
</tr>
<tr>
<td>Supported crystal equivalent</td>
<td>( ESR_{LFXO} )</td>
<td></td>
<td>—</td>
<td>—</td>
<td>70</td>
<td>kΩ</td>
</tr>
<tr>
<td>series resistance (ESR)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supported range of crystal</td>
<td>( C_{LFXO_CL} )</td>
<td>On each of LFXTAL_N and LFXTAL_P pins</td>
<td>6</td>
<td>—</td>
<td>18</td>
<td>pF</td>
</tr>
<tr>
<td>load capacitance (^1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>On-chip tuning cap range (^2)</td>
<td>( C_{LFXO_T} )</td>
<td></td>
<td>8</td>
<td>—</td>
<td>40</td>
<td>pF</td>
</tr>
<tr>
<td>On-chip tuning cap step size</td>
<td>( SS_{LFXO} )</td>
<td></td>
<td>—</td>
<td>0.25</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td>Current consumption after</td>
<td>( I_{LFXO} )</td>
<td>( ESR = 70 \ \text{kOhm}, C_L = 7 \ \text{pF}, \ \text{GAIN}^4 = 2, \ \text{AGC}^4 = 1 )</td>
<td>—</td>
<td>273</td>
<td>—</td>
<td>nA</td>
</tr>
<tr>
<td>startup (^3)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Start-up time</td>
<td>( t_{LFXO} )</td>
<td>( ESR = 70 \ \text{kOhm}, C_L = 7 \ \text{pF}, \ \text{GAIN}^4 = 2 )</td>
<td>—</td>
<td>308</td>
<td>—</td>
<td>ms</td>
</tr>
</tbody>
</table>

**Note:**
1. Total load capacitance as seen by the crystal.
2. The effective load capacitance seen by the crystal will be \( C_{LFXO\_T}/2 \). This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.
3. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU\_PWRCTRL register.
4. In CMU\_LFXOCTRL register.

4.1.9.2 High-Frequency Crystal Oscillator (HFXO)

Table 4.23. High-Frequency Crystal Oscillator (HFXO)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Crystal frequency</td>
<td>( f_{HFXO} )</td>
<td>38.4 MHz required for radio transceiver operation</td>
<td>—</td>
<td>38.4</td>
<td>—</td>
<td>MHz</td>
</tr>
<tr>
<td>Frequency tolerance for the crystal</td>
<td>( FT_{HFXO} )</td>
<td></td>
<td>-40</td>
<td>—</td>
<td>40</td>
<td>ppm</td>
</tr>
</tbody>
</table>
### 4.1.9.3 Low-Frequency RC Oscillator (LFRCO)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oscillation frequency</td>
<td>$f_{\text{LFRCO}}$</td>
<td>ENVREF(^1) = 1</td>
<td>31.3</td>
<td>32.768</td>
<td>33.6</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ENVREF(^1) = 0</td>
<td>31.3</td>
<td>32.768</td>
<td>33.4</td>
<td>kHz</td>
</tr>
<tr>
<td>Startup time</td>
<td>$t_{\text{LFRCO}}$</td>
<td>—</td>
<td>500</td>
<td>—</td>
<td>—</td>
<td>µs</td>
</tr>
<tr>
<td>Current consumption (^2)</td>
<td>$I_{\text{LFRCO}}$</td>
<td>ENVREF = 1 in CMU_LFRCOCTRL</td>
<td>—</td>
<td>342</td>
<td>—</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ENVREF = 0 in CMU_LFRCOCTRL</td>
<td>—</td>
<td>494</td>
<td>—</td>
<td>nA</td>
</tr>
</tbody>
</table>

**Note:**

1. In CMU_LFRCOCTRL register.
2. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
4.1.9.4 High-Frequency RC Oscillator (HFRCO)

Table 4.25. High-Frequency RC Oscillator (HFRCO)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency accuracy</td>
<td>f_{HFRCO,ACC}</td>
<td>At production calibrated frequencies, across supply voltage and temperature</td>
<td>-2.5</td>
<td>—</td>
<td>2.5</td>
<td>%</td>
</tr>
<tr>
<td>Start-up time</td>
<td>f_{HFRCO}</td>
<td>$f_{HFRCO} \geq 19$ MHz</td>
<td>—</td>
<td>300</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$4 &lt; f_{HFRCO} &lt; 19$ MHz</td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{HFRCO} &lt; 4$ MHz</td>
<td>—</td>
<td>2.5</td>
<td>—</td>
<td>µs</td>
</tr>
<tr>
<td>Current consumption on all</td>
<td>I_{HFRCO}</td>
<td>$f_{HFRCO} = 38$ MHz</td>
<td>—</td>
<td>267</td>
<td>299</td>
<td>µA</td>
</tr>
<tr>
<td>supplies</td>
<td></td>
<td>$f_{HFRCO} = 32$ MHz</td>
<td>—</td>
<td>224</td>
<td>248</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{HFRCO} = 26$ MHz</td>
<td>—</td>
<td>189</td>
<td>211</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{HFRCO} = 19$ MHz</td>
<td>—</td>
<td>154</td>
<td>172</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{HFRCO} = 16$ MHz</td>
<td>—</td>
<td>133</td>
<td>148</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{HFRCO} = 13$ MHz</td>
<td>—</td>
<td>118</td>
<td>135</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{HFRCO} = 7$ MHz</td>
<td>—</td>
<td>89</td>
<td>100</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{HFRCO} = 4$ MHz</td>
<td>—</td>
<td>34</td>
<td>44</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{HFRCO} = 2$ MHz</td>
<td>—</td>
<td>29</td>
<td>40</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{HFRCO} = 1$ MHz</td>
<td>—</td>
<td>26</td>
<td>36</td>
<td>µA</td>
</tr>
<tr>
<td>Coarse trim step size (% of</td>
<td>SS_{HFRCO_COARS}E</td>
<td>—</td>
<td>0.8</td>
<td>—</td>
<td>—</td>
<td>%</td>
</tr>
<tr>
<td>period)</td>
<td></td>
<td>—</td>
<td>0.1</td>
<td>—</td>
<td>—</td>
<td>%</td>
</tr>
<tr>
<td>Fine trim step size (% of period)</td>
<td>SS_{HFRCO_FINE}</td>
<td>—</td>
<td>0.2</td>
<td>—</td>
<td>—</td>
<td>% RMS</td>
</tr>
<tr>
<td>Period jitter</td>
<td>P_{HFRCO}</td>
<td>—</td>
<td>3.47</td>
<td>—</td>
<td>6.15</td>
<td>MHz</td>
</tr>
<tr>
<td>Frequency limits</td>
<td>f_{HFRCO_BAND}</td>
<td>FREQRANGE = 0, FINETUNGEN = 0</td>
<td>6.24</td>
<td>—</td>
<td>11.45</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FREQRANGE = 3, FINETUNGEN = 0</td>
<td>11.3</td>
<td>—</td>
<td>19.8</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FREQRANGE = 6, FINETUNGEN = 0</td>
<td>13.45</td>
<td>—</td>
<td>22.8</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FREQRANGE = 7, FINETUNGEN = 0</td>
<td>16.5</td>
<td>—</td>
<td>29.0</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FREQRANGE = 8, FINETUNGEN = 0</td>
<td>23.11</td>
<td>—</td>
<td>40.63</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FREQRANGE = 10, FINETUNGEN = 0</td>
<td>27.27</td>
<td>—</td>
<td>48</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FREQRANGE = 12, FINETUNGEN = 0</td>
<td>33.33</td>
<td>—</td>
<td>54</td>
<td>MHz</td>
</tr>
</tbody>
</table>
4.1.9.5 Ultra-low Frequency RC Oscillator (ULFRCO)

Table 4.26. Ultra-low Frequency RC Oscillator (ULFRCO)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oscillation frequency</td>
<td>fULFRCO</td>
<td></td>
<td>0.95</td>
<td>1</td>
<td>1.07</td>
<td>kHz</td>
</tr>
</tbody>
</table>

4.1.10 Flash Memory Characteristics

Table 4.27. Flash Memory Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash erase cycles before failure</td>
<td>ECFLASH</td>
<td>Burst write, 128 words, average time per word</td>
<td>10000</td>
<td>—</td>
<td>—</td>
<td>cycles</td>
</tr>
<tr>
<td>Flash data retention</td>
<td>RETFLASH</td>
<td></td>
<td>10</td>
<td>—</td>
<td>—</td>
<td>years</td>
</tr>
<tr>
<td>Word (32-bit) programming time</td>
<td>tW_PROG</td>
<td>Single word</td>
<td>62</td>
<td>68.9</td>
<td>80</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Burst write, 128 words, average time per word</td>
<td>20</td>
<td>26.3</td>
<td>30</td>
<td>µs</td>
</tr>
<tr>
<td>Page erase time</td>
<td>tPERASE</td>
<td></td>
<td>20</td>
<td>29.5</td>
<td>40</td>
<td>ms</td>
</tr>
<tr>
<td>Mass erase time</td>
<td>tMERASE</td>
<td></td>
<td>20</td>
<td>30</td>
<td>40</td>
<td>ms</td>
</tr>
<tr>
<td>Device erase time</td>
<td>tDERASE</td>
<td></td>
<td>—</td>
<td>56.2</td>
<td>70</td>
<td>ms</td>
</tr>
<tr>
<td>Erase current</td>
<td>IERASE</td>
<td>Page Erase</td>
<td>—</td>
<td>—</td>
<td>2.0</td>
<td>mA</td>
</tr>
<tr>
<td>Write current</td>
<td>IWRITE</td>
<td></td>
<td>—</td>
<td>—</td>
<td>3.5</td>
<td>mA</td>
</tr>
<tr>
<td>Supply voltage during flash erase and write</td>
<td>VFLASH</td>
<td></td>
<td>1.62</td>
<td>—</td>
<td>3.6</td>
<td>V</td>
</tr>
</tbody>
</table>

Note:
1. Flash data retention information is published in the Quarterly Quality and Reliability Report.
2. From setting the ERASEPAGE bit in MSC_WRITECMD to 1 until the BUSY bit in MSC_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
3. Mass erase is issued by the CPU and erases all flash.
4. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW).
5. From setting the DEVICEERASE bit in AAP_CMD to 1 until the ERASEBUSY bit in AAP_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
6. Measured at 25 °C.
# 4.1.11 General-Purpose I/O (GPIO)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input low voltage</td>
<td>$V_{IL}$</td>
<td>GPIO pins</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>Input high voltage</td>
<td>$V_{IH}$</td>
<td>GPIO pins</td>
<td>IOVDD*0.7</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>Output high voltage relative to IOVDD</td>
<td>$V_{OH}$</td>
<td>Sourcing 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH¹ = WEAK</td>
<td>IOVDD*0.8</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sourcing 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH¹ = WEAK</td>
<td>IOVDD*0.6</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sourcing 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH¹ = STRONG</td>
<td>IOVDD*0.8</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sourcing 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH¹ = STRONG</td>
<td>IOVDD*0.6</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>Output low voltage relative to IOVDD</td>
<td>$V_{OL}$</td>
<td>Sinking 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH¹ = WEAK</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH¹ = WEAK</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH¹ = STRONG</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH¹ = STRONG</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>Input leakage current</td>
<td>$I_{IOLEAK}$</td>
<td>All GPIO except LFXO pins, GPIO ≤ IOVDD</td>
<td>—</td>
<td>0.1</td>
<td>30</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LFXO Pins, GPIO ≤ IOVDD</td>
<td>—</td>
<td>0.1</td>
<td>50</td>
<td>nA</td>
</tr>
<tr>
<td>Input leakage current on 5VTOL pads above IOVDD</td>
<td>$I_{5VTOLLEAK}$</td>
<td>IOVDD &lt; GPIO ≤ IOVDD + 2 V</td>
<td>—</td>
<td>3.3</td>
<td>15</td>
<td>µA</td>
</tr>
<tr>
<td>I/O pin pull-up/pull-down resistor</td>
<td>$R_{PUD}$</td>
<td>—</td>
<td>30</td>
<td>40</td>
<td>65</td>
<td>kΩ</td>
</tr>
<tr>
<td>Pulse width of pulses removed by the glitch suppression filter</td>
<td>$I_{IOGLITCH}$</td>
<td>—</td>
<td>15</td>
<td>25</td>
<td>45</td>
<td>ns</td>
</tr>
</tbody>
</table>
### Output Fall Time

Output fall time, From 70\% to 30\% of $V_{IO}$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output fall time, From 70% to 30% of $V_{IO}$</td>
<td>t_IOOF</td>
<td>$C_L = 50$ pF, DRIVESTRENGTH(^1) = STRONG, SLEWRATE(^1) = 0x6</td>
<td></td>
<td>1.8</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_L = 50$ pF, DRIVESTRENGTH(^1) = WEAK, SLEWRATE(^1) = 0x6</td>
<td></td>
<td>4.5</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

### Output Rise Time

Output rise time, From 30\% to 70\% of $V_{IO}$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output rise time, From 30% to 70% of $V_{IO}$</td>
<td>t_IOOR</td>
<td>$C_L = 50$ pF, DRIVESTRENGTH(^1) = STRONG, SLEWRATE = 0x6(^1)</td>
<td></td>
<td>2.2</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_L = 50$ pF, DRIVESTRENGTH(^1) = WEAK, SLEWRATE(^1) = 0x6</td>
<td></td>
<td>7.4</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Note:

1. In GPIO\_Pn\_CTRL register.

### 4.1.12 Voltage Monitor (VMON)

#### Table 4.29. Voltage Monitor (VMON)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply current (including $I_{SENSE}$)</td>
<td>$I_{VMON}$</td>
<td>In EM0 or EM1, 1 active channel</td>
<td></td>
<td>6.3</td>
<td>8</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In EM0 or EM1, All channels active</td>
<td></td>
<td>12.5</td>
<td>15</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In EM2, EM3 or EM4, 1 channel active and above threshold</td>
<td></td>
<td>62</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In EM2, EM3 or EM4, 1 channel active and below threshold</td>
<td></td>
<td>62</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In EM2, EM3 or EM4, All channels active and above threshold</td>
<td></td>
<td>99</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In EM2, EM3 or EM4, All channels active and below threshold</td>
<td></td>
<td>99</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>Loading of monitored supply</td>
<td>$I_{SENSE}$</td>
<td>In EM0 or EM1</td>
<td></td>
<td>2</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In EM2, EM3 or EM4</td>
<td></td>
<td>2</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>Threshold range</td>
<td>$V_{VMON_RANGE}$</td>
<td>1.62 — 3.4 V</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Threshold step size</td>
<td>$N_{VMON_STESP}$</td>
<td>Coarse — 200 — mV</td>
<td></td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fine — 20 — mV</td>
<td></td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Response time</td>
<td>$t_{VMON_RES}$</td>
<td>Supply drops at 1V/µs rate</td>
<td></td>
<td>460</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Hysteresis</td>
<td>$V_{VMON_HYST}$</td>
<td></td>
<td></td>
<td>26</td>
<td></td>
<td>mV</td>
</tr>
</tbody>
</table>
4.1.13 Analog to Digital Converter (ADC)

Specified at 1 Msps, ADCCLK = 16 MHz, BIASPROG = 0, GPBIASACC = 0, unless otherwise indicated.

**Table 4.30. Analog to Digital Converter (ADC)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>$V_{\text{RESOLUTION}}$</td>
<td></td>
<td>6</td>
<td>—</td>
<td>12</td>
<td>Bits</td>
</tr>
<tr>
<td>Input voltage range</td>
<td>$V_{\text{ADCIN}}$</td>
<td>Single ended</td>
<td>—</td>
<td>—</td>
<td>$V_{\text{FS}}$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Differential</td>
<td>$-V_{\text{FS}}/2$</td>
<td>—</td>
<td>$V_{\text{FS}}/2$</td>
<td>V</td>
</tr>
<tr>
<td>Input range of external reference voltage, single ended and differential</td>
<td>$V_{\text{ADCREFIN_P}}$</td>
<td></td>
<td>1</td>
<td>—</td>
<td>$V_{\text{AVDD}}$</td>
<td>V</td>
</tr>
<tr>
<td>Power supply rejection</td>
<td>$\text{PSRR}_{\text{ADC}}$</td>
<td>At DC</td>
<td>—</td>
<td>80</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Analog input common mode rejection ratio</td>
<td>$\text{CMRR}_{\text{ADC}}$</td>
<td>At DC</td>
<td>—</td>
<td>80</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Current from all supplies, using internal reference buffer. Continuous operation. WARMUPMODE$^3$ = KEEPADCWARM</td>
<td>$I_{\text{ADC CONTINUOUS_LP}}$</td>
<td>1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1</td>
<td>4</td>
<td>—</td>
<td>270</td>
<td>290</td>
</tr>
<tr>
<td></td>
<td></td>
<td>250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 1</td>
<td>4</td>
<td>—</td>
<td>125</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 1</td>
<td>4</td>
<td>—</td>
<td>80</td>
<td>—</td>
</tr>
<tr>
<td>Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE$^3$ = NORMAL</td>
<td>$I_{\text{ADC NORMAL_LP}}$</td>
<td>35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1</td>
<td>4</td>
<td>—</td>
<td>45</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 1</td>
<td>4</td>
<td>—</td>
<td>8</td>
<td>—</td>
</tr>
<tr>
<td>Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE$^3$ = KEEPINSTANDBY or KEEPINSLOWACC</td>
<td>$I_{\text{ADC STANDBY_LP}}$</td>
<td>125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1</td>
<td>4</td>
<td>—</td>
<td>105</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1</td>
<td>4</td>
<td>—</td>
<td>70</td>
<td>—</td>
</tr>
<tr>
<td>Current from all supplies, using internal reference buffer. Continuous operation. WARMUPMODE$^3$ = KEEPADCWARM</td>
<td>$I_{\text{ADC CONTINUOUS_HP}}$</td>
<td>1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0</td>
<td>4</td>
<td>—</td>
<td>325</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 0</td>
<td>4</td>
<td>—</td>
<td>175</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 0</td>
<td>4</td>
<td>—</td>
<td>125</td>
<td>—</td>
</tr>
<tr>
<td>Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE$^3$ = NORMAL</td>
<td>$I_{\text{ADC NORMAL_HP}}$</td>
<td>35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0</td>
<td>4</td>
<td>—</td>
<td>85</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0</td>
<td>4</td>
<td>—</td>
<td>16</td>
<td>—</td>
</tr>
<tr>
<td>Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE$^3$ = KEEPINSTANDBY or KEEPINSLOWACC</td>
<td>$I_{\text{ADC STANDBY_HP}}$</td>
<td>125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0</td>
<td>4</td>
<td>—</td>
<td>160</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>35 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0</td>
<td>4</td>
<td>—</td>
<td>125</td>
<td>—</td>
</tr>
<tr>
<td>Current from HFPERCLK</td>
<td>$I_{\text{ADC CLK}}$</td>
<td>HFPERCLK = 16 MHz</td>
<td>—</td>
<td>140</td>
<td>—</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Test Condition</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Unit</td>
</tr>
<tr>
<td>------------------------------------------------</td>
<td>-------------</td>
<td>---------------------------------</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>--------</td>
</tr>
<tr>
<td>ADC clock frequency</td>
<td>$f_{\text{ADCClock}}$</td>
<td></td>
<td>16</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Throughput rate</td>
<td>$f_{\text{ADCRate}}$</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>Msps</td>
</tr>
<tr>
<td>Conversion time</td>
<td>$t_{\text{ADCConv}}$</td>
<td>6 bit</td>
<td>7</td>
<td></td>
<td></td>
<td>cycles</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8 bit</td>
<td>9</td>
<td></td>
<td></td>
<td>cycles</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12 bit</td>
<td>13</td>
<td></td>
<td></td>
<td>cycles</td>
</tr>
<tr>
<td>Startup time of reference generator and ADC core</td>
<td>$t_{\text{ADCStart}}$</td>
<td>WARMUPMODE$^3$ = NORMAL</td>
<td>5</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>WARMUPMODE$^3$ = KEEPIN-STANDBY</td>
<td>2</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>WARMUPMODE$^3$ = KEEPINSLO-WACC</td>
<td>1</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>SNDR at 1Msps and $f_{\text{IN}}$ = 10kHz</td>
<td>$\text{SNDR}_{\text{ADC}}$</td>
<td>Internal reference$^6$, differential measurement</td>
<td>58</td>
<td>67</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>External reference$^7$, differential measurement</td>
<td>68</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Spurious-free dynamic range (SFDR)</td>
<td>$\text{SFDR}_{\text{ADC}}$</td>
<td>1 MSamples/s, 10 kHz full-scale sine wave</td>
<td>75</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Differential non-linearity (DNL)</td>
<td>$\text{DNL}_{\text{ADC}}$</td>
<td>12 bit resolution, No missing codes</td>
<td>-1</td>
<td></td>
<td>2</td>
<td>LSB</td>
</tr>
<tr>
<td>Integral non-linearity (INL), End point method</td>
<td>$\text{INL}_{\text{ADC}}$</td>
<td>12 bit resolution</td>
<td>-6</td>
<td></td>
<td>6</td>
<td>LSB</td>
</tr>
<tr>
<td>Offset error</td>
<td>$V_{\text{ADCOFFSETERR}}$</td>
<td>Using internal reference</td>
<td>-3</td>
<td>0</td>
<td>3</td>
<td>LSB</td>
</tr>
<tr>
<td>Gain error in ADC</td>
<td>$V_{\text{ADCGAIN}}$</td>
<td>Using internal reference</td>
<td>-0.2</td>
<td></td>
<td>3.5</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Using external reference</td>
<td>-1</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Temperature sensor slope</td>
<td>$V_{\text{TS SLOPE}}$</td>
<td></td>
<td>-1.84</td>
<td></td>
<td></td>
<td>mV/°C</td>
</tr>
</tbody>
</table>

**Note:**

1. The absolute voltage allowed at any ADC input is dictated by the power rail supplied to on-chip circuitry, and may be lower than the effective full scale voltage. All ADC inputs are limited to the ADC supply (AVDD or DVDD depending on EMU_PWRCTRL_ANASW). Any ADC input routed through the APORT will further be limited by the IOVDD supply to the pin.
2. PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL.
3. In ADCn_CNTL register.
4. In ADCn_BIASPROG register.
5. Derived from ADCCLK.
6. Internal reference option used corresponds to selection 2V5 in the SINGLECTRL_REF or SCANCTRL_REF register field. The differential input range with this configuration is ± 1.25 V. Typical value is characterized using full-scale sine wave input. Minimum value is production-tested using sine wave input at 1.5 dB lower than full scale.
7. External reference is 1.25 V applied externally to ADCnEXTREFP, with the selection CONF in the SINGLECTRL_REF or SCANCTRL_REF register field and VREFP in the SINGLECTRLX_VREFSEL or SCANCTRLX_VREFSEL field. The differential input range with this configuration is ± 1.25 V.
### 4.1.14 Analog Comparator (ACMP)

**Table 4.31. Analog Comparator (ACMP)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min (Typ)</th>
<th>Max (Unit)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>$V_{ACMPIN}$</td>
<td>$V_{ACMPVDD} = ACMPn_CTRL_PWRSEL \uparrow$</td>
<td>—</td>
<td>$V_{ACMPVDD}$ V</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>$V_{ACMPVDD}$</td>
<td>$BIASPROG^2 \leq 0x10$ or $FULLBIAS^2 = 0$</td>
<td>1.8</td>
<td>$V_{VREGVDD_{MAX}}$ V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$0x10 &lt; BIASPROG^2 \leq 0x20$ and $FULLBIAS^2 = 1$</td>
<td>2.1</td>
<td>$V_{VREGVDD_{MAX}}$ V</td>
</tr>
<tr>
<td>Active current not including voltage reference</td>
<td>$I_{ACMP}$</td>
<td>$BIASPROG^2 = 1$, $FULLBIAS^2 = 0$</td>
<td>—</td>
<td>50 nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$BIASPROG^2 = 0x10$, $FULLBIAS^2 = 0$</td>
<td>—</td>
<td>306 nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$BIASPROG^2 = 0x02$, $FULLBIAS^2 = 1$</td>
<td>—</td>
<td>6.1 µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$BIASPROG^2 = 0x20$, $FULLBIAS^2 = 1$</td>
<td>—</td>
<td>74 µA</td>
</tr>
<tr>
<td>Current consumption of internal voltage reference</td>
<td>$I_{ACMPREF}$</td>
<td>VLP selected as input using 2.5 V Reference / 4 (0.625 V)</td>
<td>—</td>
<td>50 nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VLP selected as input using VDD</td>
<td>—</td>
<td>20 nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VBDIV selected as input using 1.25 V reference / 1</td>
<td>—</td>
<td>4.1 µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VADIV selected as input using VDD/1</td>
<td>—</td>
<td>2.4 µA</td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Test Condition</td>
<td>Min</td>
<td>Typ</td>
</tr>
<tr>
<td>-----------</td>
<td>--------</td>
<td>----------------</td>
<td>-----</td>
<td>-----</td>
</tr>
<tr>
<td>Hysteresis ($V_{CM} = 1.25,V$, $BIASPROG^2 = 0x10$, FULL-BIAS$^2 = 1$)</td>
<td>$V_{ACMPHYST}$</td>
<td>$HYSTSEL^4 = HYST0$</td>
<td>-3</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$HYSTSEL^4 = HYST1$</td>
<td>5</td>
<td>18</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$HYSTSEL^4 = HYST2$</td>
<td>12</td>
<td>33</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$HYSTSEL^4 = HYST3$</td>
<td>17</td>
<td>46</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$HYSTSEL^4 = HYST4$</td>
<td>23</td>
<td>57</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$HYSTSEL^4 = HYST5$</td>
<td>26</td>
<td>68</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$HYSTSEL^4 = HYST6$</td>
<td>30</td>
<td>79</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$HYSTSEL^4 = HYST7$</td>
<td>34</td>
<td>90</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$HYSTSEL^4 = HYST8$</td>
<td>-3</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$HYSTSEL^4 = HYST9$</td>
<td>-27</td>
<td>-18</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$HYSTSEL^4 = HYST10$</td>
<td>-50</td>
<td>-33</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$HYSTSEL^4 = HYST11$</td>
<td>-67</td>
<td>-45</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$HYSTSEL^4 = HYST12$</td>
<td>-86</td>
<td>-57</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$HYSTSEL^4 = HYST13$</td>
<td>-104</td>
<td>-67</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$HYSTSEL^4 = HYST14$</td>
<td>-130</td>
<td>-78</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$HYSTSEL^4 = HYST15$</td>
<td>-155</td>
<td>-88</td>
</tr>
<tr>
<td>Comparator delay$^5$</td>
<td>$t_{ACMPDELAY}$</td>
<td>$BIASPROG^2 = 1$, FULLBIAS$^2 = 0$</td>
<td>—</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$BIASPROG^2 = 0x10$, FULLBIAS$^2 = 0$</td>
<td>—</td>
<td>3.7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$BIASPROG^2 = 0x02$, FULLBIAS$^2 = 1$</td>
<td>—</td>
<td>360</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$BIASPROG^2 = 0x20$, FULLBIAS$^2 = 1$</td>
<td>—</td>
<td>35</td>
</tr>
<tr>
<td>Offset voltage</td>
<td>$V_{ACMPOFFSET}$</td>
<td>$BIASPROG^2 = 0x10$, FULLBIAS$^2 = 1$</td>
<td>-35</td>
<td>—</td>
</tr>
<tr>
<td>Reference voltage</td>
<td>$V_{ACMPREF}$</td>
<td>Internal 1.25 V reference</td>
<td>1</td>
<td>1.25</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Internal 2.5 V reference</td>
<td>1.98</td>
<td>2.5</td>
</tr>
<tr>
<td>Capacitive sense internal resistance</td>
<td>$R_{CSRES}$</td>
<td>$CSRESSEL^6 = 0$</td>
<td>—</td>
<td>infinite</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$CSRESSEL^6 = 1$</td>
<td>—</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$CSRESSEL^6 = 2$</td>
<td>—</td>
<td>27</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$CSRESSEL^6 = 3$</td>
<td>—</td>
<td>39</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$CSRESSEL^6 = 4$</td>
<td>—</td>
<td>51</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$CSRESSEL^6 = 5$</td>
<td>—</td>
<td>102</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$CSRESSEL^6 = 6$</td>
<td>—</td>
<td>164</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$CSRESSEL^6 = 7$</td>
<td>—</td>
<td>239</td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Test Condition</td>
<td>Min</td>
<td>Typ</td>
</tr>
<tr>
<td>-----------</td>
<td>--------</td>
<td>----------------</td>
<td>-----</td>
<td>-----</td>
</tr>
</tbody>
</table>

**Note:**

1. ACMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD.
2. In ACMPn_CTRL register.
3. The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference. $I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$.
4. In ACMPn_HYSTERESIS registers.
5. ± 100 mV differential drive.
4.1.15 Digital to Analog Converter (VDAC)

DRIVESTRENGTH = 2 unless otherwise specified. Primary VDAC output.

Table 4.32. Digital to Analog Converter (VDAC)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage</td>
<td>( V_{\text{DACOUT}} )</td>
<td>Single-Ended</td>
<td>0</td>
<td>—</td>
<td>( V_{\text{VREF}} )</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Differential(^1)</td>
<td>(-V_{\text{VREF}})</td>
<td>—</td>
<td>( V_{\text{VREF}} )</td>
<td>V</td>
</tr>
<tr>
<td>Current consumption including references (2 channels)(^2)</td>
<td>( I_{\text{DAC}} )</td>
<td>500 ksps, 12-bit, DRIVESTRENGTH = 2, REFSEL = 4</td>
<td>—</td>
<td>396</td>
<td>—</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>44.1 ksps, 12-bit, DRIVESTRENGTH = 1, REFSEL = 4</td>
<td>—</td>
<td>72</td>
<td>—</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>200 Hz refresh rate, 12-bit Sample-Off mode in EM2, DRIVESTRENGTH = 2, BGRREQTIME = 1, EM2REFENTIME = 9, REFSEL = 4, SETTLETIME = 0x0A, WARMUPTIME = 0x02</td>
<td>—</td>
<td>1.2</td>
<td>—</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Current from HFPERCLK(^3)</td>
<td>( I_{\text{DAC_CLK}} )</td>
<td>—</td>
<td>5.8</td>
<td>—</td>
<td>—</td>
<td>( \mu A/\text{MHz} )</td>
</tr>
<tr>
<td>Sample rate</td>
<td>( S_{\text{DAC}} )</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>500</td>
<td>ksps</td>
</tr>
<tr>
<td>DAC clock frequency</td>
<td>( f_{\text{DAC}} )</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>MHz</td>
</tr>
<tr>
<td>Conversion time</td>
<td>( t_{\text{DACCONV}} )</td>
<td>( f_{\text{DAC}} = 1\text{MHz} )</td>
<td>2</td>
<td>—</td>
<td>—</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>Settling time</td>
<td>( t_{\text{DACSETTLE}} )</td>
<td>50% fs step settling to 5 LSB</td>
<td>—</td>
<td>2.5</td>
<td>—</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>Startup time</td>
<td>( t_{\text{DACSTARTUP}} )</td>
<td>Enable to 90% fs output, settling to 10 LSB</td>
<td>—</td>
<td>—</td>
<td>12</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>Output impedance</td>
<td>( R_{\text{OUT}} )</td>
<td>DRIVESTRENGTH = 2, 0.4 ( V ) ( \leq ) ( V_{\text{OUT}} ) ( \leq ) ( V_{\text{OPA}} ) - 0.4 ( V ), (-8 \text{ mA} &lt; I_{\text{OUT}} &lt; 8 \text{ mA}, ) Full supply range</td>
<td>—</td>
<td>2</td>
<td>—</td>
<td>( \Omega )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DRIVESTRENGTH = 0 or 1, 0.4 ( V ) ( \leq ) ( V_{\text{OUT}} ) ( \leq ) ( V_{\text{OPA}} ) - 0.4 ( V ), (-400 \mu A &lt; I_{\text{OUT}} &lt; 400 \mu A, ) Full supply range</td>
<td>—</td>
<td>2</td>
<td>—</td>
<td>( \Omega )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DRIVESTRENGTH = 2, 0.1 ( V ) ( \leq ) ( V_{\text{OUT}} ) ( \leq ) ( V_{\text{OPA}} ) - 0.1 ( V ), (-2 \text{ mA} &lt; I_{\text{OUT}} &lt; 2 \text{ mA}, ) Full supply range</td>
<td>—</td>
<td>2</td>
<td>—</td>
<td>( \Omega )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DRIVESTRENGTH = 0 or 1, 0.1 ( V ) ( \leq ) ( V_{\text{OUT}} ) ( \leq ) ( V_{\text{OPA}} ) - 0.1 ( V ), (-100 \mu A &lt; I_{\text{OUT}} &lt; 100 \mu A, ) Full supply range</td>
<td>—</td>
<td>2</td>
<td>—</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>Power supply rejection ratio(^4)</td>
<td>( \text{PSRR} )</td>
<td>( V_{\text{out}} = 50% \text{ fs. DC} )</td>
<td>—</td>
<td>65.5</td>
<td>—</td>
<td>( \text{dB} )</td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Test Condition</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Unit</td>
</tr>
<tr>
<td>---------------------------------------------------------------------------</td>
<td>-------------------------------</td>
<td>-----------------------------------------------------</td>
<td>-----</td>
<td>------</td>
<td>------</td>
<td>------</td>
</tr>
<tr>
<td>Signal to noise and distortion ratio (1 kHz sine wave),</td>
<td>SNDR&lt;sub&gt;DAC&lt;/sub&gt;</td>
<td>500 ksps, single-ended, internal 1.25V reference</td>
<td>___</td>
<td>60.4</td>
<td>___</td>
<td>dB</td>
</tr>
<tr>
<td>Noise band limited to 250 kHz</td>
<td></td>
<td>500 ksps, single-ended, internal 2.5V reference</td>
<td>___</td>
<td>61.6</td>
<td>___</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500 ksps, single-ended, 3.3V VDD reference</td>
<td>___</td>
<td>64.0</td>
<td>___</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500 ksps, differential, internal 1.25V reference</td>
<td>___</td>
<td>63.3</td>
<td>___</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500 ksps, differential, internal 2.5V reference</td>
<td>___</td>
<td>64.4</td>
<td>___</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500 ksps, differential, 3.3V VDD reference</td>
<td>___</td>
<td>65.8</td>
<td>___</td>
<td>dB</td>
</tr>
<tr>
<td>Signal to noise and distortion ratio (1 kHz sine wave),</td>
<td>SNDR&lt;sub&gt;DAC_BAND&lt;/sub&gt;</td>
<td>500 ksps, single-ended, internal 1.25V reference</td>
<td>___</td>
<td>65.3</td>
<td>___</td>
<td>dB</td>
</tr>
<tr>
<td>Noise band limited to 22 kHz</td>
<td></td>
<td>500 ksps, single-ended, internal 2.5V reference</td>
<td>___</td>
<td>66.7</td>
<td>___</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500 ksps, single-ended, 3.3V VDD reference</td>
<td>___</td>
<td>70.0</td>
<td>___</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500 ksps, differential, internal 1.25V reference</td>
<td>___</td>
<td>67.8</td>
<td>___</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500 ksps, differential, internal 2.5V reference</td>
<td>___</td>
<td>69.0</td>
<td>___</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500 ksps, differential, 3.3V VDD reference</td>
<td>___</td>
<td>68.5</td>
<td>___</td>
<td>dB</td>
</tr>
<tr>
<td>Total harmonic distortion</td>
<td>THD</td>
<td>500 ksps, single-ended, internal 1.25V reference</td>
<td>___</td>
<td>65.3</td>
<td>___</td>
<td>dB</td>
</tr>
<tr>
<td>Differential non-linearity&lt;sup&gt;5&lt;/sup&gt;</td>
<td>DNL&lt;sub&gt;DAC&lt;/sub&gt;</td>
<td>-0.99</td>
<td>___</td>
<td>1</td>
<td>___</td>
<td>LSB</td>
</tr>
<tr>
<td>Intergral non-linearity</td>
<td>INL&lt;sub&gt;DAC&lt;/sub&gt;</td>
<td>-4</td>
<td>___</td>
<td>4</td>
<td>___</td>
<td>LSB</td>
</tr>
<tr>
<td>Offset error&lt;sup&gt;6&lt;/sup&gt;</td>
<td>V&lt;sub&gt;OFFSET&lt;/sub&gt;</td>
<td>T = 25 °C</td>
<td>-8</td>
<td>___</td>
<td>8</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Across operating temperature range</td>
<td>-25</td>
<td>___</td>
<td>25</td>
<td>mV</td>
</tr>
<tr>
<td>Gain error&lt;sup&gt;6&lt;/sup&gt;</td>
<td>V&lt;sub&gt;GAIN&lt;/sub&gt;</td>
<td>T = 25 °C, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN)</td>
<td>-2.5</td>
<td>___</td>
<td>2.5</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>T = 25 °C, Internal reference (REFSEL = 1V25 or 2V5)</td>
<td>-5</td>
<td>___</td>
<td>5</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>T = 25 °C, External reference (REFSEL = VDD or EXT)</td>
<td>-1.8</td>
<td>___</td>
<td>1.8</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Across operating temperature range, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN)</td>
<td>-3.5</td>
<td>___</td>
<td>3.5</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Across operating temperature range, Internal reference (REFSEL = 1V25 or 2V5)</td>
<td>-7.5</td>
<td>___</td>
<td>7.5</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Across operating temperature range, External reference (REFSEL = VDD or EXT)</td>
<td>-2.0</td>
<td>___</td>
<td>2.0</td>
<td>%</td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Test Condition</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Unit</td>
</tr>
<tr>
<td>-----------------------------------------------</td>
<td>--------</td>
<td>----------------</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>------</td>
</tr>
<tr>
<td>External load capacitance, OUTSCALE=0</td>
<td>CLOAD</td>
<td></td>
<td>—</td>
<td>—</td>
<td>75</td>
<td>pF</td>
</tr>
</tbody>
</table>

**Note:**
1. In differential mode, the output is defined as the difference between two single-ended outputs. Absolute voltage on each output is limited to the single-ended range.
2. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load.
3. Current from HFPERCLK is dependent on HFPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC module is enabled in the CMU.
4. PSRR calculated as $20 \times \log_{10}(\Delta VDD / \Delta V_{OUT})$, VDAC output at 90% of full scale.
5. Entire range is monotonic and has no missing codes.
6. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.
### 4.1.16 Current Digital to Analog Converter (IDAC)

#### Table 4.33. Current Digital to Analog Converter (IDAC)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of ranges</td>
<td>( N_{\text{IDAC_RANGES}} )</td>
<td></td>
<td></td>
<td>4</td>
<td></td>
<td>ranges</td>
</tr>
<tr>
<td>Output current</td>
<td>( I_{\text{IDAC_OUT}} )</td>
<td>( \text{RANGSEL}^1 = \text{RANGE0} )</td>
<td>0.05</td>
<td></td>
<td>1.6</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{RANGSEL}^1 = \text{RANGE1} )</td>
<td>1.6</td>
<td></td>
<td>4.7</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{RANGSEL}^1 = \text{RANGE2} )</td>
<td>0.5</td>
<td></td>
<td>16</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{RANGSEL}^1 = \text{RANGE3} )</td>
<td>2</td>
<td></td>
<td>64</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Linear steps within each range</td>
<td>( N_{\text{IDAC_STEPS}} )</td>
<td></td>
<td></td>
<td>32</td>
<td></td>
<td>steps</td>
</tr>
<tr>
<td>Step size</td>
<td>( SS_{\text{IDAC}} )</td>
<td>( \text{RANGSEL}^1 = \text{RANGE0} )</td>
<td></td>
<td>50</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{RANGSEL}^1 = \text{RANGE1} )</td>
<td></td>
<td>100</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{RANGSEL}^1 = \text{RANGE2} )</td>
<td></td>
<td>500</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{RANGSEL}^1 = \text{RANGE3} )</td>
<td></td>
<td>2</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Total accuracy, ( \text{STEPSEL}^1 = 0x10 )</td>
<td>( ACC_{\text{IDAC}} )</td>
<td>( \text{EM0 or EM1, AVDD=3.3 V, T = 25}^\circ \text{C} )</td>
<td>-3</td>
<td></td>
<td>3</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{EM0 or EM1, Across operating temperature range} )</td>
<td>-18</td>
<td></td>
<td>22</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{EM2 or EM3, Source mode, RANGSEL}^1 = \text{RANGE0, AVDD=3.3 V, T = 25}^\circ \text{C} )</td>
<td></td>
<td>-2</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{EM2 or EM3, Source mode, RANGSEL}^1 = \text{RANGE1, AVDD=3.3 V, T = 25}^\circ \text{C} )</td>
<td></td>
<td>-1.7</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{EM2 or EM3, Source mode, RANGSEL}^1 = \text{RANGE2, AVDD=3.3 V, T = 25}^\circ \text{C} )</td>
<td></td>
<td>-0.8</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{EM2 or EM3, Source mode, RANGSEL}^1 = \text{RANGE3, AVDD=3.3 V, T = 25}^\circ \text{C} )</td>
<td></td>
<td>-0.5</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{EM2 or EM3, Sink mode, RANGSEL}^1 = \text{RANGE0, AVDD=3.3 V, T = 25}^\circ \text{C} )</td>
<td></td>
<td>-0.7</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{EM2 or EM3, Sink mode, RANGSEL}^1 = \text{RANGE1, AVDD=3.3 V, T = 25}^\circ \text{C} )</td>
<td></td>
<td>-0.6</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{EM2 or EM3, Sink mode, RANGSEL}^1 = \text{RANGE2, AVDD=3.3 V, T = 25}^\circ \text{C} )</td>
<td></td>
<td>-0.5</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{EM2 or EM3, Sink mode, RANGSEL}^1 = \text{RANGE3, AVDD=3.3 V, T = 25}^\circ \text{C} )</td>
<td></td>
<td>-0.5</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Start up time</td>
<td>( t_{\text{IDAC_SU}} )</td>
<td>Output within 1% of steady state value</td>
<td></td>
<td>5</td>
<td></td>
<td>( \mu s )</td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Test Condition</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Unit</td>
</tr>
<tr>
<td>--------------------------------------------------------------------------</td>
<td>----------</td>
<td>---------------------------------------------------------------------------------</td>
<td>------</td>
<td>------</td>
<td>------</td>
<td>------</td>
</tr>
<tr>
<td>Settling time, (output settled within 1% of steady state value)</td>
<td>$t_{IDAC_SETTLE}$</td>
<td>Range setting is changed</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Step value is changed</td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>µs</td>
</tr>
<tr>
<td>Current consumption$^2$</td>
<td>$I_{IDAC}$</td>
<td>EM0 or EM1 Source mode, excluding output current, Across operating temperature range</td>
<td>—</td>
<td>11</td>
<td>15</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EM0 or EM1 Sink mode, excluding output current, Across operating temperature range</td>
<td>—</td>
<td>13</td>
<td>18</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EM2 or EM3 Source mode, excluding output current, T = 25 °C</td>
<td>—</td>
<td>0.023</td>
<td>—</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EM2 or EM3 Sink mode, excluding output current, T = 25 °C</td>
<td>—</td>
<td>0.041</td>
<td>—</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EM2 or EM3 Source mode, excluding output current, T ≥ 85 °C</td>
<td>—</td>
<td>11</td>
<td>—</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EM2 or EM3 Sink mode, excluding output current, T ≥ 85 °C</td>
<td>—</td>
<td>13</td>
<td>—</td>
<td>µA</td>
</tr>
<tr>
<td>Output voltage compliance in source mode, source current change relative to current sourced at 0 V</td>
<td>$I_{COMP_SRC}$</td>
<td>RANGESEL1=0, output voltage = min($V_{IOVDD}$, $V_{AVDD2}$-100 mV)</td>
<td>—</td>
<td>0.11</td>
<td>—</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RANGESEL1=1, output voltage = min($V_{IOVDD}$, $V_{AVDD2}$-100 mV)</td>
<td>—</td>
<td>0.06</td>
<td>—</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RANGESEL1=2, output voltage = min($V_{IOVDD}$, $V_{AVDD2}$-150 mV)</td>
<td>—</td>
<td>0.04</td>
<td>—</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RANGESEL1=3, output voltage = min($V_{IOVDD}$, $V_{AVDD2}$-250 mV)</td>
<td>—</td>
<td>0.03</td>
<td>—</td>
<td>%</td>
</tr>
<tr>
<td>Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD</td>
<td>$I_{COMP_SINK}$</td>
<td>RANGESEL1=0, output voltage = 100 mV</td>
<td>—</td>
<td>0.12</td>
<td>—</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RANGESEL1=1, output voltage = 100 mV</td>
<td>—</td>
<td>0.05</td>
<td>—</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RANGESEL1=2, output voltage = 150 mV</td>
<td>—</td>
<td>0.04</td>
<td>—</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RANGESEL1=3, output voltage = 250 mV</td>
<td>—</td>
<td>0.03</td>
<td>—</td>
<td>%</td>
</tr>
</tbody>
</table>

Note:
1. In IDAC_CURPROG register.
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRES in the IDAC_CTRL register. Setting PWRES to 1 selects IOVDD. With PWRES cleared to 0, ANASW selects between AVDD (0) and DVDD (1).
### 4.1.17 Capacitive Sense (CSEN)

#### Table 4.34. Capacitive Sense (CSEN)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single conversion time (1x accumulation)</td>
<td>$t_{CNV}$</td>
<td>12-bit SAR Conversions</td>
<td>—</td>
<td>20.2</td>
<td>—</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>16-bit SAR Conversions</td>
<td>—</td>
<td>26.4</td>
<td>—</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Delta Modulation Conversion (single comparison)</td>
<td>—</td>
<td>1.55</td>
<td>—</td>
<td>µs</td>
</tr>
<tr>
<td>Maximum external capacitive load</td>
<td>$C_{EXTMAX}$</td>
<td>IREFPROG=7 (Gain = 1x), including routing parasitics</td>
<td>—</td>
<td>68</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IREFPROG=0 (Gain = 10x), including routing parasitics</td>
<td>—</td>
<td>680</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td>Maximum external series impedance</td>
<td>$R_{EXTMAX}$</td>
<td></td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>kΩ</td>
</tr>
<tr>
<td>Supply current, EM2 bonded conversions, WARMUP-MODE=NORMAL, WAR-MUPCNT=0</td>
<td>$I_{CSEN_BOND}$</td>
<td>12-bit SAR conversions, 20 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)&lt;sup&gt;1&lt;/sup&gt;</td>
<td>—</td>
<td>326</td>
<td>—</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Delta Modulation conversions, 20 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)&lt;sup&gt;1&lt;/sup&gt;</td>
<td>—</td>
<td>226</td>
<td>—</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12-bit SAR conversions, 200 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)&lt;sup&gt;1&lt;/sup&gt;</td>
<td>—</td>
<td>33</td>
<td>—</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Delta Modulation conversions, 200 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)&lt;sup&gt;1&lt;/sup&gt;</td>
<td>—</td>
<td>25</td>
<td>—</td>
<td>nA</td>
</tr>
<tr>
<td>Supply current, EM2 scan conversions, WARMUP-MODE=NORMAL, WAR-MUPCNT=0</td>
<td>$I_{CSEN_EM2}$</td>
<td>12-bit SAR conversions, 20 ms scan rate, IREFPROG=0 (Gain = 10x), 8 samples per scan&lt;sup&gt;1&lt;/sup&gt;</td>
<td>—</td>
<td>690</td>
<td>—</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Delta Modulation conversions, 20 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), IREFPROG=0 (Gain = 10x), 8 samples per scan&lt;sup&gt;1&lt;/sup&gt;</td>
<td>—</td>
<td>515</td>
<td>—</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12-bit SAR conversions, 200 ms scan rate, IREFPROG=0 (Gain = 10x), 8 samples per scan&lt;sup&gt;1&lt;/sup&gt;</td>
<td>—</td>
<td>79</td>
<td>—</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Delta Modulation conversions, 200 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), IREFPROG=0 (Gain = 10x), 8 samples per scan&lt;sup&gt;1&lt;/sup&gt;</td>
<td>—</td>
<td>57</td>
<td>—</td>
<td>nA</td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Test Condition</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Unit</td>
</tr>
<tr>
<td>---------------------------------------------------------------------------</td>
<td>-------------</td>
<td>---------------------------------------------------------------------------------</td>
<td>-----</td>
<td>------</td>
<td>------</td>
<td>--------</td>
</tr>
<tr>
<td>Supply current, continuous conversions, WARMUP-MODE=KEEPCSENWARM</td>
<td>I_{CSEN_ACTIVE}</td>
<td>SAR or Delta Modulation conversions of 33 pF capacitor, IREFPROG=0 (Gain = 10x), always on</td>
<td></td>
<td>90.5</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>HFPERCLK supply current</td>
<td>I_{CSEN_HFPERCLK}</td>
<td>Current contribution from HFPERCLK when clock to CSEN block is enabled.</td>
<td></td>
<td>2.25</td>
<td></td>
<td>µA/MHz</td>
</tr>
</tbody>
</table>

**Note:**

1. Current is specified with a total external capacitance of 33 pF per channel. Average current is dependent on how long the module is actively sampling channels within the scan period, and scales with the number of samples acquired. Supply current for a specific application can be estimated by multiplying the current per sample by the total number of samples per period (total_current = single_sample_current * (number_of_channels * accumulation)).
4.18 Operational Amplifier (OPAMP)

Unless otherwise indicated, specified conditions are: Non-inverting input configuration, VDD = 3.3 V, DRIVESTRENGTH = 2, MAIN-OUTEN = 1, CLOAD = 75 pF with OUTSCALE = 0, or CLOAD = 37.5 pF with OUTSCALE = 1. Unit gain buffer and 3X-gain connection as specified in table footnotes.1 2

Table 4.35. Operational Amplifier (OPAMP)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage (from AVDD)</td>
<td>VOPA</td>
<td>HCMDIS = 0, Rail-to-rail input range</td>
<td>2</td>
<td>—</td>
<td>3.8</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HCMDIS = 1</td>
<td>1.62</td>
<td>—</td>
<td>3.8</td>
<td>V</td>
</tr>
<tr>
<td>Input voltage</td>
<td>VIN</td>
<td>HCMDIS = 0, Rail-to-rail input range</td>
<td>VVSS</td>
<td>—</td>
<td>VOPA</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HCMDIS = 1</td>
<td>VVSS</td>
<td>—</td>
<td>VOPA</td>
<td>V</td>
</tr>
<tr>
<td>Input impedance</td>
<td>RIN</td>
<td></td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>MΩ</td>
</tr>
<tr>
<td>Output voltage</td>
<td>VOUT</td>
<td>VVSS</td>
<td>—</td>
<td>—</td>
<td>VOPA</td>
<td>V</td>
</tr>
<tr>
<td>Load capacitance</td>
<td>CLOAD</td>
<td>OUTSCALE = 0</td>
<td>—</td>
<td>—</td>
<td>75</td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OUTSCALE = 1</td>
<td>—</td>
<td>—</td>
<td>37.5</td>
<td>pF</td>
</tr>
<tr>
<td>Output impedance</td>
<td>ROUT</td>
<td>DRIVESTRENGTH = 2 or 3, 0.4 V ≤ VOUT ≤ VOPA - 0.4 V, -8 mA &lt; IOUT &lt; 8 mA, Buffer connection, Full supply range</td>
<td>—</td>
<td>0.25</td>
<td>—</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DRIVESTRENGTH = 0 or 1, 0.4 V ≤ VOUT ≤ VOPA - 0.4 V, -400 μA &lt; IOUT &lt; 400 μA, Buffer connection, Full supply range</td>
<td>—</td>
<td>0.6</td>
<td>—</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DRIVESTRENGTH = 2 or 3, 0.1 V ≤ VOUT ≤ VOPA - 0.1 V, -2 mA &lt; IOUT &lt; 2 mA, Buffer connection, Full supply range</td>
<td>—</td>
<td>0.4</td>
<td>—</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DRIVESTRENGTH = 0 or 1, 0.1 V ≤ VOUT ≤ VOPA - 0.1 V, -100 μA &lt; IOUT &lt; 100 μA, Buffer connection, Full supply range</td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>Ω</td>
</tr>
<tr>
<td>Internal closed-loop gain</td>
<td>GCL</td>
<td>Buffer connection</td>
<td>0.99</td>
<td>1</td>
<td>1.01</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3x Gain connection</td>
<td>2.93</td>
<td>2.99</td>
<td>3.05</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>16x Gain connection</td>
<td>15.07</td>
<td>15.7</td>
<td>16.33</td>
<td>-</td>
</tr>
<tr>
<td>Active current</td>
<td>IOPA</td>
<td>DRIVESTRENGTH = 3, OUT-SCALE = 0</td>
<td>—</td>
<td>580</td>
<td>—</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DRIVESTRENGTH = 2, OUT-SCALE = 0</td>
<td>—</td>
<td>176</td>
<td>—</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DRIVESTRENGTH = 1, OUT-SCALE = 0</td>
<td>—</td>
<td>13</td>
<td>—</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DRIVESTRENGTH = 0, OUT-SCALE = 0</td>
<td>—</td>
<td>4.7</td>
<td>—</td>
<td>μA</td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Test Condition</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Unit</td>
</tr>
<tr>
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<td>--------</td>
<td>-------------------------</td>
<td>------</td>
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<tr>
<td>Open-loop gain</td>
<td>G\text{OL}</td>
<td>DRIVESTRENGTH = 3</td>
<td></td>
<td>135</td>
<td></td>
<td>dB</td>
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<td>DRIVESTRENGTH = 2</td>
<td></td>
<td>137</td>
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<td>dB</td>
</tr>
<tr>
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<td></td>
<td>DRIVESTRENGTH = 1</td>
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<td>121</td>
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<td>dB</td>
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<td>DRIVESTRENGTH = 0</td>
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<td>109</td>
<td></td>
<td>dB</td>
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<tr>
<td>Loop unit-gain frequency</td>
<td>UGF</td>
<td>DRIVESTRENGTH = 3, Buffer connection</td>
<td></td>
<td>3.38</td>
<td></td>
<td>MHz</td>
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<td></td>
<td>DRIVESTRENGTH = 2, Buffer connection</td>
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<td>0.9</td>
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<td>MHz</td>
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<td></td>
<td></td>
<td>DRIVESTRENGTH = 1, Buffer connection</td>
<td></td>
<td>132</td>
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<td>kHz</td>
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<td></td>
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<td>DRIVESTRENGTH = 0, Buffer connection</td>
<td></td>
<td>34</td>
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<td>kHz</td>
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<td></td>
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<td>DRIVESTRENGTH = 3, 3x Gain connection</td>
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<td>2.57</td>
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<td>MHz</td>
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<td></td>
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<td>DRIVESTRENGTH = 2, 3x Gain connection</td>
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<td>0.71</td>
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<td>DRIVESTRENGTH = 1, 3x Gain connection</td>
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<td>113</td>
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<td>DRIVESTRENGTH = 0, 3x Gain connection</td>
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<tr>
<td>Phase margin</td>
<td>PM</td>
<td>DRIVESTRENGTH = 3, Buffer connection</td>
<td></td>
<td>67</td>
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<td>DRIVESTRENGTH = 2, Buffer connection</td>
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<td>69</td>
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<td>°</td>
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<td>DRIVESTRENGTH = 1, Buffer connection</td>
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<td>63</td>
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<td>°</td>
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<td>DRIVESTRENGTH = 0, Buffer connection</td>
<td></td>
<td>68</td>
<td></td>
<td>°</td>
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<tr>
<td>Output voltage noise</td>
<td>N\text{OUT}</td>
<td>DRIVESTRENGTH = 3, Buffer connection, 10 Hz - 10 MHz</td>
<td></td>
<td>146</td>
<td></td>
<td>µVrms</td>
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<td>DRIVESTRENGTH = 2, Buffer connection, 10 Hz - 10 MHz</td>
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<td>163</td>
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<td>µVrms</td>
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<tr>
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<td></td>
<td>DRIVESTRENGTH = 1, Buffer connection, 10 Hz - 1 MHz</td>
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<td>170</td>
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<td>µVrms</td>
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<tr>
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<td></td>
<td>DRIVESTRENGTH = 0, Buffer connection, 10 Hz - 1 MHz</td>
<td></td>
<td>176</td>
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<td>µVrms</td>
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<td></td>
<td>DRIVESTRENGTH = 3, 3x Gain connection, 10 Hz - 10 MHz</td>
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<td>313</td>
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<td>µVrms</td>
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<td></td>
<td>DRIVESTRENGTH = 2, 3x Gain connection, 10 Hz - 10 MHz</td>
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<td>271</td>
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<td>µVrms</td>
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<td></td>
<td>DRIVESTRENGTH = 1, 3x Gain connection, 10 Hz - 1 MHz</td>
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<td>µVrms</td>
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<td></td>
<td>DRIVESTRENGTH = 0, 3x Gain connection, 10 Hz - 1 MHz</td>
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<td>245</td>
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<td>µVrms</td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Test Condition</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Unit</td>
</tr>
<tr>
<td>--------------------</td>
<td>--------</td>
<td>---------------------------------------------------------------------------------</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>-------</td>
</tr>
<tr>
<td>Slew rate(^6)</td>
<td>SR</td>
<td>\text{DRIVESTRENGTH} = 3, \text{INCBW}=1(^7)</td>
<td></td>
<td>4.7</td>
<td></td>
<td>V/µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>\text{DRIVESTRENGTH} = 3, \text{INCBW}=0</td>
<td></td>
<td>1.5</td>
<td></td>
<td>V/µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>\text{DRIVESTRENGTH} = 2, \text{INCBW}=1(^7)</td>
<td></td>
<td>1.27</td>
<td></td>
<td>V/µs</td>
</tr>
<tr>
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<td></td>
<td>\text{DRIVESTRENGTH} = 2, \text{INCBW}=0</td>
<td></td>
<td>0.42</td>
<td></td>
<td>V/µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>\text{DRIVESTRENGTH} = 1, \text{INCBW}=1(^7)</td>
<td></td>
<td>0.17</td>
<td></td>
<td>V/µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>\text{DRIVESTRENGTH} = 1, \text{INCBW}=0</td>
<td></td>
<td>0.058</td>
<td></td>
<td>V/µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>\text{DRIVESTRENGTH} = 0, \text{INCBW}=1(^7)</td>
<td></td>
<td>0.044</td>
<td></td>
<td>V/µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>\text{DRIVESTRENGTH} = 0, \text{INCBW}=0</td>
<td></td>
<td>0.015</td>
<td></td>
<td>V/µs</td>
</tr>
<tr>
<td>Startup time(^8)</td>
<td>T(_{\text{START}})</td>
<td>\text{DRIVESTRENGTH} = 2</td>
<td></td>
<td></td>
<td>12</td>
<td>µs</td>
</tr>
<tr>
<td>Input offset voltage</td>
<td>V(_{\text{OSI}})</td>
<td>\text{DRIVESTRENGTH} = 2 or 3, (T = 25\ ^\circ\text{C})</td>
<td>-2</td>
<td></td>
<td>2</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>\text{DRIVESTRENGTH} = 1 or 0, (T = 25\ ^\circ\text{C})</td>
<td>-2</td>
<td></td>
<td>2</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>\text{DRIVESTRENGTH} = 2 or 3, across operating temperature range</td>
<td>-12</td>
<td></td>
<td>12</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>\text{DRIVESTRENGTH} = 1 or 0, across operating temperature range</td>
<td>-30</td>
<td></td>
<td>30</td>
<td>mV</td>
</tr>
<tr>
<td>DC power supply rejection ratio(^9)</td>
<td>PSRR(_{\text{DC}})</td>
<td>Input referred</td>
<td></td>
<td>70</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>DC common-mode rejection ratio(^9)</td>
<td>CMRR(_{\text{DC}})</td>
<td>Input referred</td>
<td></td>
<td>70</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Total harmonic distortion</td>
<td>THD(_{\text{OPA}})</td>
<td>\text{DRIVESTRENGTH} = 2, 3x Gain connection, (1 \text{ kHz}, V_{\text{OUT}} = 0.1 \text{ V to V}_{\text{OPA}} = 0.1 \text{ V})</td>
<td></td>
<td>90</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>\text{DRIVESTRENGTH} = 0, 3x Gain connection, (0.1 \text{ kHz}, V_{\text{OUT}} = 0.1 \text{ V to V}_{\text{OPA}} = 0.1 \text{ V})</td>
<td></td>
<td>90</td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>
### Electrical Specifications

#### Parameter Symbol Test Condition Min Typ Max Unit

**Note:**

1. Specified configuration for Unit gain buffer configuration is: INCBW = 0, HCMDIS = 0, RESINSEL = DISABLE. V\(_{\text{INPUT}}\) = 0.5 V, V\(_{\text{OUTPUT}}\) = 0.5 V.
2. Specified configuration for 3X-Gain configuration is: INCBW = 1, HCMDIS = 1, RESINSEL = VSS, V\(_{\text{INPUT}}\) = 0.5 V, V\(_{\text{OUTPUT}}\) = 1.5 V. Nominal voltage gain is 3.
3. If the maximum C\(_{\text{LOAD}}\) is exceeded, an isolation resistor is required for stability. See AN0038 for more information.
4. Current into the load resistor is excluded. When the OPAMP is connected with closed-loop gain > 1, there will be extra current to drive the resistor feedback network. The internal resistor feedback network has total resistance of 143.5 kOhm, which will cause another ~10 µA current when the OPAMP drives 1.5 V between output and ground.
5. In unit gain connection, UGF is the gain-bandwidth product of the OPAMP. In 3x Gain connection, UGF is the gain-bandwidth product of the OPAMP and 1/3 attenuation of the feedback network.
6. Step between 0.2V and V\(_{\text{OPA}}\)-0.2V, 10%-90% rising/falling range.
7. When INCBW is set to 1 the OPAMP bandwidth is increased. This is allowed only when the non-inverting close-loop gain is ≥ 3, or the OPAMP may not be stable.
8. From enable to output settled. In sample-and-off mode, RC network after OPAMP will contribute extra delay. Settling error < 1mV.
9. When HCMDIS=1 and input common mode transitions the region from V\(_{\text{OPA}}\)-1.4V to V\(_{\text{OPA}}\)-1V, input offset will change. PSRR and CMRR specifications do not apply to this transition region.

#### 4.1.19 Pulse Counter (PCNT)

**Table 4.36. Pulse Counter (PCNT)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input frequency</td>
<td>F(_{\text{IN}})</td>
<td>Asynchronous Single and Quadrature Modes</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sampled Modes with Debounce filter set to 0</td>
<td>—</td>
<td>—</td>
<td>8</td>
<td>kHz</td>
</tr>
</tbody>
</table>

#### 4.1.20 Analog Port (APORT)

**Table 4.37. Analog Port (APORT)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply current¹ ²</td>
<td>I(_{\text{APORT}})</td>
<td>Operation in EM0/EM1</td>
<td>—</td>
<td>7</td>
<td>—</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Operation in EM2/EM3</td>
<td>—</td>
<td>63</td>
<td>—</td>
<td>nA</td>
</tr>
</tbody>
</table>

**Note:**

1. Supply current increase that occurs when an analog peripheral requests access to APORT. This current is not included in reported module currents. Additional peripherals requesting access to APORT do not incur further current.
2. Specified current is for continuous APORT operation. In applications where the APORT is not requested continuously (e.g. periodic ACMP requests from LESENSE in EM2), the average current requirements can be estimated by multiplying the duty cycle of the requests by the specified continuous current number.
### 4.1.21 I2C

#### 4.1.21.1 I2C Standard-mode (Sm)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCL clock frequency$^2$</td>
<td>$f_{SCL}$</td>
<td></td>
<td>0</td>
<td></td>
<td>100</td>
<td>kHz</td>
</tr>
<tr>
<td>SCL clock low time $t_{LOW}$</td>
<td></td>
<td></td>
<td>4.7</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>SCL clock high time $t_{HIGH}$</td>
<td></td>
<td></td>
<td>4</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>SDA set-up time $t_{SU_DAT}$</td>
<td></td>
<td></td>
<td>250</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>SDA hold time$^3$ $t_{HD_DAT}$</td>
<td></td>
<td></td>
<td>100</td>
<td></td>
<td>3450</td>
<td>ns</td>
</tr>
<tr>
<td>Repeated START condition set-up time</td>
<td>$t_{SU_STA}$</td>
<td></td>
<td>4.7</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>(Repeated) START condition hold time</td>
<td>$t_{HD_STA}$</td>
<td></td>
<td>4</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>STOP condition set-up time $t_{SU_STO}$</td>
<td></td>
<td></td>
<td>4</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Bus free time between a STOP and START condition $t_{BUF}$</td>
<td></td>
<td></td>
<td>4.7</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
</tbody>
</table>

**Note:**
1. For CLHR set to 0 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time ($t_{HD_DAT}$) needs to be met only when the device does not stretch the low time of SCL ($t_{LOW}$).
### 4.1.21.2 I2C Fast-mode (Fm)$^1$

Table 4.39. I2C Fast-mode (Fm)$^1$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCL clock frequency$^2$</td>
<td>$f_{SCL}$</td>
<td></td>
<td>0</td>
<td></td>
<td>400</td>
<td>kHz</td>
</tr>
<tr>
<td>SCL clock low time</td>
<td>$t_{LOW}$</td>
<td></td>
<td>1.3</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>SCL clock high time</td>
<td>$t_{HIGH}$</td>
<td></td>
<td>0.6</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>SDA set-up time</td>
<td>$t_{SU_DAT}$</td>
<td></td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>SDA hold time$^3$</td>
<td>$t_{HD_DAT}$</td>
<td></td>
<td>100</td>
<td></td>
<td>900</td>
<td>ns</td>
</tr>
<tr>
<td>Repeated START condition set-up time</td>
<td>$t_{SU_STA}$</td>
<td></td>
<td>0.6</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>(Repeated) START condition hold time</td>
<td>$t_{HD_STA}$</td>
<td></td>
<td>0.6</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>STOP condition set-up time</td>
<td>$t_{SU_STO}$</td>
<td></td>
<td>0.6</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Bus free time between a STOP and START condition</td>
<td>$t_{BUF}$</td>
<td></td>
<td>1.3</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
</tbody>
</table>

**Note:**
1. For CLHR set to 1 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time ($t_{HD\_DAT}$) needs to be met only when the device does not stretch the low time of SCL ($t_{LOW}$).
4.1.21.3 I2C Fast-mode Plus (Fm+)¹

Table 4.40. I2C Fast-mode Plus (Fm+)¹

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCL clock frequency²</td>
<td>fSCL</td>
<td></td>
<td>0</td>
<td>—</td>
<td>1000</td>
<td>kHz</td>
</tr>
<tr>
<td>SCL clock low time</td>
<td>tLOW</td>
<td></td>
<td>0.5</td>
<td>—</td>
<td>—</td>
<td>µs</td>
</tr>
<tr>
<td>SCL clock high time</td>
<td>tHIGH</td>
<td></td>
<td>0.26</td>
<td>—</td>
<td>—</td>
<td>µs</td>
</tr>
<tr>
<td>SDA set-up time</td>
<td>tSU_DAT</td>
<td></td>
<td>50</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>SDA hold time</td>
<td>tHD_DAT</td>
<td></td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Repeated START condition set-up time</td>
<td>tSU_STA</td>
<td></td>
<td>0.26</td>
<td>—</td>
<td>—</td>
<td>µs</td>
</tr>
<tr>
<td>(Repeated) START condition hold time</td>
<td>tHD_STA</td>
<td></td>
<td>0.26</td>
<td>—</td>
<td>—</td>
<td>µs</td>
</tr>
<tr>
<td>STOP condition set-up time</td>
<td>tSU_STO</td>
<td></td>
<td>0.26</td>
<td>—</td>
<td>—</td>
<td>µs</td>
</tr>
<tr>
<td>Bus free time between a STOP and START condition</td>
<td>tBUF</td>
<td></td>
<td>0.5</td>
<td>—</td>
<td>—</td>
<td>µs</td>
</tr>
</tbody>
</table>

Note:

1. For CLHR set to 0 or 1 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual.
## 4.1.22 USART SPI

### SPI Master Timing

Table 4.41. SPI Master Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCLK period</td>
<td>tSCLK</td>
<td></td>
<td>2 *</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>tHFPERCLK</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CS to MOSI</td>
<td>tCS_MO</td>
<td></td>
<td>-12.5</td>
<td></td>
<td>14</td>
<td>ns</td>
</tr>
<tr>
<td>SCLK to MOSI</td>
<td>tSCLK_MO</td>
<td></td>
<td>-8.5</td>
<td></td>
<td>10.5</td>
<td>ns</td>
</tr>
<tr>
<td>MISO setup time</td>
<td>tSU_MI</td>
<td>IOVDD = 1.62 V</td>
<td>90</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IOVDD = 3.0 V</td>
<td>42</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>MISO hold time</td>
<td>tH_MI</td>
<td></td>
<td>-9</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

**Note:**
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of VDD (figure shows 50% of VDD).
3. tHFPERCLK is one period of the selected HFPERCLK.

![Figure 4.1. SPI Master Timing Diagram](image-url)
## SPI Slave Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCLK period 1 2 3</td>
<td>t_SCLK</td>
<td></td>
<td>6 * t_HFPERCLK</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>SCLK high time 1 2 3</td>
<td>t_SCLK_HI</td>
<td></td>
<td>2.5 * t_HFPERCLK</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>SCLK low time 1 2 3</td>
<td>t_SCLK_LO</td>
<td></td>
<td>2.5 * t_HFPERCLK</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>CS active to MISO 1 2</td>
<td>t_CS_ACT_MI</td>
<td></td>
<td>4</td>
<td>—</td>
<td>70</td>
<td>ns</td>
</tr>
<tr>
<td>CS disable to MISO 1 2</td>
<td>t_CS_DIS_MI</td>
<td></td>
<td>4</td>
<td>—</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>MOSI setup time 1 2</td>
<td>t_SU_MO</td>
<td></td>
<td>12.5</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>MOSI hold time 1 2 3</td>
<td>t_H_MO</td>
<td></td>
<td>13</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>SCLK to MISO 1 2 3</td>
<td>t_SCLK_MI</td>
<td></td>
<td>6 + 1.5 * t_HFPERCLK</td>
<td>—</td>
<td>45 + 2.5 * t_HFPERCLK</td>
<td>ns</td>
</tr>
</tbody>
</table>

### Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of V_DD (figure shows 50% of V_DD).
3. t_HFPERCLK is one period of the selected HFPERCLK.

### Figure 4.2. SPI Slave Timing Diagram
5. Typical Connection Diagrams

5.1 Typical MGM13S Connections

Typical connections for the MGM13S module are shown in Figure 5.1 Typical Connections for MGM13S with UART Network Co-Processor on page 68 and Figure 5.2 Typical Connections for MGM13S with SPI Network Co-Processor on page 69. These diagrams show connections for:

- Power supplies
- Antenna loop for internal antenna usage or external antenna connection - The RF and ANTENNA pins should be tied together for correct operation of the module. An optional 0R resistor can be added between RF and ANTENNA, making it possible to measure the signal between these pins.
- Reset line
- UART or SPI connection to an external host for Network Co-Processor (NCP) usage (optional)
- 32.768 kHz crystal - Required in applications that must meet 500 ppm Bluetooth Sleep Clock accuracy requirement. More accurate crystals can be used to reduce the listening window and thereby reduce overall current consumption. Recommended crystal is KDS part number 1TJG125DP1A0012 or equivalent.

Note: It is recommended to connect the RESETn line to the host CPU when NCP mode is used.

![Diagram of MGM13S connections](image-url)

Figure 5.1. Typical Connections for MGM13S with UART Network Co-Processor
Figure 5.2. Typical Connections for MGM13S with SPI Network Co-Processor

Note: It is possible to power the IOVDD pin at 1.8 V from the DC-DC output (1V8). However, the 1V8 output is off by default, and IOVDD must be powered when programming the device. Any system that powers IOVDD directly from 1V8 must power IOVDD externally during initial programming.

Two common debug interface options are shown in Figure 5.3 Common Debug Connections on page 69. Refer to AN958 for more information and additional options.

Figure 5.3. Common Debug Connections
6. Layout Guidelines

For optimal performance of the MGM13S, please follow the PCB layout guidelines and ground plane recommendations indicated in this section.

6.1 Layout Guidelines

This section contains generic PCB layout and design guidelines for the MGM13S module. For optimal performance:
- Place the module at the edge of the PCB, as shown in the figures in this chapter.
- Do not place any metal (traces, components, etc.) in the antenna clearance area.
- Connect all ground pads directly to a solid ground plane.
- Place the ground vias as close to the ground pads as possible.

![Figure 6.1. MGM13S PCB Top Layer Design](image)

The following rules are recommended for the PCB design:
- Trace to copper clearance 150um
- PTH drill size 300um
- PTH annular ring 150um

**Important:**

The antenna area must align with the pads precisely. Please refer to the recommended PCB land pattern for exact dimensions.

![Figure 6.2. MGM13S PCB Middle and Bottom Layer Design](image)
Layout checklist for MGM13S:
1. Antenna area is aligned relative to the module pads as shown in the recommended PCB land pattern.
2. Clearance area within the inner layers and bottom layer is covering the whole antenna area as shown in the layout guidelines.
3. The antenna loop is implemented on the top layer as shown in the layout guidelines.
4. All dimensions within the antenna area are precisely as shown in the recommended PCB land pattern.
5. The module is placed near the edge of the PCB with max 1mm indentation.
6. The module is not placed in the corner of the PCB.

6.2 Effect of PCB Width

The MGM13S module should be placed at the center of the PCB edge. The width of the board has an impact to the radiated efficiency and, more importantly, there should be enough ground plane on both sides of the module for optimal antenna performance. Figure 6.4 MGM13S PCB Top Layer Design on page 71 gives an indication of ground plane size vs. maximum achievable range.

The impact of the board size to the radiated performance is a generic feature of all PCB and chip antennas and it is not a unique feature of the MGM13S. For the MGM13S the depth of the board is not important and does not impact the radiated performance.
6.3 Effect of Plastic and Metal Materials

The antenna on the MGM13S is insensitive to the effects of nearby plastic and other materials with low dielectric constant. No separation between the MGM13S and plastic or other materials is needed. The board thickness does not have any impact on the module either.

Any metal within the antenna area or in close proximity to the antenna area may detune the antenna. In this case it is possible to retune the antenna by adjusting the width of the antenna loop. To avoid detuning of the antenna, the minimum distance to any metal should be more than 3 mm. Encapsulating the module inside metal casing will prevent the radiation of the antenna.

Figure 6.5 Antenna Tuning on page 72 shows how it is possible to adjust the frequency of the antenna by adjusting the width of the antenna loop. The antenna is extremely robust against any objects in close proximity or in direct contact with the antenna and it is recommended not to adjust the dimensions of the antenna area unless it is clear that a metal object, such as a coin cell battery, within the antenna area is detuning the antenna.

![Antenna Tuning Diagram]

Figure 6.5. Antenna Tuning

6.4 Effects of Human Body

Placing the module in contact with or very close to the human body will negatively impact antenna efficiency and reduce range.
6.5 2D Radiation Pattern Plots

Figure 6.6. Typical 2D Radiation Pattern – Front View

Figure 6.7. Typical 2D Radiation Pattern – Side View
Figure 6.8. Typical 2D Radiation Pattern – Top View
7. Pin Definitions

7.1 MGM13S Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 7.2 GPIO Functionality Table or 7.3 Alternate Functionality Overview.
### Table 7.1. MGM13S Device Pinout

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin(s)</th>
<th>Description</th>
<th>Pin Name</th>
<th>Pin(s)</th>
<th>Description</th>
</tr>
</thead>
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<tr>
<td>VSS</td>
<td>1-51</td>
<td>Ground</td>
<td>ANTENNA</td>
<td>2</td>
<td>50 Ohm input pin for internal antenna.</td>
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<tr>
<td>RF</td>
<td>3</td>
<td>50 Ohm I/O for external antenna connection.</td>
<td>PD9</td>
<td>6</td>
<td>GPIO (5V)</td>
</tr>
<tr>
<td>PD10</td>
<td>7</td>
<td>GPIO (5V)</td>
<td>PD11</td>
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<td>GPIO (5V)</td>
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<tr>
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<td>GPIO (5V)</td>
<td>PD13</td>
<td>10</td>
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</tr>
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<td>PD14</td>
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<td>PD15</td>
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<td>PB14</td>
<td>21</td>
<td>GPIO</td>
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<tr>
<td>VBATT</td>
<td>22</td>
<td>Battery supply voltage input to the internal DC-DC and analog supply.</td>
<td>1V8</td>
<td>23</td>
<td>1.8V output of the internal DC-DC converter. Internally decoupled - do not add external decoupling.</td>
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<td>IOVDD</td>
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<td>Digital IO power supply.</td>
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<td>GPIO (5V)</td>
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<td>GPIO (5V)</td>
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<tr>
<td>PF7</td>
<td>43</td>
<td>GPIO (5V)</td>
<td>RESETn</td>
<td>44</td>
<td>Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.</td>
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<td>ANT_GND</td>
<td>47</td>
<td>Antenna ground.</td>
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**Note:**
1. GPIO with 5V tolerance are indicated by (5V).
7.2 GPIO Functionality Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of each GPIO pin, followed by the functionality available on that pin. Refer to 7.3 Alternate Functionality Overview for a list of GPIO locations available for each function.

<table>
<thead>
<tr>
<th>GPIO Name</th>
<th>Pin Alternate Functionality / Description</th>
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<tr>
<td>PA0</td>
<td>BUSDY BUSCX ADC0_EXTN</td>
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<td>TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CCO #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 WTIM0_CC0 #0 LE- TIM0_OUT0 #0 LE- TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31</td>
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<tr>
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<td>US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31</td>
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<td>FRC_DCLK #0 FRC_DOUT #31 FRC_DFRAME #30 MODEM_DCLK #0 MODEM_DIN #31 MODEM_DOUT #30</td>
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<td>BUSCY BUSDX ADC0_EXTP VDAC0_EXT VDAC0_EXT / OPA1_OUTALT #1 BUSDY BUSCX OPA0_P</td>
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<td>TIM0_CC0 #1 TIM0_CC1 #0 TIM0_CC2 #31 TIM0_CDTI0 #30 TIM0_CDTI1 #29 TIM0_CDTI2 #28 TIM1_CCO #1 TIM1_CC1 #0 TIM1_CC2 #31 TIM1_CC3 #30 WTIM0_CC0 #1 LE- TIM0_OUT0 #1 LE- TIM0_OUT1 #0 PCNT0_S0IN #1 PCNT0_S1IN #0</td>
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<tr>
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<td>US0_TX #1 US0_RX #0 US0_CLK #31 US0_CS #30 US0_CTS #29 US0_RTS #28 US1_TX #1 US1_RX #0 US1_CLK #31 US1_CS #30 US1_CTS #29 US1_RTS #28 LEU0_TX #1 LEU0_RX #0 I2C0_SDA #1 I2C0_SCL #0</td>
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<td>VDAC0_OUT1ALT / OPA1_OUTALT #1 BUSDY BUSCX OPA0_P</td>
</tr>
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<td>TIM0_CC0 #2 TIM0_CC1 #1 TIM0_CC2 #0 TIM0_CDTI0 #31 TIM0_CDTI1 #30 TIM0_CDTI2 #29 TIM1_CCO #2 TIM1_CC1 #1 TIM1_CC2 #0 TIM1_CC3 #31 WTIM0_CC0 #2 WTIM0_CC1 #0 LE- TIM0_OUT0 #2 LE- TIM0_OUT1 #1 PCNT0_S0IN #2 PCNT0_S1IN #1</td>
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<tr>
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<td>US0_TX #2 US0_RX #1 US0_CLK #0 US0_CS #31 US0_CTS #30 US0_RTS #29 US1_TX #2 US1_RX #1 US1_CLK #0 US1_CS #31 US1_CTS #30 US1_RTS #29 LEU0_TX #2 LEU0_RX #1 I2C0_SDA #2 I2C0_SCL #1</td>
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<td>CMU_CLK0 #0 PRS_CH6 #1 PRS_CH7 #0 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #1 LES_CH8</td>
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Table 7.2. GPIO Functionality Table
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<th>GPIO Name</th>
<th>Pin Alternate Functionality / Description</th>
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<td>BUSCY BUSDX VDAC0_OUT0 / OPAO_OUT</td>
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<td>TIM0_CDTI2 #30 TIM1_CC0 #3 TIM1_CC1 #2</td>
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<td>TIM1_CC2 #1 TIM1_CC3 #0</td>
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<td>TIM0_OUT1 #2 PCNT0_S0IN #3 PCNT0_S1IN #2</td>
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<td>US0_TX #3 US0_RX #2 USO_CLK #1 US0_CS #0</td>
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<td>US0_CTS #31 US0_RTS #30 US1_TX #3 US1_RX</td>
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<td>#2 US1_CLK #1 US1_CS #0 US1_CTS #31 US1_RTS #30</td>
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<td>LEU0_TX #3 LEU0_RX #2 I2C0_SDA #3 I2C0_SCL #2</td>
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7.3 Alternate Functionality Overview

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings and the associated GPIO pin. Refer to 7.2 GPIO Functionality Table for a list of functions available on each GPIO pin.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

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<td>Description</td>
<td>LESENSE channel 8.</td>
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<td>LES_CH9</td>
<td>0: PA1</td>
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<td>LES_CH10</td>
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<td>LES_CH11</td>
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<td>LES_CH12</td>
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<td>LES_CH13</td>
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<td>LETIM0_OUT0</td>
<td>0: PA0</td>
<td>1: PA1</td>
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<td>Low Energy Timer LETIM0, output channel 0.</td>
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<tr>
<td>LETIM0_OUT1</td>
<td>0: PA1</td>
<td>1: PA2</td>
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<td>Description</td>
<td>Low Energy Timer LETIM0, output channel 1.</td>
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<td>Alternate LOCATION</td>
<td>Functionality</td>
<td>0 - 3</td>
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<tr>
<td>LEU0_RX</td>
<td>0: PA1</td>
<td>4: PA5</td>
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**Description:**
LEUART0 Receive input.

| LEU0_TX            | 0: PA0        | 4: PA4 | 8: PB13 | 12: PC7 | 16: PC11 | 20: PD12 | 24: PF0 | 28: PF4 |

**Description:**
LEUART0 Transmit output. Also used as receive input in half duplex communication.


**Description:**
Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.

| MODEM_DCLK         | 0: PA0        | 4: PA4 | 8: PB13 | 12: PC7 | 16: PC11 | 20: PD12 | 24: PF0 | 28: PF4 |

**Description:**
MODEM data clock out.


**Description:**
MODEM data in.


**Description:**
MODEM data out.

<p>| OPA0_P            | 0: PA2        | 4: PA5 | 8: PB14 | 12: PC8 | 16: PD9 | 20: PD13 | 24: PF1 | 28: PF5 |</p>
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<tr>
<th>Alternate</th>
<th>LOCATION</th>
<th>Description</th>
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<tbody>
<tr>
<td>OPA2_N</td>
<td>0: PB13</td>
<td>Operational Amplifier 2 external negative input.</td>
</tr>
<tr>
<td>OPA2_OUT</td>
<td>0: PB12</td>
<td>Operational Amplifier 2 output.</td>
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<tr>
<td>OPA2_P</td>
<td>0: PB11</td>
<td>Operational Amplifier 2 external positive input.</td>
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<tr>
<td>PCNT0_S0IN</td>
<td>0: PA0, 1: PA1, 2: PA2, 3: PA3, 4: PA4, 5: PA5, 6: PB11, 7: PB12</td>
<td>Pulse Counter PCNT0 input number 0.</td>
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<tr>
<td>PCNT0_S1IN</td>
<td>0: PA1, 1: PA2, 2: PA3, 3: PA4, 4: PA5, 5: PB11, 6: PB12, 7: PB13</td>
<td>Pulse Counter PCNT0 input number 1.</td>
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<td>0: PF0, 1: PF1, 2: PF2, 3: PF3, 4: PF4, 5: PF5, 6: PF6, 7: PF7</td>
<td>Peripheral Reflex System PRS, channel 0.</td>
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<td>0: PF1, 1: PF2, 2: PF3, 3: PF4, 4: PF5, 5: PF6, 6: PF7</td>
<td>Peripheral Reflex System PRS, channel 1.</td>
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<td>0: PF3, 1: PF4, 2: PF5, 3: PF6, 4: PF7</td>
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<td><strong>0 - 3</strong></td>
<td><strong>4 - 7</strong></td>
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<td>PRS_CH5</td>
<td>0: PD10</td>
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<td>1: PA1</td>
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<td>Timer 0 Capture Compare input / output channel 2.</td>
<td>Timer 0 Complementary Dead Time Insertion channel 0.</td>
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<td>US1_RX Asynchronous Receive.</td>
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<td>US1_RX Synchronous mode Master Input / Slave Output (MISO).</td>
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**US1_TX**

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<td>0: PA0</td>
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<td>US1_TX Asynchronous Transmit. Also used as receive input in half duplex communication.</td>
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<td>US1_TX Synchronous mode Master Output / Slave Input (MOSI).</td>
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**US2_CLK**

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**US2_CS**

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**US2_CTS**

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<td>US2_CTS Clear To Send hardware flow control input.</td>
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**US2_RTS**

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<td>US2_RTS Request To Send hardware flow control output.</td>
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**US2_RX**

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<td>13: PF0</td>
<td>14: PF1</td>
<td>US2_RX Asynchronous Receive.</td>
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<td>14: PF1</td>
<td>15: PF3</td>
<td>US2_RX Synchronous mode Master Input / Slave Output (MISO).</td>
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<td>15: PF3</td>
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<td>VDAC0_OUT0 / OPA0_OUT</td>
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<td>VDAC0_OUT1ALT / OPA1_OUTALT</td>
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<td>W TIM0_CC2</td>
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<td>11: PB11</td>
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<td>Description</td>
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<tr>
<td>WTIM0_CDTI0</td>
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<td>Wide timer 0 Complimentary Dead Time Insertion channel 0.</td>
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<td>WTIM0_CDTI1</td>
<td>5: PB11, 6: PB12, 7: PB13</td>
<td>Wide timer 0 Complimentary Dead Time Insertion channel 1.</td>
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<td>WTIM0_CDTI2</td>
<td>3: PB11, 4: PB12, 5: PB13, 6: PB14, 7: PB15</td>
<td>Wide timer 0 Complimentary Dead Time Insertion channel 2.</td>
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</table>
7.4 Analog Port (APORT) Client Maps

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, DACs, etc. The APORT consists of a set of shared buses, switches, and control logic needed to configurably implement the signal routing. Figure 7.2 APORT Connection Diagram on page 101 shows the APORT routing for this device family (note that available features may vary by part number). A complete description of APORT functionality can be found in the Reference Manual.

Client maps for each analog circuit using the APORT are shown in the following tables. The maps are organized by bus, and show the peripheral's port connection, the shared bus, and the connection from specific bus channel numbers to GPIO pins.
In general, enumerations for the pin selection field in an analog peripheral's register can be determined by finding the desired pin connection in the table and then combining the value in the Port column (APORT__), and the channel identifier (CH__). For example, if pin PF7 is available on port APORT2X as CH23, the register field enumeration to connect to PF7 would be APORT2XCH23. The shared bus used by this connection is indicated in the Bus column.

### Table 7.4. ACMP0 Bus and Pin Mapping

| Port  | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|-------|-----|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| APORT1X | BUSAX |     |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| APORT1Y | BUSAY |     |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| APORT2X | BUSBX |     |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| APORT2Y | BUSBY |     |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| APORT3X | BUSCX |     |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| APORT3Y | BUSCY |     |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| APORT4X | BUSDX |     |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| APORT4Y | BUSDY |     |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |

MGM13S Mighty Gecko SiP Module Data Sheet

Pin Definitions

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<table>
<thead>
<tr>
<th>Port</th>
<th>BUS</th>
<th>Bus Mapping</th>
</tr>
</thead>
<tbody>
<tr>
<td>APORT1X</td>
<td>BUSSX</td>
<td>CH10, CH11</td>
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<tr>
<td>APORT1Y</td>
<td>BUSY</td>
<td>CH11, CH12</td>
</tr>
<tr>
<td>APORT2X</td>
<td>BUSX</td>
<td>CH12, CH13</td>
</tr>
<tr>
<td>APORT2Y</td>
<td>BUSY</td>
<td>CH13, CH14</td>
</tr>
<tr>
<td>APORT3X</td>
<td>BUSX</td>
<td>CH14, CH15</td>
</tr>
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<td>BUSY</td>
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<td>BUSX</td>
<td>CH16, CH17</td>
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<td>CH17, CH18</td>
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<table>
<thead>
<tr>
<th>Port</th>
<th>Bus Mapping</th>
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<td>PF0, PF1</td>
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<td>PORT1Y</td>
<td>PC0, PC1</td>
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<tr>
<td>PORT2X</td>
<td>PF2, PF3</td>
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<td>PORT2Y</td>
<td>PC2, PC3</td>
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<td>PORT3X</td>
<td>PF4, PF5</td>
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<td>PORT3Y</td>
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<td>PF6, PF7</td>
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<td>PORT4Y</td>
<td>PC6, PC7</td>
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Table 7.5. ACMP1 Bus and Pin Mapping
| Port   | Bus     | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH09 | CH08 | CH07 | CH06 | CH05 | CH04 | CH03 | CH02 | CH01 | CH00 | CH09 |
|--------|---------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| A PORT1 | BUSAX  | PF7  | PF6  | PF5  | PF4  | PF3  | PF2  | PF1  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  |
| A PORT1 | BUSAY  | PF7  | PF6  | PF5  | PF4  | PF3  | PF2  | PF1  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  |
| A PORT2 | BUSBX  | PF7  | PF6  | PF5  | PF4  | PF3  | PF2  | PF1  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  |
| A PORT2 | BUSBY  | PF7  | PF6  | PF5  | PF4  | PF3  | PF2  | PF1  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  |
| A PORT3 | BUSCX  | PF7  | PF6  | PF5  | PF4  | PF3  | PF2  | PF1  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  |
| A PORT3 | BUSCY  | PF7  | PF6  | PF5  | PF4  | PF3  | PF2  | PF1  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  |
| A PORT4 | BUSDX  | PF7  | PF6  | PF5  | PF4  | PF3  | PF2  | PF1  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  |
| A PORT4 | BUSDY  | PF7  | PF6  | PF5  | PF4  | PF3  | PF2  | PF1  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  | PF0  |

Table 7.6. ADC0 Bus and Pin Mapping
### Table 7.7. CSEN Bus and Pin Mapping

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### Table 7.8. IDAC0 Bus and Pin Mapping

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*CEXT* and *CEXTSENSE* are the external interrupt pins for the Mighty Gecko SiP Module.

*APORT1X, APORT1Y, APORT3X, APORT3Y, APORT2X, APORT2Y, APORT4X, APORT4Y* are the port pins for the Mighty Gecko SiP Module.

*BUSAX, BUSAY, BUSCX, BUSCY, BUSBX, BUSBY, BUSDX, BUSDY* are the bus pins for the Mighty Gecko SiP Module.

*PF0, PF1, PF2, PF3, PF4, PF5, PF6, PC0, PC1, PC2, PC3, PC4, PC5, PC6, PC7* are the pin definitions for the Mighty Gecko SiP Module.
| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH08 | CH07 | CH06 | CH05 | CH04 | CH03 | CH02 | CH01 | CH00 |
|------|-----|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| OPA0_N | APORT1Y | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH08 | CH07 | CH06 | CH05 | CH04 | CH03 | CH02 | CH01 | CH00 |
|       | BUSAY |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|       | APORT2Y | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH08 | CH07 | CH06 | CH05 | CH04 | CH03 | CH02 | CH01 | CH00 |
|       | BUSBY |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|       | APORT3Y | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH08 | CH07 | CH06 | CH05 | CH04 | CH03 | CH02 | CH01 | CH00 |
|       | BUSCY |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|       | APORT4Y | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH08 | CH07 | CH06 | CH05 | CH04 | CH03 | CH02 | CH01 | CH00 |
|       | BUSDY |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|       | APORT5Y | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH08 | CH07 | CH06 | CH05 | CH04 | CH03 | CH02 | CH01 | CH00 |
|       | BUSCY |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|       | APORT6Y | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH08 | CH07 | CH06 | CH05 | CH04 | CH03 | CH02 | CH01 | CH00 |
|       | BUSCY |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|       | APORT7Y | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH08 | CH07 | CH06 | CH05 | CH04 | CH03 | CH02 | CH01 | CH00 |
|       | BUSCY |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |

Table 7.9. VDAC0 / OPA Bus and Pin Mapping
| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9  | CH8  | CH7  | CH6  | CH5  | CH4  | CH3  | CH2  | CH1  | CH0  |
|------|-----|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| OPA1_N | APORT1Y | BUSAY | PB15 | PB13 | PB11 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|       | APORT2Y | BUSBY | PB14 | PB12 | PB11 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|       | APORT3Y | BUSCY | PB15 | PB13 | PB11 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|       | APORT4Y | BUSDY | PB14 | PB12 | PB11 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| OPA1_P | APORT1X | BUSAX | PB15 | PB13 | PB11 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|       | APORT2X | BUSBX | PB14 | PB12 | PB11 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|       | APORT3X | BUSCX | PB15 | PB13 | PB11 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|       | APORT4X | BUSDX | PB14 | PB12 | PB11 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| OPA2_N | APORT1Y | BUSAY | PB15 | PB13 | PB11 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|       | APORT2Y | BUSBY | PB14 | PB12 | PB11 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|       | APORT3Y | BUSCY | PB15 | PB13 | PB11 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
|       | APORT4Y | BUSDY | PB14 | PB12 | PB11 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |

MGM13S Mighty Gecko SiP Module Data Sheet
Pin Definitions
| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|------|-----|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| OPA2_OUT | Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
| APORT1Y | BUSAY | PB15 | PB13 | PB11 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| APORT2Y | BUSBY | PB14 | PB12 | PB11 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| APORT3Y | BUSCY | PB13 | PB12 | PB11 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| APORT4Y | BUSDY | PB15 | PB13 | PB11 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |

| VDAC0_OUT / OPA0_OUT | Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|-----------------------|-----|-----|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| APORT1Y | BUSAY | PB15 | PB13 | PB11 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| APORT2Y | BUSBY | PB14 | PB12 | PB11 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| APORT3Y | BUSCY | PB13 | PB12 | PB11 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| APORT4Y | BUSDY | PB15 | PB13 | PB11 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| Port  | Bus | CH1 | CH2 | CH3 | CH4 | CH5 | CH6 | CH7 | CH8 | CH9 | CH10 | CH11 | CH12 | CH13 | CH14 | CH15 | CH16 | CH17 | CH18 | CH19 | CH20 | CH21 | CH22 | CH23 | CH24 | CH25 | CH26 | CH27 | CH28 | CH29 | CH30 | CH31 |
|-------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| VDAC0_OUT1 / OPA1_OUT | APORT1Y BUSY | PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |
| APORT2Y BUSY | PB15 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| APORT3Y BUSY | PB13 | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 |
| APORT4Y BUSY | PB11 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 |
|               | PB12 | PC8  | PC7  | PC6  | PC5  | PC4  | PC3 |
|               | PB14 | PC15 | PC14 | PC13 | PC12 | PC11 | PC10|
|               | PB16 | PC16 | PC15 | PC14 | PC13 | PC12 | PC11|
|               | PB17 | PC17 | PC16 | PC15 | PC14 | PC13 | PC12|
|               | PB18 | PC18 | PC17 | PC16 | PC15 | PC14 | PC13|
|               | PB19 | PC19 | PC18 | PC17 | PC16 | PC15 | PC14|
|               | PB20 | PC20 | PC19 | PC18 | PC17 | PC16 | PC15|
|               | PB21 | PC21 | PC20 | PC19 | PC18 | PC17 | PC16|
|               | PB22 | PC22 | PC21 | PC20 | PC19 | PC18 | PC17|
|               | PB23 | PC23 | PC22 | PC21 | PC20 | PC19 | PC18|
|               | PB24 | PC24 | PC23 | PC22 | PC21 | PC20 | PC19|
|               | PB25 | PC25 | PC24 | PC23 | PC22 | PC21 | PC20|
|               | PB26 | PC26 | PC25 | PC24 | PC23 | PC22 | PC21|
|               | PB27 | PC27 | PC26 | PC25 | PC24 | PC23 | PC22|
|               | PB28 | PC28 | PC27 | PC26 | PC25 | PC24 | PC23|
|               | PB29 | PC29 | PC28 | PC27 | PC26 | PC25 | PC24|
|               | PB30 | PC30 | PC29 | PC28 | PC27 | PC26 | PC25|
|               | PB31 | PC31 | PC30 | PC29 | PC28 | PC27 | PC26|
|               | PB32 | PC32 | PC31 | PC30 | PC29 | PC28 | PC27|
|               | PB33 | PC33 | PC32 | PC31 | PC30 | PC29 | PC28|
|               | PB34 | PC34 | PC33 | PC32 | PC31 | PC30 | PC29|
|               | PB35 | PC35 | PC34 | PC33 | PC32 | PC31 | PC30|
|               | PB36 | PC36 | PC35 | PC34 | PC33 | PC32 | PC31|
|               | PB37 | PC37 | PC36 | PC35 | PC34 | PC33 | PC32|
|               | PB38 | PC38 | PC37 | PC36 | PC35 | PC34 | PC33|
|               | PB39 | PC39 | PC38 | PC37 | PC36 | PC35 | PC34|
|               | PB40 | PC40 | PC39 | PC38 | PC37 | PC36 | PC35|
|               | PB41 | PC41 | PC40 | PC39 | PC38 | PC37 | PC36|
|               | PB42 | PC42 | PC41 | PC40 | PC39 | PC38 | PC37|
|               | PB43 | PC43 | PC42 | PC41 | PC40 | PC39 | PC38|
|               | PB44 | PC44 | PC43 | PC42 | PC41 | PC40 | PC39|
|               | PB45 | PC45 | PC44 | PC43 | PC42 | PC41 | PC40|
|               | PB46 | PC46 | PC45 | PC44 | PC43 | PC42 | PC41|
|               | PB47 | PC47 | PC46 | PC45 | PC44 | PC43 | PC42|
|               | PB48 | PC48 | PC47 | PC46 | PC45 | PC44 | PC43|
|               | PB49 | PC49 | PC48 | PC47 | PC46 | PC45 | PC44|
|               | PB50 | PC50 | PC49 | PC48 | PC47 | PC46 | PC45|
|               | PB51 | PC51 | PC50 | PC49 | PC48 | PC47 | PC46|
|               | PB52 | PC52 | PC51 | PC50 | PC49 | PC48 | PC47|
|               | PB53 | PC53 | PC52 | PC51 | PC50 | PC49 | PC48|
|               | PB54 | PC54 | PC53 | PC52 | PC51 | PC50 | PC49|
|               | PB55 | PC55 | PC54 | PC53 | PC52 | PC51 | PC50|
|               | PB56 | PC56 | PC55 | PC54 | PC53 | PC52 | PC51|
|               | PB57 | PC57 | PC56 | PC55 | PC54 | PC53 | PC52|
|               | PB58 | PC58 | PC57 | PC56 | PC55 | PC54 | PC53|
|               | PB59 | PC59 | PC58 | PC57 | PC56 | PC55 | PC54|
|               | PB60 | PC60 | PC59 | PC58 | PC57 | PC56 | PC55|
|               | PB61 | PC61 | PC60 | PC59 | PC58 | PC57 | PC56|
|               | PB62 | PC62 | PC61 | PC60 | PC59 | PC58 | PC57|
|               | PB63 | PC63 | PC62 | PC61 | PC60 | PC59 | PC58|
|               | PB64 | PC64 | PC63 | PC62 | PC61 | PC60 | PC59|
|               | PB65 | PC65 | PC64 | PC63 | PC62 | PC61 | PC60|
|               | PB66 | PC66 | PC65 | PC64 | PC63 | PC62 | PC61|
|               | PB67 | PC67 | PC66 | PC65 | PC64 | PC63 | PC62|
|               | PB68 | PC68 | PC67 | PC66 | PC65 | PC64 | PC63|
|               | PB69 | PC69 | PC68 | PC67 | PC66 | PC65 | PC64|
|               | PB70 | PC70 | PC69 | PC68 | PC67 | PC66 | PC65|
|               | PB71 | PC71 | PC70 | PC69 | PC68 | PC67 | PC66|
|               | PB72 | PC72 | PC71 | PC70 | PC69 | PC68 | PC67|
|               | PB73 | PC73 | PC72 | PC71 | PC70 | PC69 | PC68|
|               | PB74 | PC74 | PC73 | PC72 | PC71 | PC70 | PC69|
|               | PB75 | PC75 | PC74 | PC73 | PC72 | PC71 | PC70|
|               | PB76 | PC76 | PC75 | PC74 | PC73 | PC72 | PC71|
|               | PB77 | PC77 | PC76 | PC75 | PC74 | PC73 | PC72|
|               | PB78 | PC78 | PC77 | PC76 | PC75 | PC74 | PC73|
|               | PB79 | PC79 | PC78 | PC77 | PC76 | PC75 | PC74|
|               | PB80 | PC80 | PC79 | PC78 | PC77 | PC76 | PC75|
|               | PB81 | PC81 | PC80 | PC79 | PC78 | PC77 | PC76|
|               | PB82 | PC82 | PC81 | PC80 | PC79 | PC78 | PC77|
|               | PB83 | PC83 | PC82 | PC81 | PC80 | PC79 | PC78|
|               | PB84 | PC84 | PC83 | PC82 | PC81 | PC80 | PC79|
|               | PB85 | PC85 | PC84 | PC83 | PC82 | PC81 | PC80|
8. Package Specifications

8.1 MGM13S Package Dimensions

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<td>0.27</td>
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<td>0.37</td>
</tr>
</tbody>
</table>

Figure 8.1. MGM13S Package Dimensions
<table>
<thead>
<tr>
<th>Dimension</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td></td>
<td>6.50 BSC</td>
<td></td>
</tr>
<tr>
<td>D2</td>
<td></td>
<td>2.92 BSC</td>
<td></td>
</tr>
<tr>
<td>D3</td>
<td></td>
<td>4.50 BSC</td>
<td></td>
</tr>
<tr>
<td>D4</td>
<td></td>
<td>0.68 BSC</td>
<td></td>
</tr>
<tr>
<td>D5</td>
<td></td>
<td>0.60 BSC</td>
<td></td>
</tr>
<tr>
<td>e</td>
<td></td>
<td>0.50 BSC</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td></td>
<td>6.50 BSC</td>
<td></td>
</tr>
<tr>
<td>E2</td>
<td></td>
<td>1.00 BSC</td>
<td></td>
</tr>
<tr>
<td>E3</td>
<td></td>
<td>5.50 BSC</td>
<td></td>
</tr>
<tr>
<td>E4</td>
<td></td>
<td>4.00 BSC</td>
<td></td>
</tr>
<tr>
<td>E5</td>
<td></td>
<td>0.60 BSC</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>0.43</td>
<td>0.48</td>
<td>0.53</td>
</tr>
<tr>
<td>L1</td>
<td>0.11</td>
<td>0.16</td>
<td>0.21</td>
</tr>
<tr>
<td>L2</td>
<td>0.34</td>
<td>0.39</td>
<td>0.44</td>
</tr>
<tr>
<td>L3</td>
<td>0.24</td>
<td>0.29</td>
<td>0.34</td>
</tr>
<tr>
<td>L4</td>
<td>0.14</td>
<td>0.19</td>
<td>0.24</td>
</tr>
<tr>
<td>L5</td>
<td>0.62</td>
<td>0.67</td>
<td>0.72</td>
</tr>
<tr>
<td>eD1</td>
<td></td>
<td>1.20 BSC</td>
<td></td>
</tr>
<tr>
<td>eD2</td>
<td></td>
<td>2.40 BSC</td>
<td></td>
</tr>
<tr>
<td>eD3</td>
<td></td>
<td>0.07 BSC</td>
<td></td>
</tr>
<tr>
<td>eD4</td>
<td></td>
<td>1.50 BSC</td>
<td></td>
</tr>
<tr>
<td>eE1</td>
<td></td>
<td>0.30 BSC</td>
<td></td>
</tr>
<tr>
<td>eE2</td>
<td></td>
<td>0.20 BSC</td>
<td></td>
</tr>
<tr>
<td>eE3</td>
<td></td>
<td>1.60 BSC</td>
<td></td>
</tr>
<tr>
<td>eE4</td>
<td></td>
<td>1.65 BSC</td>
<td></td>
</tr>
<tr>
<td>eE5</td>
<td></td>
<td>0.80 BSC</td>
<td></td>
</tr>
<tr>
<td>aaa</td>
<td></td>
<td>0.10</td>
<td></td>
</tr>
<tr>
<td>bbb</td>
<td></td>
<td>0.10</td>
<td></td>
</tr>
<tr>
<td>ccc</td>
<td></td>
<td>0.10</td>
<td></td>
</tr>
<tr>
<td>ddd</td>
<td></td>
<td>0.10</td>
<td></td>
</tr>
<tr>
<td>eee</td>
<td></td>
<td>0.10</td>
<td></td>
</tr>
<tr>
<td>Dimension</td>
<td>MIN</td>
<td>NOM</td>
<td>MAX</td>
</tr>
<tr>
<td>-----------</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
</tr>
</tbody>
</table>

**Note:**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Tolerances are:
   a. Decimal:
      - X.X = ±0.1
      - X.XX = ±0.05
      - X.XXX = ±0.03
   b. Angular:
      - ±0.1 Degrees
4. This drawing conforms to the JEDEC Solid State Outline MO-220.
5. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
6. Hatching lines means package shielding area.
7. Solid pattern (3.1x3.1mm) shows non-shielding area including its side walls. For side wall, borderline between shielding area and not-shielding area could not be defined clearly like top side.
8.2 MGM13S Recommended PCB Land Pattern

This section describes the recommended PCB land pattern for the MGM13S. The antenna copper clearance area is shown in Figure 8.2 MGM13S Recommended Antenna Clearance on page 113, while the X-Y coordinates of pads relative to the origin are shown in Table 8.1 MGM13S Pad Coordinates and Sizing on page 114. The origin is the center point of pin number 47. It is very important to align the antenna area relative to the module pads precisely.

![Figure 8.2. MGM13S Recommended Antenna Clearance](image-url)
## Table 8.1. MGM13S Pad Coordinates and Sizing

<table>
<thead>
<tr>
<th>Pad No.</th>
<th>Pad coordinates (X,Y)</th>
<th>Pad size (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>47</td>
<td>Pad Center, Origin (0,0)</td>
<td>0.32 x 0.48</td>
</tr>
<tr>
<td>1</td>
<td>(0, -1.60)</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>(0, -2.10)</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>(0, -5.60)</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>(0.60, -5.75)</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>(5.10, -5.75)</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>(5.70, -5.60)</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>(5.70, 0.10)</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>(5.10, -0.10)</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>(5.10, -1.65)</td>
<td></td>
</tr>
<tr>
<td>45</td>
<td>(0.60, -1.65)</td>
<td></td>
</tr>
<tr>
<td>49</td>
<td>(0, -1.00)</td>
<td></td>
</tr>
<tr>
<td>46</td>
<td>(2.92, 0)</td>
<td></td>
</tr>
<tr>
<td>50</td>
<td>1.65, -3.70)</td>
<td>0.67 x 0.67</td>
</tr>
<tr>
<td>51</td>
<td>4.05, -3.70)</td>
<td></td>
</tr>
</tbody>
</table>
### Table 8.2. MGM13S Recommended PCB Land Pattern

<table>
<thead>
<tr>
<th>Symbol</th>
<th>NOM (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>b</td>
<td>0.32 BSC</td>
</tr>
<tr>
<td>D1</td>
<td>5.50 BSC</td>
</tr>
<tr>
<td>D2</td>
<td>3.70 BSC</td>
</tr>
<tr>
<td>D3</td>
<td>4.00 BSC</td>
</tr>
<tr>
<td>D4</td>
<td>0.05 BSC</td>
</tr>
<tr>
<td>D5</td>
<td>1.65 BSC</td>
</tr>
<tr>
<td>eD1</td>
<td>1.00 BSC</td>
</tr>
<tr>
<td>eD2</td>
<td>0.60 BSC</td>
</tr>
<tr>
<td>eD3</td>
<td>0.15 BSC</td>
</tr>
<tr>
<td>e</td>
<td>0.50 BSC</td>
</tr>
<tr>
<td>E1</td>
<td>5.70 BSC</td>
</tr>
<tr>
<td>E2</td>
<td>5.10 BSC</td>
</tr>
<tr>
<td>E3</td>
<td>3.60 BSC</td>
</tr>
<tr>
<td>E4</td>
<td>2.92 BSC</td>
</tr>
<tr>
<td>E5</td>
<td>1.65 BSC</td>
</tr>
<tr>
<td>E6</td>
<td>4.50 BSC</td>
</tr>
<tr>
<td>E7</td>
<td>4.50 BSC</td>
</tr>
<tr>
<td>L</td>
<td>0.48 BSC</td>
</tr>
<tr>
<td>Symbol</td>
<td>NOM (mm)</td>
</tr>
<tr>
<td>--------</td>
<td>----------</td>
</tr>
<tr>
<td>L1</td>
<td>0.67 BSC</td>
</tr>
<tr>
<td>eE1</td>
<td>0.60 BSC</td>
</tr>
<tr>
<td>eE2</td>
<td>0.60 BSC</td>
</tr>
<tr>
<td>eE3</td>
<td>2.40 BSC</td>
</tr>
</tbody>
</table>

Notes:

1. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05mm is assumed.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
4. The stencil thickness should be 0.100mm (4 mils).
5. The stencil aperture to land pad size recommendation is 70% paste coverage.
6. Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.
8.3 MGM13S Package Marking

The figure below shows the package markings printed on the module.

**Explanations:**

<table>
<thead>
<tr>
<th>Marking</th>
<th>Explanation</th>
</tr>
</thead>
<tbody>
<tr>
<td>MGM13Sxxx</td>
<td>Model Number</td>
</tr>
<tr>
<td>FCCIDQ0Q13</td>
<td>FCC Certification ID</td>
</tr>
<tr>
<td>IC5123A-13</td>
<td>IC5123A-13</td>
</tr>
<tr>
<td>R-CRM-BGT-13</td>
<td>KC (Korea) Certification ID</td>
</tr>
<tr>
<td>YWWTTTTT</td>
<td>1. Y = Manufacturing Year</td>
</tr>
<tr>
<td></td>
<td>2. WW = Manufacturing Work Week</td>
</tr>
<tr>
<td></td>
<td>3. TTTT = Trace Code</td>
</tr>
</tbody>
</table>

![MGM13S Package Marking](image)
9. Soldering Recommendations

9.1 Soldering Recommendations

The MGM13S is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven, and particular type of solder paste used.

- Refer to technical documentations of particular solder paste for profile configurations.
- Avoid usining more than two reflow cycles.
- A no-clean, type-3 solder paste is recommended.
- A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- Recommended stencil thickness is 0.100mm (4 mils).
- Refer to the recommended PCB land pattern for an example stencil aperture size.
- For further recommendation, please refer to the JEDEC/IPC J-STD-020, IPC-SM-782 and IPC 7351 guidelines.
- Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.
10. Certifications

10.1 Qualified Antenna Types

The MGM13S variants supporting an external antenna have been designed to operate with a standard 2.14 dBi dipole antenna. Any antenna of a different type or with a gain higher than 2.14 dBi is strictly prohibited for use with this device. Using an antenna of a different type or gain more than 2.14 dBi will require additional testing for FCC, CE and IC. The required antenna impedance is 50 Ω.

Table 10.1. Qualified Antennas for MGM13S

<table>
<thead>
<tr>
<th>Antenna Type</th>
<th>Maximum Gain</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dipole</td>
<td>2.14 dBi</td>
</tr>
</tbody>
</table>

10.2 Bluetooth

The MGM13S is pre-qualified as a Low Energy RF-PHY tested component, having Declaration ID of TBD and QDID of TBD. For the qualification of an end product embedding the MGM13S, the above should be combined with the most up to date Wireless Gecko Link Layer and Host components.

10.3 CE

The MGM13S02 module is in conformity with the essential requirements and other relevant requirements of the Radio Equipment Directive (RED) (2014/53/EU). Please note that every application using the MGM13S02 will need to perform the radio EMC tests on the end product, according to EN 301 489-17. It is ultimately the responsibility of the manufacturer to ensure the compliance of the end-product. The specific product assembly may have an impact to RF radiated characteristics, and manufacturers should carefully consider RF radiated testing with the end-product assembly. A formal DoC is available via www.silabs.com

The MGM13S12 module is in conformity with the essential requirements and other relevant requirements of the Radio Equipment Directive (RED) at nominal 10 dBm transmit power.

The transmit power of the module is not limited and when an end product is using MGM13S12, the end product manufacturer is responsible that the end product is in conformity of all relevant requirements of the RED.
10.4 FCC

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesirable operation.

Any changes or modifications not expressly approved by Silicon Labs could void the user’s authority to operate the equipment.

FCC RF Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure compliance. This transmitter meets both portable and mobile limits as demonstrated in the RF Exposure Analysis. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

OEM Responsibilities to comply with FCC Regulations:

OEM integrator is responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

- With MGM13S12 the antenna(s) must be installed such that a minimum separation distance of 50.5 mm is maintained between the radiator (antenna) and all persons at all times.
- With MGM13S02 the antenna(s) must be installed such that a minimum separation distance of 0 mm is maintained between the radiator (antenna) and all persons at all times.
- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

Important Note:

In the event that the above conditions cannot be met (for certain configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling

The variants of MGM13S Modules are labeled with their own FCC ID. If the FCC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

"Contains Transmitter Module FCC ID: QOQ13"

Or

"Contains FCC ID: QOQ13"

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.
ISEDC

This radio transmitter (IC: 5123A-13) has been approved by Industry Canada to operate with the antenna types listed above, with the maximum permissible gain indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

This device complies with Industry Canada’s license-exempt RSS standards. Operation is subject to the following two conditions:
1. This device may not cause interference; and
2. This device must accept any interference, including interference that may cause undesired operation of the device.

RF Exposure Statement

Exception from routine SAR evaluation limits are given in RSS-102 Issue 5.

The models MGM13S12A and MGM13S12N meet the given requirements when the minimum separation distance to human body is 40 mm.

The models MGM13S02A and MGM13S02N meet the given requirements when the minimum separation distance to human body is 20 mm.

RF exposure or SAR evaluation is not required when the separation distance is same or more than stated above. If the separation distance is less than stated above the OEM integrator is responsible for evaluating the SAR.

OEM Responsibilities to comply with IC Regulations

The MGM13S modules have been certified for integration into products only by OEM integrators under the following conditions:
• The antenna(s) must be installed such that a minimum separation distance as stated above is maintained between the radiator (antenna) and all persons at all times.
• The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter.

As long as the two conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

IMPORTANT NOTE

In the event that these conditions cannot be met (for certain configurations or co-location with another transmitter), then the ISEDC authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate ISEDC authorization.

End Product Labeling

The MGM13S module is labeled with its own IC ID. If the IC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

“Contains Transmitter Module IC: 5123A-13”

or

“Contains IC: 5123A-13”

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.
ISEDCA (Français)

Industrie Canada a approuvé l'utilisation de cet émetteur radio (IC: 5123A-13) en conjonction avec des antennes de type dipolaire à 2.14dBi ou des antennes embarquées, intégrée au produit. L'utilisation de tout autre type d’antenne avec ce composant est proscrite.

Ce composant est conforme aux normes RSS, exonérées de licence d'Industrie Canada. Son mode de fonctionnement est soumis aux deux conditions suivantes:

1. Ce composant ne doit pas générer d’interférences.
2. Ce composant doit pouvoir être soumis à tout type de perturbation y compris celle pouvant nuire à son bon fonctionnement.

Déclaration d'exposition RF

L'exception tirée des limites courantes d'évaluation SAR est donnée dans le document RSS-102 Issue 5.

Les modules MGM13S12A and MGM13S12N répondent aux exigences requises lorsque la distance minimale de séparation avec le corps humain est de 40 mm.

Les modules MGM13S02A and MGM13S02N répondent aux exigences requises lorsque la distance minimale de séparation avec le corps humain est de 20 mm.

La déclaration d'exposition RF ou l'évaluation SAR n'est pas nécessaire lorsque la distance de séparation est identique ou supérieure à celle indiquée ci-dessus. Si la distance de séparation est inférieure à celle mentionnées plus haut, il incombe à l'intégrateur OEM de procéder à une évaluation SAR.

Responsabilités des OEM pour une mise en conformité avec le Règlement du Circuit Intégré

Le module MGM13S a été approuvé pour l'intégration dans des produits finaux exclusivement réalisés par des OEM sous les conditions suivantes:

- L'antenne (s) doit être installée de sorte qu'une distance de séparation minimale indiquée ci-dessus soit maintenue entre le radiateur (antenne) et toutes les personnes avoisinante, ce à tout moment.
- Le module émetteur ne doit pas être localisé ou fonctionner avec une autre antenne ou un autre transmetteur que celle indiquée plus haut.

Tant que les deux conditions ci-dessus sont respectées, il n’est pas nécessaire de tester ce transmetteur de façon plus poussée. Cependant, il incombe à l’intégrateur OEM de s’assurer de la bonne conformité du produit fini avec les autres normes auxquelles il pourrait être soumis de fait de l’utilisation de ce module (par exemple, les émissions des périphériques numériques, les exigences de périphériques PC, etc.).

REM AR QUE I M P O RT AN T E

Dans le cas où ces conditions ne peuvent être satisfaites (pour certaines configurations ou co-implantation avec un autre émetteur), l’autorisation ISEDC n’est plus considérée comme valide et le numéro d’identification ID IC ne peut pas être apposé sur le produit final. Dans ces circonstances, l’intégrateur OEM sera responsable de la réévaluation du produit final (y compris le transmetteur) et de l'obtention d’une autorisation ISEDC distincte.

Étiquetage des produits finis

Les modules MGM13S sont étiquetés avec leur propre ID IC. Si l'ID IC n’est pas visible lorsque le module est intégré au sein d’un autre produit, cet autre produit dans lequel le module est installé devra porter une étiquette faisant apparaître les référence du module intégré. Dans un tel cas, sur le produit final doit se trouver une étiquette aisément lisible sur laquelle figurent les informations suivantes:

“Contient le module transmetteur: 5123A-13 ”

or

“Contient le circuit: 5123A-13”

L’intégrateur OEM doit être conscient qu’il ne doit pas fournir, dans le manuel d’utilisation, d'informations relatives à la façon d'installer ou de d'enlever ce module RF ainsi que sur la procédure à suivre pour modifier les paramètres liés à la radio.
10.6 Japan

The MGM13S02A and MGM13S02N are certified in Japan with certification number TBD.

Since September 1, 2014 it is allowed (and highly recommended) that a manufacturer who integrates a radio module in their host equipment can place the certification mark and certification number (the same marking/number as depicted on the label of the radio module) on the outside of the host equipment. The certification mark and certification number must be placed close to the text in the Japanese language which is provided below. This change in the Radio Law has been made in order to enable users of the combination of host and radio module to verify if they are actually using a radio device which is approved for use in Japan.

Certification Text to be Placed on the Outside Surface of the Host Equipment:

当該機器には電波法に基づく、技術基準適合証明等を受けた特定無線設備を装着している。

Translation of the text:

“This equipment contains specified radio equipment that has been certified to the Technical Regulation Conformity Certification under the Radio Law.”

The "Giteki" marking shown in the figures below must be affixed to an easily noticeable section of the specified radio equipment. Note that additional information may be required if the device is also subject to a telecom approval.

Figure 10.1. GITEKI Mark and ID

Figure 10.2. GITEKI Mark
11. Revision History

Revision 1.0
October 2018
• Added Electrical Specifications Tables for VDAC, CSEN, OPAMP, PCNT and APORT.
• 5.1 Typical MGM13S Connections: Updated diagram to show IOVDD connection to Host CPU supply.
• Table 7.2 GPIO Functionality Table on page 77: Sorted by GPIO name.
• Removed unbonded I/O from APORT mapping tables.
• Packaging figures updated with latest annotations.
• Removed tape and reel specifications section.
• Added detailed certification information.
• Added package marking specifications in 8.3 MGM13S Package Marking.
• Added certification chapter.

Revision 0.5
April 2018
• Removed PLFRCO content.
• Added V2 part numbers to Table 2.1 Ordering Information on page 3.
• Updated 4.1 Electrical Characteristics with latest characterization data and test limits.
• 5.1 Typical MGM13S Connections: Added optional 32.768 kHz crystal connection.
• 5.1 Typical MGM13S Connections: Corrected RTS/CTS naming on Host CPU for UART connection.
• 5.1 Typical MGM13S Connections: Corrected TCK/TMS order on standard ARM Cortex debug connector.
• 7.1 MGM13S Device Pinout: Changed pin 47 name from VSS to ANT_GND.
• 7.1 MGM13S Device Pinout: Corrected numbering of pins 50 and 51.
• Updated 8.2 MGM13S Recommended PCB Land Pattern with latest drawings and dimension recommendations.

Revision 0.1
July 10, 2017
• Initial Release.
Discretion
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