

# uClamp3331ZA μClamp® 1-Line, 3.3V ESD Protection

### **PROTECTION PRODUCTS**

### **Description**

μClamp® TVS diodes are designed to protect sensitive electronics from damage or latch-up due to ESD. They are designed to replace multilayer varistors (MLVs) in portable applications such as cell phones, notebook computers, and other portable electronics. TVS diodes offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

µClamp®3331ZA features extremely good ESD protection characteristics highlighted by extremely low dynamic resistance, low peak ESD clamping voltage, and high ESD withstand voltage (+/-30kV contact per IEC 61000-4-2). Each device will protect one data or power line operating at 3.3 Volts.

 $\mu$ Clamp3331ZA is in a 2-pin SLP0603P2X3F package measuring 0.6 x 0.3 mm with a nominal height of only 0.25mm. Leads are finished with NiAu. The small package gives the designer the flexibility to protect single lines in applications where arrays are not practical. The combination of small size and high ESD surge capability makes them ideal for use in portable applications such as cellular phones and wearables.

### **Features**

- High ESD withstand voltage: +/-30kV (contact) and +/-30kV (air)per IEC 61000-4-2
- Ultra-small 0201 package
- · Protects one line
- · Low ESD clamping voltage
- Working voltage: 3.3V
- · Capacitance: 20pF Maximum
- Low leakage current
- Low dynamic resistance: 0.07 Ohms Typical
- Solid-state silicon-avalanche technology

### **Mechanical Characteristics**

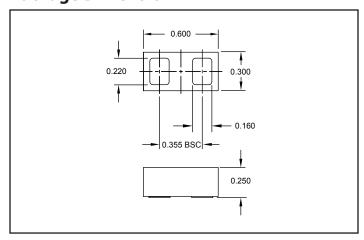
- SLP0603P2X3F package
- Pb-Free, Halogen Free, RoHS/WEEE compliant
- Nominal Dimensions: 0.6 x 0.3 x 0.25 mm
- Lead Finish: NiAu
- · Marking: Marking code
- Packaging: Tape and Reel

## **Applications**

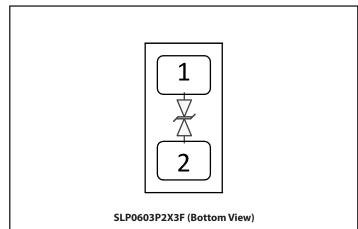
- Cellular Handsets & Accessories
- · Keypads, Side Keys, Audio Ports
- · Portable Instrumentation
- Notebook Computers
- Tablet PC

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### **Package Dimension**



## **Schematic & Pin Configuration**



# **Absolute Maximum Rating**

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P <sub>PK</sub>	30	W
Peak Pulse Current (tp = 8/20μs)	I <sub>PP</sub>	5	A
ESD per IEC 61000-4-2 (Air) <sup>(1)</sup> ESD per IEC 61000-4-2 (Contact) <sup>(1)</sup>	V <sub>ESD</sub>	±30 ±30	kV
Operating Temperature	T <sub>J</sub>	-40 to +125	∘C
Storage Temperature	T <sub>STG</sub>	-55 to +150	°C

# Electrical Characteristics (T=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Units
Reverse Stand-Off Voltage	V <sub>RWM</sub>	T = -40 to +125			3.3	V
Reverse Breakdown Voltage	V <sub>BR</sub>	$I_t = 1 \text{mA}$	3.9		6.5	V
Reverse Leakage Current	I <sub>R</sub>	$V_{RWM} = 3.3V$			350	nA
Clamping Voltage	V <sub>c</sub>	$I_{pp} = 5A$ , $tp = 8/20 \mu s$			10	V
ESD Clamping Voltage <sup>2</sup>	W	I= 4A, tlp = 0.2/100ns		7.0		V
	V <sub>C</sub>	I=16A, tlp = 0.2/100ns		7.8		
Dynamic Resistance <sup>2,3</sup>	R <sub>DYN</sub>	tlp = 0.2/100ns		0.07		Ω
Junction Capacitance	C <sub>J</sub>	$V_R = 0V, f = 1MHz$		16.5	20	pF

#### Notes

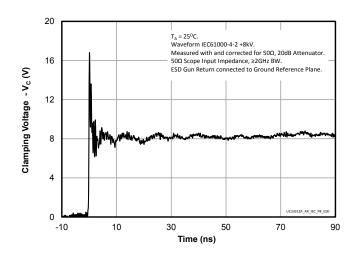
<sup>1)</sup> Measured with a 20dB attenuator, 50 Ohm scope input impedance, 2GHz bandwidth. ESD gun return path connected to ESD ground plane.

<sup>2)</sup> Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns,  $I_{TLP}$  and  $V_{TLP}$  averaging window: t1 = 70ns to t2 = 90ns.

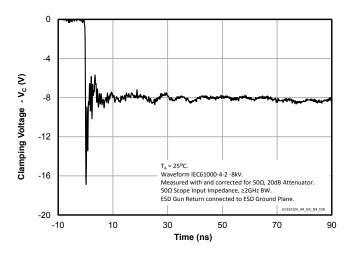
<sup>3)</sup> Dynamic resistance calculated from  $\rm I_{\rm TLP} = 4A$  to  $\rm I_{\rm TLP} = 16A$ 

# **Typical Characteristics**

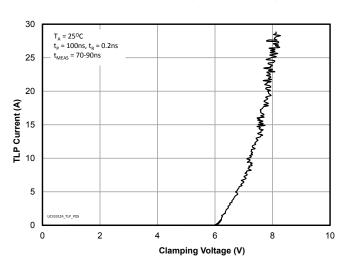
#### ESD Clamping (8kV Contact per IEC 61000-4-2)



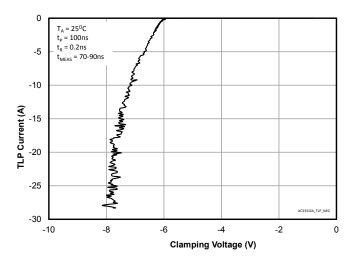
## ESD Clamping (-8kV Contact per IEC 61000-4-2)



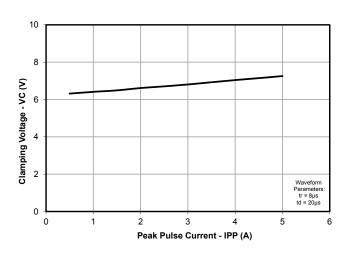
**TLP Characteristic (Positive Pulse)** 



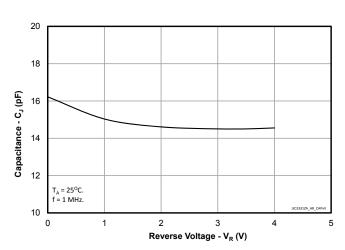
TLP Characteristic (Negative Pulse)



Clamping Characteristic (8/20us Waveform)



Capacitance vs. Reverse Voltage



## **Application Information**

### **Assembly Guidelines**

The small size of this device means that some care must be taken during the mounting process to insure reliable-solder joints. The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing-parameters will require some experimentation to get the desired solder application. Semtech's recommendedmounting pattern is based on the following design guidelines:

### **Land Pattern**

The recommended land pattern follows IPC standards and is designed for maximum solder coverage. Detailed dimensions are shown elsewhere in this document.

#### **Solder Stencil**

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. An area

ratio of 0.70 – 0.75 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

Area Ratio = (L \* W) / (2 \* (L + W) \* T)

Where:

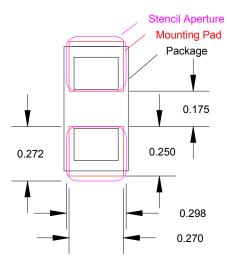
L = Aperture Length

W = Aperture Width

T = Stencil Thickness

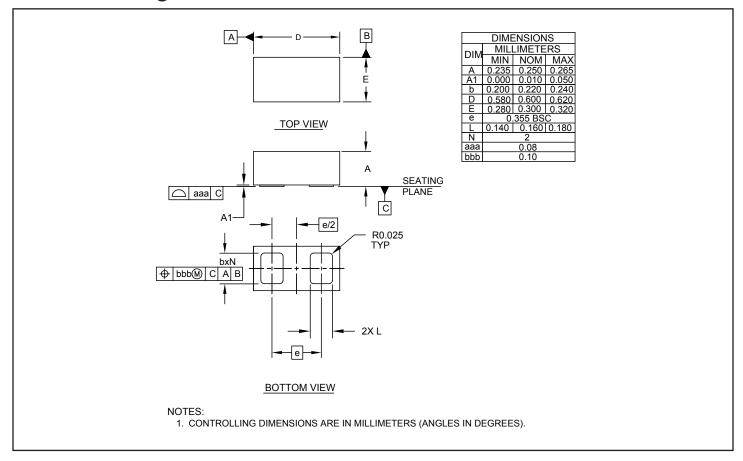
Semtech recommends a stencil thickness of 0.100mm for this device. The stencil should be laser cut with electropolishedfinish. The stencil should have a positive taper of approximately 5 degrees. Electro polishing and tapering the walls results in reduced surface friction and better paste release. For small pitch components, Semtech recommends a square aperture with rounded corners for consistent solder release. Due to the small aperture size, a solder paste with Type 4 or smaller particles are recommended.

### **Recommended Mounting Pattern**

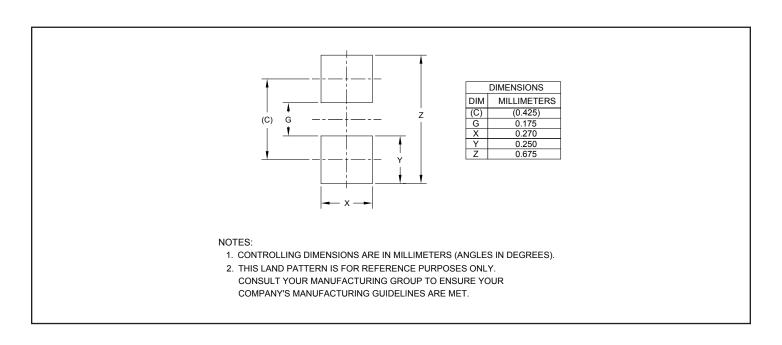


Assembly Parameter	Recommendation		
Solder Stencil Design	Laser cut, Electro-polished		
Aperture shape	Rectangular with rounded corners		
Solder Stencil Thickness	0.100 mm (0.004")		
Solder Paste Type	Type 4 size sphere or smaller		
Solder Reflow Profile	Per JEDEC J-STD-020		
PCB Solder Pad Design	Non-Solder mask defined		
PCB Pad Finish	OSP OR NiAu		

# **Outline Drawing - SLP0603P2X3F**



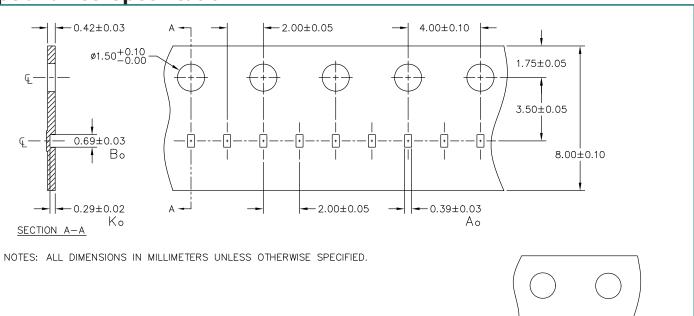
### Land Pattern - SLP0603P2X3F



# **Marking Code**



# **Tape and Reel Specification**



## **Ordering Information**

Part Number	<b>Qty per Reel</b>	Reel Size			
uClamp3331ZATFT	15,000	7"			
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#### **Contact Information**

Semtech Corporation 200 Flynn Road, Camarillo, CA 93012 Phone: (805) 498-2111, Fax: (805) 498-3804 www.semtech.com