MAX16150

Nano-Power Pushbutton On/Off Controller and Battery Seal

General Description

The MAX16150A and the MAX16150B are pushbutton on/off controllers with a switch de-bouncer and built-in latch. These devices accept a noisy input from a mechanical switch and produce a clean latched output and a one-shot interrupt output in response to a switch closure exceeding the debounce period at $\overline{PB\_IN}$. The MAX16150A de-asserts the latched output when the switch closure period exceeds the shutdown period while the MAX16150B does not de-assert the latched output in response to switch closure. For the MAX16150B, a longer switch closure results in longer interrupt signal.

The MAX16150A and MAX16150B operate from a supply range of +1.3V to +5.5V and consume less than 20nA of supply current to ensure minimal battery current in low-power applications. The robust switch input ($\overline{PB\_IN}$) handles ±60V levels and is ±25kV ESD protected for use in harsh industrial environments. The latched output can serve as a logic signal to control a pass transistor or regulator, or it can serve as a switch to connect the load directly to the power supply when load current is less than 20mA. A separate $\overline{INT}$ output provides a system interrupt whenever a valid pushbutton signal is detected. An asynchronous $\overline{CLR}$ input allows an external signal to force the latched output to the off state. Under-voltage lockout circuitry ensures that OUT and $\overline{INT}$ are de-asserted upon power-up.

The MAX16150A and MAX16150B operate over the -40°C to +125°C temperature range are available in a 1mm x 1.5mm, 6-bump WLP and a 6-pin thin SOT-23 packages.

Applications

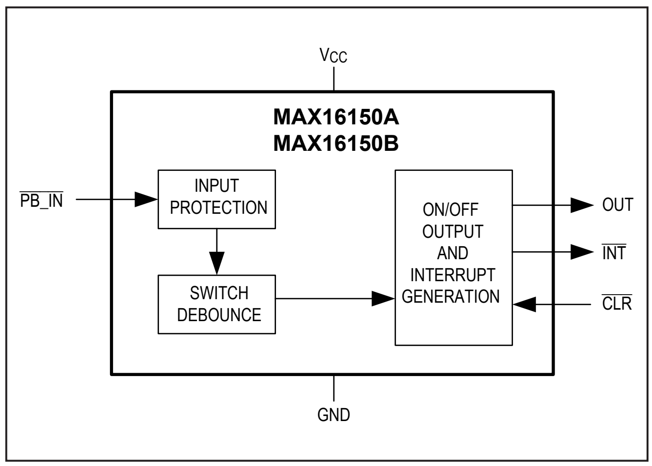
- Portable Instruments
- Handheld Consumer Electronics
- Industrial Equipment
- Disposable Low-Power Electronics

Benefits and Features

- Low Power
  - 20nA (Max) Standby Current
  - 50ms and 2s Debounce Timing Options
- 8s and 16s Shutdown Periods
- Latched Output Supplies 20mA Load Current from Battery
- One-shot $\overline{INT}$ Output on each switch closure
- 32ms $\overline{INT}$ Duration
- Pushbutton Input Handle Up to ±60V
- ±15kV HMB ESD Protection
- SOT23-6 and 1mm x 1.5mm 6-bump WLP packages

Ordering Information appears at end of data sheet.

Simplified Block Diagram



Absolute Maximum Ratings

VCC to GND ....-0.3V to +6V
$\overline{\text{PB\_IN}}$ to GND ....-60V to +60V
$\overline{\text{CLR}}$, $\overline{\text{INT}}$, OUT to GND ....-0.3V to 6V
Continuous Power Dissipation
(Multilayer Board) SOT23-6 (T_A = +70°C, derate 8.70mW/°C
above +70°C.) 696mW

Continuous Power Dissipation
(Multilayer Board) WLP (T_A = +70°C, derate 10.50mW/°C
above +70°C.) .... mW to 840mW
Operating Temperature Range .... -40°C to +125°C
Junction Temperature ....+150°C
Storage Temperature Range .... -40°C to +150°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

SOT

Package Code	U6-1
Outline Number	**21-0058**
Land Pattern Number	**90-0175**
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	NA
Junction to Case (θ_{JC})	80°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	115°C/W
Junction to Case (θ_{JC})	80°C/W

WLP

Package Code	W60C1-2
Outline Number	
Land Pattern Number	Refer to **Application Note 1891**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	95.15°C/W
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{CC} = V_{MIN} to V_{MAX}, T_A = -40°C to +125°C, Limits over the operating temperature range and relevant supply voltage range are guaranteed by production and/or characterization. Typical values are at T_A = +25°C and V_{CC} = +3.3V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}		1.3		5.5	V
Undervoltage-Lockout Threshold	V_{UVLO}	V_{CC} falling		**TBD**	**TBD** (1.2)	V
Undervoltage Lockout Hysteresis			**TBD**	50	**TBD**	mV
Power Supply Current	I_{SB}	V_{CC} = 5V, OUT not asserted, $\overline{\text{PB\_IN}}$ not connected. -40°C ≤ T_A ≤ +70°C			20	nA
		V_{CC} = 5V, OUT not asserted, $\overline{\text{PB\_IN}}$ not connected. -40°C ≤ T_A ≤ +125°C		**TBD**	**TBD**	
	I_{CC}	During $\overline{\text{PB\_IN}}$ detection or $\overline{\text{INT}}$ assertion		25	TBD	µA
	I_{SB_UVLO}	V_{CC} < 1.,3V, I_{OUT} = 0, $\overline{\text{PB\_IN}}$ not connected, $\overline{\text{CLR}}$ not asserted		100	300	nA
Timing Accuracy		Deviation from nominal value of debounce time (t_{DB}), shutoff time (t_{SO}), and interrupt time (t_{INT})	-20	**±TBD**	+20	%
$\overline{\text{PB\_IN}}$ Threshold	V_{IL_PB}				0.3 V_{CC}	V
	V_{IH_PB}		0.7 V_{CC}			
$\overline{\text{PB\_IN}}$ Hysteresis				**TBD** (100)		mV
$\overline{\text{PB\_IN}}$ Pull-Up Resistance		0 > $V_{\overline{PB\_IN}}$ < V_{CC}	500	1000	1500	kΩ
$\overline{\text{PB\_IN}}$ Input Current	I_{IN}	$V_{\overline{PB\_IN}}$ = ±60V	-170		+170	µA
		0V ≤ $V_{\overline{PB\_IN}}$ ≤ V_{CC}	TBD	36	**TBD**	
$\overline{\text{PB\_IN}}$ Voltage Range		Continuous; 0V ≤ V_{CC} ≤ 5.0V	-60		+60	V
		Transient; 0V ≤ V_{CC} ≤ 5.5V	-60		+60	
$\overline{\text{CLR}}$ Threshold	V_{IL_CLR}				0.3 V_{CC}	V
	V_{IH_CLR}		0.7 V_{CC}			
$\overline{\text{CLR}}$ Input Current	I_{CLR}		-10	1	+10	nA

Electrical Characteristics (continued)

(V_{CC} = V_{MIN} to V_{MAX}, T_A = -40°C to +125°C, Limits over the operating temperature range and relevant supply voltage range are guaranteed by production and/or characterization. Typical values are at T_A = +25°C and V_{CC} = +3.3V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CLR}$ Falling Edge to OUT Low Propagation Delay	t_{CO}	R_L = 10kΩ, C_L = 100pF		200		ns
$\overline{CLR}$ Lockout Time		Period following rising edge of OUT during which transitions on $\overline{CLR}$ are ignored.	51.2	64	76.8	ms
OUT Output Voltage	V_{OL}	I_{SINK} = 1.6mA			0.4	V
	V_{OH}	V_{CC} = 3.3V, I_{SOURCE} = 20mA	V_{CC} - 100			mV
		V_{CC} = 2.0V, I_{OUT} = **TBD**	V_{CC} - 100			
		V_{CC} = 1.3V, I_{SOURCE} = **TBD**	V_{CC} - 100			
$\overline{INT}$ Output Voltage	V_{OL_INT}	I_{SINK} = 1mA			0.2	V
$\overline{INT}$ Leakage Current				1	±10	nA
Interrupt Pulse Duration	t_{INT}	Beginning at t_{DB}.	25.6	32	38.4	ms
		Beginning at end of t_{SO}	102.4	128	153.6	
ESD Protection		PB_IN Human Body Model		±15		kV

Typical Operating Characteristics

(MAX16150A/B: V_{DD} =+3.3V, 25°C; T_A = 25°C unless otherwise noted,)

TBD
TOC01

TBD
TOC02

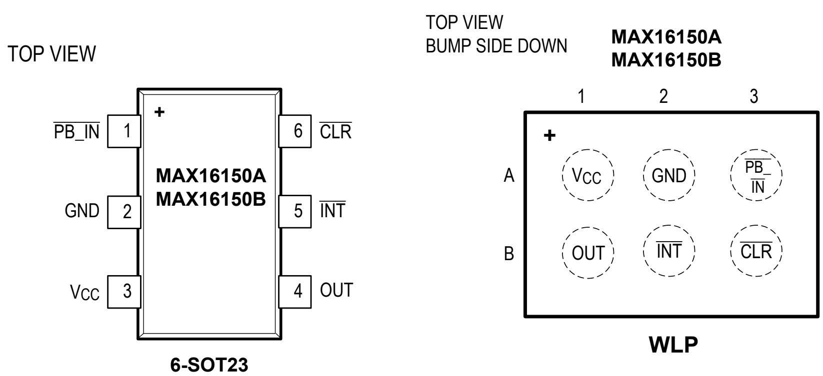
TBD
TOC03

TBD
TOC04

TBD
TOC05

TBD
TOC06

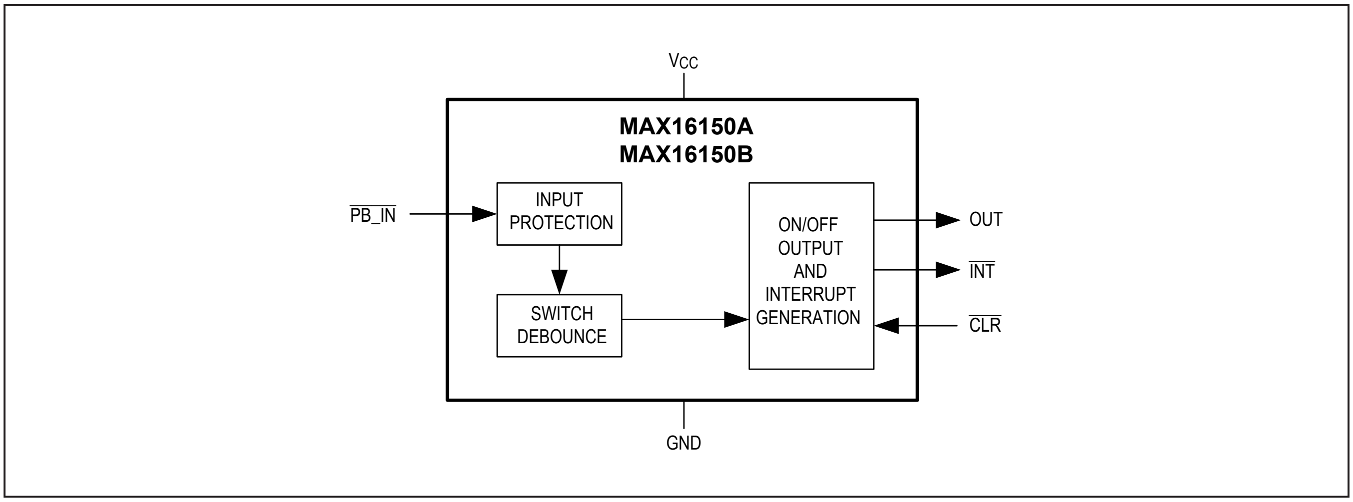
Pin Configurations



Pin Description

PIN		NAME	FUNCTION
SOT23-6	WLP		
1	A3	PB_IN	Pushbutton input. PB_IN is internally pulled up to V_{CC}. Holding PB_IN low for a period greater than the debounce time (t_{DB}) forces OUT to latch high and generates a 1-shot pulse at INT. For the MAX16150A, holding PB_IN low for a period greater than the shutdown period (t_{SO}) de-assert OUT. For the MAX16150B, holding PB_IN low for a period greater than shutdown period (t_{SO}) generates an extended interrupt pulse but does not de-assert OUT.
2	A2	GND	Ground.
3	A1	VCC	Power supply input. Bypass with a 0.1µF capacitor to ground.
4	B1	OUT	Active-High, Push-Pull Latch Output. OUT is connected to V_{CC} when high.
5	B2	INT	Active-Low, Open-Drain Interrupt/Reset Output. INT is a one-shot output pulse. INT asserts for the interrupt timeout period when PB_IN is held low for a period greater than the debounce time (t_{DB}). INT is high impedance when de-asserted, even when pulled above V_{CC}.
6	B3	CLR	Clear input. Pulling CLR low de-asserts the latched OUT signal. If OUT is de-asserted, pulling CLR does not change OUT's state.

Functional Diagrams



Detailed Description

The MAX16150A and the MAX16150B are pushbutton on/off controllers with a switch debouncer and latched output for controlling system power. A switch closure that is stable for a period greater than or equal to the debounce time, t_{DB}, causes OUT to assert high. Driving $\overline{\text{CLR}}$ low causes OUT to de-assert. For the MAX16150A a switch closure period greater than or equal to the shutdown period, t_{SO}, will cause OUT to de-assert. Each debounced switch closure also causes one-shot $\overline{\text{INT}}$ output.; see Table 1 below for more detail.

MAX16150

The MAX16150A and the MAX16150B operate from supply voltages between +1.3V and 5.5V and consume 20nA of supply current when OUT is in the de-asserted state. Whenever OUT is de-asserted, the state of $\overline{\text{CLR}}$ is ignored. After asserting OUT, $\overline{\text{CLR}}$ continues to be ignored for a period of 2x the $\overline{\text{INT}}$ period. For low-power applications (up to about 20mA output current), OUT can drive the load directly. Each debounced switch closure causes $\overline{\text{INT}}$ to assert. A switch closure longer than t_{SO} results in $\overline{\text{INT}}$ asserting for a period that is 4x longer than the nominal $\overline{\text{INT}}$ period. This longer $\overline{\text{INT}}$ can be used to signal the system to perform a specific function, or to initiate a shutdown process. Closing the switch longer than this extended $\overline{\text{INT}}$ period will not cause further assertion of $\overline{\text{INT}}$.

The MAX16150A de-asserts OUT when $\overline{\text{PB\_IN}}$ is held low for a period equal to or greater than the shutdown period, t_{SO}. In the MAX16150B, holding $\overline{\text{PB\_IN}}$ low for a duration equal to or greater than the shutdown period (t_{SO}) does not de-assert OUT. Instead the MAX16150B outputs a longer interrupt signal.

Table 1. Available MAX16150/MAX16151 versions

VERSION	SUPPLY VOLTAGE RANGE	DEBOUNCE TIME (t_{DB})	SHUTDOWN PERIOD (t_{SO})	INTERRUPT PERIOD (SWITCH CLOSURE > t_{DB}	INTERRUPT PERIOD (SWITCH CLOSURE > t_{SO}	SWITCH CLOSURE > t_{SO}
MAX16150A	1.3V - 5.5V	50ms	8s	32ms	**TBD**	OUT De-asserts
MAX16150B	1.3V - 5.5V	2s	16s	32ms	**TBD**	OUT Stays Asserted

Figure 1 above shows the timing diagram of the MAX16150A. A switch closure of a duration greater than t_{DB} causes OUT to assert. A switch closure of a duration greater than t_{SO} causes OUT to de-assert. Typically, $\overline{\text{INT}}$ and $\overline{\text{CLR}}$ are pulled up either to OUT or to a regulated voltage controlled by OUT as depicted in the figure above. As such, $\overline{\text{INT}}$ and $\overline{\text{CLR}}$ are pulled low while OUT is de-asserted. If pulled up to a constant supply voltage, $\overline{\text{INT}}$ and $\overline{\text{CLR}}$ will behave as shown by the horizontal dashed lines while OUT is de-asserted.

Figure 2 above shows the timing diagram for the MAX16150B. A switch closure of a duration greater than t_{DB} causes OUT to assert. A switch closure of a duration greater than t_{SO} does not cause OUT to de-assert. Instead, it causes an extended interrupt. Typically, $\overline{\text{INT}}$ and $\overline{\text{CLR}}$ are pulled up either to OUT or to a regulated voltage controlled by OUT as depicted in the figure above. As such, $\overline{\text{INT}}$ and $\overline{\text{CLR}}$ are pulled low while OUT is de-asserted. If pulled up to a constant supply voltage, $\overline{\text{INT}}$ and $\overline{\text{CLR}}$ will behave as shown by the horizontal dashed lines while OUT is de-asserted.

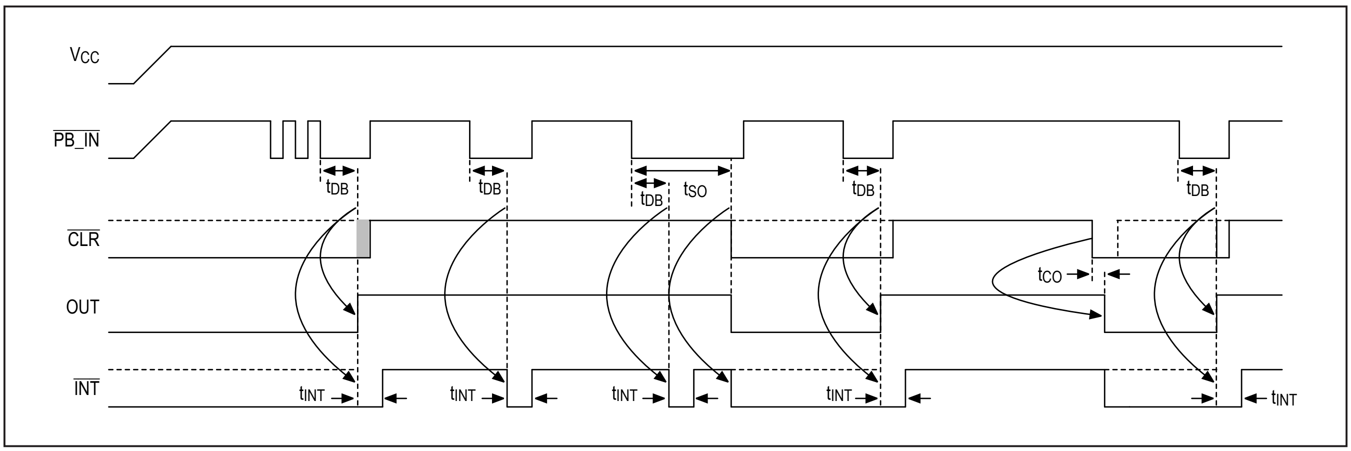


Figure 1. MAX16150A Timing Diagram

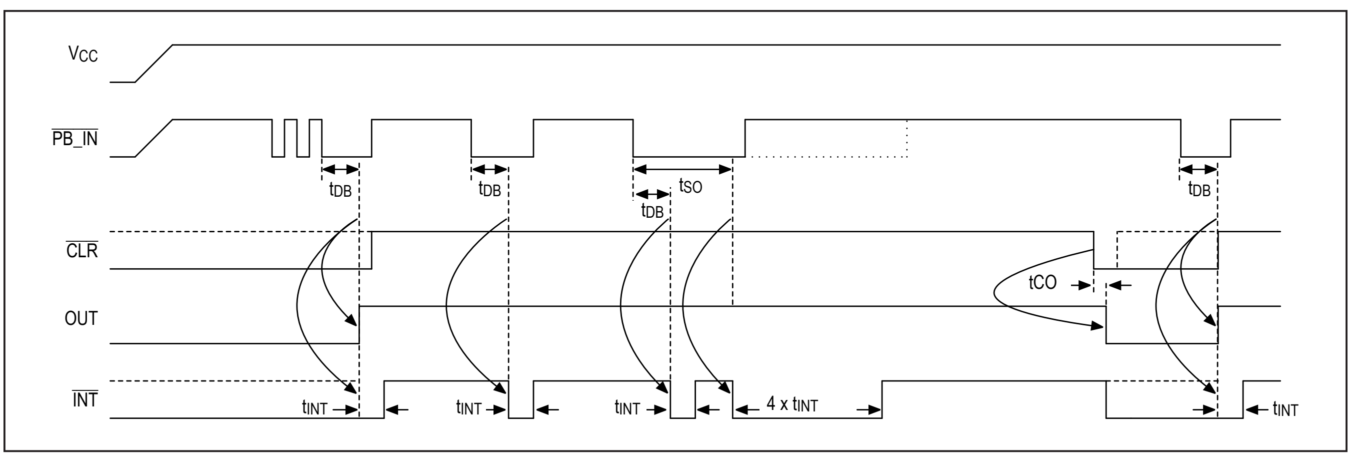


Figure 2. MAX16150B Timing Diagram

Undervoltage Lockout

The undervoltage-lockout circuitry ensures that the outputs are at the correct state on power-up. While V_{CC} is less than the **TBD**V (typ) undervoltage threshold and greater than 1.0V, OUT remains low and transitions at $\overline{\text{PB\_IN}}$ are ignored.

Robust Switch Input

The switch input ($\overline{\text{PB\_IN}}$) has overvoltage clamping diodes to protect against damaging fault conditions. Switch input voltages can safely swing ±60V to ground.

±15kV ESD Protection

ESD-protection structures are incorporated on all pins o protect against electrostatic discharges encountered during handling and assembly. The MAX16150A and the MAX16150B have extra protection against static electricity to protect against ESD of ±15kV at the switch input without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. A design advantage of these devices is that they continue working without latchup after an ESD event, which eliminates the need to power-cycle the device. ESD protection can be tested in various ways; this product is characterized for protection to ±15kV using the Human Body Model.

Human Body Model

Figure 3 shows the Human Body Model, and Figure 4 shows the current waveform it generates when discharged into a low impedance. This model consists of a100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

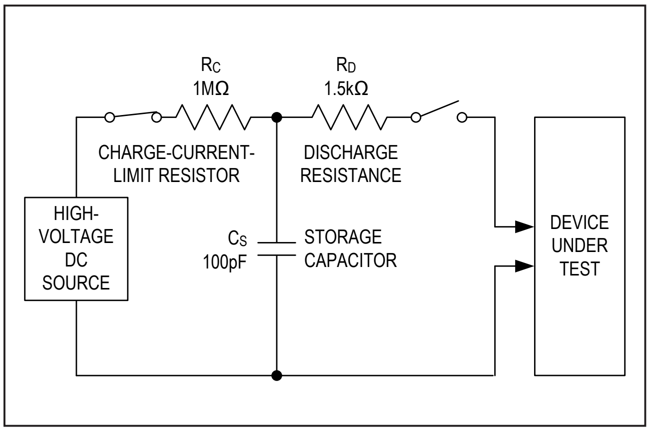


Figure 3. Human Body ESD Test Model

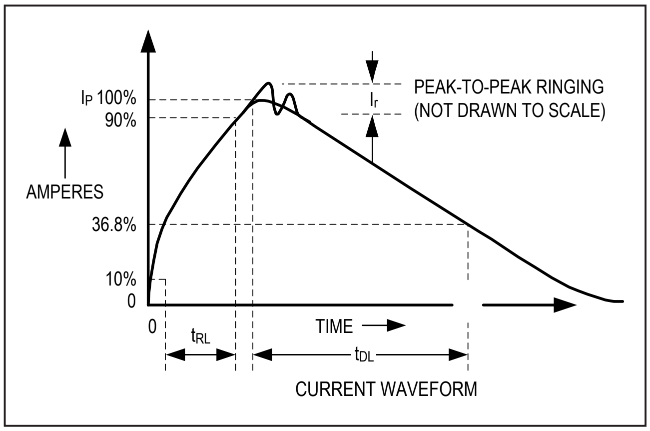
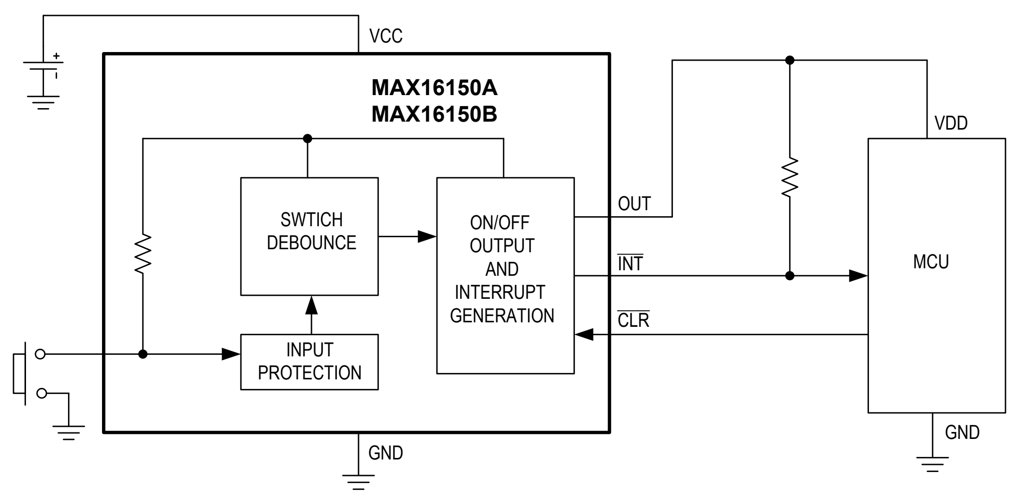


Figure 4. Human Body Current Waveform

Typical Application Circuits



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX16150AWT+T	-40ºC to +125ºC	6 WLP
MAX16150AUT+T*	-40ºC to +125ºC	6 SOT23
MAX16150BWT+T*	-40ºC to +125ºC	6 WLP
MAX16150BUT+T*	-40ºC to +125ºC	6 SOT23

+ Denotes a lead(Pb)-free/RoHS-compliant package.
T Denotes tape-and-reel.
** Denotes future products*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/18	Initial release	—

