

NVHL040N65S3F

Power MOSFET, N-Channel, SUPERFET[®] III, FRFET[®], 650 V, 65 A, 40 mΩ

Description

SUPERFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET is very suitable for the various power system for miniaturization and higher efficiency.

SUPERFET III FRFET MOSFET's optimized reverse recovery performance of body diode can remove additional component and improve system reliability.

Features

- 700 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 33.8\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 153\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 1333\text{ pF}$)
- 100% Avalanche Tested
- AEC-Q101 Qualified and PPAP Capable

Applications

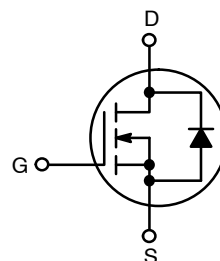
- Automotive On Board Charger HEV-EV
- Automotive DC/DC converter for HEV-EV



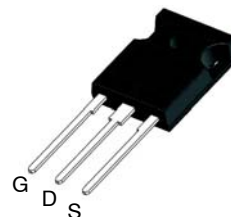
ON Semiconductor[®]

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V_{DSS}	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
650 V	40 mΩ @ 10 V	65 A

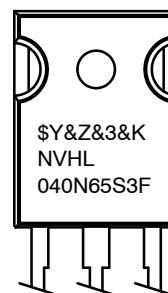


POWER MOSFET



TO-247 LONG LEADS
CASE 340CX

MARKING DIAGRAM



- \$Y = ON Semiconductor Logo
- &Z = Assembly Plant Code
- &3 = Data Code (Year & Week)
- &K = Lot
- NVHL040N65S3F = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

NVHL040N65S3F

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter	NVHL040N65S3F	Unit
V _{DSS}	Drain to Source Voltage	650	V
V _{GSS}	Gate to Source Voltage	- DC	±30
		- AC (f > 1 Hz)	±30
I _D	Drain Current	- Continuous (T _C = 25°C)	65
		- Continuous (T _C = 100°C)	45
I _{DM}	Drain Current	- Pulsed (Note 1)	162.5
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	1009	mJ
E _{AR}	Repetitive Avalanche Energy (Note 1)	4.46	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	50	
P _D	Power Dissipation	(T _C = 25°C)	446
		- Derate Above 25°C	3.57
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating; pulse-width limited by maximum junction temperature.
2. I_{AS} = 9 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 32.5 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	NVHL040N65S3F	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	0.28	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max.	40	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
NVHL040N65S3F	NVHL040N65S3F	TO-247	Tube	N/A	N/A	30 Units

NVHL040N65S3F

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	650	–	–	V
		V _{GS} = 0 V, I _D = 10 mA, T _J = 150°C	700	–	–	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, Referenced to 25°C	–	0.64	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V	–	–	10	μA
		V _{DS} = 520 V, T _C = 125°C	–	103	–	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 2.1 mA	3.0	–	5.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 32.5 A	–	33.8	40	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 32.5 A	–	40	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 1 MHz	–	5875	–	pF
C _{oss}	Output Capacitance		–	140	–	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	–	1333	–	pF
C _{oss(er.)}	Energy Related Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	–	241	–	pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 400 V, I _D = 32.5 A, V _{GS} = 10 V (Note 4)	–	153	–	nC
Q _{gs}	Gate to Source Gate Charge		–	51	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	61	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	1.9	–	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 400 V, I _D = 32.5 A, V _{GS} = 10 V R _g = 2.2 Ω (Note 4)	–	41	–	ns
t _r	Turn-On Rise Time		–	53	–	ns
t _{d(off)}	Turn-Off Delay Time		–	96	–	ns
t _f	Turn-Off Fall Time		–	28	–	ns

SOURCE-DRAIN DIODE CHARACTERISTICS

I _S	Maximum Continuous Source to Drain Diode Forward Current	–	–	65	A	
I _{SM}	Maximum Pulsed Source to Drain Diode Forward Current	–	–	162.5	A	
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 32.5 A	–	–	1.3	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 32.5 A, dI _F /dt = 100 A/μs	–	159	–	ns
Q _{rr}	Reverse Recovery Charge		–	840	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

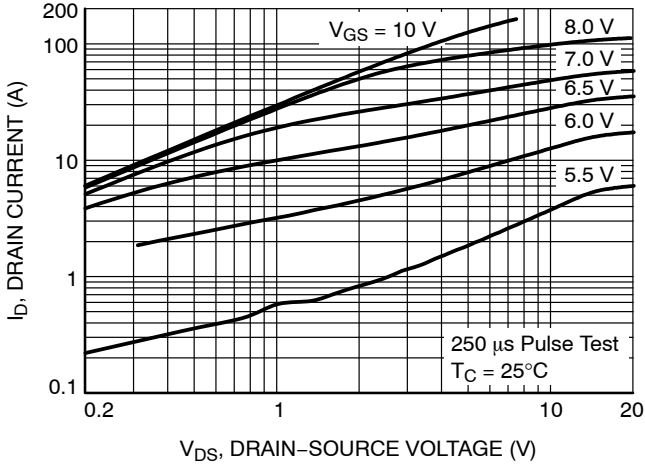


Figure 1. On-Region Characteristics

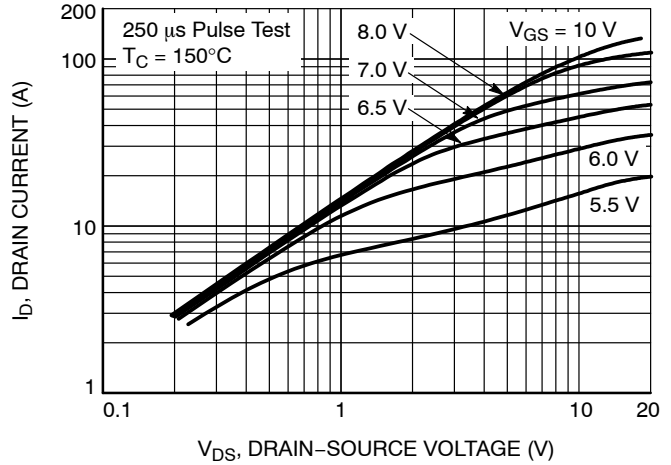


Figure 2. On-Region Characteristics

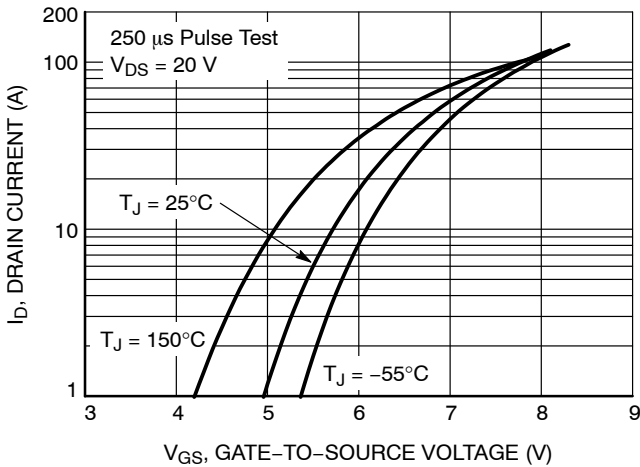


Figure 3. Transfer Characteristics

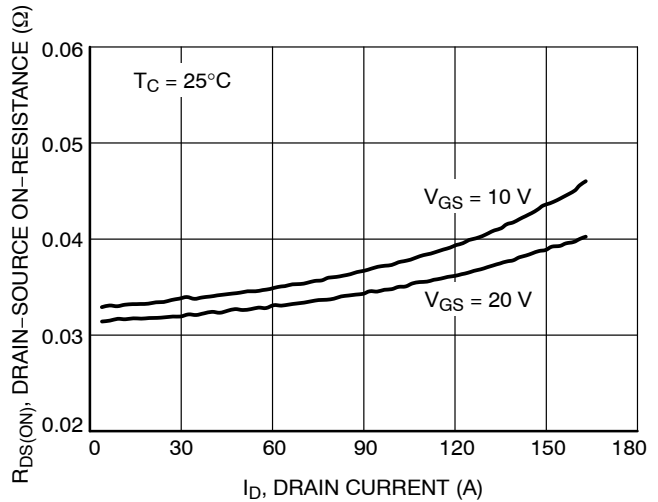


Figure 4. On-Resistance Variation vs. Drain Current and Gate Voltage

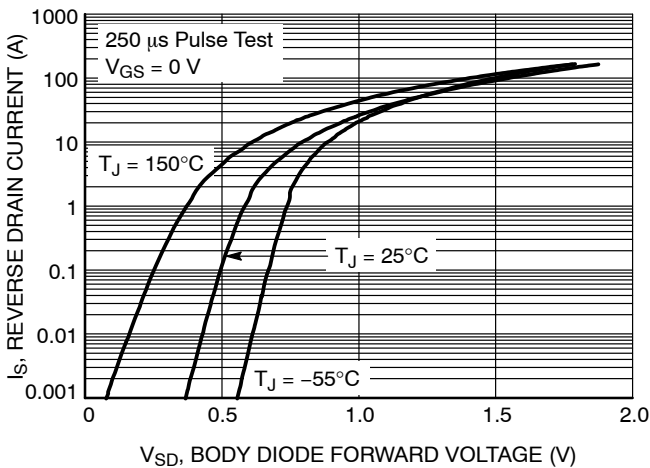


Figure 5. Body Diode Forward Voltage Variation vs. Source Current and Temperature

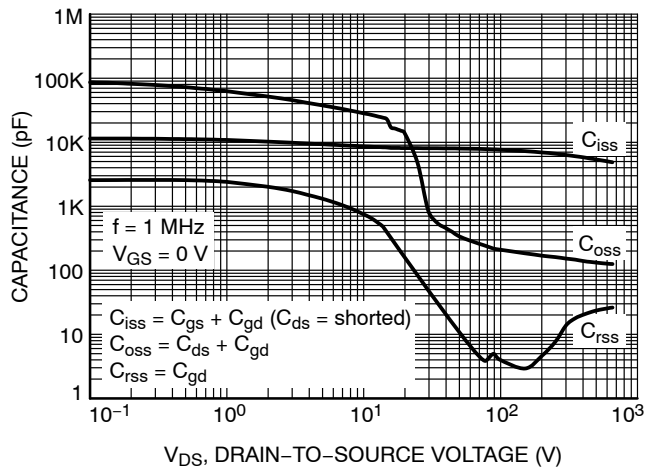


Figure 6. Capacitance Characteristics

TYPICAL CHARACTERISTICS

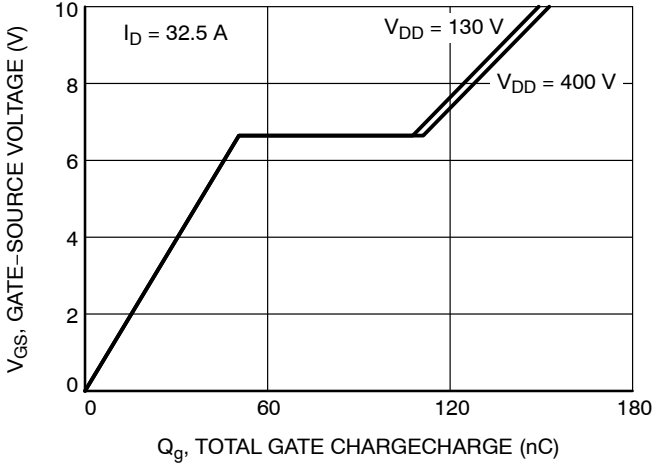


Figure 7. Gate Charge Characteristics

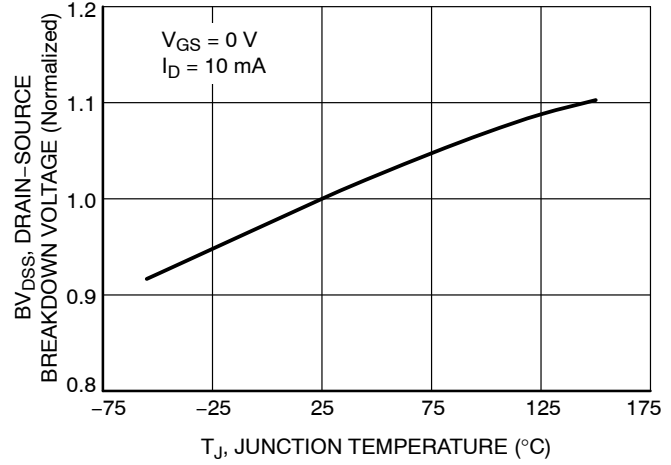


Figure 8. Breakdown Voltage Variation vs. Temperature

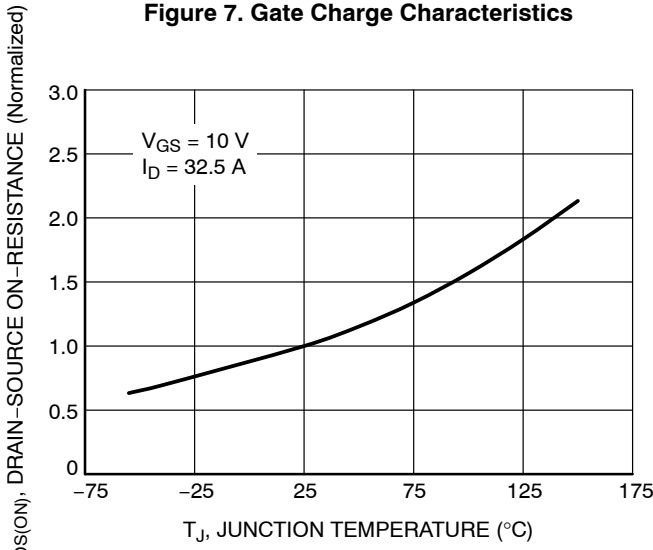


Figure 9. On-Resistance Variation vs. Temperature

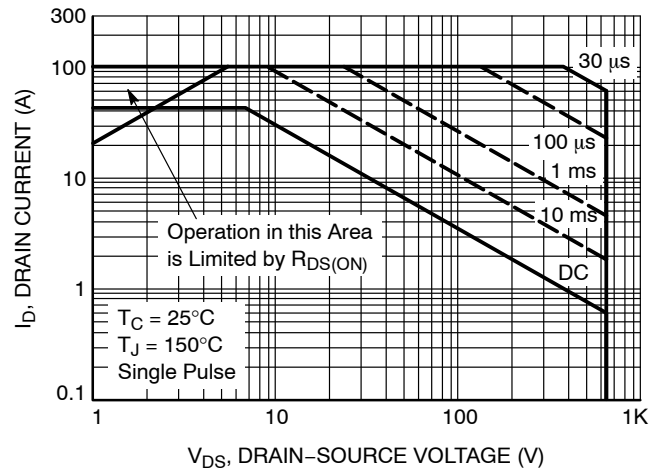


Figure 10. Maximum Safe Operating Area

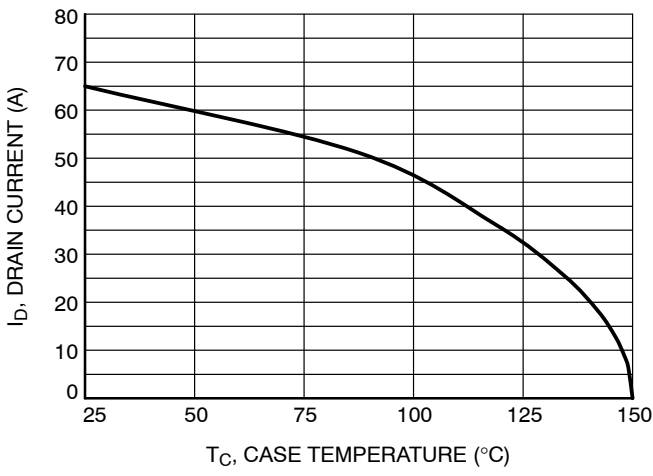


Figure 11. Maximum Drain Current vs. Case Temperature

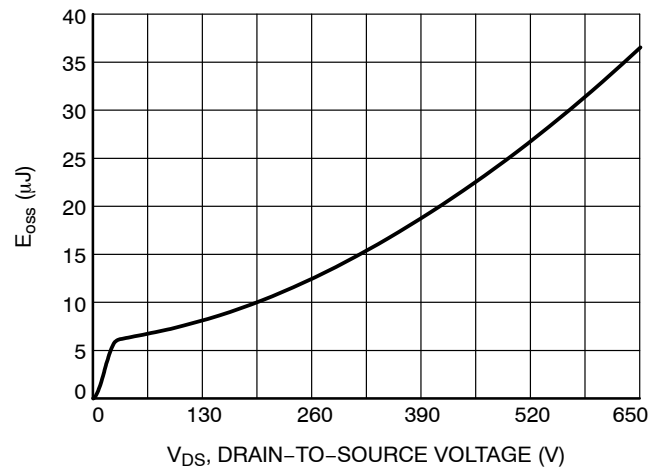


Figure 12. E_OSS vs. Drain-to-Source Voltage

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TYPICAL CHARACTERISTICS

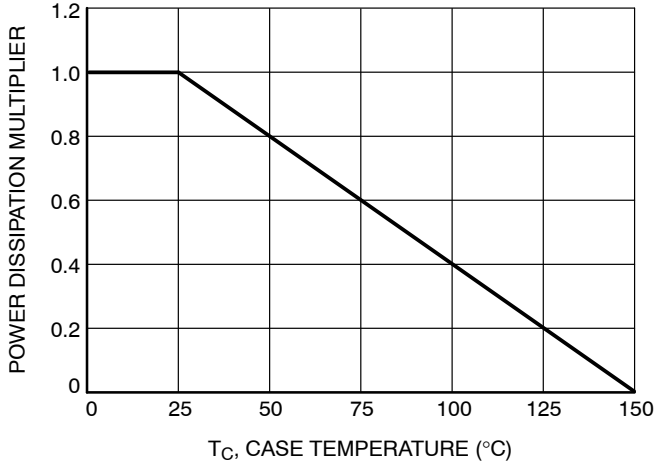


Figure 13. Normalized Power Dissipation vs. Case Temperature

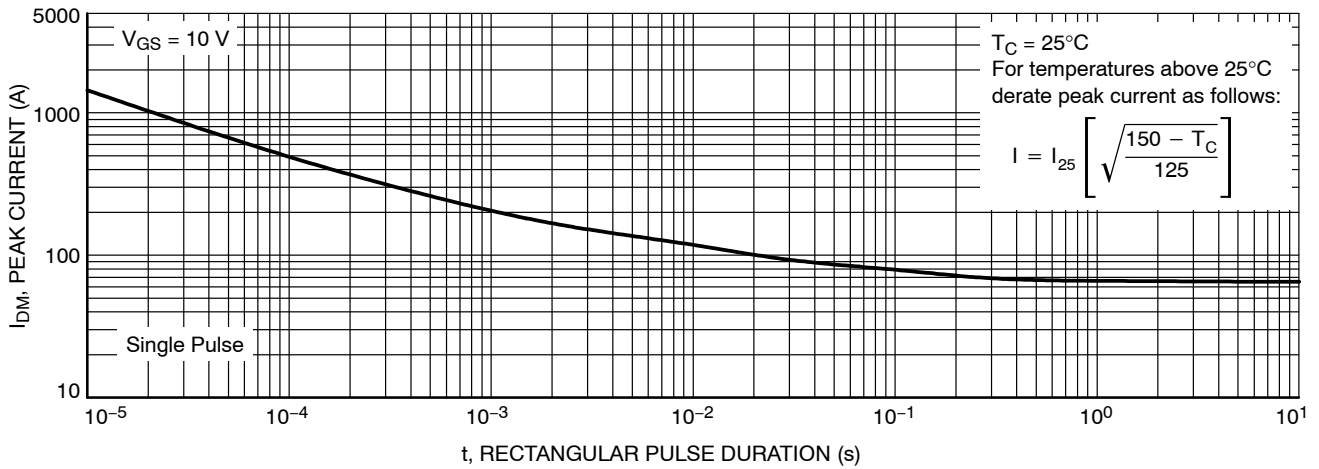


Figure 14. Peak Current Capability

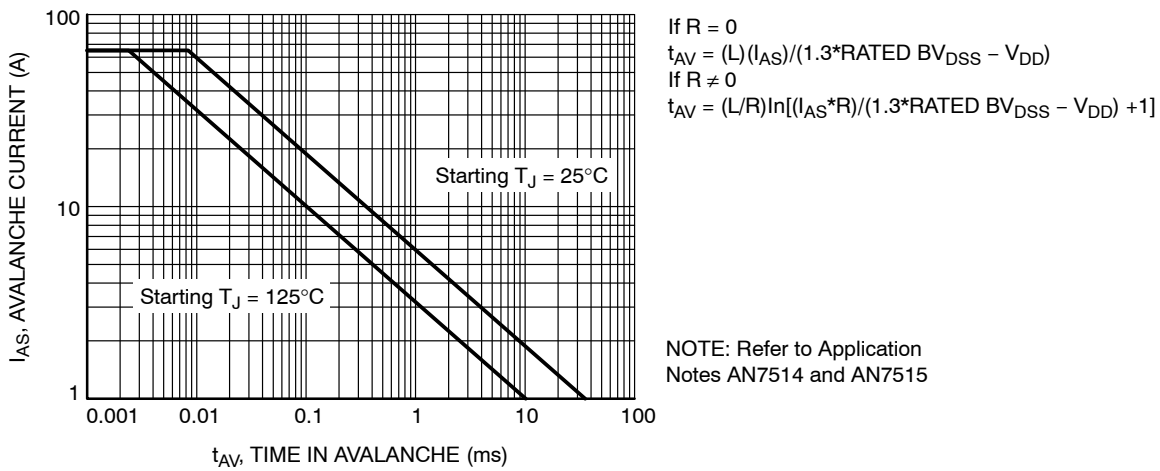


Figure 15. Unclamped Inductive Switching Capability

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TYPICAL CHARACTERISTICS

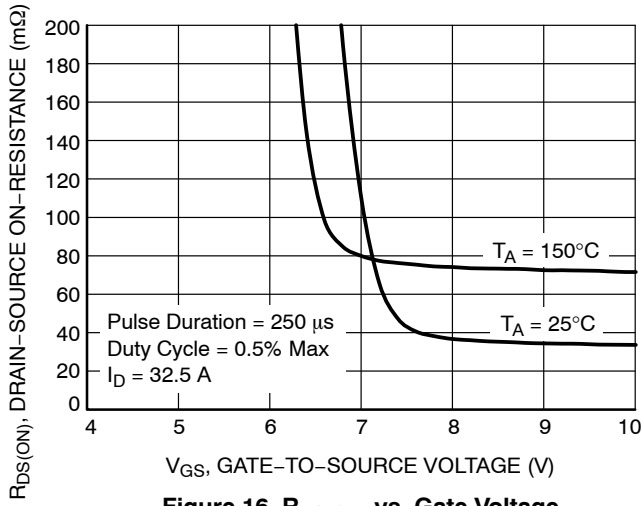


Figure 16. $R_{DS(ON)}$ vs. Gate Voltage

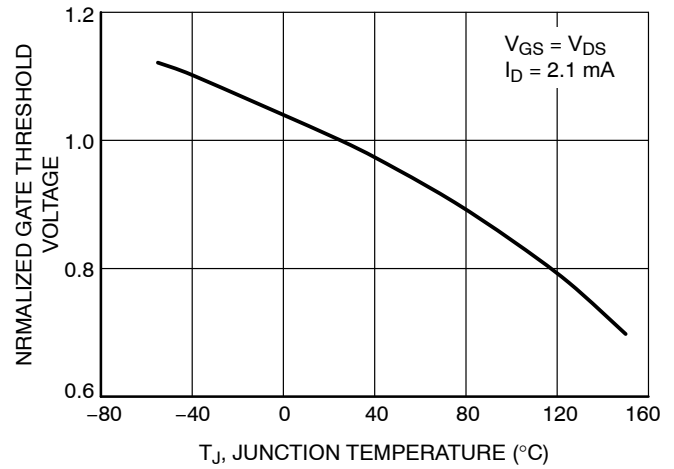


Figure 17. Normalized Gate Threshold Voltage vs. Temperature

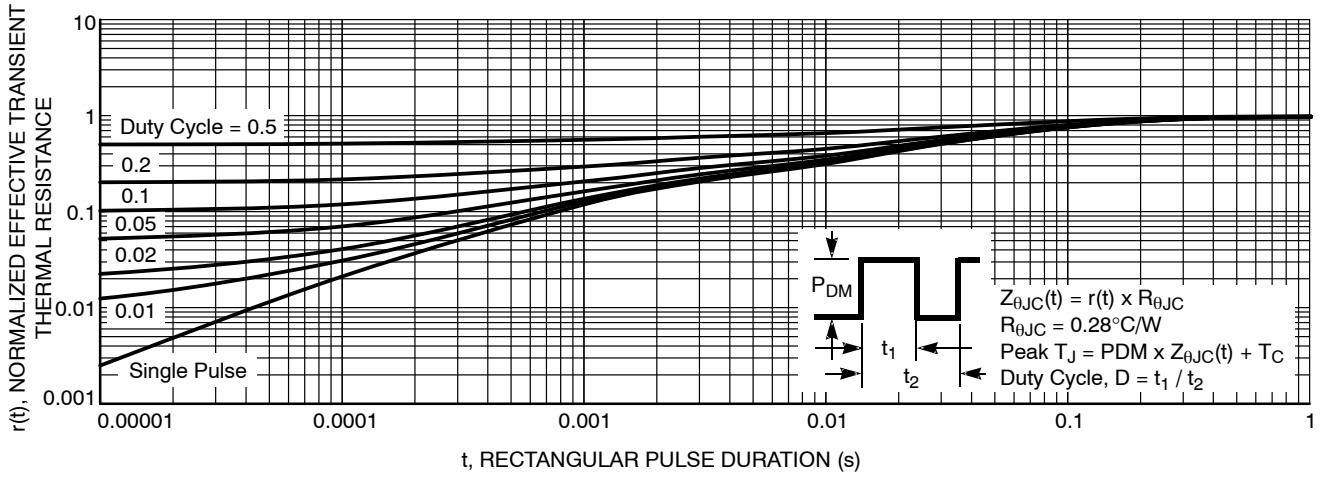


Figure 18. Transient Thermal Response Curve

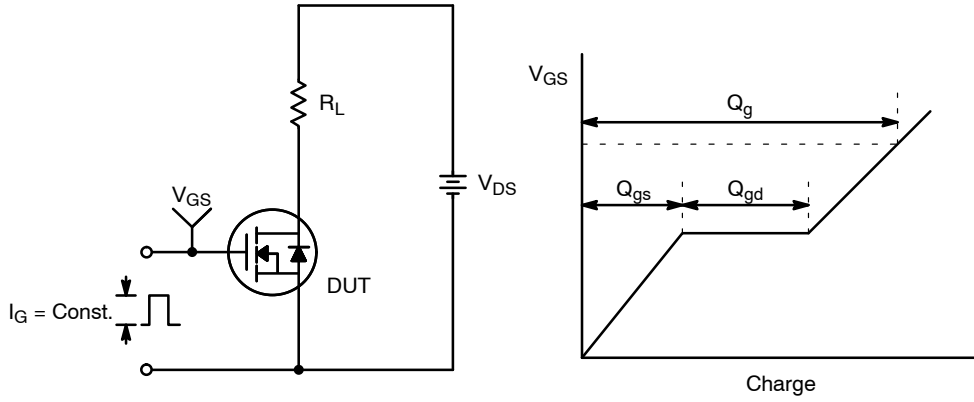


Figure 19. Gate Charge Test Circuit & Waveform

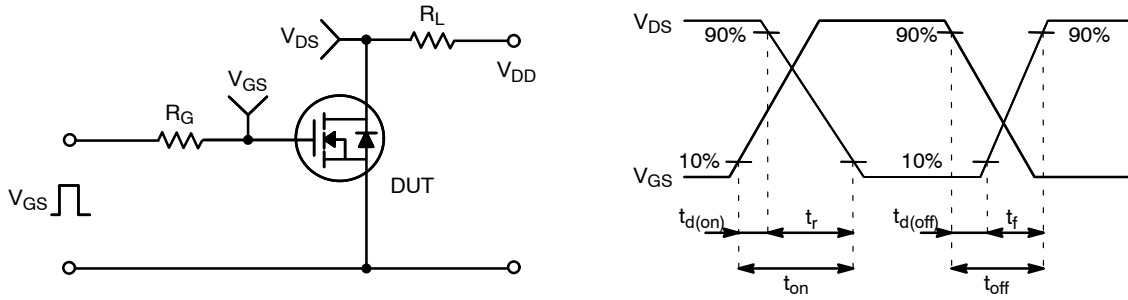


Figure 20. Resistive Switching Test Circuit & Waveforms

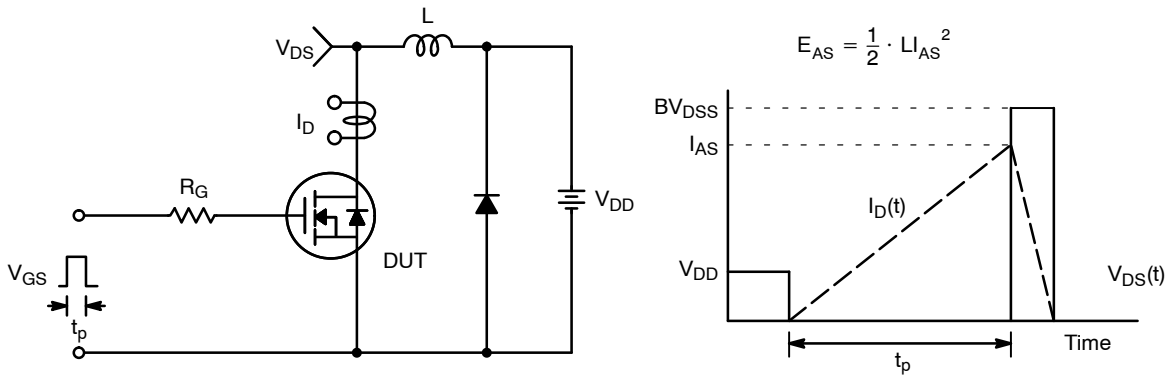


Figure 21. Unclamped Inductive Switching Test Circuit & Waveforms

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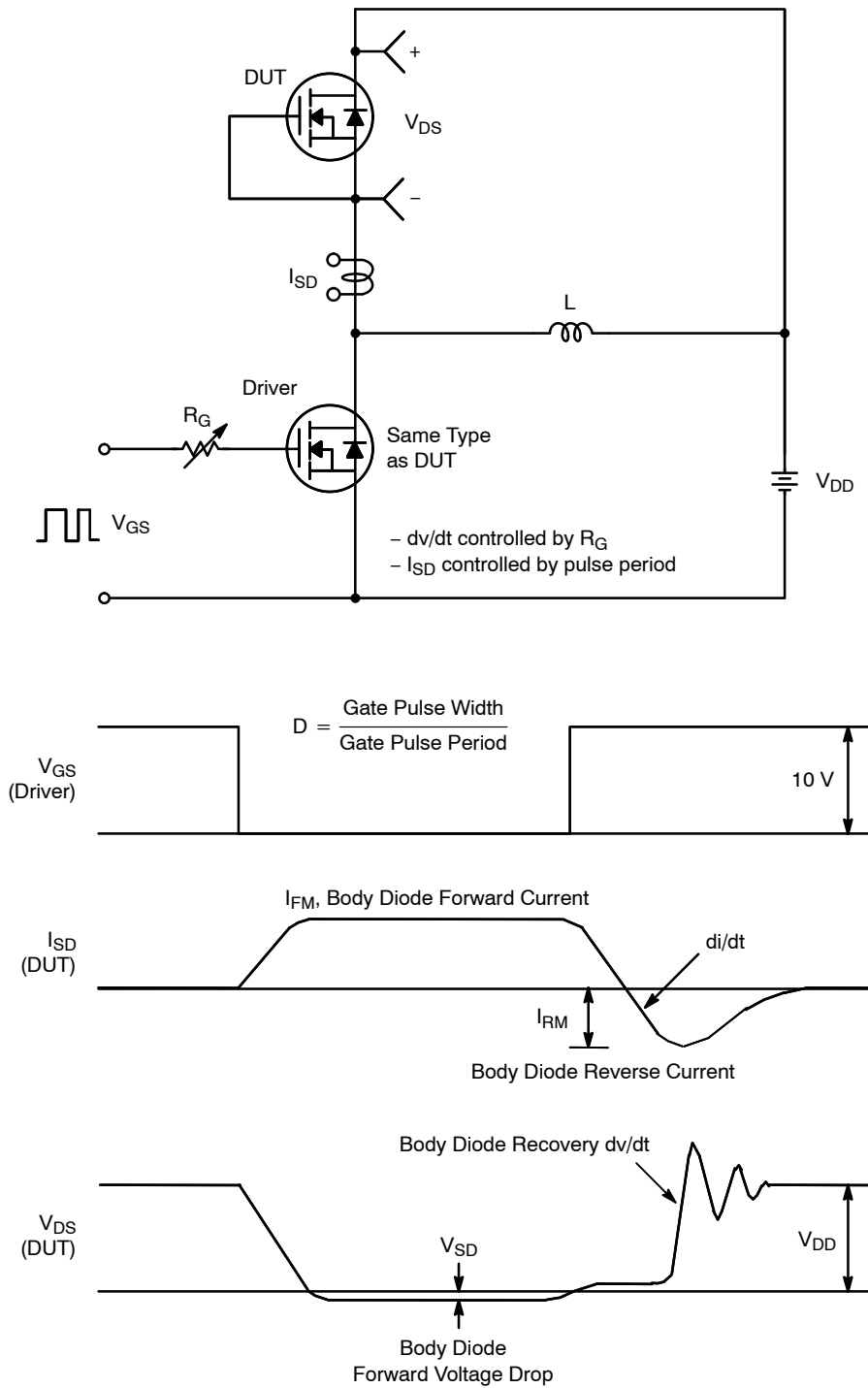
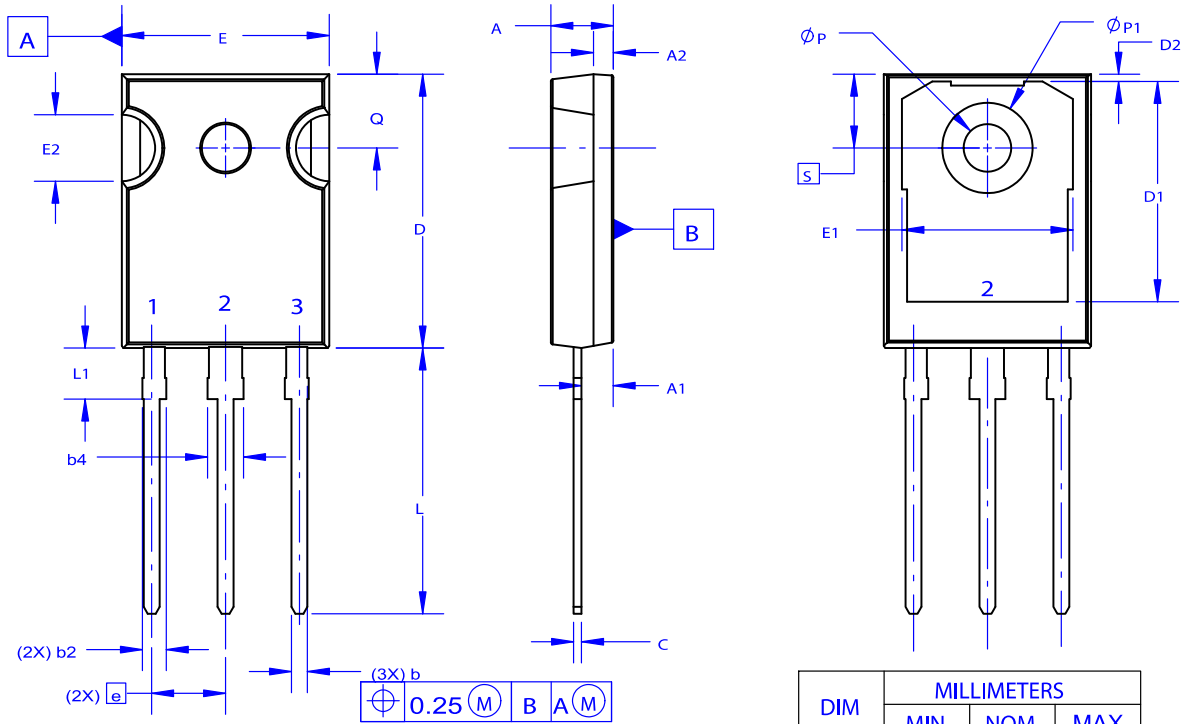


Figure 22. Peak Diode Recovery dv/dt Test Circuit & Waveforms

NVHL040N65S3F

PACKAGE DIMENSIONS


TO-247-3LD
CASE 340CX
ISSUE O



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
- D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
- E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

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