ROHM SEMICONDUCTOR

Datasheet

Sound Processor with Built-in 3-band Equalizer

BD37534FV

General Description

BD37534FV is a sound processor with built-in 3-band equalizer for car audio. A stereo input selector is available that functions to switch single end input and ground isolation input, input-gain control, main volume, loudness, 5ch fader volume, LPF for subwoofer and mixing input. Moreover, "Advanced switch circuit", which is an original ROHM technology, can reduce various switching noise (ex. No-signal, low frequency like 20Hz & large signal inputs). Also, "Advanced switch" makes microcomputer control easier, and constructs a high quality car audio system.

Features

- Reduced switching noise of input gain control, mute, main volume, fader volume, bass, middle, treble, loudness by using advanced switch circuit
- Built-in differential input selector that can make various combination of single-ended / differential input.
- Built-in ground isolation amplifier inputs, which is ideal for external stereo input.
- Built-in input gain controller reduces volume switching noise of a portable audio input.
- Decreased number of external components due to built-in 3-band equalizer filter, LPF for subwoofer and loudness filter. It is possible to freely control the Q, Gv, fo of the 3-band equalizer and fc of the LPF and Gv of the loudness through the I^2C BUS control
- A gain adjustment quantity of ±20dB with a 1 dB step gain adjustment is possible for the bass, middle and treble.
- Equipped with terminals for the subwoofer outputs. Also, the audio signal outputs of the front, rear and subwoofer can be chosen using the I^2C BUS control.
- Built-in mixing input and mixing attenuator.
- Energy-saving design resulting in low current consumption is achieved by utilizing the BiCMOS process. It has the advantage of quality over scaling down the power heat control of the internal regulators..
- Input pins and output pins are organized and separately laid out to keep the signal flow in one direction. This consequently simplifies the pattern layout of the set board and decreases the board dimensions.
- It is possible to control the I^2C BUS with 3.3V / 5V.

Applications

It is optimal for car audio systems. It can also be used for audio equipment of mini Compo, micro Compo, TV, etc.

Key Specifications

- Power Supply Voltage Range: 7.0V to 9.5V
- Circuit Current (No Signal): 38mA(Typ)
- Total Harmonic Distortion 1: (FRONT,REAR) 0.001%(Typ)
- Total Harmonic Distortion 2: (SUBWOOFER) 0.002%(Typ)
- Maximum Input Voltage: 2.3Vrms (Typ)
- Cross-talk Between Selectors: -100dB (Typ)
- Volume Control Range: +15dB to -79dB
- Output Noise Voltage 1: (FRONT,REAR) 3.8µVrms(Typ)
- Output Noise Voltage 2: (SUBWOOFER) 4.8µVrms(Typ)
- Residual Output Noise Voltage: 1.8µVrms (Typ)
- Operating Temperature Range: -40°C to +85°C

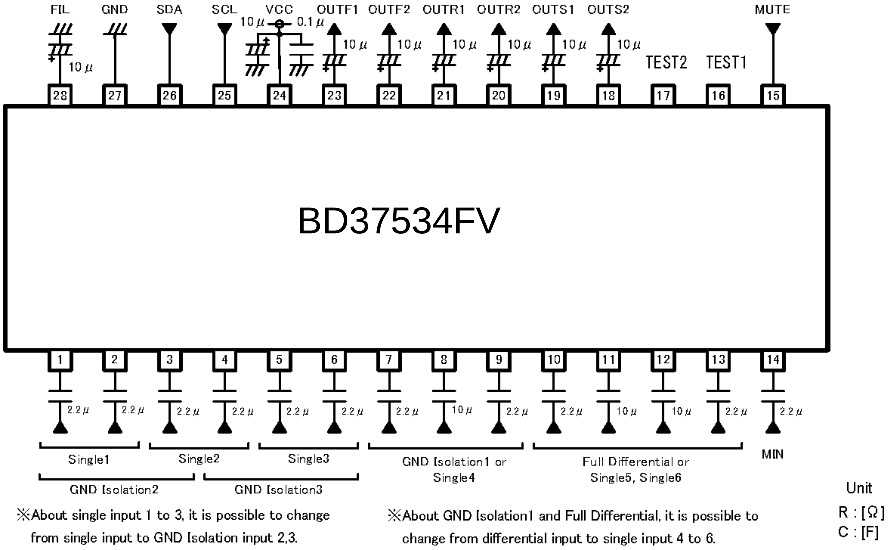
Package

W(Typ) x D(Typ) x H(Max)

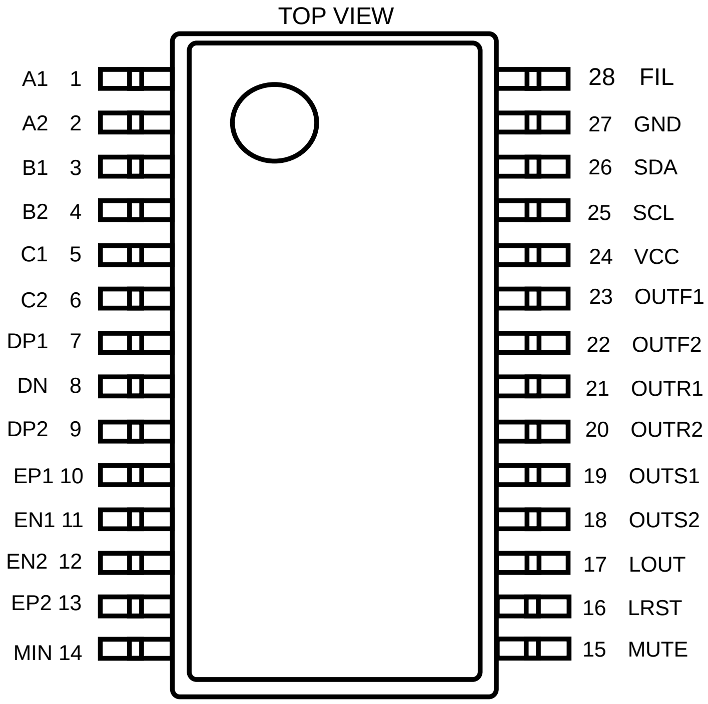
SSOP-B28
10.0mm x 7.60mm x 1.35mm

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Typical Application Circuit



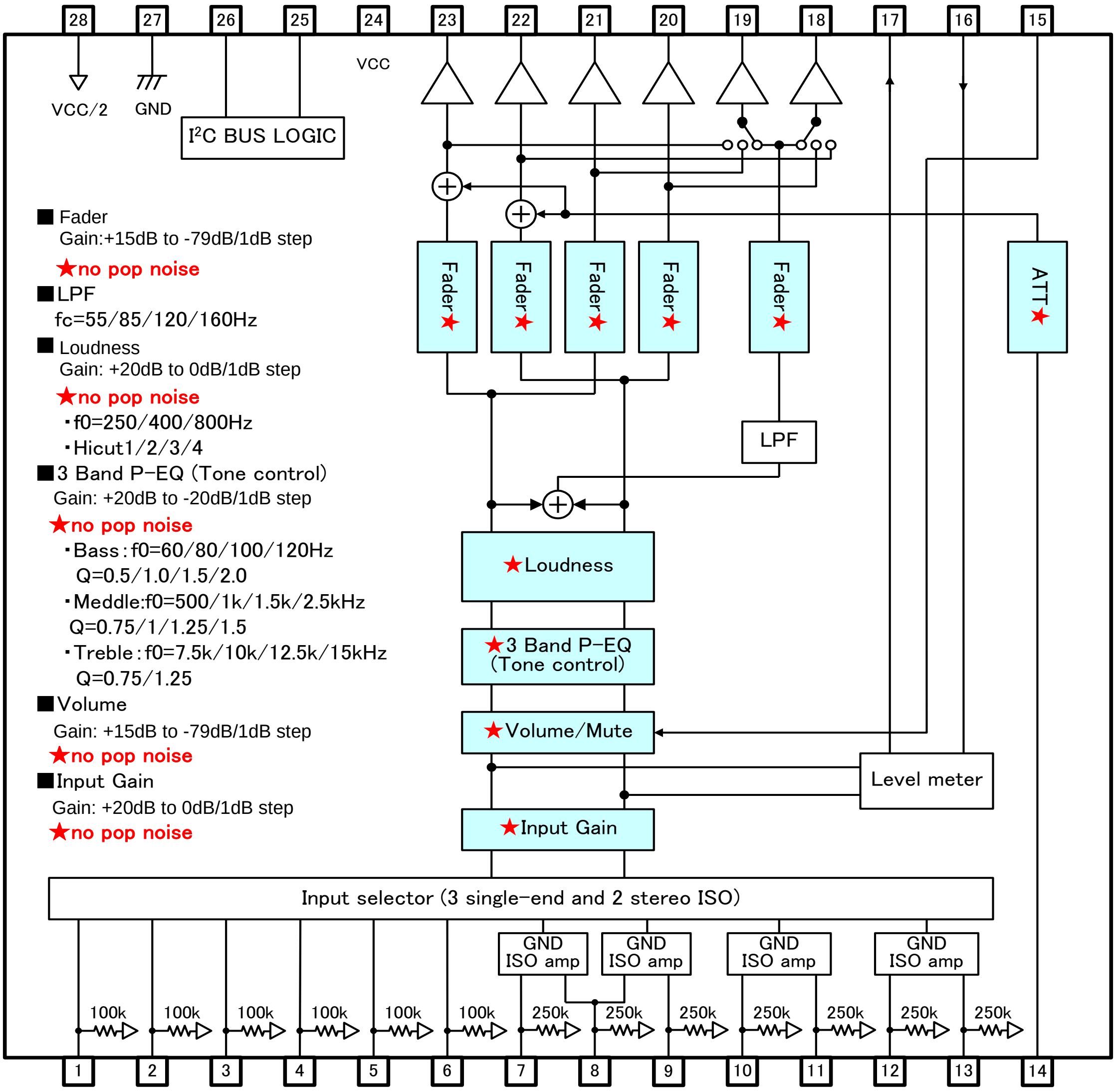
Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	A1	A input terminal of 1ch	15	MUTE	External compulsory mute terminal
2	A2	A input terminal of 2ch	16	LRST	Level meter reset terminal
3	B1	B input terminal of 1ch	17	LOUT	Output terminal for Level meter
4	B2	B input terminal of 2ch	18	OUTS2	Subwoofer output terminal of 2ch
5	C1	C input terminal of 1ch	19	OUTS1	Subwoofer output terminal of 1ch
6	C2	C input terminal of 2ch	20	OUTR2	Rear output terminal of 2ch
7	DP1	D positive input terminal of 1ch	21	OUTR1	Rear output terminal of 1ch
8	DN	D negative input terminal	22	OUTF2	Front output terminal of 2ch
9	DP2	D positive input terminal of 2ch	23	OUTF1	Front output terminal of 1ch
10	EP1	E positive input terminal of 1ch	24	VCC	Power supply terminal
11	EN1	E negative input terminal of 1ch	25	SCL	I^2C Communication clock terminal
12	EN2	E negative input terminal of 2ch	26	SDA	I^2C Communication data terminal
13	EP2	E positive input terminal of 2ch	27	GND	GND terminal
14	MIN	Mixing input terminal	28	FIL	VCC/2 terminal

Block Diagram



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	10.0	V
Input Voltage	V_{IN}	V_{CC}+0.3 to GND-0.3	V
Power Dissipation	Pd	1.06 (Note 1)	W
Storage Temperature	Tstg	-55 to +150	°C

(Note 1) When mounted on the standard board (70 x 70 x 1.6(mm^3), derate by 8.5mW/°C for Ta above 25°C.
Thermal resistance θja = 117.6(°C/W)
Material : A FR4 grass epoxy board (3% or less of copper foil area)

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Limit	Unit
Power Supply Voltage	V_{CC}	7.0 to 9.5	V
Temperature	Topr	-40 to +85	°C

Electrical Characteristics

(Unless otherwise noted, Ta=25°C, V_{CC}=8.5V, f=1kHz, V_{IN}=1Vrms, Rg=600Ω, R_L=10kΩ, A1 input, Input gain 0dB, Mute OFF, Volume 0dB, Tone control 0dB, Loudness 0dB, LPF OFF, Mixing OFF, Fader 0dB)

BLOCK	Parameter	Symbol	Limit Min	Limit Typ	Limit Max	Unit	Conditions
GENERAL	Circuit Current	I_Q	-	38	48	mA	No signal
GENERAL	Voltage Gain	G_V	-1.5	0	1.5	dB	G_V=20log(V_{OUT}/V_{IN})
GENERAL	Channel Balance	CB	-1.5	0	1.5	dB	CB = G_{V1}-G_{V2}
GENERAL	Total Harmonic Distortion 1 (FRONT,REAR)	THD+N1	-	0.001	0.05	%	V_{OUT}=1Vrms BW=400Hz-30KHz
GENERAL	Total Harmonic Distortion 2 (SUBWOOFER)	THD+N2	-	0.002	0.05	%	V_{OUT}=1Vrms BW=400Hz-30KHz
GENERAL	Output Noise Voltage 1 (FRONT,REAR) *	V_{NO1}	-	3.8	15	μVrms	Rg = 0Ω BW = IHF-A
GENERAL	Output Noise Voltage 2 (SUBWOOFER) *	V_{NO2}	-	4.8	15	μVrms	Rg = 0Ω BW = IHF-A
GENERAL	Residual Output Noise Voltage *	V_{NOR}	-	1.8	10	μVrms	Fader = -∞dB Rg = 0Ω BW = IHF-A
GENERAL	Crosstalk Between Channels *	CTC	-	-100	-90	dB	Rg = 0Ω CTC=20log(V_{OUT}/V_{IN}) BW = IHF-A
GENERAL	Ripple Rejection	RR	-	-70	-40	dB	f=1KHz V_{RR}=100mVrms RR=20log(V_{CC} IN/V_{OUT})
INPUT SELECTOR	Input Impedance(A, B, C)	R_{IN_S}	70	100	130	kΩ	
INPUT SELECTOR	Input Impedance (D, E)	R_{IN_D}	175	250	325	kΩ	
INPUT SELECTOR	Maximum Input Voltage	V_{IM}	2.1	2.3	-	Vrms	V_{IM} at THD+N(V_{OUT})=1% BW=400Hz-30KHz
INPUT SELECTOR	Crosstalk Between Selectors *	CTS	-	-100	-90	dB	Rg = 0Ω CTS=20log(V_{OUT}/V_{IN}) BW = IHF-A
INPUT SELECTOR	Common Mode Rejection Ratio * (D, E)	CMRR	50	65	-	dB	XP1 and XN input XP2 and XN input CMRR=20log(V_{IN}/V_{OUT}) BW = IHF-A,[*X・・・D,E]
INPUT GAIN	Minimum Input Gain	G_{IN_MIN}	-2	0	+2	dB	Input gain 0dB V_{IN}=100mVrms G_{IN}=20log(V_{OUT}/V_{IN})
INPUT GAIN	Maximum Input Gain	G_{IN_MAX}	+18	+20	+22	dB	Input gain +20dB V_{IN}=100mVrms G_{IN}=20log(V_{OUT}/V_{IN})
INPUT GAIN	Gain Set Error	G_{IN_ERR}	-2	0	+2	dB	GAIN=+20dB to +1dB

Electrical Characteristics - continued

BLOCK	Parameter	Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
MUTE	Mute Attenuation *	G_{MUTE}	-	-105	-85	dB	Mute ON G_{MUTE}=20log(V_{OUT}/V_{IN}) BW = IHF-A
VOLUME	Maximum Gain	G_{V_MAX}	13	15	17	dB	Volume = 15dB V_{IN}=100mVrms G_V=20log(V_{OUT}/V_{IN})
	Maximum Attenuation *	G_{V_MIN}	-	-100	-85	dB	Volume = -∞dB G_V=20log(V_{OUT}/V_{IN}) BW = IHF-A
	Attenuation Set Error 1	G_{V_ERR1}	-2	0	+2	dB	GAIN & ATT=+15dB to -15dB
	Attenuation Set Error 2	G_{V_ERR2}	-3	0	+3	dB	ATT=-16dB to -47dB
	Attenuation Set Error 3	G_{V_ERR3}	-4	0	+4	dB	ATT=-48dB to -79dB
BASS	Maximum Boost Gain	G_{B_BST}	18	20	22	dB	GAIN=+20dB f=100Hz V_{IN}=100mVrms GB=20log (V_{OUT}/V_{IN})
	Maximum Cut Gain	G_{B_CUT}	-22	-20	-18	dB	GAIN=-20dB f=100Hz V_{IN}=2Vrms GB=20log (V_{OUT}/V_{IN})
	Gain Set Error	G_{B_ERR}	-2	0	+2	dB	Gain=+20dB to -20dB f=100Hz
MIDDLE	Maximum Boost Gain	G_{M_BST}	18	20	22	dB	Gain=+20dB f=1KHz V_{IN}=100mVrms GM=20log (V_{OUT}/V_{IN})
	Maximum Cut Gain	G_{M_CUT}	-22	-20	-18	dB	Gain=-20dB f=1KHz V_{IN}=2Vrms GM=20log (V_{OUT}/V_{IN})
	Gain Set Error	G_{M_ERR}	-2	0	+2	dB	GAIN=+20dB to -20dB f=1KHz
TREBLE	Maximum Boost Gain	G_{T_BST}	18	20	22	dB	Gain=+20dB f=10kHz V_{IN}=100mVrms GT=20log (V_{OUT}/V_{IN})
	Maximum Cut Gain	G_{T_CUT}	-22	-20	-18	dB	Gain=-20dB f=10kHz V_{IN}=2Vrms GT=20log (V_{OUT}/V_{IN})
	Gain Set Error	G_{T_ERR}	-2	0	+2	dB	Gain=+20dB to -20dB f=10kHz
MIXING	Input Impedance	R_{IN_M}	19	27	35	kΩ	
	Maximum Input Voltage	V_{IM_M}	2.0	2.2	-	Vrms	V_{IM} at THD+N(V_{OUT})=1% BW=400Hz-30KHz
	Maximum Attenuation *	G_{MX_MIN}	-	-100	-85	dB	MIX=OFF G_{MX}=20log(V_{OUT}/V_{IN}) BW=INF-A
	Maximum Gain	G_{MX_MAX}	5	7	9	dB	ATT=+7dB G_{MX}=20log(V_{OUT}/V_{IN})
FADER / SUBWOOFER	Maximum Boost Gain	G_{F_BST}	13	15	17	dB	Fader=15dB V_{IN}=100mVrms G_F=20log(V_{OUT}/V_{IN})
	Maximum Attenuation *	G_{F_MIN}	-	-100	-90	dB	Fader = -∞dB GF=20log(V_{OUT}/V_{IN}) BW = IHF-A
	Gain Set Error	G_{F_ERR}	-2	0	+2	dB	Gain=+15dB to +1dB
	Attenuation Set Error 1	G_{F_ERR1}	-2	0	+2	dB	ATT=-1dB to -15dB
	Attenuation Set Error 2	G_{F_ERR2}	-3	0	+3	dB	ATT=-16dB to -47dB
	Attenuation Set Error 3	G_{F_ERR3}	-4	0	+4	dB	ATT=-48dB to -79dB
	Output Impedance	R_{OUT}	-	-	50	Ω	V_{IN}=100mVrms
	Maximum Output Voltage	V_{OM}	2	2.2	-	Vrms	THD+N=1% BW=400Hz-30KHz

Electrical Characteristics - continued

BLOCK	Parameter	Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
LOUDNESS	Maximum Gain	G_{L_MAX}	17	20	23	dB	Gain 20dB V_{IN}=100mVrms GL=20log(V_{OUT}/V_{IN})
	Gain Set Error	G_{L_ERR}	-2	0	+2	dB	GAIN=+20dB to +1dB
Level meter	Maximum Output Voltage	V_{L_MAX}	2.8	3.1	3.5	V	
	Output Offset Voltage	V_{L_OFF}	-	0	100	mV	

VP-9690A (Average value detection, effective value display) filter by Matsushita Communication is used for * measurement.
Phase between input / output is same.

Typical Performance Curves

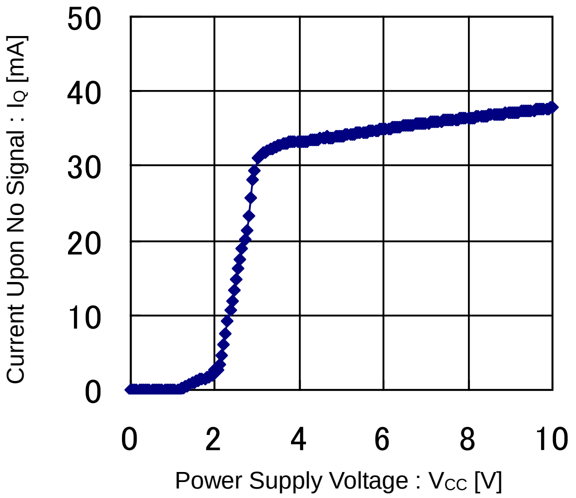


Figure 1. Circuit Current (No Signal) vs Power Supply Voltage

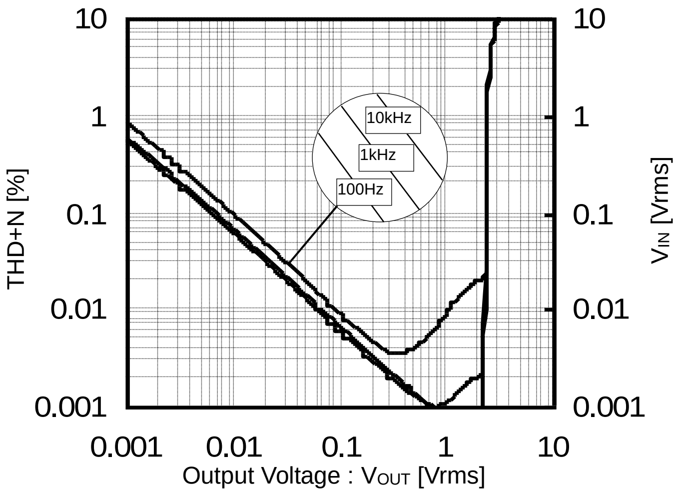


Figure 2. THD+N vs Output Voltage

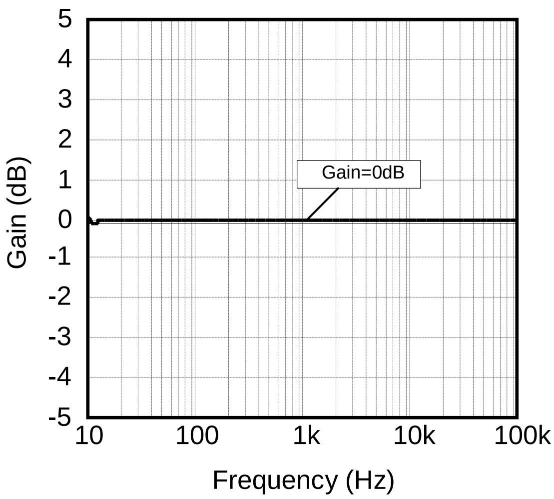


Figure 3. Gain vs Frequency

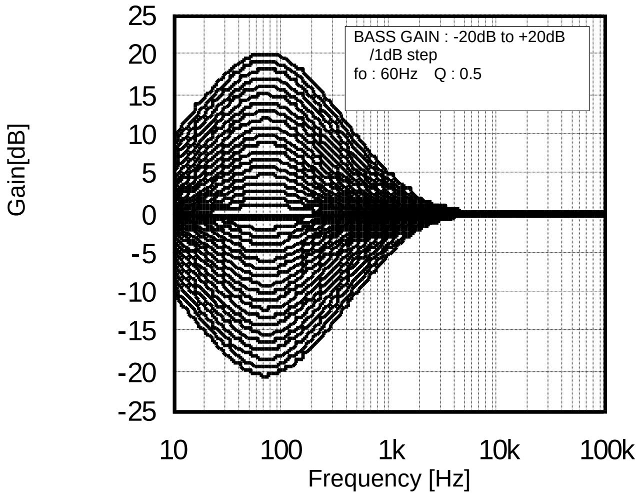


Figure 4. Bass Gain vs Frequency

Typical Performance Curves – continued

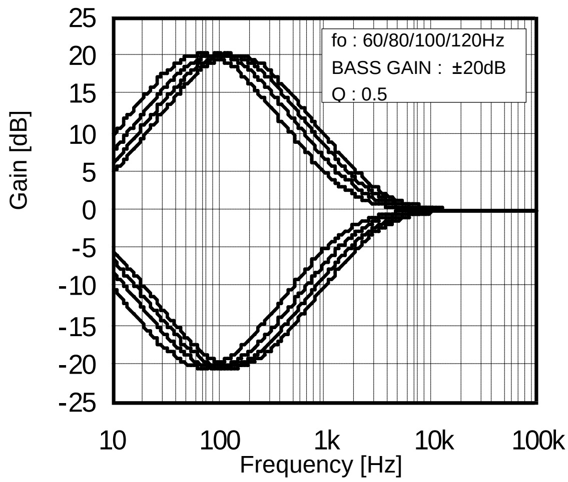


Figure 5. Bass fo vs Frequency

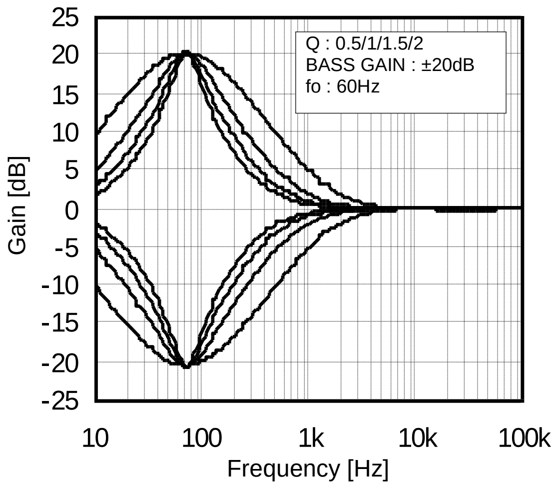


Figure 6. Bass Q vs Frequency

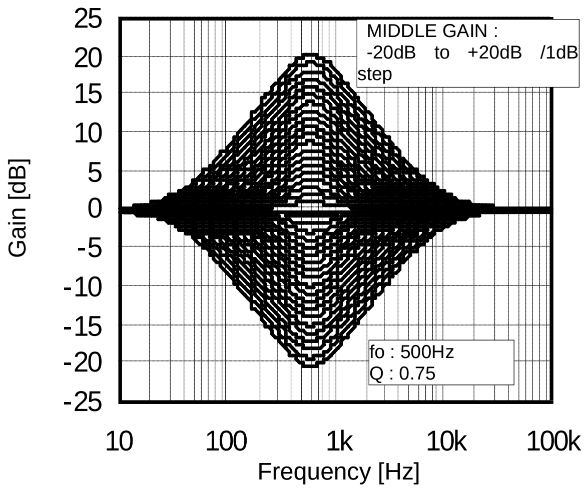


Figure 7. Middle Gain vs Frequency

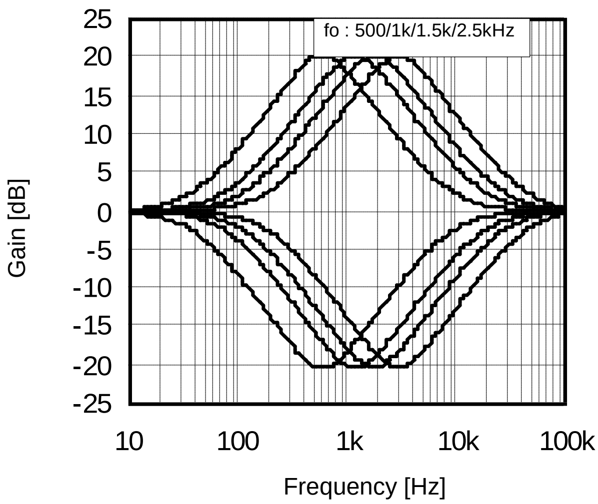


Figure 8. Middle fo vs Frequency

Typical Performance Curves – continued

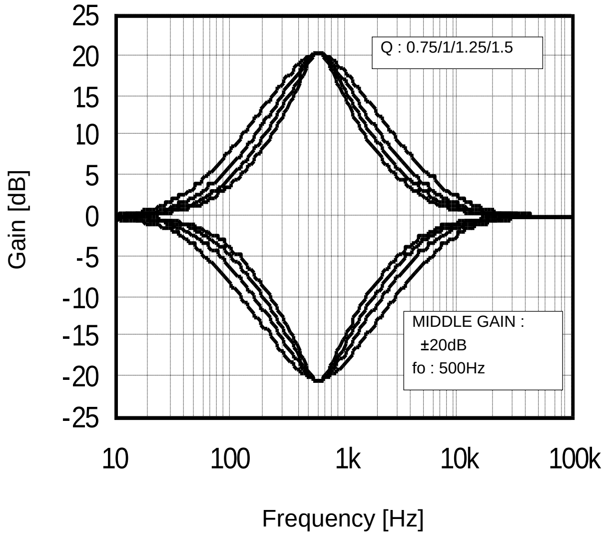


Figure 9. Middle Q vs Frequency

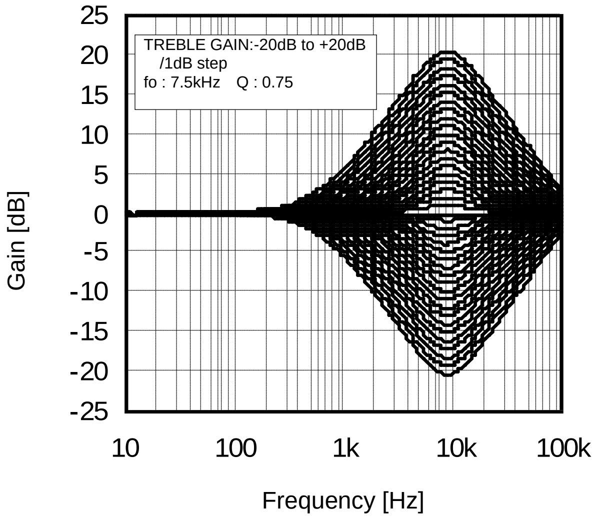


Figure 10. Treble Gain vs Frequency

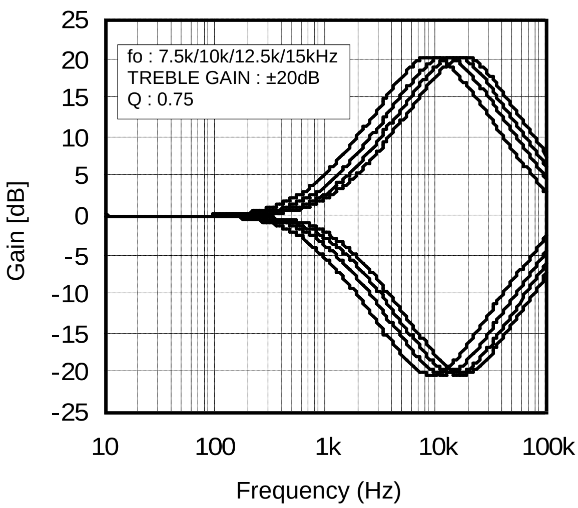


Figure 11. Treble fo vs Frequency

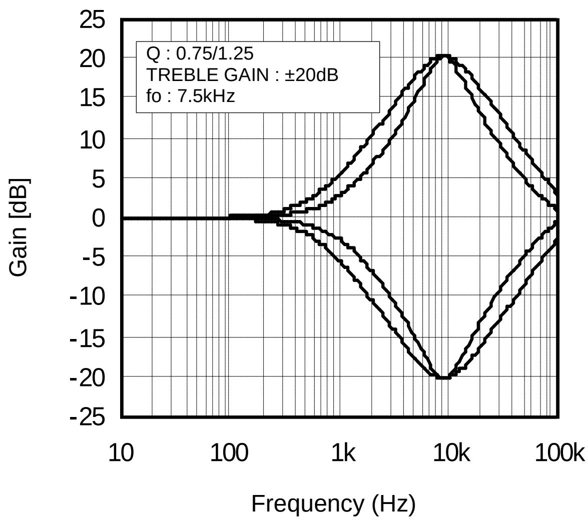


Figure 12. Treble Q vs Frequency

Typical Performance Curves – continued

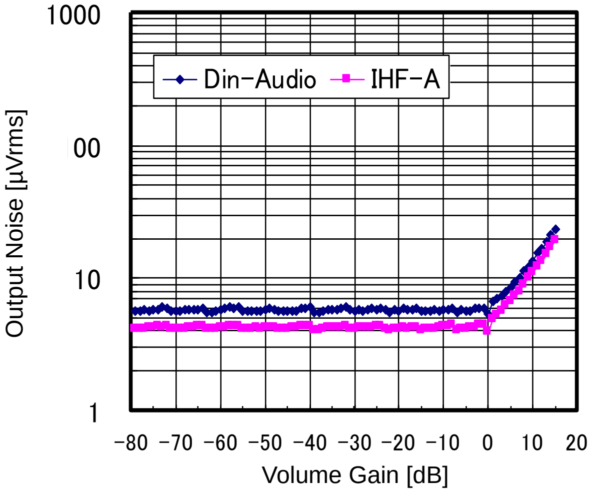


Figure 13. Output Noise vs Volume Gain

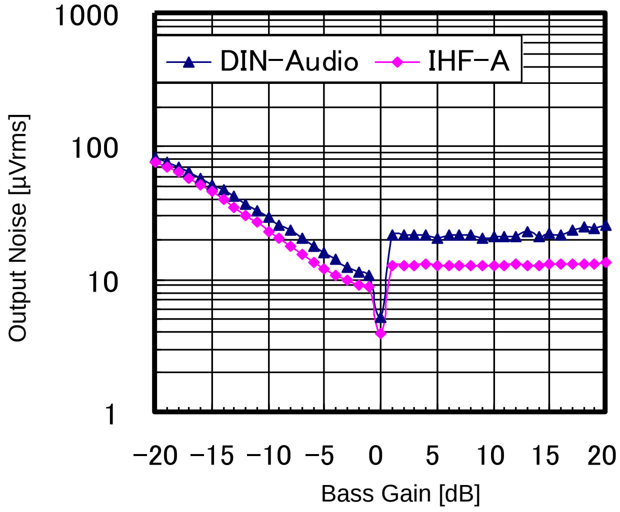


Figure 14. Output Noise vs Bass Gain

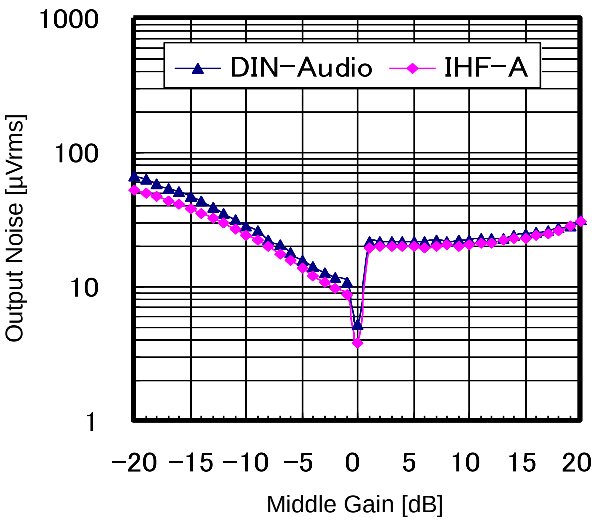


Figure 15. Output Noise vs Middle Gain

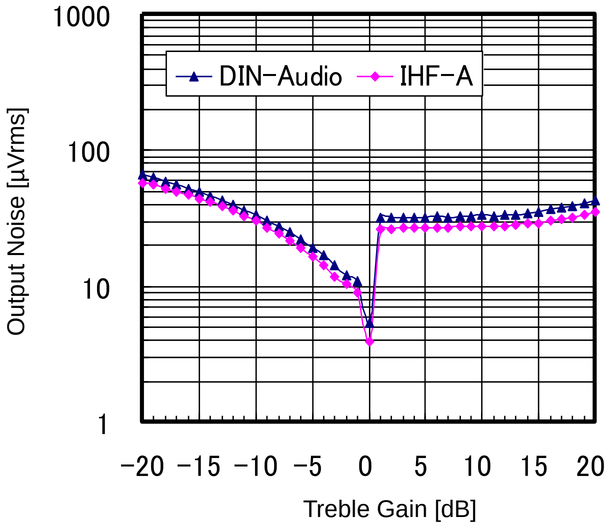


Figure 16. Output Noise vs Treble Gain

Typical Performance Curves – continued

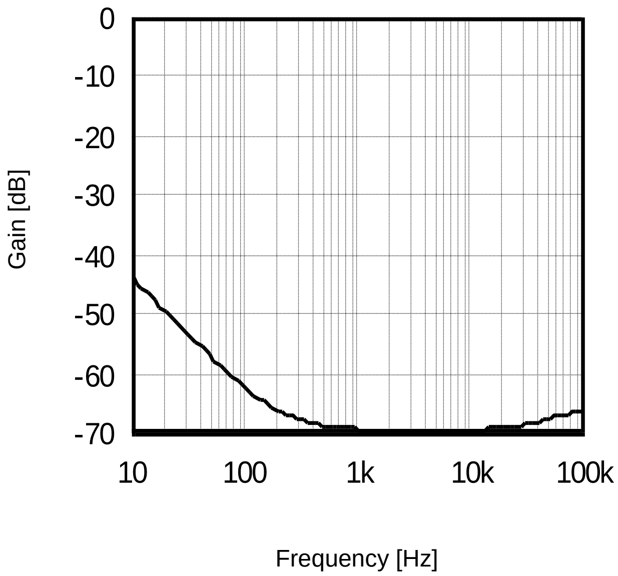


Figure 17. CMRR vs Frequency

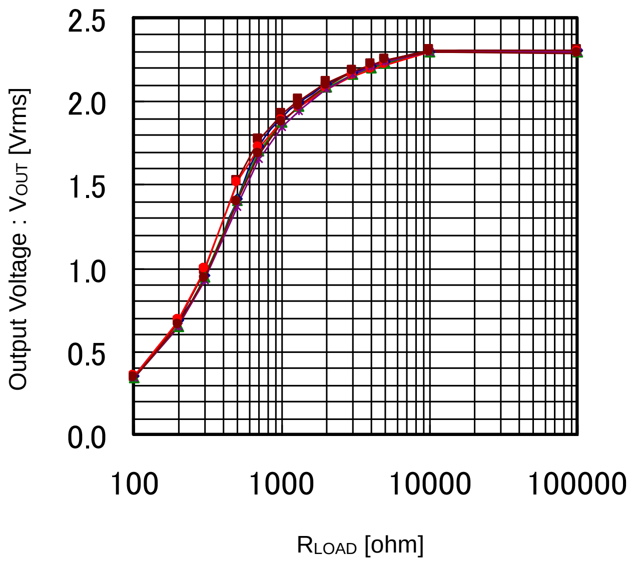


Figure 18. Output Voltage vs R_{LOAD}

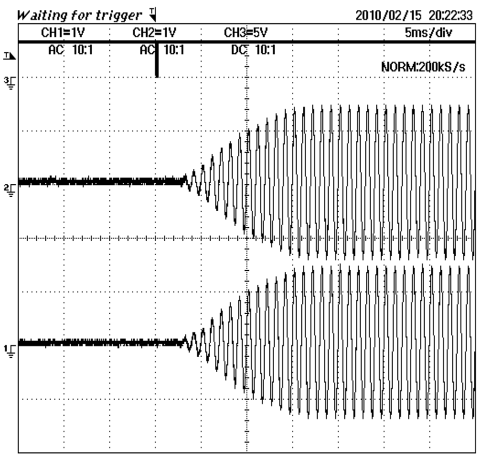


Figure 19. Advanced Switch 1

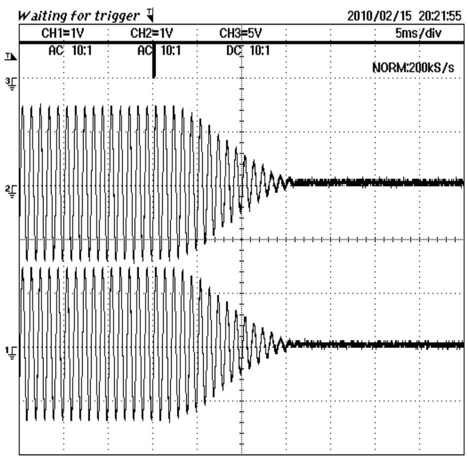


Figure 20. Advanced Switch 2

Typical Performance Curves – continued

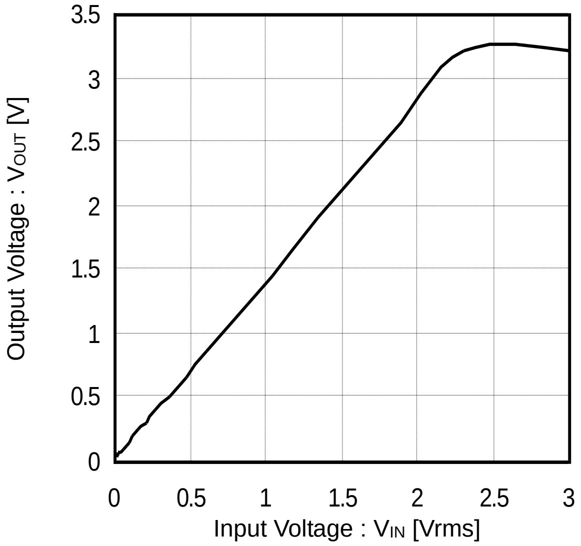


Figure 21. Output Voltage vs Level Meter V_{IN}

Timing Chart

CONTROL SIGNAL SPECIFICATION

(1) Electrical Specifications and Timing for Bus Lines and I/O Stages

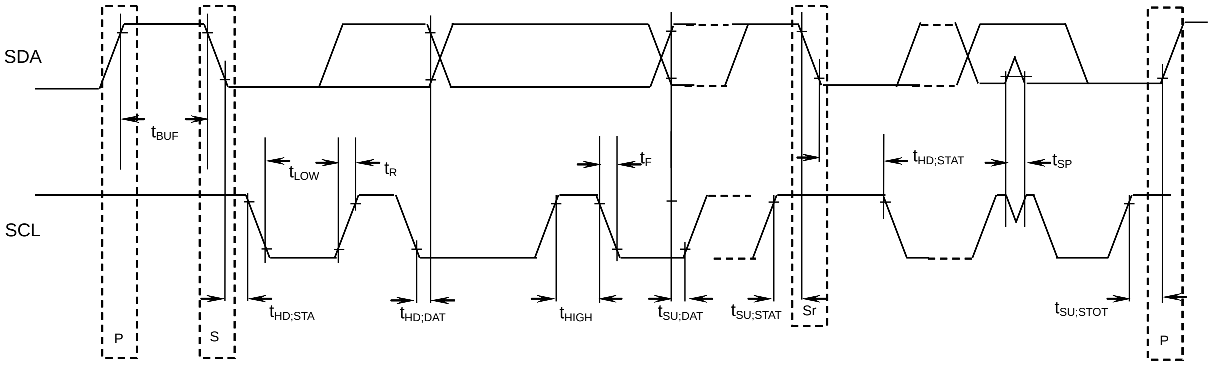


Figure 22. Definition of Timing on the I²C-bus

Table 1 Characteristics of the SDA and SCL bus lines for I²C-bus devices
(Unless otherwise noted, Ta=25°C, V_{CC}=8.5V)

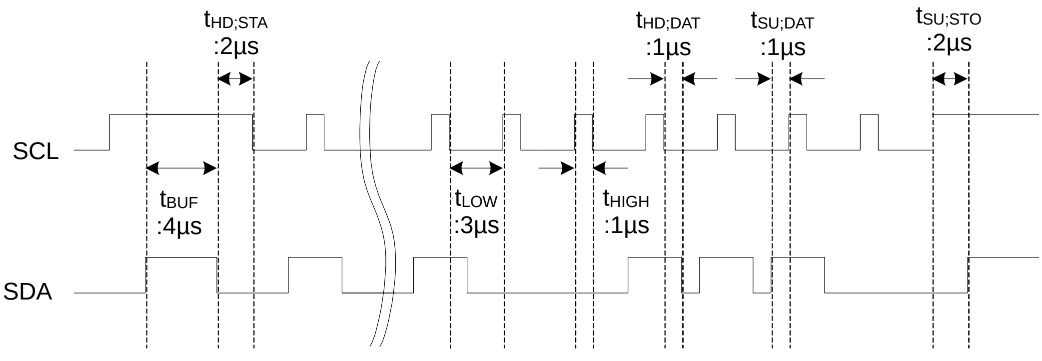
Parameter		Symbol	Fast-mode I²C-bus		Unit
			Min	Max	
1	SCL clock frequency	f_{SCL}	0	400	kHz
2	Bus free time between a STOP and START condition	t_{BUF}	1.3	-	µS
3	Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6	-	µS
4	LOW period of the SCL clock	t_{LOW}	1.3	-	µS
5	HIGH period of the SCL clock	t_{HIGH}	0.6	-	µS
6	Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	-	µS
7	Data hold time	$t_{HD;DAT}$	0.06(Note)	-	µS
8	Data set-up time	$t_{SU;DAT}$	120	-	ns
9	Set-up time for STOP condition	$t_{SU;STO}$	0.6	-	µS

All values referred to VIH Min and VIL Max Levels (see Table 2).

(Note) The device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIH Min of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
About 7($t_{HD;DAT}$), 8($t_{SU;DAT}$), make the setup in which the margin is fully in.

Table 2 Characteristics of the SDA and SCL I/O stages for I²C-bus devices

Parameter		Symbol	Fast-mode devices		Unit
			Min	Max	
10	LOW level input voltage	V_{IL}	-0.3	+1	V
11	HIGH level input voltage	V_{IH}	2.3	5	V
12	Pulse width of spikes which must be suppressed by the input filter.	t_{SP}	0	50	ns
13	LOW level output voltage: at 3mA sink current	V_{OL1}	0	0.4	V
14	Input current each I/O pin with an input voltage between 0.4V and 4.5V.	I_I	-10	+10	µA



SCL clock frequency : 250kHz

Figure 23. A Command Timing Example in the I²C Data Transmission

(2) I²C BUS FORMAT

	MSB	LSB	MSB	LSB	MSB	LSB		

S	Slave Address	A	Select Address	A	Data	A	P
1bit	8bit	1bit	8bit	1bit	8bit	1bit	1bit

S = Start conditions (Recognition of start bit)
Slave Address = Recognition of slave address. 7 bits in upper order are voluntary. The least significant bit is “L” due to writing.
A = ACKNOWLEDGE bit (Recognition of acknowledgement)
Select Address = Select every of volume, bass and treble.
Data = Data on every volume and tone.
P = Stop condition (Recognition of stop bit)

(3) I²C BUS Interface Protocol

(a) Basic Form

S	Slave Address	A	Select Address	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		

(b) Automatic increment (Select Address increases (+1) according to the number of data.

S	Slave Address	A	Select Address	A	Data1	A	Data2	A	····	DataN	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB			MSB LSB		

(Example) ①Data1 shall be set as data of address specified by Select Address.
②Data2 shall be set as data of address specified by Select Address +1.
③DataN shall be set as data of address specified by Select Address +N-1.

(c) Configuration unavailable for transmission (In this case, only Select Address1 is set.

S	Slave Address	A	Select Address1	A	Data	A	Select Address 2	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB		MSB LSB		

(Note) If any data is transmitted as Select Address 2 next to data, it is recognized as data, not as Select Address 2.

(4) Slave Address

MSB LSB

A6	A5	A4	A3	A2	A1	A0	R/W	
1	0	0	0	0	0	0	0	80H

(5) Select Address & Data

Items	Select Address (hex)	MSB			Data				LSB
		D7	D6	D5	D4	D3	D2	D1	D0
Initial setup 1	01	Advanced switch ON/OFF	0	Advanced switch time of Input Gain/Volume Tone/Fader/Loudness/Mixing		0	1	Advanced switch time of Mute	
Initial setup 2	02	LPF Phase	Level Meter RESET	Subwoofer Output Select		0	Subwoofer LPF fc		
Initial setup 3	03	0	0	0	Loudness fo		0	0	1
Input Selector	05	Full-diff Type	0	0	Input selector				
Input gain	06	Mute ON/OFF	0	0	Input Gain				
Volume gain	20	Volume Gain / Attenuation							
Fader 1ch Front	28	Fader Gain / Attenuation							
Fader 2ch Front	29	Fader Gain / Attenuation							
Fader 1ch Rear	2A	Fader Gain / Attenuation							
Fader 2ch Rear	2B	Fader Gain / Attenuation							
Fader Subwoofer	2C	Fader Gain / Attenuation							
Mixing	30	Mixing Gain / Attenuation							
Bass setup	41	0	0	Bass fo		0	0	Bass Q	
Middle setup	44	0	0	Middle fo		0	0	Middle Q	
Treble setup	47	0	0	Treble fo		0	0	0	Treble Q
Bass gain	51	Bass Boost/ Cut	0	0	Bass Gain				
Middle gain	54	Middle Boost/ Cut	0	0	Middle Gain				
Treble gain	57	Treble Boost/ Cut	0	0	Treble Gain				
Loudness Gain	75	0	Loudness Hicut		Loudness Gain				
System Reset	FE	1	0	0	0	0	0	0	1

Advanced switch

Note

1. The Advanced Switch works in the latch part while changing from one function to another.

2. Upon continuous data transfer, the Select Address rolls over because of the automatic increment function, as shown below.

→01→02→03→05→06→20→28→29→2A→2B→2C

→30→41→44→47→51→54→57→75

3. Advanced switch is not used for functions of input selector and subwoofer output select etc. Therefore, please turn on MUTE when changing the settings of this side of a set.

4. When using Mute function of this IC at the time of changing input selector, please switch mute ON/OFF while waiting for advanced-mute time.

Select address 01 (hex)

Time	MSB	Advanced switch time of Mute						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0.6msec	Advanced Switch ON/OFF	0	Advanced switch time of Input gain/Volume Tone/Fader/Loudness /Mixing		0	1	0	0
1.0msec							0	1
1.4msec							1	0
3.2msec							1	1

Time	MSB	Advanced switch time of Input gain/Volume/Tone/Fader/Loudness/Mixing						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
4.7 msec	Advanced Switch ON/OFF	0	0	0	0	1	Advanced switch Time of Mute	
7.1 msec			0	1				
11.2 msec			1	0				
14.4 msec			1	1				

Mode	MSB	Advanced switch ON/OFF						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0	0	Advanced switch time of Input gain/Volume Tone/Fader/Loudness /Mixing		0	1	Advanced switch Time of Mute	
ON	1							

Select address 02(hex)

fc	MSB	Subwoofer LPF fc						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	LPF Phase	Level Meter RESET	Subwoofer Output Select		0	0	0	0
55Hz						0	0	1
85Hz						0	1	0
120Hz						0	1	1
160Hz						1	0	0
Prohibition						Other setting		

Mode	MSB	Subwoofer Output Select						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
LPF	LPF Phase	Level Meter RESET	0	0	0	Subwoofer LPF fc		
Front			0	1				
Rear			1	0				
Prohibition			1	1				

Mode	MSB	Level Meter RESET						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
HOLD	LPF Phase	0	Subwoofer output select		0	Subwoofer LPF fc		
RESET		1						

Phase	MSB	LPF Phase						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0°	0	Level Meter RESET	Subwoofer output select		0	Subwoofer LPF fc		
180°	1							

: Initial Condition

Select address 03(hex)

f0	MSB			Loudness fo				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
250Hz	0	0	0	0	0	0	0	1
400Hz				0	1			
800Hz				1	0			
Prohibition				1	1			

Select address 05(hex)

Mode			MSB			Input Selector				LSB
	OUTF1	OUTF2	D7	D6	D5	D4	D3	D2	D1	D0
A	A1	A2	Full-diff bias type select	0	0	0	0	0	0	0
B	B1	B2				0	0	0	0	1
C	C1	C2				0	0	0	1	0
D single	DP1	DP2				0	0	0	1	1
E1 single	EP1	EN1				0	1	0	1	0
E2 single	EN2	EP2				0	1	0	1	1
A diff	A1	B1				0	1	1	1	1
C diff	B2	C2				1	0	0	0	0
D diff	DP1	DP2				0	0	1	1	0
E full diff	EP1	EP2				0	1	0	0	0
Input SHORT						0	1	0	0	1
Prohibition						Other setting				

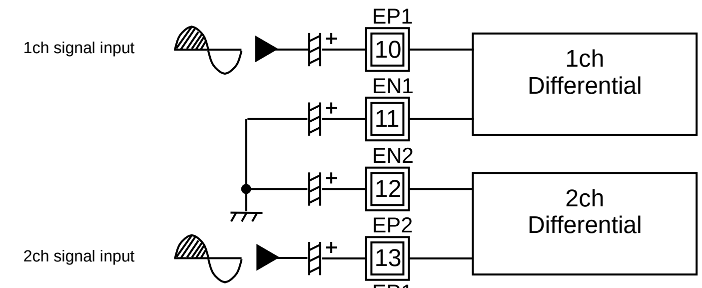
Input SHORT : The input impedance of each input terminal is lowered from 100kΩ(TYP) to 6 kΩ(TYP).
(For quick charge of coupling capacitor)

Mode	MSB			Full-diff Bias Type Select				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Negative Input	0	0	0	Input Selector				
Bias	1							

: Initial condition

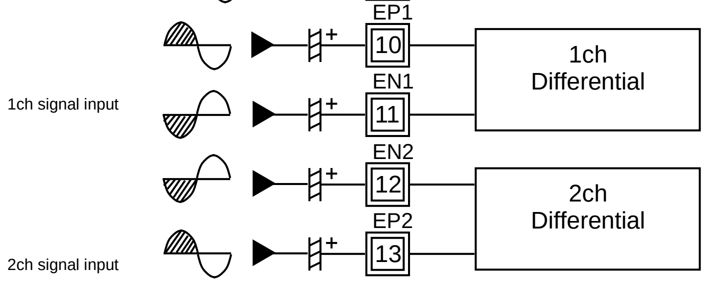
Negative input type

For Ground –isolation type)



Bias type

For differential amplifier type



Select address 06 (hex)

Gain	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
	Input Gain							
0dB	Mute ON/OFF	0	0	0	0	0	0	0
1dB				0	0	0	0	1
2dB				0	0	0	1	0
3dB				0	0	0	1	1
4dB				0	0	1	0	0
5dB				0	0	1	0	1
6dB				0	0	1	1	0
7dB				0	0	1	1	1
8dB				0	1	0	0	0
9dB				0	1	0	0	1
10dB				0	1	0	1	0
11dB				0	1	0	1	1
12dB				0	1	1	0	0
13dB				0	1	1	0	1
14dB				0	1	1	1	0
15dB				0	1	1	1	1
16dB				1	0	0	0	0
17dB				1	0	0	0	1
18dB				1	0	0	1	0
19dB				1	0	0	1	1
20dB				1	0	1	0	0
Prohibition				1	1	0	1	1
				:	:	:	:	:
				1	1	1	1	1

Mode	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
	Mute ON/OFF							
OFF	0	0	0	Input Gain				
ON	1							

: Initial condition

Select address 20, 28, 29, 2A, 2B, 2C (hex)

Gain & ATT	MSB	Vol, Fader Gain / Attenuation						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Prohibition	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1
	:	:	:	:	:	:	:	:
	0	1	1	1	0	0	0	0
15dB	0	1	1	1	0	0	0	1
14dB	0	1	1	1	0	0	1	0
13dB	0	1	1	1	0	0	1	1
:	:	:	:	:	:	:	:	:
-77dB	1	1	0	0	1	1	0	1
-78dB	1	1	0	0	1	1	1	0
-79dB	1	1	0	0	1	1	1	1
Prohibition	1	1	0	1	0	0	0	0
	:	:	:	:	:	:	:	:
	1	1	1	1	1	1	1	0
-∞dB	1	1	1	1	1	1	1	1

Select address 30(hex)

Gain & ATT	MSB	Mixing Gain / Attenuation						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Prohibition	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1
	:	:	:	:	:	:	:	:
	0	1	1	1	1	0	0	0
7dB	0	1	1	1	1	0	0	1
6dB	0	1	1	1	1	0	1	0
5dB	0	1	1	1	1	0	1	1
:	:	:	:	:	:	:	:	:
-77dB	1	1	0	0	1	1	0	1
-78dB	1	1	0	0	1	1	1	0
-79dB	1	1	0	0	1	1	1	1
Prohibition	1	1	0	1	0	0	0	0
	:	:	:	:	:	:	:	:
	1	1	1	1	1	1	1	0
MIX OFF	1	1	1	1	1	1	1	1

: Initial condition

Select address 41(hex)

Q factor	MSB		Bass Q factor					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0.5	0	0	Bass fo		0	0	0	0
1.0							0	1
1.5							1	0
2.0							1	1

fo	MSB		Bass fo					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
60Hz	0	0	0	0	0	0	Bass Q factor	
80Hz			0	1				
100Hz			1	0				
120Hz			1	1				

Select address 44(hex)

Q factor	MSB		Middle Q factor					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0.75	0	0	Middle fo		0	0	0	0
1.0							0	1
1.25							1	0
1.5							1	1

fo	MSB		Middle fo					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
500Hz	0	0	0	0	0	0	Middle Q factor	
1kHz			0	1				
1.5kHz			1	0				
2.5kHz			1	1				

Select address 47 (hex)

Q factor	MSB		Treble Q factor					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0.75	0	0	Treble fo		0	0	0	0
1.25								1

fo	MSB		Treble fo					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
7.5kHz	0	0	0	0	0	0	0	Treble Q factor
10kHz			0	1				
12.5kHz			1	0				
15kHz			1	1				

: Initial condition

Select address 51, 54, 57 (hex)

Gain	MSB D7	D6	D5	Bass/Middle/Treble Gain D4	D3	D2	D1	LSB D0
0dB	Bass/ Middle/ Treble Boost /cut	0	0	0	0	0	0	0
1dB				0	0	0	0	1
2dB				0	0	0	1	0
3dB				0	0	0	1	1
4dB				0	0	1	0	0
5dB				0	0	1	0	1
6dB				0	0	1	1	0
7dB				0	0	1	1	1
8dB				0	1	0	0	0
9dB				0	1	0	0	1
10dB				0	1	0	1	0
11dB				0	1	0	1	1
12dB				0	1	1	0	0
13dB				0	1	1	0	1
14dB				0	1	1	1	0
15dB				0	1	1	1	1
16dB				1	0	0	0	0
17dB				1	0	0	0	1
18dB				1	0	0	1	0
19dB				1	0	0	1	1
20dB				1	0	1	0	0
Prohibition				1	0	1	0	1
				:	:	:	:	:
				1	1	1	1	0
				1	1	1	1	1

Mode	MSB D7	D6	D5	Bass/Middle/Treble Boost/Cut D4	D3	D2	D1	LSB D0
Boost	0	0	0	Bass/Middle/Treble Gain				
Cut	1							

: Initial condition

Select address 75 (hex)

Mode	MSB	Loudness Hicut					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Hicut1	0	0	0	Loudness Gain				
Hicut2		0	1					
Hicut3		1	0					
Hicut4		1	1					

Gain	MSB	Loudness Gain						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	0	Loudness Hicut		0	0	0	0	0
1dB				0	0	0	0	1
2dB				0	0	0	1	0
3dB				0	0	0	1	1
4dB				0	0	1	0	0
5dB				0	0	1	0	1
6dB				0	0	1	1	0
7dB				0	0	1	1	1
8dB				0	1	0	0	0
9dB				0	1	0	0	1
10dB				0	1	0	1	0
11dB				0	1	0	1	1
12dB				0	1	1	0	0
13dB				0	1	1	0	1
14dB				0	1	1	1	0
15dB				0	1	1	1	1
16dB				1	0	0	0	0
17dB				1	0	0	0	1
18dB				1	0	0	1	0
19dB				1	0	0	1	1
20dB				1	0	1	0	0
Prohibition				1	0	1	0	1
				:	:	:	:	:
				1	1	1	1	1

: Initial condition

(6) About Power ON Reset

Built-in IC initialization is made during power ON of the supply voltage. Please send initial data to all addresses at supply voltage on. Also, please turn ON MUTE at the set side until initial data is sent.

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Rise Time of VCC	t_{RISE}	33	-	-	µsec	V_{CC} rise time from 0V to 5V
VCC Voltage of Release Power ON Reset	V_{POR}	-	4.1	-	V	

(7) About External Compulsory Mute Terminal

It is possible to forcibly set MUTE externally by setting the input voltage at the MUTE terminal.

Mute Voltage Condition	Mode
GND to 1.0V	MUTE ON
2.3V to V_{CC}	MUTE OFF

Establish the mode of MUTE using a defined voltage condition.

Application Information

1. Function and Specifications

<table>
<tr><th>Function</th><th>Specifications</th></tr>
<tr><td>Input selector</td><td>・ (Stereo input)
・ Single-End/Diff/Full-Diff
(Possible to set the number of single-end/diff/full-diff as follows:)
<table>
<tr><th></th><th>Single-End</th><th>Differential</th><th>Full-Differential</th></tr>
<tr><td>Mode 1</td><td>0</td><td>3</td><td>1</td></tr>
<tr><td>Mode 2</td><td>1</td><td>2</td><td>1</td></tr>
<tr><td>Mode 3</td><td>3</td><td>1</td><td>1</td></tr>
<tr><td>Mode 4</td><td>4</td><td>0</td><td>1</td></tr>
<tr><td>Mode 5</td><td>5</td><td>1</td><td>0</td></tr>
<tr><td>Mode 6</td><td>6</td><td>0</td><td>0</td></tr>
</table>Table.1 Combination of input selector</td></tr>
<tr><td>Input gain</td><td>・ +20dB to 0dB (1dB step)
・ Possible to use “Advanced switch” for prevention of switching noise.</td></tr>
<tr><td>Mute</td><td>・ Possible to use “Advanced switch” for prevention of switching noise.</td></tr>
<tr><td>Volume</td><td>・ +15dB to -79dB (1dB step), -∞dB
・ Possible to use “Advanced switch” for prevention of switching noise.</td></tr>
<tr><td>Bass</td><td>・ +20dB to -20dB (1dB step)
・ Q=0.5, 1, 1.5, 2
・ fo=60, 80, 100, 120Hz
・ Possible to use “Advanced switch” when changing gain</td></tr>
<tr><td>Middle</td><td>・ +20dB to -20dB (1dB step)
・ Q=0.75, 1, 1.25, 1.5
・ fo=500, 1k, 1.5k 2.5kHz
・ Possible to use “Advanced switch” when changing gain</td></tr>
<tr><td>Treble</td><td>・ +20dB to -20dB (1dB step)
・ Q=0.75, 1.25
・ fo=7.5k, 10k, 12.5k, 15kHz
・ Possible to use “Advanced switch” when changing gain</td></tr>
<tr><td>Fader</td><td>・ +15dB to -79dB(1dB step), -∞dB
・ Possible to use “Advanced switch” for prevention of switching noise.</td></tr>
<tr><td>Loudness</td><td>・ 20dB to 0dB(1dB step)
・ fo=250/400/800Hz
・ Possible to use “Advanced switch” for prevention of switching noise.</td></tr>
<tr><td>LPF</td><td>・ fc=55/85/120/160Hz, pass
・ Phase shift (0°/180°)</td></tr>
<tr><td>Mixing</td><td>・ Monaural input
・ +7dB to -79dB (1dB step), -∞dB
・ Possible to use “Advanced switch” for prevention of switching noise.</td></tr>
<tr><td>Level meter</td><td>・ I^{2}C BUS control
・ DC Output</td></tr>
</table>

2. Volume / Fader Volume / Mixing Attenuation of the Details

(dB)	D7	D6	D5	D4	D3	D2	D1	D0	(dB)	D7	D6	D5	D4	D3	D2	D1	D0
+15	0	1	1	1	0	0	0	1	-33	1	0	1	0	0	0	0	1
+14	0	1	1	1	0	0	1	0	-34	1	0	1	0	0	0	1	0
+13	0	1	1	1	0	0	1	1	-35	1	0	1	0	0	0	1	1
+12	0	1	1	1	0	1	0	0	-36	1	0	1	0	0	1	0	0
+11	0	1	1	1	0	1	0	1	-37	1	0	1	0	0	1	0	1
+10	0	1	1	1	0	1	1	0	-38	1	0	1	0	0	1	1	0
+9	0	1	1	1	0	1	1	1	-39	1	0	1	0	0	1	1	1
+8	0	1	1	1	1	0	0	0	-40	1	0	1	0	1	0	0	0
+7	0	1	1	1	1	0	0	1	-41	1	0	1	0	1	0	0	1
+6	0	1	1	1	1	0	1	0	-42	1	0	1	0	1	0	1	0
+5	0	1	1	1	1	0	1	1	-43	1	0	1	0	1	0	1	1
+4	0	1	1	1	1	1	0	0	-44	1	0	1	0	1	1	0	0
+3	0	1	1	1	1	1	0	1	-45	1	0	1	0	1	1	0	1
+2	0	1	1	1	1	1	1	0	-46	1	0	1	0	1	1	1	0
+1	0	1	1	1	1	1	1	1	-47	1	0	1	0	1	1	1	1
0	1	0	0	0	0	0	0	0	-48	1	0	1	1	0	0	0	0
-1	1	0	0	0	0	0	0	1	-49	1	0	1	1	0	0	0	1
-2	1	0	0	0	0	0	1	0	-50	1	0	1	1	0	0	1	0
-3	1	0	0	0	0	0	1	1	-51	1	0	1	1	0	0	1	1
-4	1	0	0	0	0	1	0	0	-52	1	0	1	1	0	1	0	0
-5	1	0	0	0	0	1	0	1	-53	1	0	1	1	0	1	0	1
-6	1	0	0	0	0	1	1	0	-54	1	0	1	1	0	1	1	0
-7	1	0	0	0	0	1	1	1	-55	1	0	1	1	0	1	1	1
-8	1	0	0	0	1	0	0	0	-56	1	0	1	1	1	0	0	0
-9	1	0	0	0	1	0	0	1	-57	1	0	1	1	1	0	0	1
-10	1	0	0	0	1	0	1	0	-58	1	0	1	1	1	0	1	0
-11	1	0	0	0	1	0	1	1	-59	1	0	1	1	1	0	1	1
-12	1	0	0	0	1	1	0	0	-60	1	0	1	1	1	1	0	0
-13	1	0	0	0	1	1	0	1	-61	1	0	1	1	1	1	0	1
-14	1	0	0	0	1	1	1	0	-62	1	0	1	1	1	1	1	0
-15	1	0	0	0	1	1	1	1	-63	1	0	1	1	1	1	1	1
-16	1	0	0	1	0	0	0	0	-64	1	1	0	0	0	0	0	0
-17	1	0	0	1	0	0	0	1	-65	1	1	0	0	0	0	0	1
-18	1	0	0	1	0	0	1	0	-66	1	1	0	0	0	0	1	0
-19	1	0	0	1	0	0	1	1	-67	1	1	0	0	0	0	1	1
-20	1	0	0	1	0	1	0	0	-68	1	1	0	0	0	1	0	0
-21	1	0	0	1	0	1	0	1	-69	1	1	0	0	0	1	0	1
-22	1	0	0	1	0	1	1	0	-70	1	1	0	0	0	1	1	0
-23	1	0	0	1	0	1	1	1	-71	1	1	0	0	0	1	1	1
-24	1	0	0	1	1	0	0	0	-72	1	1	0	0	1	0	0	0
-25	1	0	0	1	1	0	0	1	-73	1	1	0	0	1	0	0	1
-26	1	0	0	1	1	0	1	0	-74	1	1	0	0	1	0	1	0
-27	1	0	0	1	1	0	1	1	-75	1	1	0	0	1	0	1	1
-28	1	0	0	1	1	1	0	0	-76	1	1	0	0	1	1	0	0
-29	1	0	0	1	1	1	0	1	-77	1	1	0	0	1	1	0	1
-30	1	0	0	1	1	1	1	0	-78	1	1	0	0	1	1	1	0
-31	1	0	0	1	1	1	1	1	-79	1	1	0	0	1	1	1	1
-32	1	0	1	0	0	0	0	0	-∞	1	1	1	1	1	1	1	1

Mixing Adjustable range is +7dB to -∞dB.

: Initial condition

(1) About Level Meter

(a) The Operation of Circuit
Level meter is a function which outputs a DC voltage proportional to the magnitude of the sound signal. It detects the peak level of the signal and retains that peak level, so that it is possible to monitor the magnitude of the signal by resetting the DC voltage within a suitable interval.

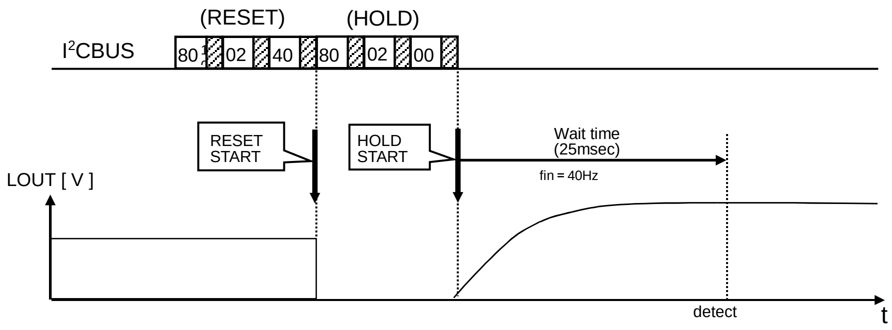
(b) The Way to Reset Level Meter Output
There are two kinds of methods of the reset.

① Please send reset data through the I^2C BUS.To reset output of level meter: Send D6 = “ 1 “ of select address 02(hex).
To cancel output reset of level meter (HOLD): Send D6 = “ 0 “ of select address 02(hex).

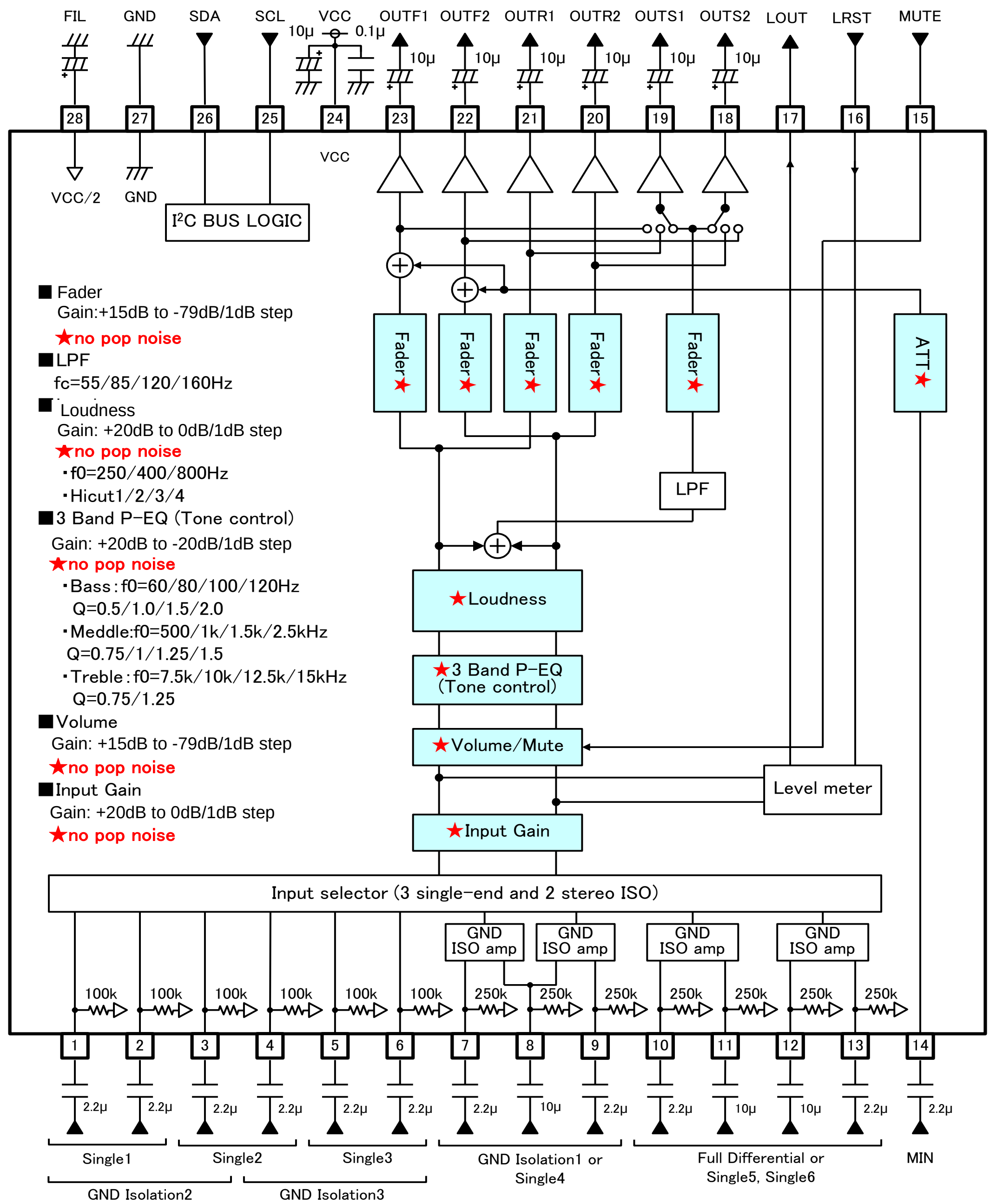
② Please control external terminal(LRST)
To reset output of level meter: LRST terminal set to HIGL level.
To cancel output reset of level meter (HOLD): LRST terminal set to LOW level.

(c) The Settings About Period of Reset
Peak hold operation will start after HOLD data is transmitted. Set the WAIT time after HOLD data transmission according to the frequency bandwidth detected.
WAIT time must be set to a minimum of one cycle over the detected frequency bandwidth.
Ex. Detected frequency bandwidth is above 40Hz, 『40Hz = 25ms = WAIT time』

Transmission Example by I^2C BUS



3. Application Circuit



(Note) About single input 1 to 3, it is possible to change from single input to GND Isolation input 2,3.

(Note) About GND Isolation1 and Full Differential, it is possible to change from differential input to single input 4 to 6.

Unit

R : [Ω]
C : [F]

Notes on wiring

①Please connect the decoupling capacitor of the power supply in the shortest possible distance to GND.
②GND lines should be one-point connected.
③Wiring pattern of the digital signals should be as far away as possible from those of the analog signals to prevent crosstalk.
④If possible, lines of SCL and SDA of I²C BUS should not be parallel.
The lines should be shielded, if they are adjacent to each other.
⑤If possible, analog input lines should not be parallel.
The lines should be shielded, if they are adjacent to each other.

Power Dissipation

About the thermal design of the IC

Characteristics of the IC are affected by the temperature at which it is used. Exceeding absolute maximum ratings may degrade and destroy the device. Careful consideration must be given to the heat of the IC from the two standpoints of immediate damage and long-term reliability of operation.

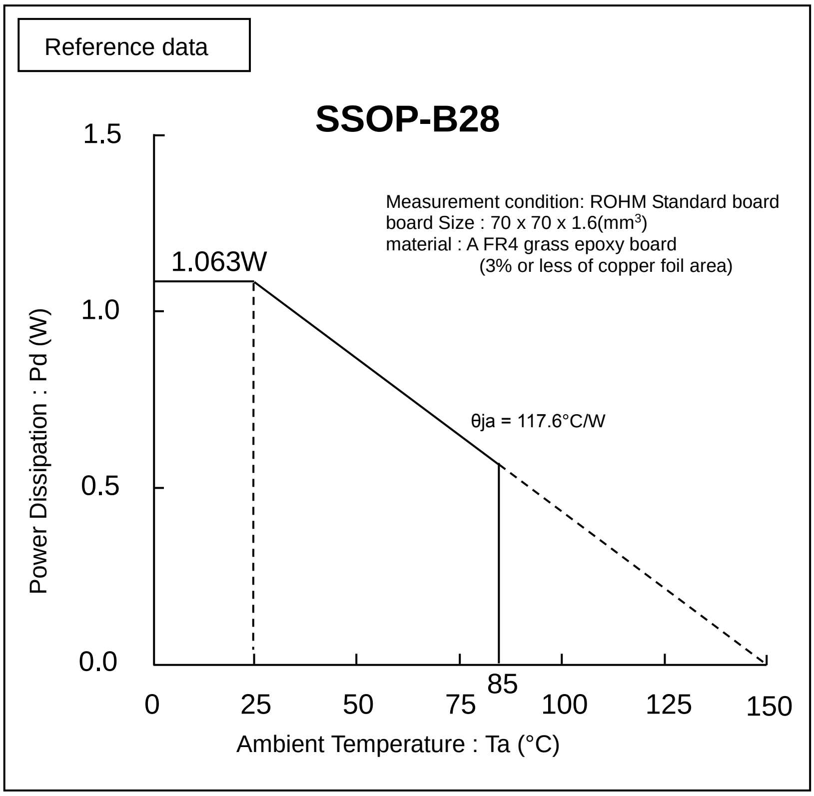
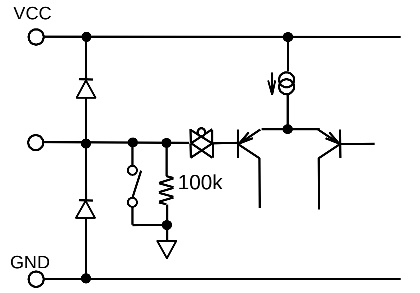
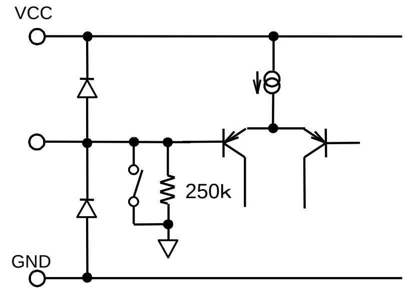
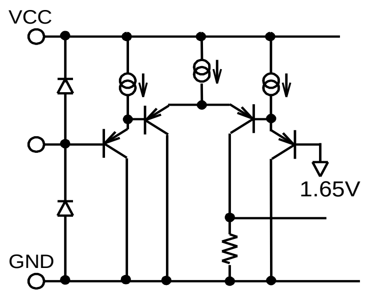
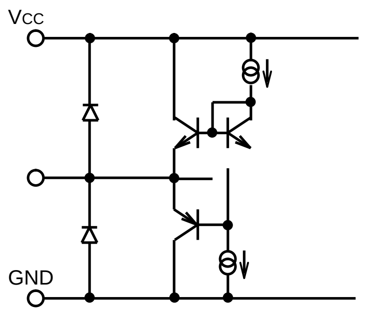
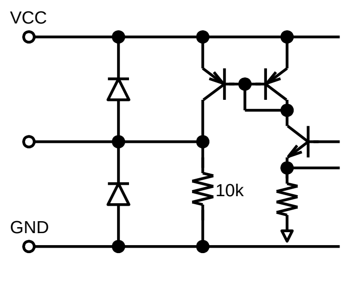


Figure 24. Temperature Derating Curve

(Note) Values are actual measurements and are not guaranteed.

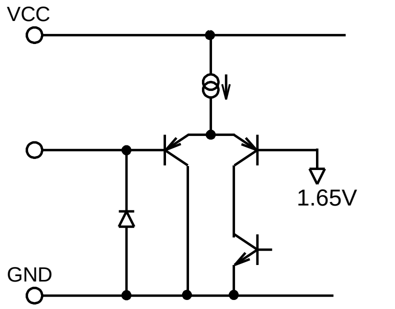
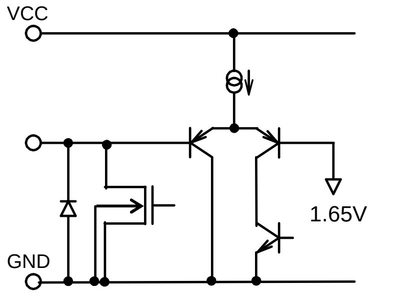
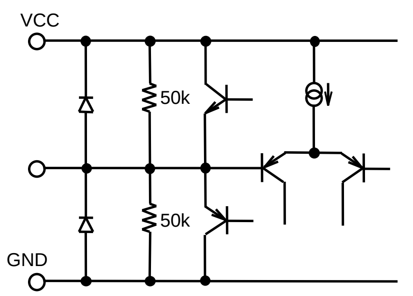
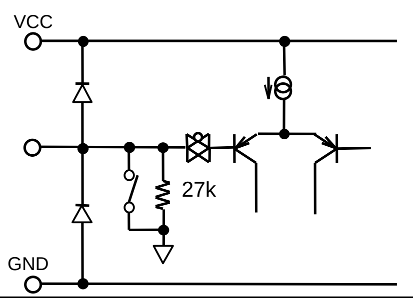
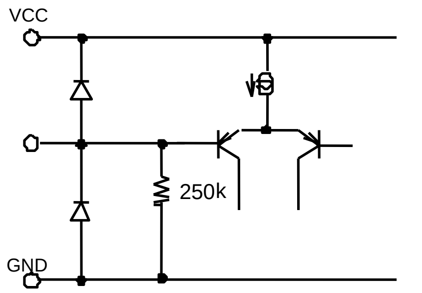
Power dissipation values vary according to the board on which the IC is mounted.

I/O Equivalent Circuits

Terminal No.	Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
1 2 3 4 5 6	A1 A2 B1 B2 C1 C2	4.25		A terminal for signal input. The input impedance is 100kΩ (Typ).
7 8 9 10 11 12 13	DP1 DN DP2 EP1 EN1 EN2 EP2	4.25		Input terminal available to Single/Differential mode. The input impedance is 250kΩ (Typ).
15	MUTE	-		A terminal for external compulsory mute. If terminal voltage is High level, the mute is OFF. And if the terminal voltage is Low level, the mute is ON.
18 19 20 21 22 23	OUTS2 OUTS1 OUTR2 OUTR1 OUTF2 OUTF1	4.25		A terminal for Fader and Subwoofer output.
17	LOUT	0 to 3.3		A terminal for level meter output Output impedance is 10kΩ (Typ).

Values in the pin explanation and input/output equivalent circuit are for reference purposes only. These are not guaranteed values.

I/O Equivalent Circuits – continued

Terminal No.	Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
24	VCC	8.5		Power supply terminal.
25	SCL	-		A terminal for clock input of I^2C BUS communication.
26	SDA	-		A terminal for data input of I^2C BUS communication.
27	GND	0		Ground terminal.
28	FIL	4.25		Voltage for reference bias of analog signal system. The simple precharge circuit and simple discharge circuit for an external capacitor are built in.
14	MIN	4.25		A terminal for signal input The input impedance is 27kΩ(Typ).
16	LRST	0		A terminal for signal input The input impedance is 250kΩ(Typ).

Values in the pin explanation and input/output equivalent circuit are for reference purposes only. These are not guaranteed values.

Operational Notes

1. **Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

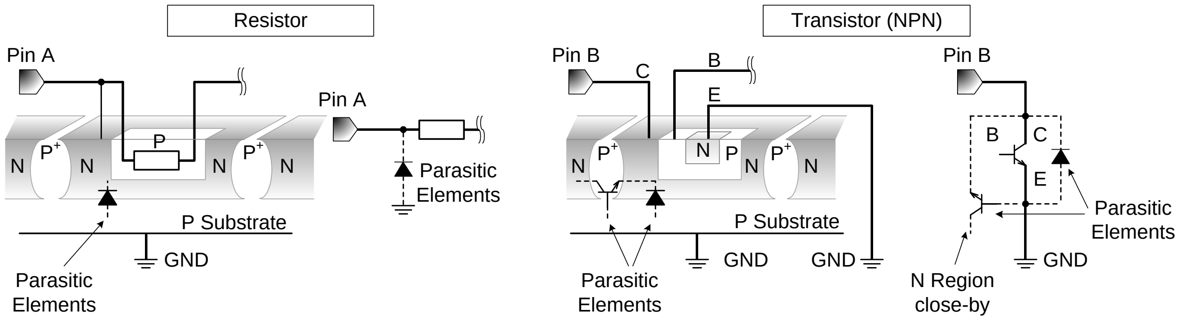
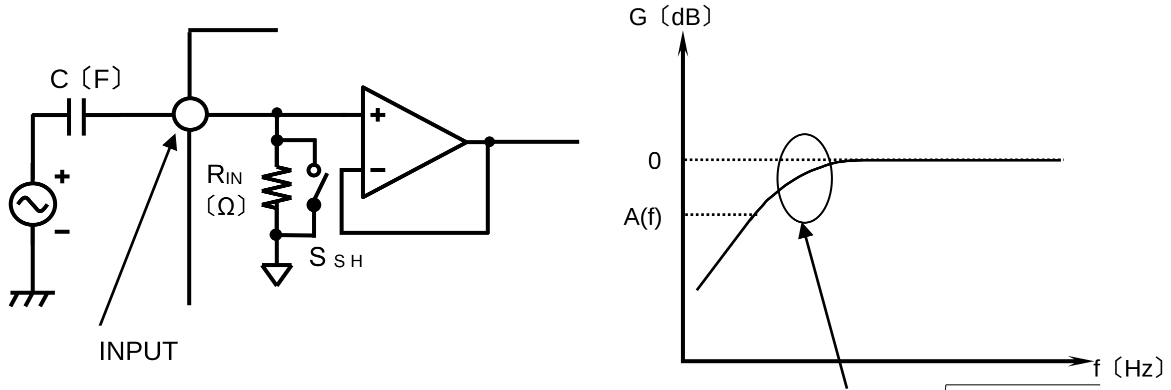


Figure 25. Example of monolithic IC structure

13. About a Signal Input Part

(a) About Input Coupling Capacitor Constant Value

The constant value of input coupling capacitor C(F) is decided with respect to the input impedance $R_{IN}(\Omega)$ at the input signal terminal of the IC that would be sufficient to form an RC characterized HPF.



$$A(f) = \sqrt{\frac{(2\pi fCR_{IN})^2}{1+(2\pi fCR_{IN})^2}}$$

(b) About the Input Selector SHORT

SHORT mode is the command which makes switch S_{SH} =ON of input selector part so that the input impedance R_{IN} of all terminals becomes small. Switch S_{SH} is OFF when SHORT command is not selected.

The constant time brought about by the small resistance inside and the capacitor outside the LSI becomes small when this command is used. The charge time of the capacitor becomes short. Since SHORT mode turns ON the switch of S_{SH} and makes it low impedance, please use it at no signal condition.

14. About Mute Terminal (Pin 15) when Power Supply is OFF

There should be no applied voltage to Mute terminal (Pin 15) when power-supply is OFF.
If in case voltage is supplied to MUTE terminal, please insert a series resistor (about 2.2kΩ) to Mute terminal.
(Please refer to Application Circuit Diagram.)

Operational Notes – continued

15. About Mixing

(a) About Specification of Fader -∞ at Mixing ON.
Mixed signal is added to the Main signal together with the Fader Gain (+15dB to -79dB) shown in the figure below. When Fader is set up in -∞, the signal after MIX is added with MUTE because the -∞ circuit of Fader is in the step after the addition circuit.

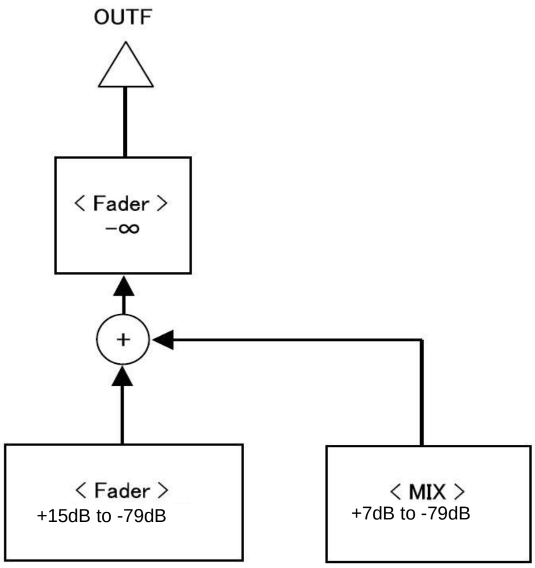
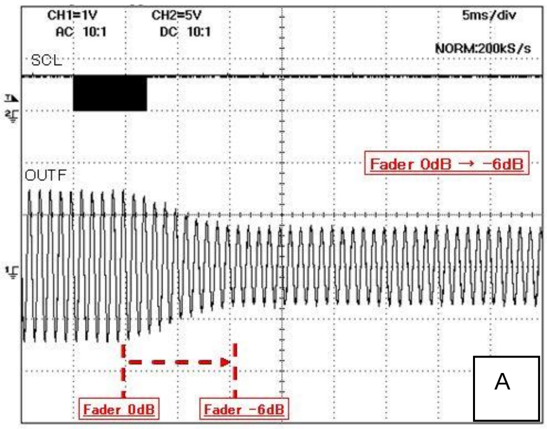
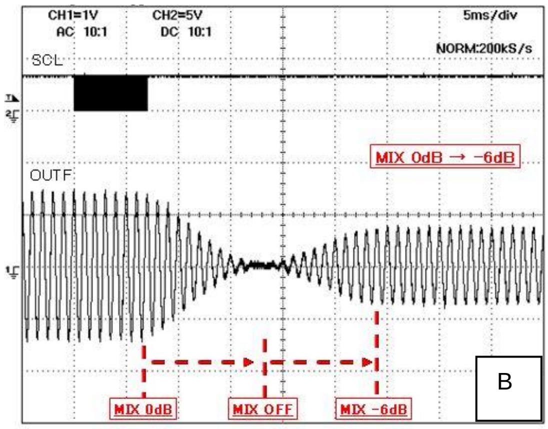


Figure 26. About Front Fader and Mixing

(b) About Advanced switching of Mixing Gain/ATT
When advanced switching of Mixing Gain/ATT works, Mixing becomes a switching movement that it passes through the state of Mixing OFF like what is shown in Figure B (from present setup of Mixing Gain/ATT to Mixing OFF to a target setup of Mixing Gain/ATT).



Fader Gain/ATT 0dB to -6dB Advanced Switching



Mixing Gain/ATT 0dB to -6dB Advanced Switching

Figure 27. Advanced Switching Movement when Mixing Gain/ATT is changed

Ordering Information

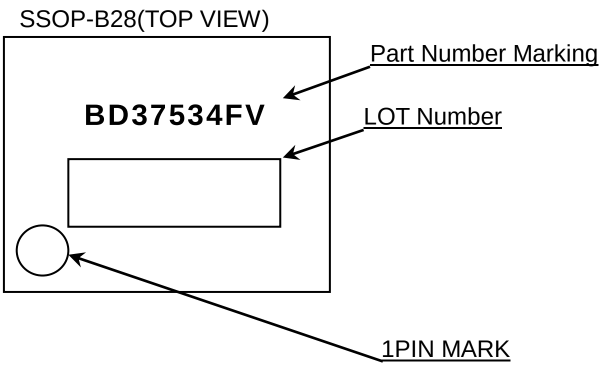
B D 3 7 5 3 4 F V - E 2

Part Number

Package
FV: SSOP-B28

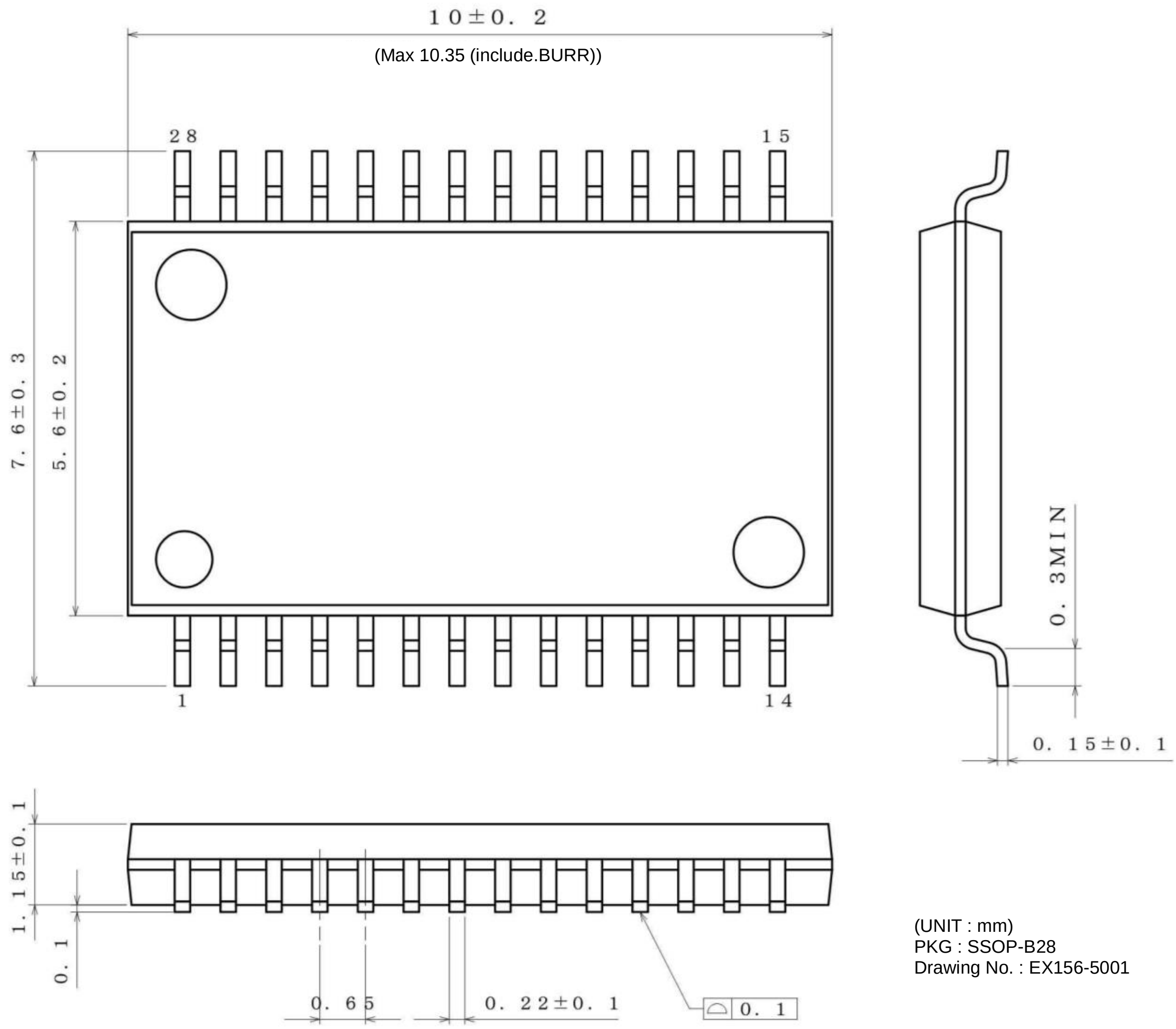
Packaging and forming specification
E2: Embossed tape and reel

Marking Diagram



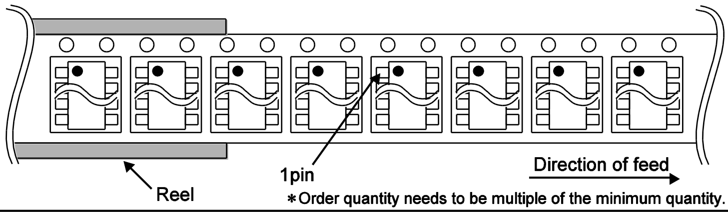
Physical Dimension, Tape and Reel Information

Package Name	SSOP-B28



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
16.Dec.2015	001	New Release

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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