

Automotive N-channel 600 V, 0.070 Ω typ., 36 A MDmesh™ DM6 Power MOSFET in an H²PAK-2 package

Datasheet - preliminary data

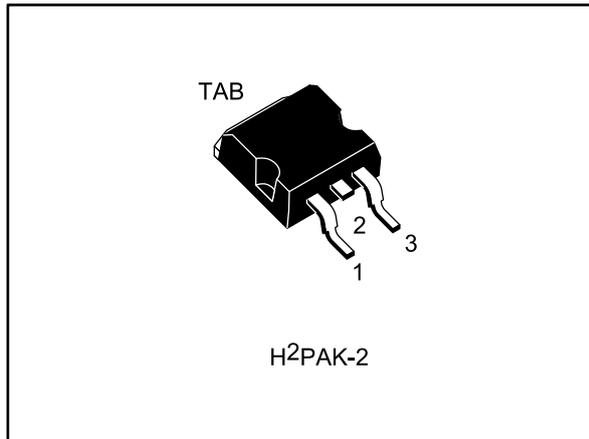
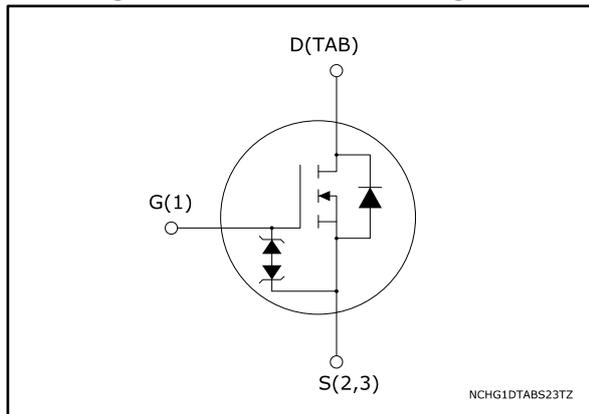


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STH47N60DM6-2AG	600 V	0.080 Ω	36 A

- Designed for automotive applications 
- Fast-recovery body diode
- Lower R_{DS(on)} x area vs previous generation
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely dv/dt ruggedness
- Zener-protected
- Excellent switching performance thanks to the extra driving source pin

Applications

- Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM6 fast recovery diode series. Compared with the previous MDmesh fast generation, DM6 combines very low recovery charge (Q_{rr}), recovery time (t_{rr}) and excellent improvement in R_{DS(on)} * area with one of the most effective switching behaviors available in the market for the most demanding high efficiency bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STH47N60DM6-2AG	47N60DM6	H ² PAK-2	Tape and reel

Contents

- 1 Electrical ratings 3**
- 2 Electrical characteristics 4**
 - 2.1 Electrical characteristics (curves)..... 6
- 3 Test circuits 8**
- 4 Package information 9**
 - 4.1 H²PAK-2 package information..... 10
 - 4.2 H²PAK-2 packing information..... 12
- 5 Revision history 14**



1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate-source voltage	±25	V
I _D	Drain current (continuous) at T _C = 25 °C	36	A
I _D	Drain current (continuous) at T _C = 100 °C	22	A
I _D ⁽¹⁾	Drain current (pulsed)	137	A
P _{TOT}	Total dissipation at T _C = 25 °C	250	W
dv/dt ⁽²⁾	Peak diode recovery voltage slope	50	V/ns
dv/dt ⁽³⁾	MOSFET dv/dt ruggedness	100	
T _J	Operating junction temperature range	-55 to 150	°C
T _{stg}	Storage temperature range		

Notes:

⁽¹⁾Pulse width limited by safe operating area

⁽²⁾I_{SD} ≤ 36 A, di/dt ≤ 800 A/μs, V_{DS peak} < V_{(BR)DSS}, V_{DD} = 480 V

⁽³⁾V_{DS} ≤ 480 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	0.5	°C/W
R _{thj-pcb}	Thermal resistance junction-pcb ⁽¹⁾	30	

Notes:

⁽¹⁾When mounted on 1 inch² FR-4, 2 Oz copper board.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T _{jmax})	7	A
E _{AS}	Single pulse avalanche energy (starting T _j = 25°C, I _D = I _{AR} , V _{DD} = 100 V)	700	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			5	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}^{(1)}$			100	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 5	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 18\text{ A}$		0.070	0.080	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	2350	-	pF
C_{oss}	Output capacitance		-	160	-	pF
C_{riss}	Reverse transfer capacitance		-	2	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$, $V_{GS} = 0\text{ V}$	-	416	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	1.6	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 36\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14: "Test circuit for gate charge behavior")	-	55	-	nC
Q_{gs}	Gate-source charge		-	12	-	nC
Q_{gd}	Gate-drain charge		-	31	-	nC

Notes:

⁽¹⁾ $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 18\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	23	-	ns
t_r	Rise time		-	5.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	57	-	ns
t_f	Fall time		-	9	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		36	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		137	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 36 \text{ A}, V_{GS} = 0 \text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 36 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}, V_{DD} = 60 \text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	115		ns
Q_{rr}	Reverse recovery charge		-	0.54		μC
I_{RRM}	Reverse recovery current		-	9.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 36 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}, V_{DD} = 60 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	210		ns
Q_{rr}	Reverse recovery charge		-	2.1		μC
I_{RRM}	Reverse recovery current		-	20.4		A

Notes:

(1)Pulse width limited by safe operating area

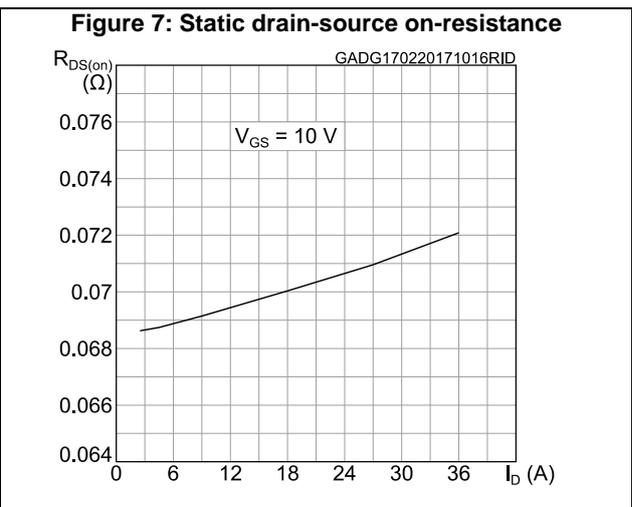
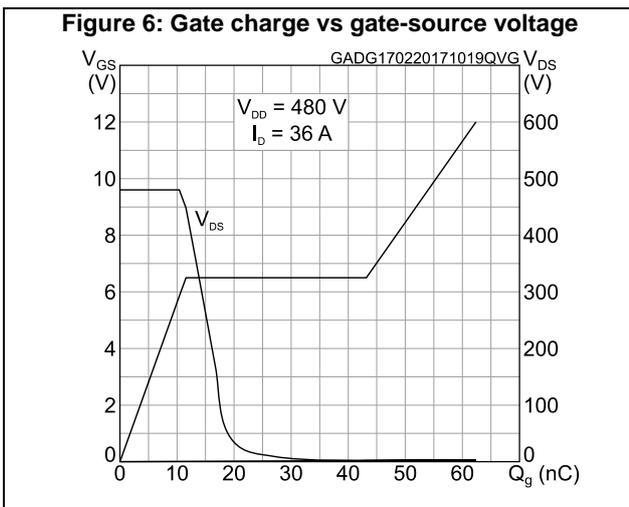
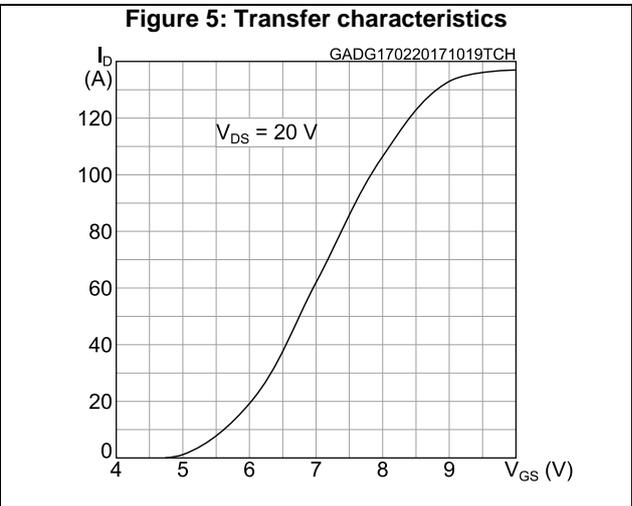
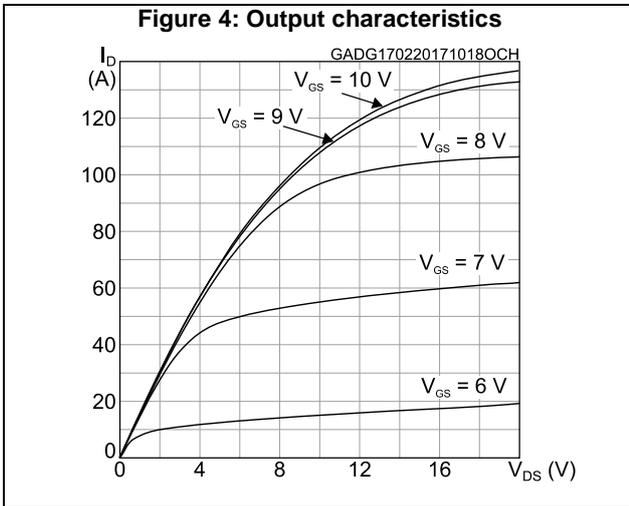
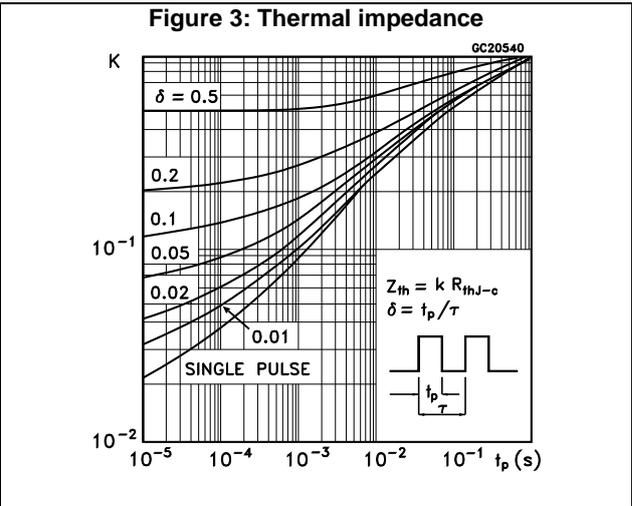
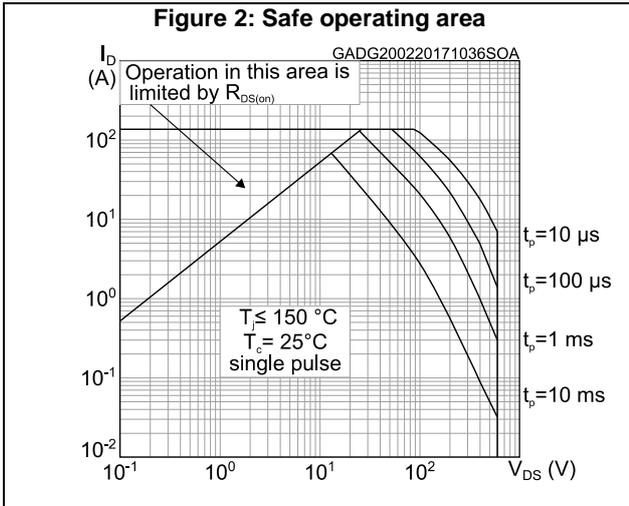
(2)Pulsed: pulse duration = 300 μs , duty cycle 1.5%

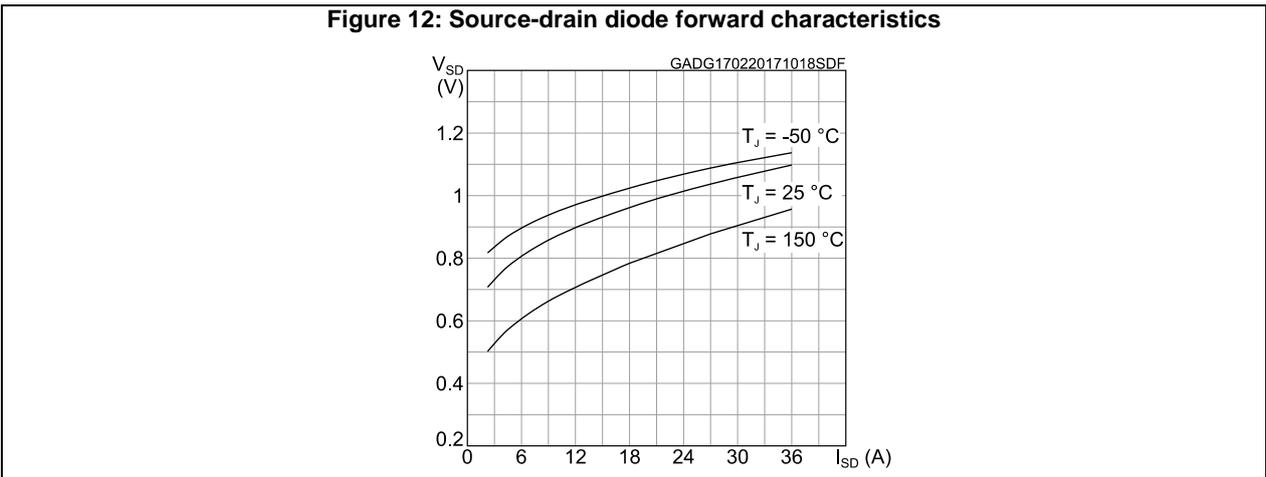
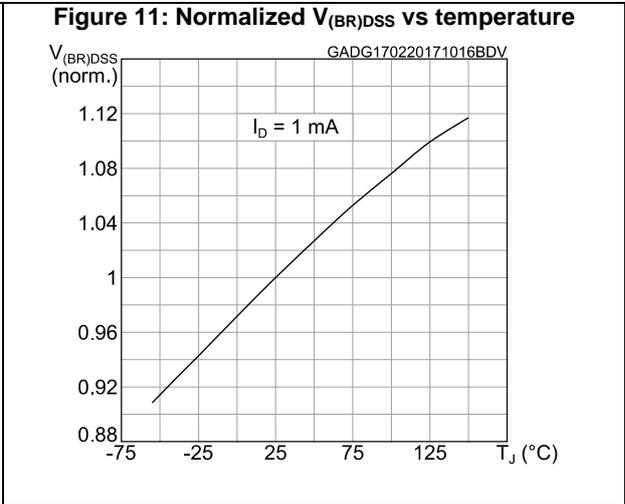
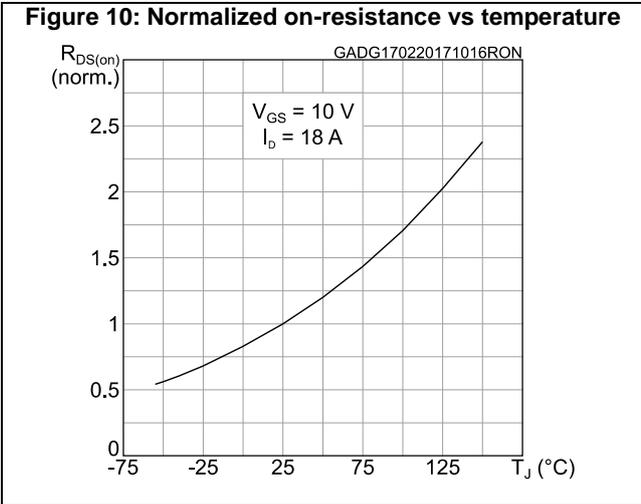
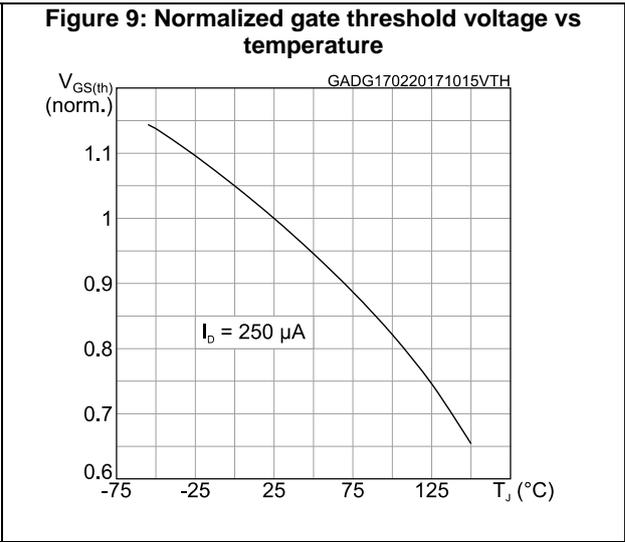
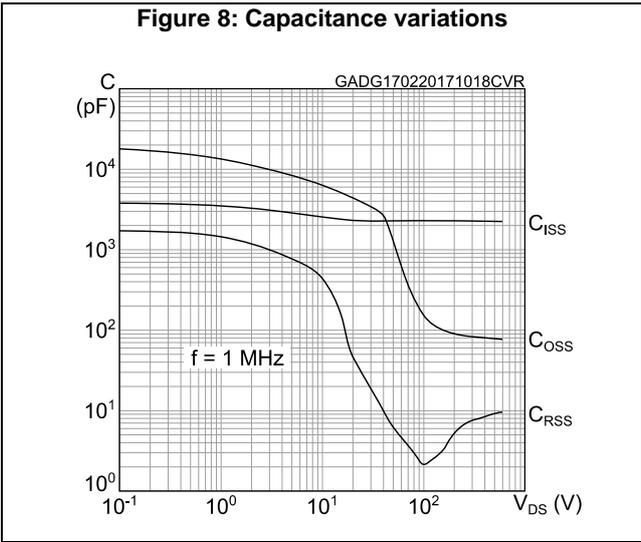
Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}, I_D = 0 \text{ A}$	± 30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

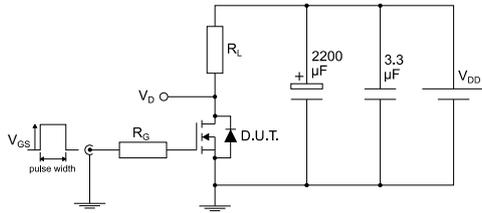
2.1 Electrical characteristics (curves)





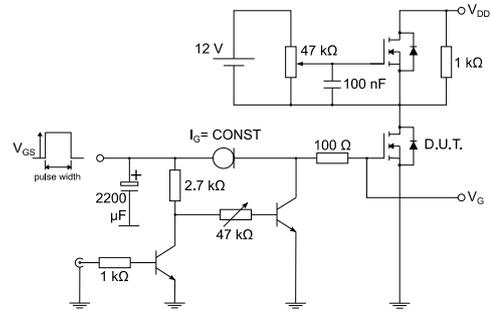
3 Test circuits

Figure 13: Test circuit for resistive load switching times



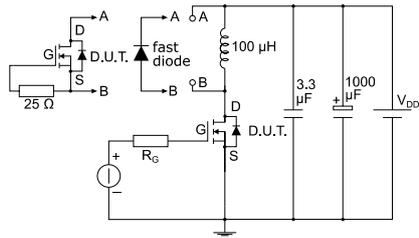
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Figure 14: Test circuit for gate charge behavior



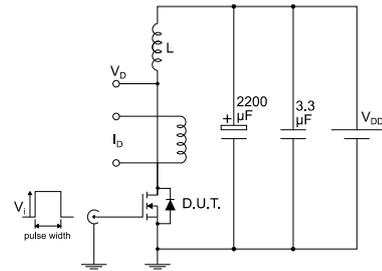
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Figure 15: Test circuit for inductive load switching and diode recovery times



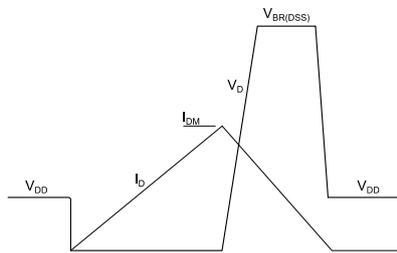
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Figure 16: Unclamped inductive load test circuit



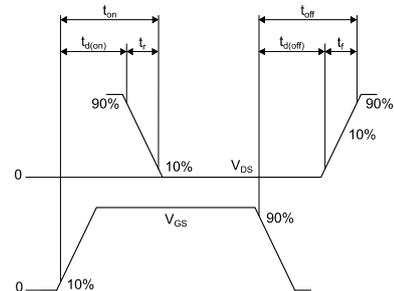
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Figure 17: Unclamped inductive waveform



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Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 H²PAK-2 package information

Figure 19: H²PAK-2 package outline

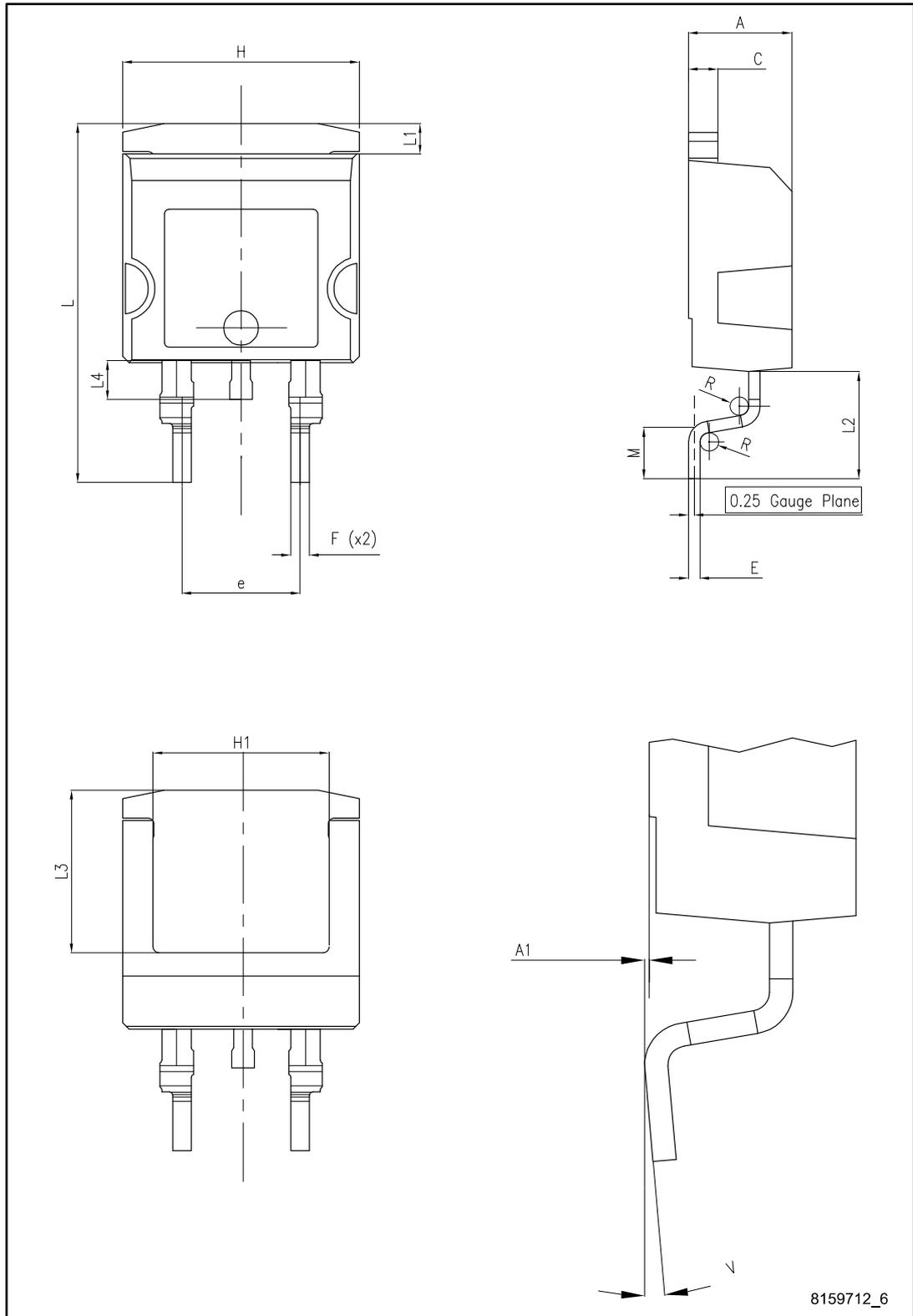
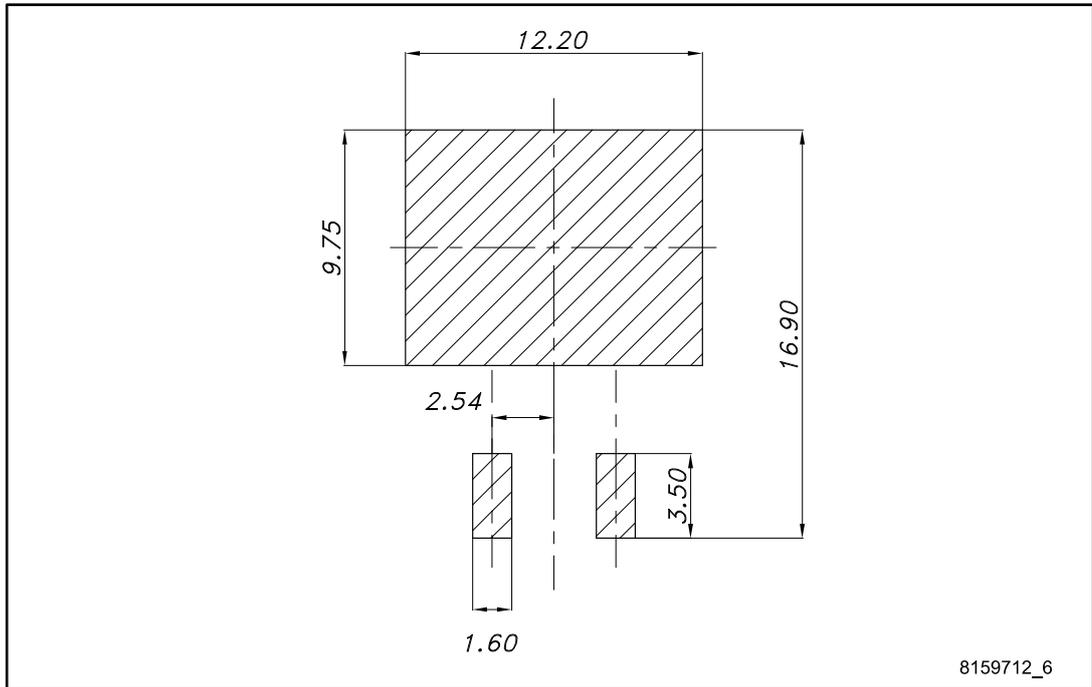


Table 10: H²PAK-2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.70
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 20: H²PAK-2 recommended footprint



4.2 H²PAK-2 packing information

Figure 21: Tape outline

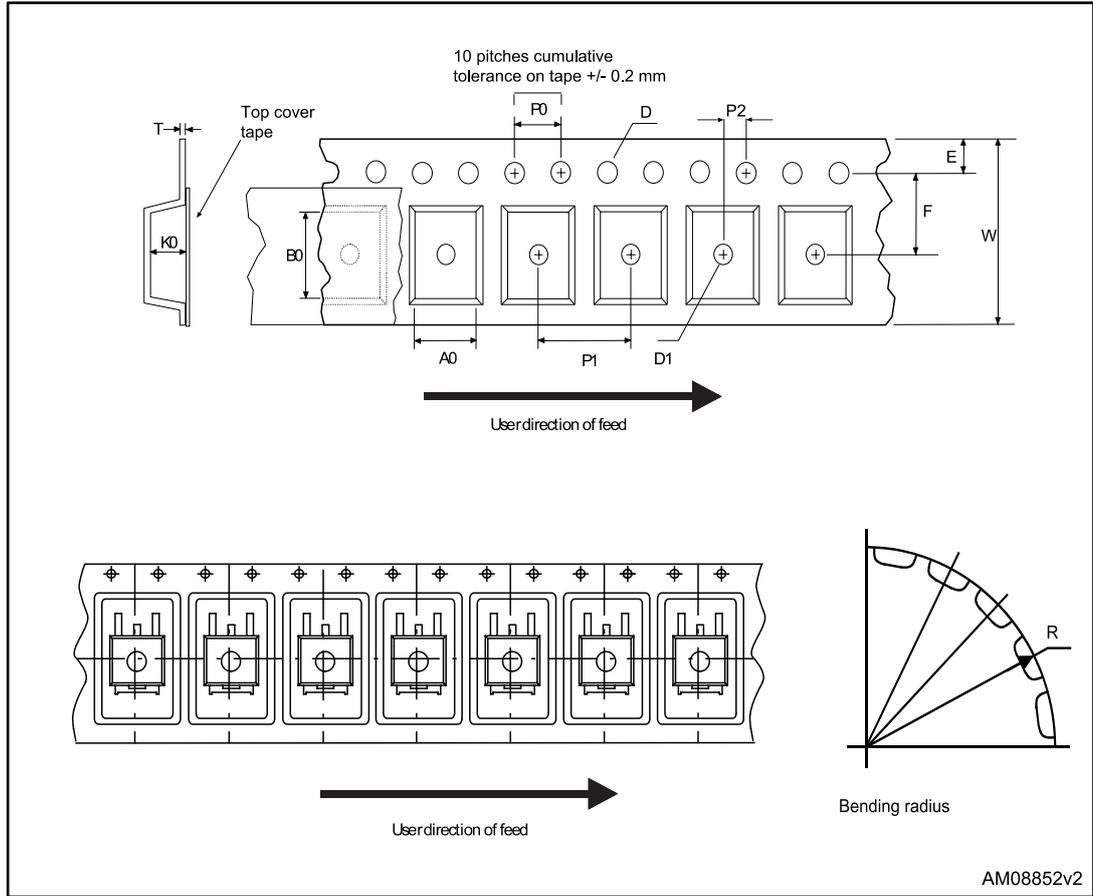


Figure 22: Reel outline

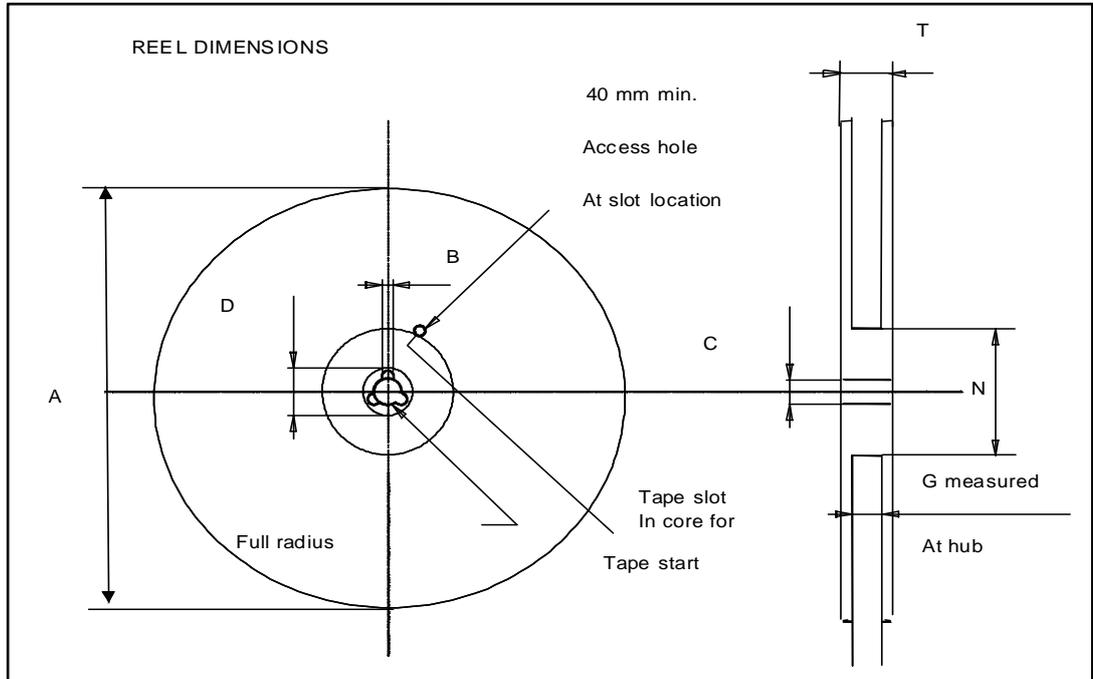


Table 11: Tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

5 Revision history

Table 12: Document revision history

Date	Revision	Changes
09-Aug-2017	1	Initial release

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