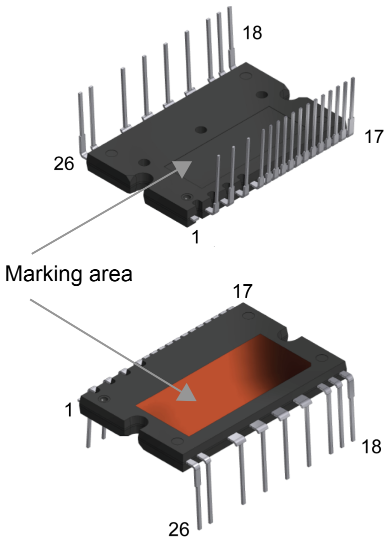
STIB1060DM2T-L

Datasheet

SLLIMM™ - 2nd series IPM, 3-phase inverter, 0.18 Ω typ., 10 A, 600 V Power MOSFET



SDIP2B-26L type L

Product status link
STIB1060DM2T-L

Product summary	
Order code	STIB1060DM2T-L
Marking	IB1060DM2T-L
Package	SDIP2B-26L type L
Packing	Tube

Features

- IPM 10 A, 600 V, 3-phase MOSFET inverter bridge including 2 control ICs for gate driving
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Internal bootstrap diode
- Undervoltage lockout of gate drivers
- Smart shutdown function
- Short-circuit protection
- Shutdown input/fault output
- Separate open-source outputs
- Built-in temperature sensor
- Comparator for fault protection
- Fast, soft recovery diodes
- 85 kΩ NTC, UL 1434, CA 4 recognized
- Fully isolated package
- Isolation rating of 1500 Vrms/min

Applications

- 3-phase inverters for motor drives
- Linear and BLDC compressor
- Aircon

Description

This new IPM, belonging to the second series of SLLIMM (small low-loss intelligent molded module), provides a compact, high-performance AC motor drive in a simple, rugged design.

It combines new ST proprietary control ICs with the high-voltage N-channel super-junction MDMesh™ DM2, providing fast-recovery diode series to increase efficiency and minimize EMI and overall losses, making it ideal for any high-efficiency converter and 3-phase inverter system. SLLIMM™ is a trademark of STMicroelectronics.

1 Internal schematic and pin description

Figure 1. **Internal schematic diagram and pin configuration**

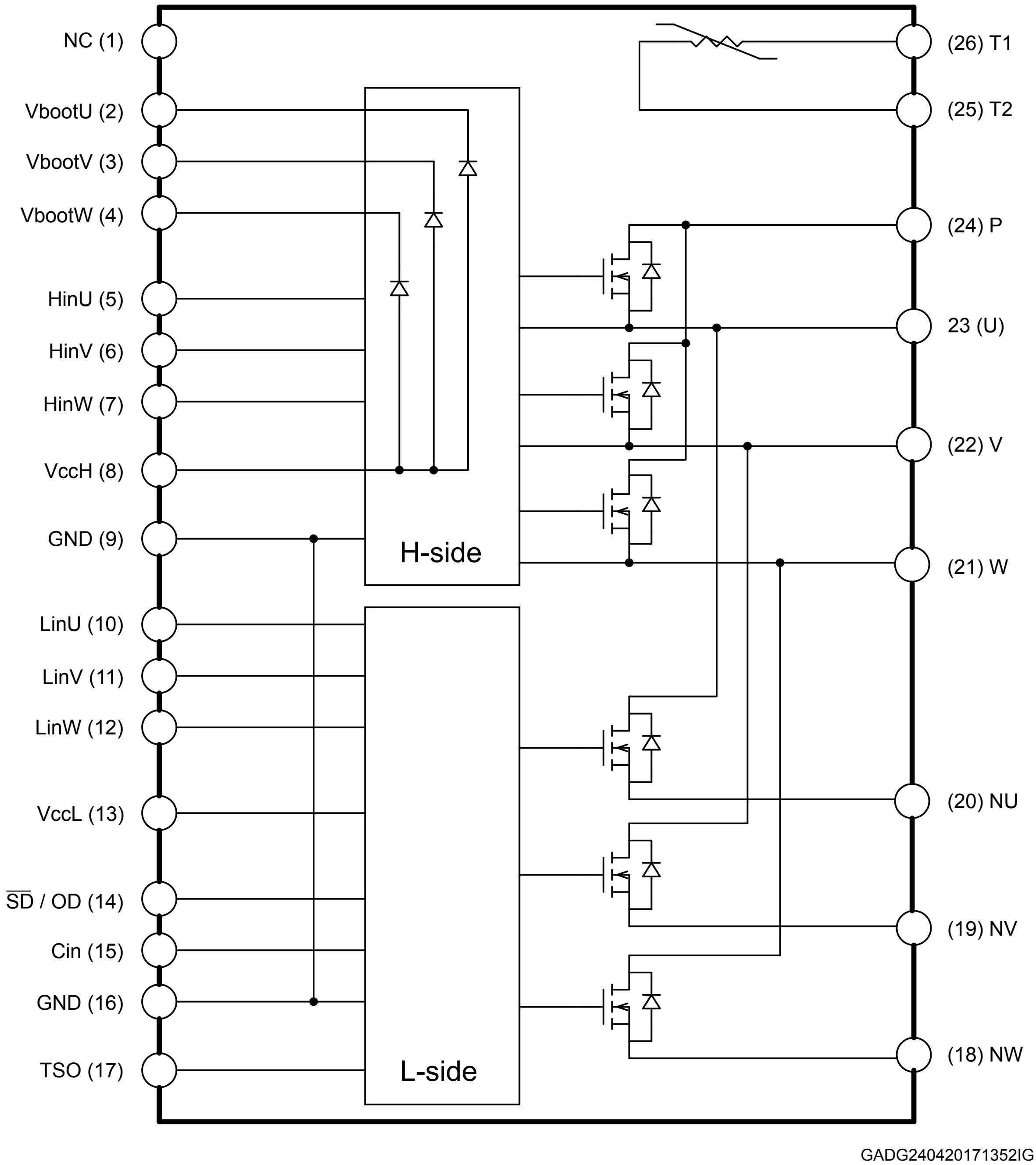


Table 1. Pin description

Pin	Symbol	Description
1	NC	-
2	VBOOTu	Bootstrap voltage for U phase
3	VBOOTv	Bootstrap voltage for V phase
4	VBOOTw	Bootstrap voltage for W phase
5	HINu	High-side logic input for U phase
6	HINv	High-side logic input for V phase
7	HINw	High-side logic input for W phase
8	VCCH	High-side low voltage power supply
9	GND	Ground
10	LINu	Low-side logic input for U phase
11	LINv	Low-side logic input for V phase
12	LINw	Low-side logic input for W phase
13	VCCL	Low-side low voltage power supply
14	$\overline{SD}$ /OD	Shutdown logic input (active low) / open-drain (comparator output)
15	CIN	Comparator input
16	GND	Ground
17	TSO	Temperature sensor output
18	NW	Negative DC input for W phase
19	NV	Negative DC input for V phase
20	NU	Negative DC input for U phase
21	W	W phase output
22	V	V phase output
23	U	U phase output
24	P	Positive DC input
25	T2	NTC thermistor terminal 2
26	T1	NTC thermistor terminal 1

2 Absolute maximum ratings

T_J = 25 °C unless otherwise noted.

Table 2. Inverter part

Symbol	Parameter	Value	Unit
V_{PN}	Supply voltage between P -N_U, -N_V, -N_W	450	V
$V_{PN(surge)}$	Supply voltage surge among P -N_U, -N_V, -N_W	500	V
V_{DSS}	MOSFET blocking voltage (or drain-source voltage) for each MOSFET (V_{IN} [(1)] = 0)	600	V
± I_D	Drain current (continuous) at T_C = 25 °C	12.5	A
± I_{DP}	Peak drain current each MOSFET (less than 1 ms)	50	A
P_{TOT}	Total dissipation at T_C=25 °C each MOSFET	78	W
t_{scw}	Short circuit withstand time, V_{DS} = 300 V, T_J = 125 °C, V_{CC} = V_{boot} = 15 V, V_{IN} = 0 to 5 V	12	µs

1. *Applied among HINx, LINx and GND for x = U, V, W*

Table 3. Control part

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage between V_{CCH}-GND, V_{CCL}-GND	- 0.3	20	V
V_{BOOT}	Bootstrap voltage	- 0.3	619	V
V_{OUT}	Output voltage among U, V, W and GND	V_{BOOT} - 21	V_{BOOT} + 0.3	V
V_{CIN}	Comparator input voltage	- 0.3	20	V
V_{IN}	Logic input voltage applied among HINx, LINx and GND	- 0.3	15	V
$V_{\overline{SD}/OD}$	Open-drain voltage	-0.3	7	V
$I_{\overline{SD}/OD}$	Open-drain sink current		10	mA
V_{TSO}	Temperature sensor output voltage	-0.3	5.5	V
I_{TSO}	Temperature sensor output current		7	mA

Table 4. Total system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, t = 60 s.)	1500	Vrms
T_J	Power chips operating junction temperature range	-40 to 150	°C
T_C	Module operation case temperature range	-40 to 125	°C

2.1 Thermal data

Table 5. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Thermal resistance junction-case single MOSFET	1.59	°C/W

3 Electrical characteristics

T_J = 25 °C unless otherwise noted.

3.1 Inverter part

Table 6. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Zero gate voltage drain current	V_{DS} = 600 V, V_{CC} = V_{boot} = 15 V			100	µA
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{CC} = V_{boot} = 15 V, V_{IN}[(1)] = 0 V, I_D = 1 mA	600			V
$R_{DS(on)}$	Static drain-source turn-on resistance	V_{CC} = V_{boot} = 15 V, V_{IN}[(1)] = 0 to 5 V, I_D = 1.0 A		0.168		Ω
		V_{CC} = V_{boot} = 15 V, V_{IN}[(1)] = 0 to 5 V, I_D = 10 A		0.180	0.210	
V_{SD}	Drain-source diode forward voltage	V_{IN}[(1)] = 0 V, I_D = 10 A		0.98	1.36	V

1. *Applied among HINx, LINx and GND for x = U, V, W.*

Table 7. Inductive load switching time and energy

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{on}[(1)]	Turn-on time	V_{DD} = 300 V, V_{CC} = V_{boot} = 15 V, V_{IN}[(2)] = 0 to 5 V, I_D = 10 A	-	560	-	ns
$t_{c(on)}$[(1)]	Cross-over time on		-	160	-	
t_{off}[(1)]	Turn-off time		-	1040	-	
$t_{c(off)}$[(1)]	Cross-over time off		-	70	-	
t_{rr}	Reverse recovery time		-	155	-	
E_{on}	Turn-on switching energy		-	465	-	µJ
E_{off}	Turn-off switching energy		-	70	-	
E_{rr}	Reverse recovery energy		-	23	-	

1. *t_{on} and t_{off} include the propagation delay times of the internal drive. $t_{C(on)}$ and $t_{C(off)}$ are the switching times of the MOSFET itself under the internally given gate driving condition.*
2. *Applied among HINx, LINx and GND for x = U, V, W.*

Figure 2. Switching time test circuit

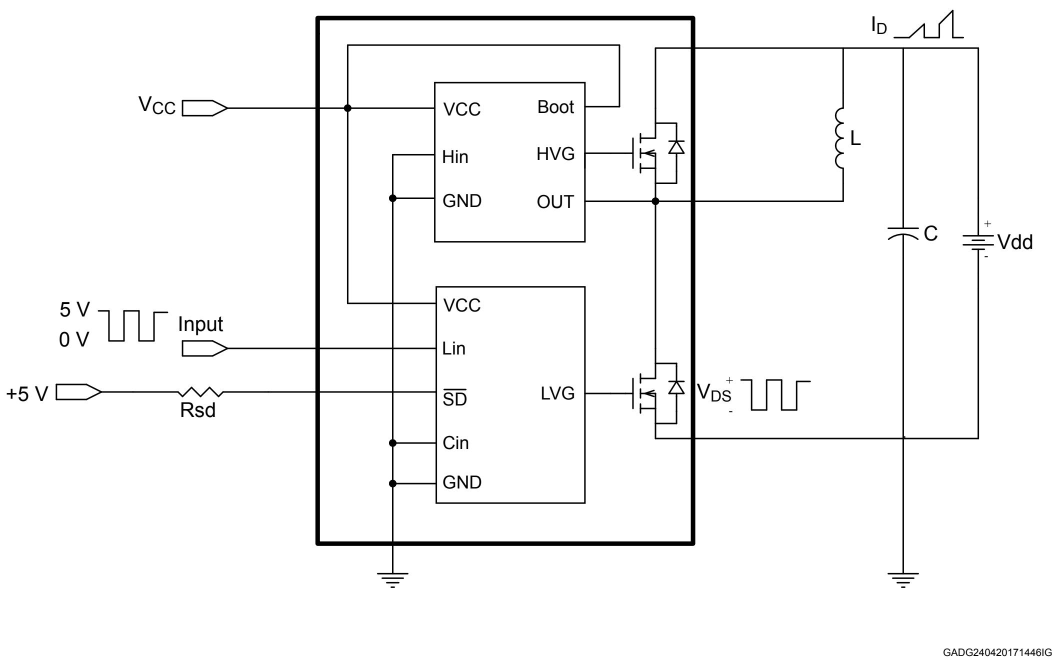
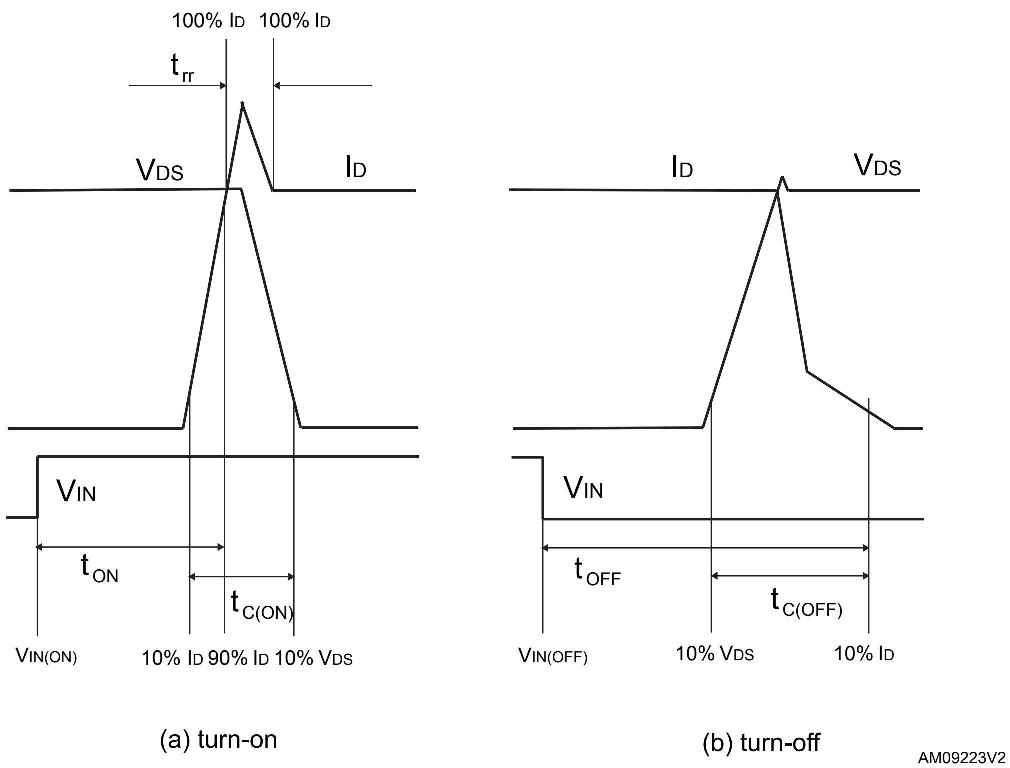


Figure 3. Switching time definition



3.2 Control/protection parts

Table 8. High- and low-side drivers

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{il}	Low logic level voltage				0.8	V
V_{ih}	High logic level voltage		2			V
I_{INh}	IN logic “1” input bias current	IN_x = 15 V	80	150	200	µA
I_{INl}	IN logic “0” input bias current	IN_x = 0 V			1	µA
High-side						
V_{CC_hys}	V_{CC} UV hysteresis		1.2	1.4	1.7	V
$V_{CCH\_th(on)}$	V_{CCH} UV turn-on threshold		11	11.5	12	V
$V_{CCH\_th(off)}$	V_{CCH} UV turn-off threshold		9.6	10.1	10.6	V
V_{BS_hys}	V_{BS} UV hysteresis		0.5	1	1.6	V
$V_{BS\_th(on)}$	V_{BS} UV turn-on threshold		10.1	11	11.9	V
$V_{BS\_th(off)}$	V_{BS} UV turn-off threshold		9.1	10	10.9	V
I_{QBSU}	Under voltage V_{BS} quiescent current	V_{BS} = 9 V, HINx(1) = 5 V		55	75	µA
I_{QBS}	V_{BS} quiescent current	V_{CC} = 15 V, HINx(1) = 5 V		125	170	µA
I_{qccu}	Under voltage quiescent supply current	V_{CC} = 9 V, HINx(1) = 0 V		190	250	µA
I_{qcc}	Quiescent current	V_{CC} = 15 V, HINx(1) = 0 V		560	730	µA
$R_{DS(on)}$	BS driver ON resistance			150		Ω
Low-side						
V_{CC_hys}	V_{CC} UV hysteresis		1.1	1.4	1.6	V
$V_{CCL\_th(on)}$	V_{CCL} UV turn-on threshold		10.4	11.6	12.4	V
$V_{CCL\_th(off)}$	V_{CCL} UV turn-off threshold		9.0	10.3	11	V
I_{qccu}	Under voltage quiescent supply current	V_{CC} = 10 V, $\overline{SD}$ pulled to 5 V through R_{SD} = 10 kΩ, CIN = LINx(1) = 0		600	800	µA
I_{qcc}	Quiescent current	V_{CC} = 15 V, $\overline{SD}$= 5 V, CIN = LINx(1) = 0		700	900	µA
V_{SSD}	Smart $\overline{SD}$ unlatch threshold		0.5	0.6	0.75	V
I_{SDh}	$\overline{SD}$ logic “1” input bias current	$\overline{SD}$ = 5 V	25	50	70	µA
I_{SDl}	$\overline{SD}$ logic “0” input bias current	$\overline{SD}$ = 0 V			1	µA

1. *Applied among HINx, LINx and GND for x = U, V, W*

Table 9. Temperature sensor output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{TSO}	Temperature sensor output voltage	T_J = 25 °C	0.974	1.16	1.345	V
I_{TSO_SNK}	Temperature sensor sink current capability			0.1		mA
I_{TSO_SRC}	Temperature sensor source current capability		4			mA

Table 10. **Sense comparator (V_{CC} = 15 V, unless otherwise is specified)**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{CIN}	CIN input bias current	V_{CIN} =1 V	-0.2		0.2	µA
V_{ref}	Internal reference voltage		460	510	560	mV
V_{OD}	Open-drain low level output voltage	I_{od} = 5 mA			500	mV
t_{CIN_SD}	C_{IN} comparator delay to $\overline{SD}$	$\overline{SD}$ pulled to 5 V through R_{SD}= 10 kΩ; measured applying a voltage step 0-1 V to pin CIN; 50 % CIN to 90 % $\overline{SD}$	240	320	410	ns
SR_{SD}	$\overline{SD}$ fall slew rate	$\overline{SD}$ pulled to 5 V through R_{SD}= 10 kΩ; C_L= 1 nF through $\overline{SD}$ and ground; 90 % $\overline{SD}$ to 10 % $\overline{SD}$		25		V/µs

The comparator stays enabled even if V_{CC} is in the UVLO condition but higher than 4 V.

4 Fault management

The device integrates an open-drain output connected to the $\overline{SD}$ pin. As soon as a fault occurs, the open-drain is activated and the LVGx outputs are forced low. Two types of fault can be identified:

- Overcurrent (OC) sensed by the internal comparator (see more detail in Section 4.1 Smart shutdown function);
- Undervoltage on supply voltage (V_{CC})

Each fault enables the SD open drain for a different time, as described in the following table.

Table 11. Fault timing

Symbol	Parameter	Event time [1]	SD open-drain enable time result [1][2]
OC	Over-current event	≤ 24 µs	24 µs
		> 24 µs	OC time
UVLO	Under-voltage lockout event	≤ 70 µs	70 µs
		> 70 µs until the VCC_LS exceeds the VCC_LS UV turn ON threshold	UVLO time

1. *Typical value (-40 °C ≤ T_J ≤ +125 °C)*
2. *Without contribution of the RC network on SD*

Actually, the device remains in a fault condition ($\overline{SD}$ at low logic level and LVGx outputs disabled) for a time also depending on the RC network connected to the $\overline{SD}$ pin. The network generates a time contribution that is added to the internal value.

Figure 4. Overcurrent timing (without contribution of the RC network on $\overline{SD}$)

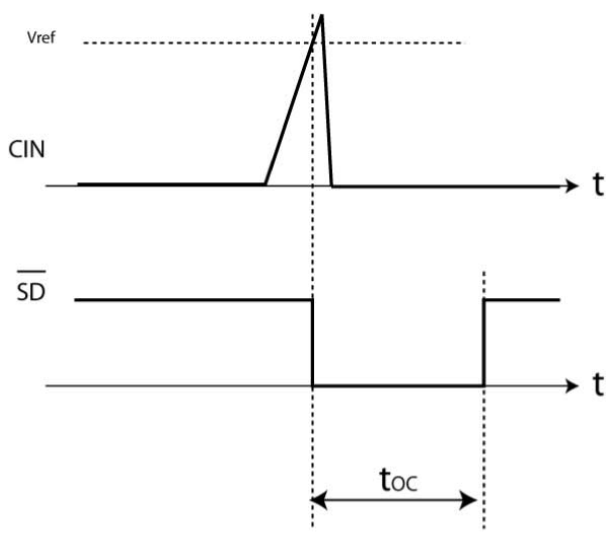


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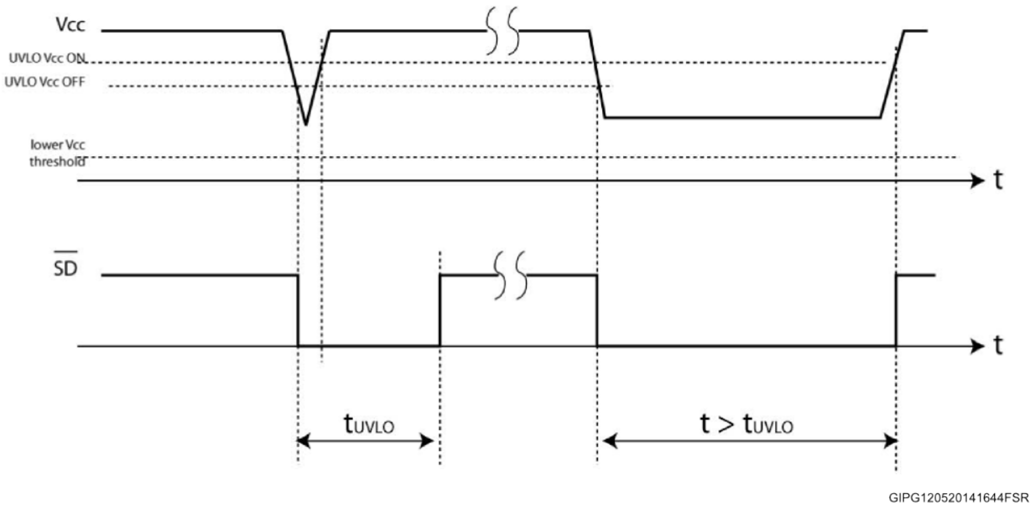
Figure 5. UVLO timing (without contribution of the RC network on $\overline{SD}$)

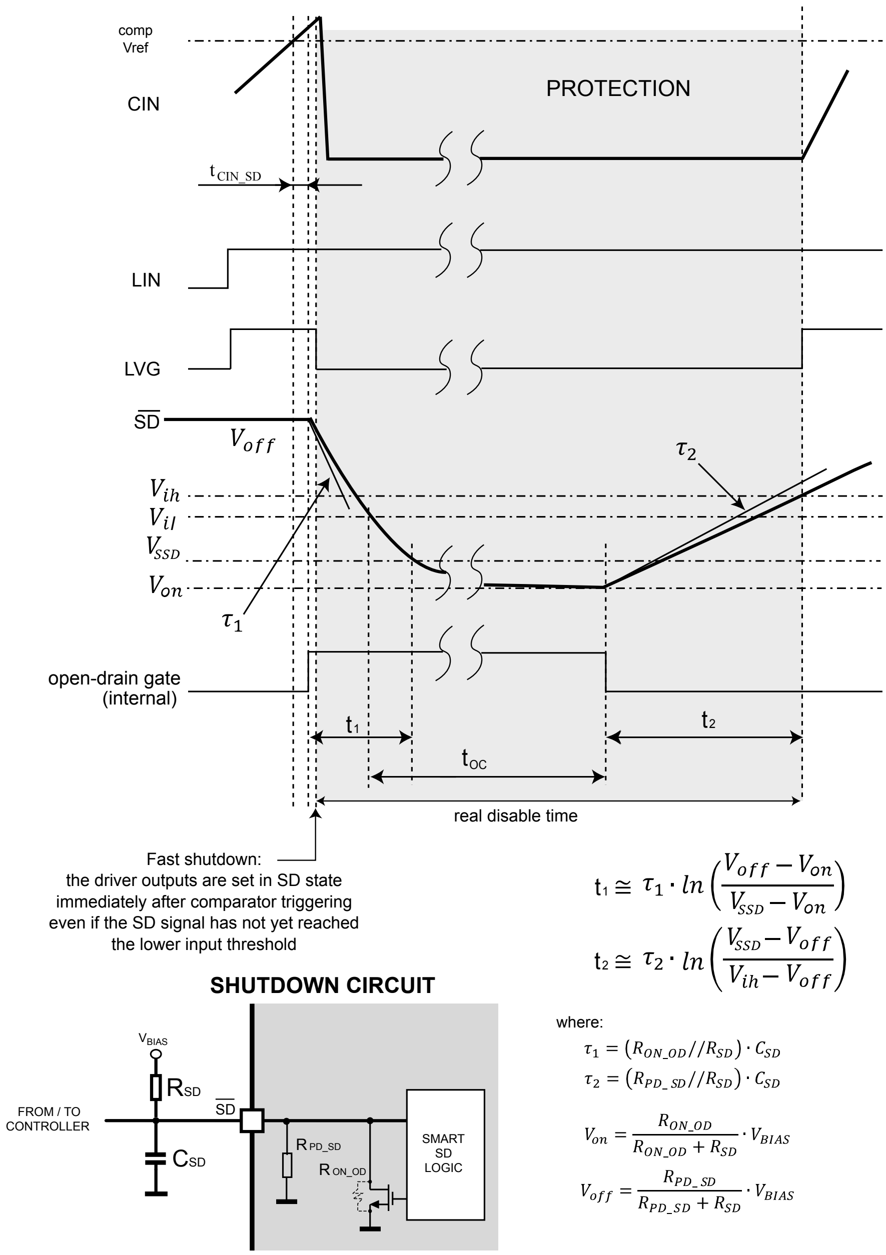


4.1 Smart shutdown function

The device integrates a comparator committed to the fault sensing function. The comparator input can be connected to an external shunt resistor in order to implement a simple overcurrent detection function.

The output signal of the comparator is fed to an integrated MOSFET with the open drain output available on the $\overline{SD}$ input. When the comparator triggers, the device is set in shutdown state and its outputs are all set to low level.

Figure 6. Smart shutdown timing waveforms in case of overcurrent event



$R_{ON\_OD} = V_{OD}/5$ mA, see Table 10. Sense comparator (V_{CC} = 15 V, unless otherwise is specified);

R_{PD_SD} (typ.) = 5 V/I_{SDh}

In common overcurrent protection designs, the comparator output is usually connected to the $\overline{SD}$ input and an RC network is connected to this $\overline{SD}$ line in order to provide a mono-stable circuit which implements a protection time that follows the fault condition.

As opposed to common fault detection systems, the device smart shutdown architecture allows the immediate turn-off of output gates driver in case of fault, by minimizing the propagation delay between the fault detection event and the actual switching off of the outputs. In fact, the time delay between the fault and the turning off of the outputs is no longer dependent on the RC value of the external network connected to the pin.

In the smart shutdown circuitry, the fault signal has a preferential path which directly switches off the outputs after the comparator triggering.

At the same time, the internal logic turns on the open-drain output and holds it on until the $\overline{SD}$ voltage goes below the V_{SSD} threshold and the t_{oc} time is elapsed.

The driver outputs restart following the input pins as soon as the voltage at the $\overline{SD}$ pin reaches the higher threshold of the $\overline{SD}$ logic input.

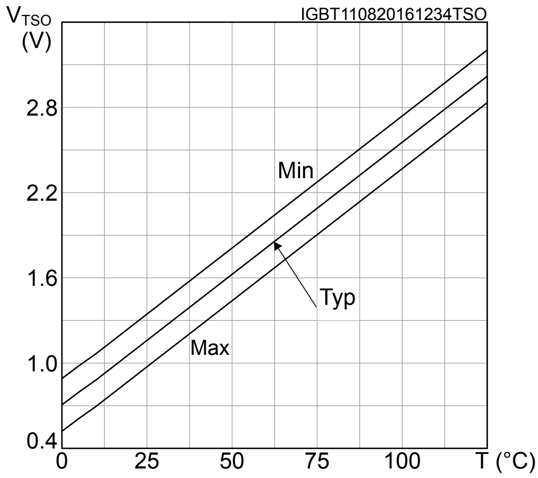
The smart shutdown system provides the possibility to increase the time constant of the external RC network (i.e., the disable time after the fault event) up to very high values without increasing the delay time of the protection.

5 Temperature monitoring solutions

5.1 TSO output

The device integrates a temperature sensor. A voltage proportional to the die temperature is available on the TSO pin. When this function is not used, the pin can be left floating.

Figure 7. V_{TSO} output characteristics vs LVIC temperature



5.2 NTC thermistor

Table 12. NTC thermistor

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{25}	Resistance	T = 25 °C		85		kΩ
R_{125}	Resistance	T = 125 °C		2.6		kΩ
B	B-constant	T = 25 to 100 °C		4092		K
T	Operating temperature range		-40		125	°C

Figure 8. NTC resistance vs temperature

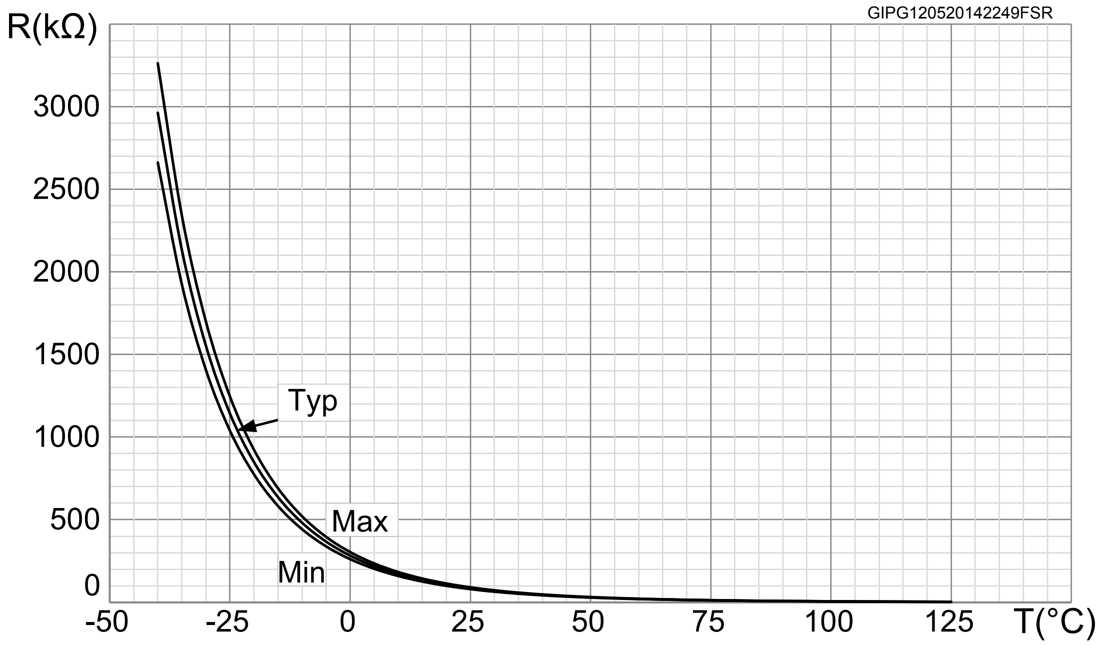
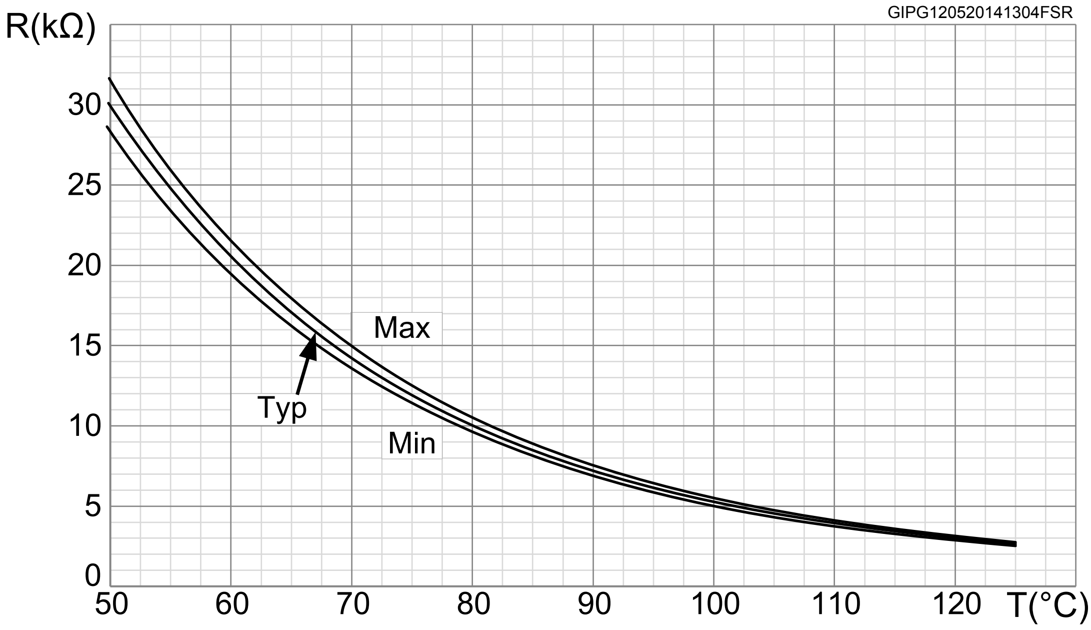
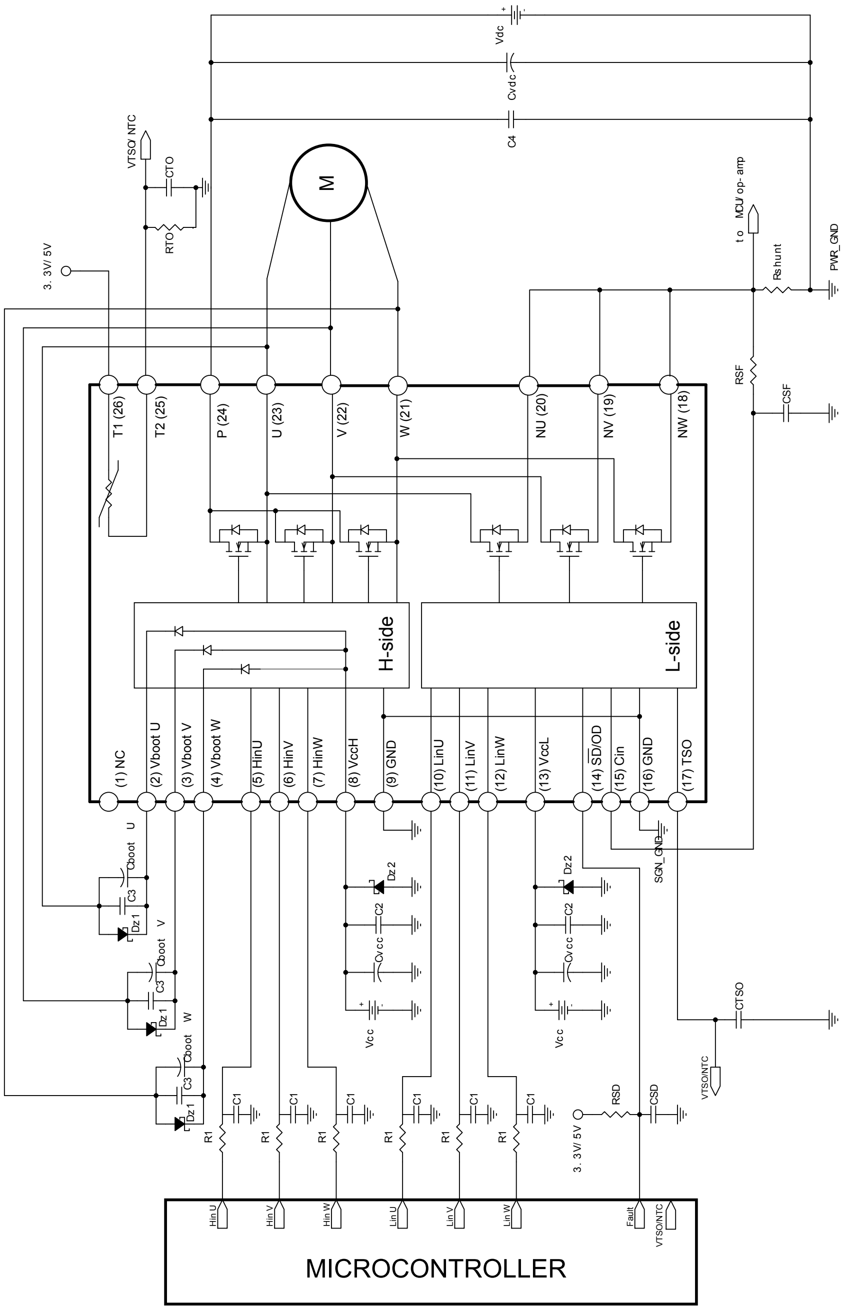


Figure 9. NTC resistance vs temperature - zoom



6 Application circuit example

Figure 10. Application circuit example



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Application designers are free to use a different scheme according to the device specifications.

6.1 Guidelines

1. Input signals HIN, LIN are active-high logic. A 100 kΩ (typ.) pull-down resistor is built-in for each input pin. To prevent input signal oscillations, the wiring of each input should be as short as possible and the use of RC filters (R_1, C_1) on each input signal is suggested. The filters should be with a time constant of about 100 ns and placed as close as possible to the IPM input pins.
2. The use of a bypass capacitor C_{VCC} (aluminum or tantalum) can reduce the transient circuit demand on the power supply. Besides, to reduce any high-frequency switching noise distributed on the power lines, a decoupling capacitor C_2 (100 to 220 nF, with low ESR and low ESL) should be placed as close as possible to each V_{cc} pin and in parallel with the bypass capacitor.
3. The use of an RC filter (R_{SF}, C_{SF}) prevents protection circuit malfunctions. The time constant (R_{SF} x C_{SF}) should be set to 1 µs and the filter must be placed as close as possible to the CIN pin.
4. The $\overline{SD}$ is an input/output pin (open-drain type if it is used as output). It should be pulled up to a power supply (i.e., MCU bias at 3.3/5 V) by a resistor value, which can keep the I_{od} no higher than 5 mA (V_{OD} ≤ 500 mV when open-drain MOSFET is ON). The filter on $\overline{SD}$ should be sized to get a desired re-starting time after a fault event and placed as close as possible to the $\overline{SD}$ pin.
5. A decoupling capacitor C_{TSO} between 1 nF and 10 nF can be used to increase the noise immunity of the TSO thermal sensor; a similar decoupling capacitor C_{OT} (between 10 nF and 100 nF) can be implemented if the NTC thermistor is available and used. In both cases, their effectiveness is improved if these capacitors are placed close to the MCU.
6. The decoupling capacitor C_3 (100 to 220 nF with low ESR and low ESL) in parallel with each C_{boot} filters high-frequency disturbances. Both C_{boot} and C_3 (if present) should be placed as close as possible to the U,V,W and V_{boot} pins. Bootstrap negative electrodes should be connected to the U,V,W terminals directly and separated from the main output wires.
7. To prevent overvoltage on the V_{CC} pin, a Zener diode (Dz1) can be used. Similarly on the V_{boot} pin, a Zener diode (Dz2) can be placed in parallel with each C_{boot}.
8. The use of the decoupling capacitor C_4 (100 to 220 nF, with low ESR and low ESL) in parallel with the electrolytic capacitor C_{Vdc} prevents surge destruction. Both capacitors C_4 and C_{Vdc} should be placed as close as possible to the IPM (C_4 has priority over C_{vdc}).
9. By integrating an application-specific type HVIC inside the module, direct coupling to the MCU terminals without an optocoupler is possible.
10. Low inductance shunt resistors should be used for phase leg current sensing.
11. In order to avoid malfunctions, the wiring on N pins, the shunt resistor and PWR_GND should be as short as possible.
12. The connection of the SGN_GND to the PWR_GND at one point only (close to the shunt resistor terminal) can reduce the impact of power ground fluctuation.

These guidelines ensure the device specifications for application designs. For further details, please refer to the relevant application note.

Table 13. Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{PN}	Supply voltage	Applied among P-Nu, N_V, N_W		300	400	V
V_{CC}	Control supply voltage	Applied to V_{CC}-GND	13.5	15	18	V
V_{BS}	High-side bias voltage	Applied to V_{BOOTi}-OUT_i for i = U, V, W	13		18	V
t_{dead}	Blanking time to prevent arm-short	For each input signal	1.5			µs
f_{PWM}	PWM input signal	-40 °C < T_C < 100 °C -40 °C < T_J < 125 °C			20	kHz
T_C	Case operation temperature				100	°C

7 Electrical characteristics (curves)

Figure 11. Output characteristics

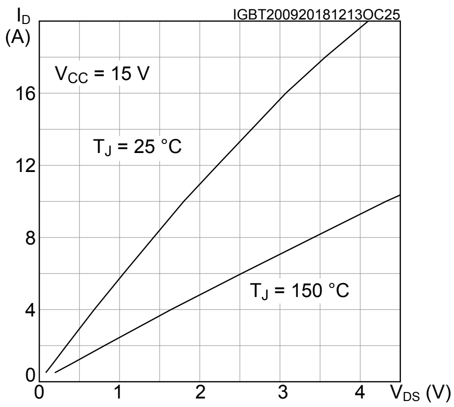


Figure 12. Diode V_{SD} vs drain current

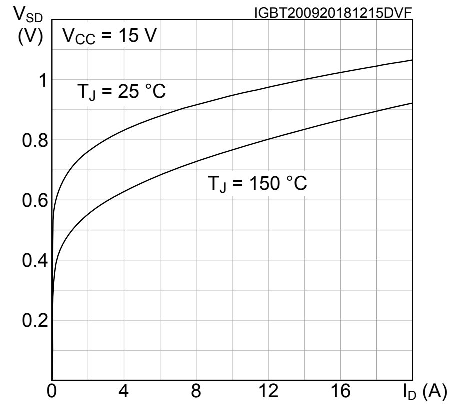


Figure 13. I_D vs temperature

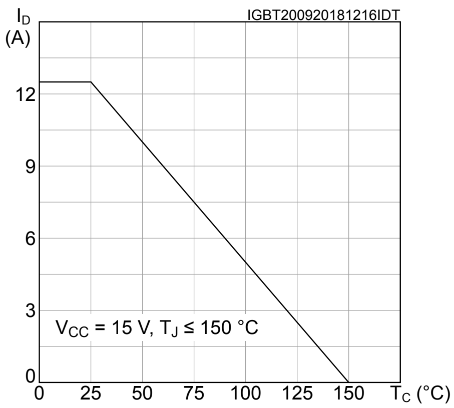


Figure 14. E_{ON} switching energy vs drain current

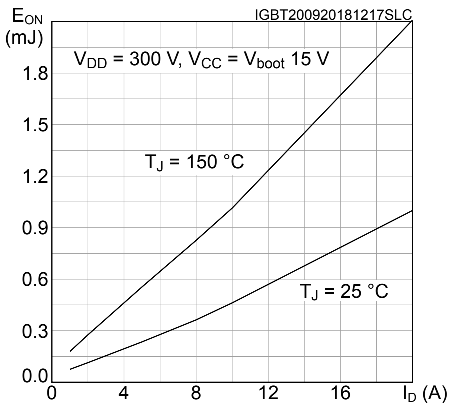


Figure 15. E_{OFF} switching energy vs drain current

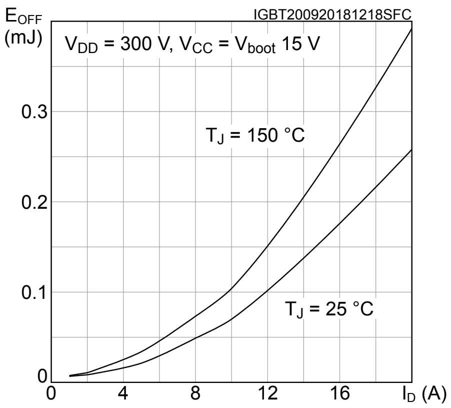
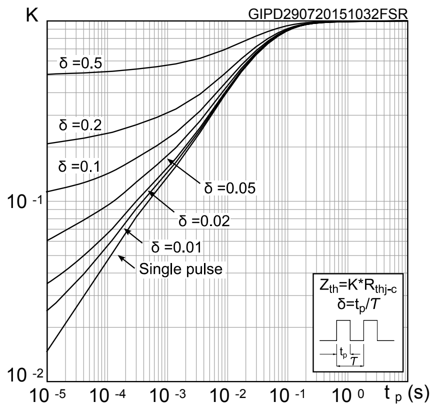


Figure 16. Thermal impedance for SDIP2B-26L MOSFET



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

8.1 SDIP2B-26L type L package information

Figure 17. SDIP2B-26L type L package outline

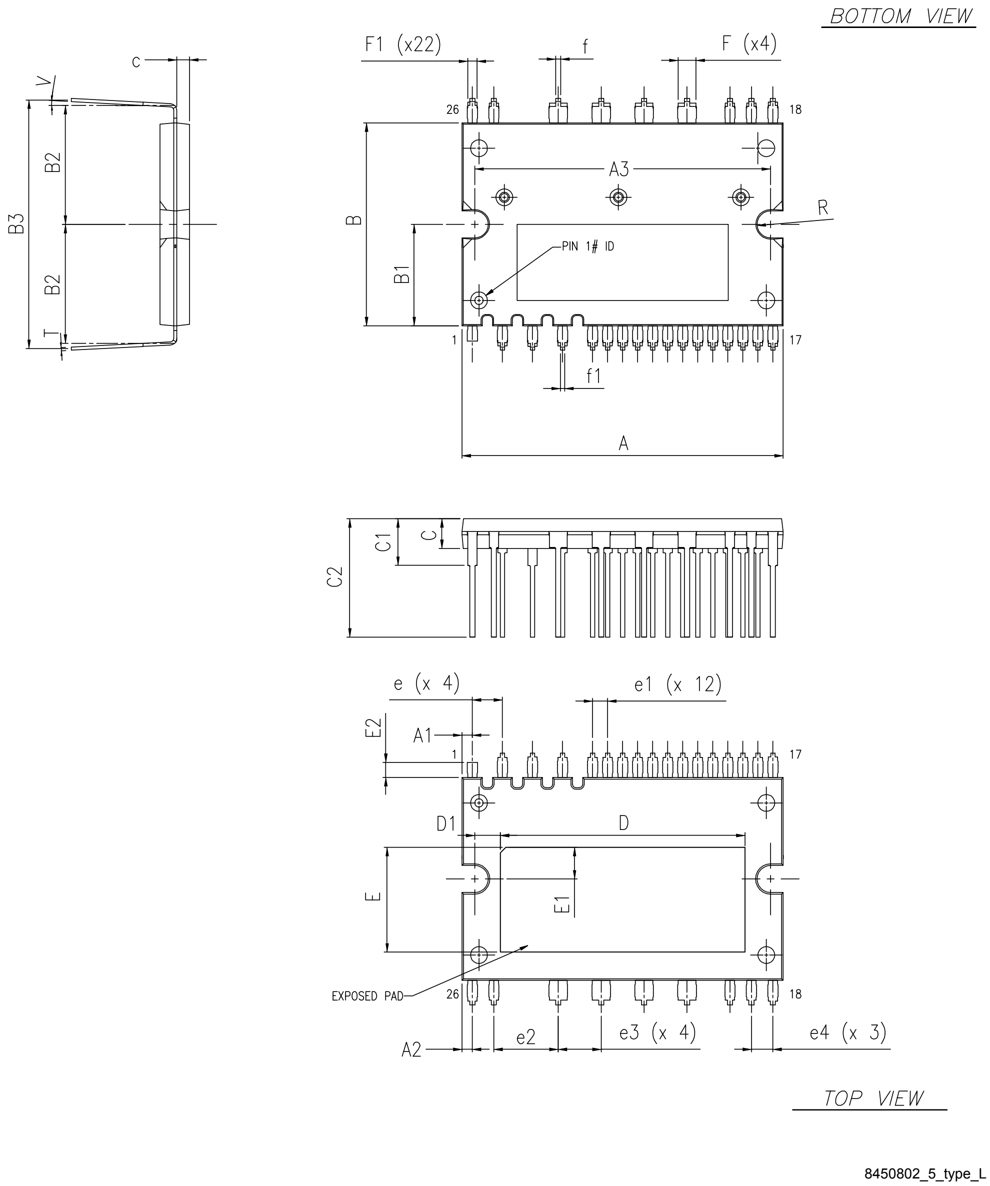


Table 14. SDIP2B-26L type L package mechanical data

Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	37.50	38.00	38.50
A1	0.97	1.22	1.47
A2	0.97	1.22	1.47
A3	34.70	35.00	35.30
c	1.45	1.50	1.55
B	23.50	24.00	24.50
B1		12.00	
B2	13.90	14.40	14.90
B3	28.90	29.40	29.90
C	3.30	3.50	3.70
C1	5.00	5.50	6.00
C2	13.50	14.00	14.50
D	28.70	29.30	29.80
D1	2.55	2.85	3.15
e	3.356	3.556	3.756
e1	1.578	1.778	1.978
e2	7.42	7.62	7.82
e3	4.88	5.08	5.28
e4	2.34	2.54	2.74
E	11.90	12.40	12.90
E1	3.45	3.75	4.05
E2		1.80	
f	0.45	0.60	0.75
f1	0.35	0.50	0.65
F	1.95	2.10	2.25
F1	0.95	1.10	1.25
R	1.55	1.575	1.60
T	0.375	0.40	0.425
V	0°		5°

Revision history

Table 15. **Document revision history**

Date	Revision	Changes
02-May-2017	1	Initial release
24-Sep-2018	2	Updated title, features and description on cover page. Updated Table 2. Inverter part, Table 5. Thermal data and Table 11. Fault timing. Updated Section 3 Electrical characteristics, Section 7 Electrical characteristics (curves) and Section 8.1 SDIP2B-26L type L package information. Minor text changes

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