




Multiprotocol wireless 32-bit MCU Arm[®]-based Cortex[®]-M4 with FPU, Bluetooth[®] Low Energy and 802.15.4 radio solution

Data brief - preliminary data

Features

- Includes ST state-of-the-art patented technology
 - Radio
 - 2.4 GHz RF transceiver supporting Bluetooth[®] specification v5.0 and IEEE 802.15.4-2011 PHY and MAC
 - RX Sensitivity: -96 dBm (Bluetooth[®] Low Energy at 1 Mbps), -100 dBm (802.15.4)
 - Programmable output power up to +6 dBm with 1 dB steps
 - Integrated balun to reduce BOM
 - Support for 2 Mbps
 - Dedicated Arm[®] 32-bit Cortex[®]-M0+ CPU for real-time Radio layer
 - Accurate RSSI to enable power control
 - Compliant with radio frequency regulations ETSI EN 300 328, EN 300 440, FCC CFR47 Part 15 and ARIB STD-T66
 - Ultra-low-power platform
 - 1.71 V to 3.6 V power supply
 - -40 °C to 85 / 105 °C temperature ranges
 - 30 nA shutdown mode
 - 600 nA Standby mode + RTC + 32 KB RAM
 - 1.8 µA Stop mode + RTC + 256 KB RAM
 - Active-mode MCU + RF (SMPS ON): < 50 µA/MHz
 - RX: 3.8 mA
 - TX at 0 dBm: 5.5 mA
 - Core: Arm[®] 32-bit Cortex[®]-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator[™]) allowing 0-wait-state execution from Flash memory, frequency up to 64 MHz, MPU, 80 DMIPS and DSP instructions
 - Supply and Reset management
 - High efficiency embedded SMPS step-down converter
- | | | |
|---|---|---|
|  |  |  |
| UFQFPN48 | VFQFPN68 | WLCSP100 |
| 7 mm x 7 mm solder pad | 8 mm x 8 mm solder pad | 0.4 mm pitch |
- Ultra-safe, low-power BOR (brownout reset) with five selectable thresholds
 - Ultra-low-power POR/PDR
 - Programmable voltage detector (PVD)
 - V_{BAT} mode with RTC and backup registers
 - Clock sources
 - 32 MHz crystal oscillator with integrated trimming capacitors (Radio and CPU clock)
 - 32 kHz crystal oscillator for RTC (LSE)
 - Internal low-power 32 kHz (±5%) RC (LSI1)
 - Internal low-power 32 kHz (stability ±500 ppm) RC (LSI2)
 - Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (better than ±0.25 % accuracy)
 - High Speed internal 16 MHz factory trimmed RC (±1%)
 - 2x PLL for system clock, USB, SAI and ADC
 - Memories
 - Up to 1 MB Flash memory with sector protection (PCROP) against R/W operations, enabling authentic Bluetooth[®] Low Energy and 802.15.4 SW stack
 - Up to 256 KB RAM, including 64 KB with hardware parity check
 - 20x32-bit Backup Register
 - Boot loader supporting, USART, SPI, I2C and USB interfaces
 - OTA (Over the Air) Bluetooth[®] Low Energy and 802.15.4 update
 - Quad SPI memory interface with XIP

- Rich Analog peripherals (down to 1.62 V)
 - 12-bit ADC 4.26MSPs, up to 16-bit with hardware oversampling, 200 μ A/MSPs
 - 2x ultra-low-power comparator
 - Accurate 2.5 V or 2.048 V reference voltage buffered output
- System peripherals
 - Inter Processor Communication Controller (IPCC) for communication with Bluetooth[®] Low Energy and 802.15.4
 - HW semaphores for resources sharing between CPUs
 - 2x DMA controllers (7x channels each) supporting ADC, SPI, I2C, USART, QSPI, SAI, AES, Timers
 - 1x USART (ISO 7816, IrDA, SPI Master, Modbus and Smartcard mode)
 - 1x LPUART (Low Power)
 - 2x SPI 32 Mbit/s
 - 2x I2C (SMBus/PMBus)
 - 1x SAI (dual channels)
 - 1x USB 2.0 FS device, crystal-less, BCD and LPM
 - Touch Sensing controller, up to 28 channels
 - LCD 8x40 with step-up converter
 - 1x 16-bit, four channels advanced timer
 - 2x 16-bits, two channels timer
 - 1x 32-bits, four channels timer
 - 2x 16-bits ultra-low-power timer
 - 1x independent SysTick
 - 1x independent watchdog
 - 1x window watchdog
- Security & ID
 - Secure Firmware Installation (SFI) for Bluetooth[®] Low Energy and 802.15.4 SW stack
 - 3x Hardware Encryption AES maximum 256-bit for the application, the Bluetooth[®] Low Energy and IEEE802.14.5
 - Customer key storage / key manager services
 - HW Public Key Authority (PKA)
 - Cryptographic algorithms: RSA, Diffie-Hellman, ECC over GF(p)
 - True random number generator (RNG)
 - Sector protection against R/W operation (PCROP)
 - CRC calculation unit
 - 96-bit unique ID
 - 64-bit unique ID. Possibility to derive 802.15.5 64-bit and Bluetooth[®] Low Energy 48-bit EUI
- Up to 72 fast I/Os, 70 of them 5 V-tolerant
- Development support
 - Serial wire debug (SWD), JTAG for the Application processor
 - Application cross trigger with input and output
 - Embedded Trace Macrocell[™] for application
- All packages are ECOPACK2[®] compliant

Table 1. Device summary

| Reference | Part numbers |
|-------------|---|
| STM32WB55xx | STM32WB55CC, STM32WB55RC, STM32WB55VC STM32WB55CE, STM32WB55RE, STM32WB55VE STM32WB55CG, STM32WB55RG, STM32WB55VG |

1 Introduction

This data brief provides information on the STM32WB55xx microcontrollers.

For information on the Arm^{®(a)} Cortex[®]-M4 and Cortex[®]-M0+ cores, refer, respectively, to the Cortex[®]-M4 Technical Reference Manual and to the Cortex[®]-M0+ Technical Reference Manual, both available from the www.arm.com website.

For information on 802.15.4 refer to the IEEE website (www.ieee.org).

For information on Bluetooth[®] refer to www.bluetooth.com.



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2 Description

The STM32WB55xx multiprotocol wireless and ultra-low-power devices embed a powerful and ultra-low-power radio compliant with the Bluetooth® Low Energy SIG specification v5.0 and with IEEE 802.15.4-2011. They contain a dedicated Arm® Cortex® -M0+ for performing all the real-time low layer operation.

The STM32WB55xx devices are designed to be extremely low-power and are based on the high-performance Arm® Cortex®-M4 32-bit RISC core operating at a frequency of up to 64 MHz. The Cortex®-M4 core features a Floating point unit (FPU) single precision that supports all Arm® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) that enhances application security.

Enhanced inter-processor communication is provided by the IPCC with six bidirectional channels. The HSEM provides hardware semaphores used to share common resources between the two processors.

The STM32WB55xx devices embed high-speed memories (Flash memory up to 1 Mbyte, up to 256 Kbyte of SRAM), a Quad-SPI Flash memory interface (available on all packages) and an extensive range of enhanced I/Os and peripherals.

Direct data transfer between memory and peripherals and from memory to memory is supported by 14 DMA channels with a full flexible channel mapping by the DMAMUX peripheral.

The STM32WB55xx devices embed several mechanisms for embedded Flash memory and SRAM: readout protection, write protection and proprietary code readout protection. Portions of the memory can be secured for Cortex® -M0+ exclusive access.

The two AES encryption engines, PKA and RNG enable lower layer MAC and upper layer cryptography. A customer key storage feature may be used to keep the keys hidden.

The devices offer one fast 16-bit ADC and two ultra-low-power comparators associated with a high accuracy reference voltage generator.

The STM32WB55xx devices embed a low-power RTC, one advanced 16-bit timer, one general-purpose 32-bit timer, two general-purpose 16-bit timers, and two 16-bit low-power timers.

In addition, up to 28 capacitive sensing channels are available. The devices also embed an integrated LCD driver up to 8x40 or 4x44, with internal step-up converter.

They also feature standard and advanced communication interfaces:

- one USART (ISO 7816, IrDA, Modbus and Smartcard mode)
- one Low Power UART (LPUART)
- two I2C (SMBus/PMBus)
- two SPI (up to 32 MHz)
- one Serial Audio Interface with two channels and three PDMs (SAI)
- one USB 2.0 FS device with embedded crystal-less oscillator, supporting BCD and LPM
- one Quad-SPI with Execute in Place (XIP) capability

The STM32WB55xx operate in the -40 to +105 °C (+125 °C junction) temperature range from a 1.71 to 3.6 V power supply. A comprehensive set of power-saving modes enables the design of low-power applications.

The STM32WB55xx integrate a high efficiency SMPS step-down converter. It includes independent power supplies for analog input for ADC and comparators, as well as a 3.3 V dedicated supply input for USB.

A V_{BAT} dedicated supply allows the devices to back up the LSE 32.768KHz oscillator, the RTC and the backup registers, thus enabling the STM32WB55xx to supply these functions even if the main V_{DD} is not present through a CR2032-like battery, a Supercap or a small rechargeable battery.

The STM32WB55xx family offers three packages, from 48 to 100 pins.

Table 2. STM32WB55xx family device features and peripheral counts

| Feature | | STM32WB55Cx | | | STM32WB55Rx | | | STM32WB55Vx | | |
|----------------------------------|----------------------|-----------------------------------|--------|--------|-----------------------------------|--------|--------|-------------------|--------|--------|
| Flash memory density | | 256 KB | 512 KB | 1 MB | 256 KB | 512 KB | 1 MB | 256 KB | 512 KB | 1 MB |
| SRAM density | | 128 KB | 256 KB | 256 KB | 128 KB | 256 KB | 256 KB | 128 KB | 256 KB | 256 KB |
| BLE | | V5.0 (2 Mbps) | | | | | | | | |
| 802.15.4 | | Yes | | | | | | | | |
| Timers | Advanced | 1 (16 bits) | | | | | | | | |
| | General purpose | 2 (16 bits) + 1 (32 bits) | | | | | | | | |
| | Low power | 2 (16 bits) | | | | | | | | |
| | SysTick | 1 | | | | | | | | |
| Comm interface | SPI | 1 | | | 2 | | | | | |
| | I2C | 2 | | | | | | | | |
| | USART ⁽¹⁾ | 1 | | | | | | | | |
| | LPUART | 1 | | | | | | | | |
| | SAI | 2 channels | | | | | | | | |
| | USB FS | Yes | | | | | | | | |
| | QSPI | 1 | | | | | | | | |
| RTC | | 1 | | | | | | | | |
| Tamper pin | | 1 | | | 3 | | | | | |
| Wakeup pin | | 2 | | | 5 | | | | | |
| LCD, COMxSEG | | Yes, 4x13 | | | Yes, 7x23 or 4x26 | | | Yes, 8x40 or 4x44 | | |
| GPIOs | | 30 | | | 49 | | | 72 | | |
| Capacitive sensing | | 1x4 | | | 3x4 | | | 7x4 | | |
| 16-bit ADC Number of channels | | 13 channels (incl. 3 internal) | | | 19 channels (incl. 3 internal) | | | | | |
| Internal V_{ref} | | No | | | Yes | | | | | |
| Analog comparator | | 2 | | | | | | | | |
| Max CPU frequency | | 64 MHz | | | | | | | | |

Table 2. STM32WB55xx family device features and peripheral counts (continued)

| Feature | STM32WB55Cx | STM32WB55Rx | STM32WB55Vx |
|-----------------------|--|---|--------------------------|
| Operating temperature | Ambient operating temperature: -40 to +105 °C Junction temperature: -40 to 125 °C | | |
| Operating voltage | 1.71 to 3.6 V | | |
| Package | UFQFPN48 7 mm x 7 mm 0.5 mm pitch, solder pad | VFQFPN68 8 mm x 8 mm 0.4 mm pitch, solder pad | WLCSP100 0.4 mm pitch |

1. USART peripheral can be used as SPI master.

3 Revision history

Table 3. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 22-Nov-2016 | 1 | Initial release. |
| 31-Jan-2018 | 2 | Changed document classification, from ST Restricted to Public. Updated <i>Features</i> and <i>Description</i> . Removed former Sections 3 to 5. |
| 15-May-2018 | 3 | Updated <i>Features</i> and <i>Description</i> . |

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