AFBR-8422IDZ

CFP2, 850 nm, 100GBASE-SR10 Compliant Pluggable 100G Ethernet Optical Transceiver

Data Sheet

Avago
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Description

Avago Technologies' AFBR-8422IDZ CFP2 SR10 is a ten channel pluggable, parallel, fiber optic transceiver for 100Gbps Ethernet Applications. The transceiver supports high speed serial links over multi-mode fiber at signalling rates up to 103.125 Gb/s (a serial line rate of 10.3125 Gb/s per channel) for link distances up to 100 m with OM3 fiber or 150 m with OM4 fiber. The product is compliant with the CFP2 industry agreement for mechanical and low speed electrical specifications. High speed electrical and optical specifications are compliant with IEEE 802.3ba Clause 86 for 100GBase-SR10 media, Clause 86A for CPPI electrical interface and Clause 45 for MDIO.

The transceiver electrical interface uses a 104 contact edge type connector, as specified in the CFP2 industry agreement. The optical interface uses a 24-fiber MTP® (MPO) fiber optic connector. This transceiver incorporates Avago Technologies proven integrated circuit and VCSEL technologies to provide reliable, high performance and consistent service.

Digital diagnostic monitoring information (DMI) is present in the AFBR-8422IDZ per the CFP2 industry agreement, providing real time monitoring information of transmitter, receiver and module operating conditions over the MDIO interface.

Applications

- 100Gb/s Ethernet Interconnects (802.3ba Clause 86)
- 10 x 10Gb/s Ethernet Interconnects (802.3ae Clause 52)
- Datacom/Telecom Switch and Router Connections
- Data Aggregation and Density Applications

Notes:
1. CFP MSA Management Interface Specification Version 2.2 r06a, July 1, 2013
2. CFP MSA CFP2 Hardware Specification Revision 1.0, July 26, 2013

Features

- Links up to 100 m using OM3 fiber and 150 m using OM4 fiber
- CFP2 Power Dissipation Class 2 with CDRs in bypass. CDRs are bypassed for lower power dissipation by default
- CFP2 Power Dissipation Class 3 with CDRs ON
- Proven High Reliability 850 nm technology: Avago VCSEL array transmitter and Avago PIN array receiver.
- Compliant to 100 GbE specifications 802.3ba (100GBase-SR10 and CPPI) up to 100 m OM3 and 150 m OM4 fiber.
- Compliant to 40GbE specifications 802.3ba (40GBase-SR4 and XLPPI) up to 100 m OM3 and 150 m OM4 fiber.
- Compatible with 10GE SR specifications per 802.3ae (10GBASE-SR) up to 100 m OM3 fiber.
- OTU4 Support at 11.18 Gb/s per channel
- CFP2 10x10Gbit/s Host Pin Map
- Class 1 eye safe per IEC60825-1 and CDRH
- Wide case temperature range (0 °C to 70 °C)
- Utilizes standard 24 lane optical fiber with MTP® (MPO) optical connector for high density and thin, lightweight cable management
- Diagnostic features per CFP2 using MDIO. Real time monitoring of:
  - Transmitter average optical power
  - Received average optical power
  - Laser bias current
  - Temperature
  - Supply Voltage
- Host Lane Loopback (eLoop) and Network Lane Loopback (oLoop) functionality
- Integrated CDRs on each transmit and receive lane
- Support CDB (Common Data Block) per CFP MSA MIS Version 2.2[1]
- CFP Management Interface Specification Version 2.2[1]
- CFP2 Hardware Specification Revision 1.0[2]
- Compliant to RoHS directives

Transceiver Block Diagram

Transmitter Section:

The optical transmitter incorporates a 10-channel VCSEL (Vertical Cavity Surface Emitting Laser) array, a 10-channel input CDR/buffer and laser driver, diagnostic monitors, laser control and bias blocks. The transmitter is designed for IEC-60825 and CDRH eye safety compliance. The Tx input stage provides CPPI compliant differential inputs per IEEE 802.3ba.

In addition to module level temperature and Vcc monitors, Avago CFP2 SR10 transceivers provide per channel monitors of VCSEL bias and transmitter optical output power through the MDIO interface. Alarm thresholds are established for the monitored diagnostics in CFP2 MDIO non-volatile registers. Flags are set and linked to the module global alarm pin (GLB_ALRMn, pin 29) via configuration parameters in CFP2 MDIO volatile registers.

AC coupling capacitors are located inside the CFP2 transceiver and are not required on the host board. For module control and interrogations, and MDIO+MDC two wire interface is provided.

Receiver Section:

The optical receiver incorporates a 10-channel PIN photodiode array, a 10-channel pre-amplifier and output CDR/buffer, diagnostic monitors and control blocks. The Rx output stage provides CPPI compliant differential inputs per IEEE 802.3ba. AC coupling capacitors are located inside the CFP2 transceiver and are not required on the host board.

In addition to module level temperature and Vcc monitors, Avago CFP2 SR10 transceivers provide per channel monitors of receiver optical input power through the MDIO interface. Alarm thresholds are established for the monitored diagnostics in CFP2 MDIO non-volatile registers. Flags are set and linked to the module global alarm pin (GLB_ALRMn, pin 29) via configuration parameters in CFP2 MDIO volatile registers.

Low Speed I/O:

The CFP2 SR10 transceiver provides two low speed interfaces to the host for module control and monitoring, one via LVCMOS hard pin signals and the other through an 802.3 compliant 1.2 V CMOS MDIO+MDC two wire serial interface.

Hard pin functions are available to support a Global Tx Disable control (pin 24, TX_DIS), a Global Low Power Mode control (pin 26, MOD_LOPWR), a global module Reset control (pin 28, MOD_RSTn), a global module Rx LOS monitor (pin 25, RX_LOS) and a global module Alarm monitor (pin 29, GLB_ALRMn). The pin functions can be customized via configuration parameters in CFP2 MDIO volatile registers.

Soft functions are available to support many control and monitoring behaviours via a two wire serial MDIO+MDC interface. Avago's CFP SR10 transceivers support clock rates from 100 kHz to 4 MHz per the CFP2 industry agreement.

Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Contacts	JEDEC Human Body Model (HBM) (JESD22-A114-B)	High speed contacts shall withstand 1000 V. All other contacts shall withstand 2000 V.
Electrostatic Discharge (ESD) to the Optical Connector Receptacle	EN61000-4-2, Criterion B	When installed in a properly grounded housing and chassis the units are subjected to 15 kV air discharges during operation and 8 kV direct discharges to the case.
Electromagnetic Interference (EMI)	FCC Part 15 CENELEC EN55022 (CISPR 22A) VCCI Class 1	System margins are dependent on customer board and chassis design.
RF Immunity	Variation of IEC 61000-4-3	Typically shows no measurable effect from a 10 V/m field swept from 80 MHz to 1 GHz applied to the module without a chassis enclosure
Laser Eye Safety and Equipment Type Testing	US FDA CDRH AEL Class 1 US21 CFP, Subchapter J per Paragraphs 1002.10 and 1002.12 (IEC) EN60825-1:1994 +A11 +A2 (IEC) EN60825-2:1994 +A1 (IEC) EN60950:1992 +A1 +A2 +A3 +A4 +A11	CDRH Certification 9720151-141 TUV File: R 72131700
Component Recognition	Underwriters Laboratories (UL) and Canadian Standards Association (CSA) Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File: E173874
RoHS Compliance	RoHS Directive 2002/95/EC and it's amendment directives 6/6	RoHS6 with exemption 7c-I
Flammability		UL 94V-0
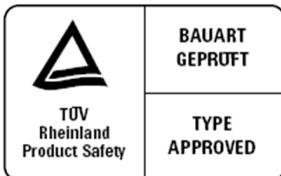
MPO Optical Lane Assignments

CFP2 Rx Optical Channel
MTP/MPO Fiber Number

MTP/MPO Fiber Number
CFP2 Tx Optical Channel

Unused Fibers   Unused Fibers

3
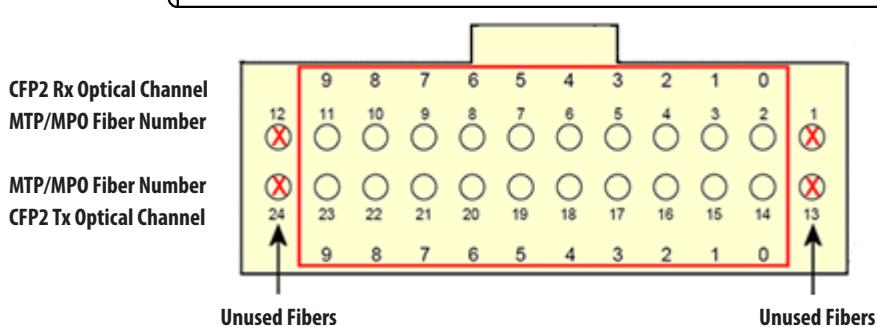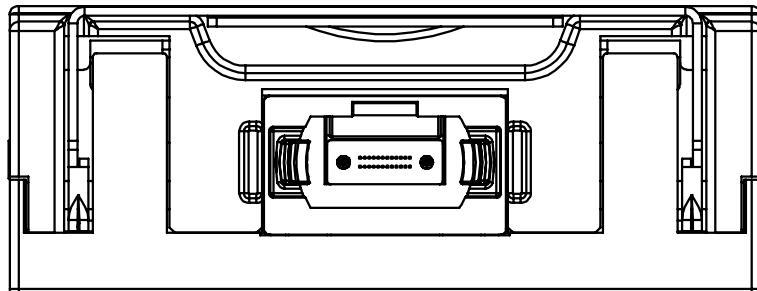
Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit	Notes
Storage Temperature	T_S	-40	85	°C	
Absolute Maximum Operating Temperature	T_C		85	°C	Note 2
3.3V Power Supply Voltage	V_{CC}	-0.5	3.6	V	Per CFP2 MSA
In Rush Current Rate (All pins, Class 3)		-200	200	mA/µs	Per CFP2 MSA
Operating Power Supply Current	I_{CC}		3.75	A	Per CFP2 MSA
Data Input Voltage – Single Ended		-0.5	Vcc+0.5	V	
Data Input Voltage – Differential	$|V_{dip}\text{-}V_{din}|$		1.0	V	Note 3
3.3 V LVCMOS Control Pin Input Voltage		-0.3	Vcc+0.3	V	Per CFP2 MSA
3.3 V LVCMOS Control Pin Output Current		-4.0	4.0	mA	Per CFP2 MSA
1.2 V CMOS Control Pin Input Voltage		-0.3	1.5	V	Per CFP2 MSA
1.2 V CMOS Control Pin Output Current		-4.0	4.0	mA	Per CFP2 MSA
Power Supply Noise	V_{rip}		2% 3%		DC – 1MHz 1 – 10MHz
Relative Humidity	RH	5	85	%	
Receiver Optical Damage Threshold	$P_{r,max}$		+3.4	dBm,avg	802.3 Clause 86

Notes:
1. Absolute Maximum Ratings are those values beyond which damage to the device may occur if limits are exceeded for other than a short period of time. See Reliability Data Sheet for specific reliability performance.
2. Electro-optical specifications are not guaranteed outside the recommended operating temperature range. Operation at or above the maximum Absolute Maximum Case Temperature for extended periods of time may adversely impact reliability.
3. This is the maximum input voltage that can be applied across the differential inputs without damaging the input circuitry.

Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Unit	Notes
Case Operating Temperature	T_C	0	70	°C	Note 1, 2
Total Power Dissipation CDRs in Bypass (Default State - Class 2 CFP2)	P_{diss}		6.0	W	Per CFP2 MSA
Total Power Dissipation CDRs ON (Class 3 CFP2)	P_{diss}		9.0	W	Per CFP2 MSA
Total Power Dissipation (Low Power Mode)	$P_{diss,lpwr}$		2.0	W	Per CFP2 MSA
Power Supply Voltage	V_{CC}	3.135	3.465	V	

Notes:
1. The Ambient Operating Temperature limitations are subject to the host system thermal design.
2. Recommended Operating Conditions are those values for which functional performance and device reliability is implied.
3. Per CFP2 industry agreement specifications.

Transmitter and Receiver Electrical Characteristics (CPPI Mode, Internal CDRs Off)

(T_c = 0 °C to 70 °C, V_{cc} = 3.3 V $\pm$ 0.1 V)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
High Speed Signalling Rate, Per Lane			10.3125		Gb/s	$\pm$ 100 ppm Per 802.3 Clause 86
High Speed Signalling Rate, Per Lane			11.18		Gb/s	Un-retimed OTU4 (OTL4.10) rate
Single Ended Input Voltage Tolerance, TP1a		-0.3		4	V	802.3 Clause 86A
AC Common Mode Input Voltage Tolerance, TP1a		15			mV,rms	802.3 Clause 86A
Differential Input Return Loss, TP1	RL,diff	Equation	86A.4.1.1		dB	802.3 Clause 86A
Differential to Common Mode Input Return Loss, TP1		10			dB	802.3 Clause 86A
J2 Jitter Tolerance, TP1a		0.17			UI	802.3 Clause 86A
J9 Jitter Tolerance, TP1a		0.29			UI	802.3 Clause 86A
Data Dependent Pulse Width Shrinkage Tolerance, TP1a		0.07			UI	802.3 Clause 86A
Input Voltage Eye Mask TP1a (X1, X2) Input Voltage Eye Mask TP1a (Y1, Y2)			0.11, 0.31 95, 350		UI mV	802.3 Clause 86A Hit Ratio = 5 x 10^{-5}
Data Output Differential Peak-to-Peak Voltage Swing, TP4		300		850	mV	
Single Ended Output Voltage, TP4		-0.3		4	V	802.3 Clause 86A
AC Common Mode Output Voltage, TP4				7.5	mV,rms	802.3 Clause 86A
Termination mismatch at 1MHz, TP4				5	%	
Differential Output Return Loss, TP4	RL,diff	Equation	86A.4.2.1		dB	802.3 Clause 86A
Common Mode Output Return Loss, TP4		Equation	86A.4.2.2		dB	802.3 Clause 86A
Output Transition Time, 20% to 80%, TP4	T_r, T_f	28			ps	802.3 Clause 86A
J2 Jitter Output, TP4				0.42	UI	802.3 Clause 86A
J9 Jitter Output, TP4				0.65	UI	802.3 Clause 86A
Data Dependent Pulse Width Shrinkage (DDPWS), TP4				0.34	UI	802.3 Clause 86A
Output Voltage Eye Mask (X1, X2) Output Voltage Eye Mask (Y1, Y2)			0.29, 0.5 150, 425		UI mV	802.3 Clause 86A Hit Ratio = 5 x 10^{-5}

Notes:
1. Internally AC coupled and terminated (100 Ω differential).
2. CDRs bypassed result in CPPI compliance per 802.3ba Clause 86A.
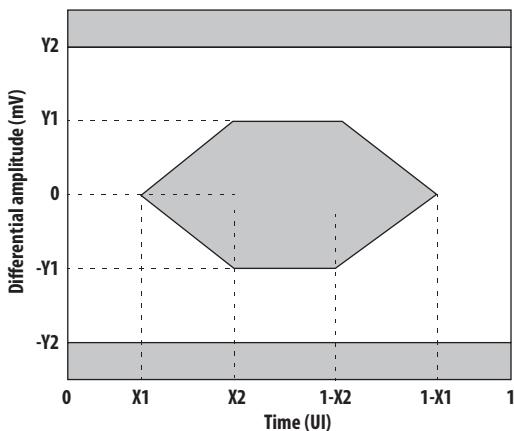
TP1a Electrical Input Eye Mask (CPPI)
Per 86A.5.3.6
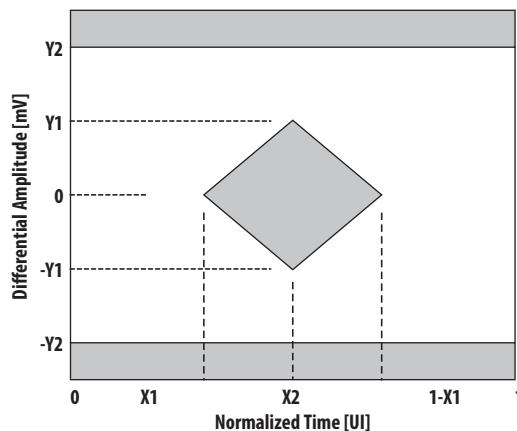
TP4 Electrical Output Eye Mask (CPPI)
Per 86A.5.3.6

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Transmitter Optical Characteristics

(T$_C$ = 0 °C to 70 °C, V$_{CcT}$, V$_{CcR}$ = 3.3 V ± 0.1 V)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Center Wavelength, TP2	λ$_C$	840		860	nm	Per 802.3 Clause 86
Spectral Width – rms, TP2	σ$_{rms}$			0.65	nm	Per 802.3 Clause 86
Average Optical Output Power, TP2	P$_{out}$	-7.6		+2.4	dBm,avg	Note 1
Modulated Optical Output Power (OMA), TP2	Tx,OMA	-5.6		+3.0	dBm,oma	Per 802.3 Clause 86
OMA Optical Power Difference between any two lanes, TP2				+4.0	dB	Per 802.3 Clause 86
Peak Optical Output Power, each lane, TP2				+4.0	dBm,pk	Per 802.3 Clause 86
Launched Power in OMA Minus TDP, each lane, TP2			-6.5		dBm,oma	Per 802.3 Clause 86
Transmitter & Dispersion Penalty, TP2	TDP			3.5	dB	Per 802.3 Clause 86
Extinction Ratio, TP2	ER	3.0			dB	Per 802.3 Clause 86
Optical Return Loss Tolerance, TP2				12	dB	Per 802.3 Clause 86
Encircled Flux, TP2			≥ 86% at 19 µm ≤ 30% at 4.5 µm			Per 802.3 Clause 86
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3, TP2		SPECIFICATION VALUES 0.23, 0.34, 0.43, 0.27, 0.35, 0.4			UI	Hit Ratio = 5 x 10^{-5}
Average Optical Output Power Tx_DIS Asserted	P$_{off}$			-30	dBm,avg	Per 802.3 Clause 86

Note:
1. Max average P$_{out}$ per 802.3ba Clause 86 is +2.4 dBm,avg. To interoperate with legacy 802.3ae Clause 52 devices the limit may need to be constrained to no more than -1.0 dBm,avg.

Mask Coordinates
X1 = 0.23
X2 = 0.34
X3 = 0.43
Y1 = 0.27
Y2 = 0.35
Y3 = 0.40
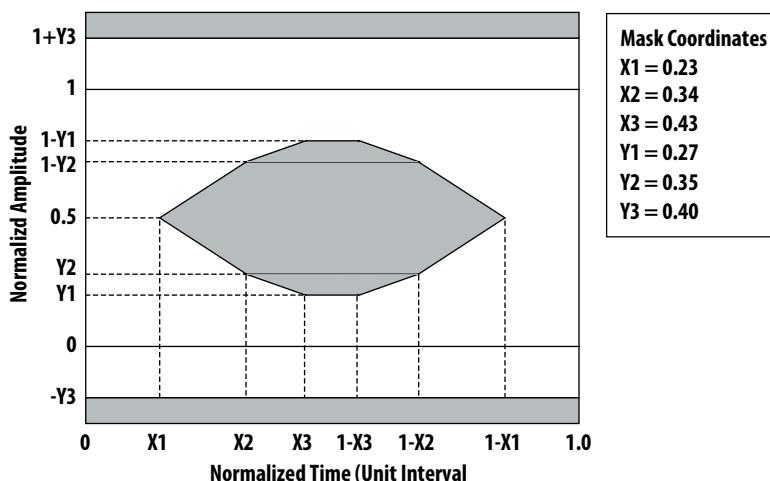
Transmitter eye mask definitions (TP2) at Hit ratio 5 x 10^{-5} hits per sample

Per Table 86-6

Receiver Optical Characteristics

(T_C = 0 °C to 70 °C, V_{ccT}, V_{ccR} = 3.3 V ± 0.1 V)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Center Wavelength, each lane, TP3	λ_C	840		860	nm	Per 802.3 Clause 86
Damage Threshold, TP3		+3.4			dBm,avg	Per 802.3 Clause 86
Average Optical Input Power, Unstressed Rx Sensitivity/Overload, each lane, TP3	P_{IN}	-9.5		+2.4	dBm,avg	Per 802.3 Clause 86
Receiver Reflectance, TP3				-12	dB	Per 802.3 Clause 86
Modulated Optical Input Power (OMA) – Overload, each lane, TP3	Rx OMA			+3.0	dBm,oma	Per 802.3 Clause 86
Modulated Optical Input Power (OMA) – Stressed Rx Sensitivity, each lane, TP3	Rx OMA	-5.4			dBm,oma	Per 802.3 Clause 86
Peak Optical Input Power, each lane, TP3				+4.0	dBm,pk	Per 802.3 Clause 86
Stressed receiver sensitivity in OMA, each lane				-5.4	dBm,oma	Per 802.3 Clause 86
Loss of Signal – Assert, TP3	P_A	-30			dBm,oma	
Loss of Signal – De-asserted, TP3	P_D			-8	dBm,oma	
Loss of Signal – Hysteresis, TP3	$P_A - P_D$	0.5			dB	
Conditions of stressed receiver sensitivity, TP3:						Per 802.3 Clause 86
Vertical eye closure penalty (VECP), each lane		1.9			dB	Per 802.3 Clause 86
Stressed eye J2, Jitter, each lane, TP3		0.30			UI	Per 802.3 Clause 86
Stressed eye J9, Jitter, each lane, TP3		0.47			UI	Per 802.3 Clause 86
OMA of each aggressor lane, TP3		-0.4			dBm	Per 802.3 Clause 86

Note:
1. Refer to IEEE 802.3 Clause 86 for conditions of Stressed Receiver Sensitivity Test and Conditions of Receiver Jitter Tolerance Test.

MDIO and MDC Electrical Characteristics

(T_C = 0 °C to 70 °C, V_{ccT}, V_{ccR} = 3.3 V ± 0.1 V)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
MDC Clock Frequency		0.1		4.0	MHz	
MDC Clock Period	t_prd	0.25		10	µs	
MDC Clock Duty Cycle		40		60	%	
MDC Clock Pulse Width		100			ns	
MDIO Data Setup Time	t_setup	10			ns	
MDIO Data Hold Tim	t_hold	10			ns	
Delay From Rising Edge MDC to MDIO Data Change	t_delay	0		175	ns	
MDIO, MDC and PRTADR2:0 Input Voltage, High	V_{IH}	0.84		1.5	V	
MDIO, MDC and PRTADR2:0 Input Voltage, Low	V_{IL}	-0.3		0.36	V	
MDIO Output Voltage, High	V_{OH}	1		1.5	V	I_{OH} = -100 µA
MDIO Output Voltage, Low	V_{OL}	-0.3		0.2	V	I_{OL} = 100 µA
MDIO Output Current, High	I_{OH}			-4	mA	V_{OH} = 1 V
MDIO Output Current, Low	I_{OL}	4			mA	V_{OL} = 0.2 V

Timing parameters

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Hardware MOD_LOPWR assert	t_MOD_LOPWR_assert			1	ms	
Hardware MOD_LOPWR deassert	t_MOD_LOPWR_deassert			1	ms	
Receiver Loss of Signal Assert Time	t_loss_assert			100	µs	
Receiver Loss of Signal De-Assert Time	t_loss_deassert			100	µs	
Global Alarm Assert Delay Time	GLB_ALRMn_assert			150	ms	This is a logical "OR" of associated MDIO alarm & status registers.
Global Alarm De-Assert Delay Time	GLB_ALRMn_deassert			150	ms	
Initialization time from Reset	t_initialize			2.5	s	
Transmitter Disabled (TX_DIS asserted)	t_deassert			100	µs	
Transmitter Enabled (TX_DIS de-asserted)	t_assert			20	ms	From TX-Off state.

Transceiver Contact Assignment and Signal Description

CFP2 Pin	Logic	Symbol	Electrical Pin Description	Plug Mating Sequence
1	Gnd	GND	GND	1
2	CML	TX9n	High Speed Data Input -, Channel 9	4
3	CML	TX9p	High Speed Data Input +, Channel 9	4
4	Gnd	GND	GND	1
5	CML	TX8n	High Speed Data Input -, Channel 8	4
6	CML	TX8p	High Speed Data Input +, Channel 8	4
7	Gnd	GND	GND	1
8	Gnd	3.3V_GND	3.3V_GND (differs from standard GND)	2
9	VCC	VCC	3.3V Supply	2
10	VCC	VCC	3.3V Supply	2
11	VCC	VCC	3.3V Supply	2
12	VCC	VCC	3.3V Supply	2
13	Gnd	3.3V_GND	3.3V_GND (differs from standard GND)	2
14	Gnd	3.3V_GND	3.3V_GND (differs from standard GND)	2
15	No Connect	VND_IO_A	Module Vendor I/O A. For mfg use only. Do not connect.	3
16	No Connect	VND_IO_B	Module Vendor I/O B. For mfg use only. Do not connect.	3
17	LVCMOS	PRG_CNTL1	Programmable Control 1, set over MDIO. MSA Default is TRXIC_RSTn.	3
18	LVCMOS	PRG_CNTL2	Programmable Control 2, set over MDIO. MSA Default is Hardware Interlock LSB.	3
19	LVCMOS	PRG_CNTL3	Programmable Control 3, set over MDIO. MSA Default is Hardware Interlock MSB.	3
20	LVCMOS	PRG_ALRM1	Programmable Alarm 1, set over MDIO. MSA Default is HI PWR_ON 1	3
21	LVCMOS	PRG_ALRM2	Programmable Alarm 2, set over MDIO. MSA Default is MOD_READY	3
22	LVCMOS	PRG_ALRM3	Programmable Alarm 3, set over MDIO. MSA Default is MOD_FAULT	3
23	Gnd	GND	GND	1
24	LVCMOS	TX_DIS	Global Transmitter Disable (For all laser channels) "1" or NC = transmitter disabled, "0" = transmitter enabled	3
25	LVCMOS	RX_LOS	Global Rx_LOS alarm (Logic OR of all optical RX channels LOS) "1": low optical signal, "0": normal condition	3
26	LVCMOS	MOD_LO PWR	Module Low Power Mode [Achieves < 2 W) "1" or NC: module in low power (safe) mode, "0": power-on enabled	4
27	GND	MOD_ABS	Module absent. Ground in transceiver. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host required.	4
28	LVCMOS	MOD_RSTn	Global Module reset. Pulled down inside module, resistor value of 4.7 kΩ to 10 kΩ. "0" resets the module, "1" or NC = module enabled. Hardware Reset: Asserting MOD_RSTn will cause a complete reset of the module. All VR values are lost and must be re-written by the Host.	3
29	LVCMOS	GLB_ALRMn	Global Module alarm. Logic OR of Fault, Alarms, Warnings, and Status Flags. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host is required.	3
30	Gnd	GND	GND	1
31	1.2V CMOS	MDC	MDIO clock line (100 kHz to 4 MHz) per 802.3ae	3
32	1.2V CMOS	MDIO	MDIO data line per 802.3ae	3
33	1.2V CMOS	PRTADR0	MDIO Physical Port Address bit 0	3
34	1.2V CMOS	PRTADR1	MDIO Physical Port Address bit 1	3
35	1.2V CMOS	PRTADR2	MDIO Physical Port Address bit 2	3
36	No Connect	VND_IO_C	Module Vendor I/O C. For mfg use only. Do not connect.	3
37	No Connect	VND_IO_D	Module Vendor I/O D. For mfg use only. Do not connect.	3
38	No Connect	VND_IO_E	Module Vendor I/O E. For mfg use only. Do not connect.	3
39	Gnd	3.3V_GND	3.3V_GND (differs from standard GND)	2
40	Gnd	3.3V_GND	3.3V_GND (differs from standard GND)	2
41	VCC	VCC	3.3V Supply	2
42	VCC	VCC	3.3V Supply	2
43	VCC	VCC	3.3V Supply	2
44	VCC	VCC	3.3V Supply	2
45	Gnd	3.3V_GND	3.3V_GND (differs from standard GND)	2
46	Gnd	GND	GND	2
47	CML	RX9n	High Speed Data Output -, Channel 9	4
~~47~~	~~CML~~	~~RX9n~~	~~High Speed Data Output -, Channel 9~~	~~4~~

CFP2 Pin	Logic	Symbol	Electrical Pin Description	Plug Mating Sequence
48	CML	RX9p	High Speed Data Output +, Channel 9	4
49	Gnd	GND	GND	1
50	CML	RX8n	High Speed Data Output -, Channel 8	4
51	CML	RX8p	High Speed Data Output +, Channel 8	4
52	Gnd	GND	GND	1
53	Gnd	GND	GND	1
54	CML	RX0p	High Speed Data Output +, Channel 0	4
55	CML	RX0n	High Speed Data Output -, Channel 0	4
56	Gnd	GND	GND	1
57	CML	RX1p	High Speed Data Output +, Channel 1	4
58	CML	RX1n	High Speed Data Output -, Channel 1	4
59	Gnd	GND	GND	1
60	CML	RX2p	High Speed Data Output +, Channel 2	4
61	CML	RX2n	High Speed Data Output -, Channel 2	4
62	Gnd	GND	GND	1
63	CML	RX3p	High Speed Data Output +, Channel 3	4
64	CML	RX3n	High Speed Data Output -, Channel 3	4
65	Gnd	GND	GND	1
66	CML	RX4p	High Speed Data Output +, Channel 4	4
67	CML	RX4n	High Speed Data Output -, Channel 4	4
68	Gnd	GND	GND	1
69	CML	RX5p	High Speed Data Output +, Channel 5	4
70	CML	RX5n	High Speed Data Output -, Channel 5	4
71	Gnd	GND	GND	1
72	CML	RX6p	High Speed Data Output +, Channel 6	4
73	CML	RX6n	High Speed Data Output -, Channel 6	4
74	Gnd	GND	GND	1
75	CML	RX7p	High Speed Data Output +, Channel 7	4
76	CML	RX7n	High Speed Data Output -, Channel 7	4
77	Gnd	GND	GND	1
78	CML	REFCLKp	No functionality in AFBR-8422IDZ	4
79	CML	REFCLKn	No functionality in AFBR-8422IDZ	4
80	Gnd	GND	GND	1
81	CML	TX0p	High Speed Data Input +, Channel 0	4
82	CML	TX0n	High Speed Data Input -, Channel 0	4
83	Gnd	GND	GND	1
84	CML	TX1p	High Speed Data Input +, Channel 1	4
85	CML	TX1n	High Speed Data Input -, Channel 1	4
86	Gnd	GND	GND	1
87	CML	TX2p	High Speed Data Input +, Channel 2	4
88	CML	TX2n	High Speed Data Input -, Channel 2	4
89	Gnd	GND	GND	1
90	CML	TX3p	High Speed Data Input +, Channel 3	4
91	CML	TX3n	High Speed Data Input -, Channel 3	4
92	Gnd	GND	GND	1
93	CML	TX4p	High Speed Data Input +, Channel 4	4
94	CML	TX4n	High Speed Data Input -, Channel 4	4
95	Gnd	GND	GND	1
96	CML	TX5p	High Speed Data Input +, Channel 5	4
97	CML	TX5n	High Speed Data Input -, Channel 5	4
98	Gnd	GND	GND	1
99	CML	TX6p	High Speed Data Input +, Channel 6	4
100	CML	TX6n	High Speed Data Input -, Channel 6	4
101	Gnd	GND	GND	1
102	CML	TX7p	High Speed Data Input +, Channel 7	4
103	CML	TX7n	High Speed Data Input -, Channel 7	4
104	Gnd	GND	GND	1

Host Lane Pins – 10x10G High Speed Electrical Interface (Tx0-9, Rx0-9)

The AFBR-8422IDZ supports 10x10G CPPI compliant electrical interfaces as defined in Ethernet IEEE 803.ba specification. The electrical connector pinouts are per the CFP2 MSA 10x 10G specifications. A non-retimed CPPI interface (per 802.3ba Clause 86A) is supported by bypassing the internal per-channel CDRs. This reduces the current/power consumption and reduces the thermal impact to the host system; this is the default state of the module.

All CDRs (Tx path, Rx path) as depicted in Transceiver Block Diagram are bypassed by default. The user must access the appropriate register to turn all CDRs on. CDR status is controlled by MDIO CFP VR1 register A015 bits 7-0 (09h = CPPI is the default for CDRs off, 01h = turn CDRs on).

All electrical inputs and outputs are internally ac coupled with the CFP2 housing. Differential impedances are nominally 100 Ω.

Network Lanes – 10x10G High Speed Optical Interface (Tx0-9, Rx0-9)

The AFBR-8422IDZ supports 10x10G SR10 multi-mode fiber optic interfaces as defined in Ethernet IEEE 802.3 Clause 86, including optical lane assignments (MPO optical connector) and link specifications.

Global Alarm Pin: (GLB_ALRMn)

The GLB_ALRMn signal pin is an output from the CFP2 module to the host using active low logic (i.e., Logic Low is an alarm condition, Logic High is normal operation). When GLB_ALRMn is asserted (driven Low) it indicates a Fault, Alarm, Warning or Status event has occurred. This reduces the need for continuous polling of status and monitor registers, while maintaining timely alerts to significant events.

GLB_ALRMn can be programmed as the LOGIC OR of the multiple inputs inputs (all of which can be read, cleared and masked in the Memory Map), including

- Module Temperature Alarms
- Module Vcc Alarms
- Global Rx_LOS Alarm

Module Reset Pin: (MOD_RSTn)

The MOD_RSTn signal pin is an input pin from the host to the CFP2 module using active low logic (i.e., Logic Low resets the CFP2 module). This pin is pulled down in the CFP2 with a resistor value of 4.7 kΩ to 10 kΩ.

Module Low Power Mode Enable Pin: (MOD_LOPWR)

The MOD_LOPWR signal pin is an input from the host to the CFP2 module using active high logic (i.e., Logic High sets the CFP2 to low power mode, Logic Low sets the CFP2 to high power mode). When the module is in low power mode it has a maximum power consumption of 2 W.

Module Absent (Not Present) Pin: (MOD_ABS)

(i.e., Logic High indicates a CFP2 is absent in the port, Logic Low indicates a CFP2 is present in the port).

Optical Transmitter Disable Pin: (TX_DIS)

The TX_DIS signal pin is an input from the host to the CFP2 module using active high logic (i.e. Logic High disables the CFP2 optical transmitters; Logic Low enables the CFP2 optical transmitters). This pin is pulled upside in the module and must be pulled down by the host to enable optical transmission.

While in the disabled state, the transmitter alarm and warning flags associated with transmit optical power and laser current will assert. To mask these flags from alarming the host, the user must configure the related masking bits in A220-A229 and A240-A249.

Optical Receiver Loss of Signal Pin: (RX_LOS)

The RX_LOS signal pin is an output from the CFP2 module to the host using active high logic (i.e. Logic High indicates one or more CFP2 optical inputs are not receiving a valid signal; Logic Low indicates all CFP2 optical inputs are receiving a valid signal).

The RX_LOS triggers on a loss of optical modulation as detected at the optical receiver.

Management Data I/O, Clock and Address Pins: (MDIO, MDC, PRTADR0, PRTADR1, PRTADR2)

The CFP2 management data interface consists of 5 pins, including 1 pin for a clock, 1 pin for data and 3 pins for a physical port address definition.

- MDC is the MDIO clock line driven by the host
- MDIO is the bi-directional data line driven by both the host and the CFP2, depending on data direction.

The MDIO bus structure follows specifications in IEEE 802.3 Clause 45 at a clock rate up to 4.0 MHz.

- PRTADR0, PRTADR1, PRTADR2 are the MDIO Physical Port address bits 0, 1 and 2

These control pins are used for the system to address all of the CFP ports contained within a host system. PRTADR0 corresponds to the LSB in the physical port addressing scheme. The 5-wire Physical Port Address lines are driven by host to set the module Physical Port Address which should match the address specified in the MDIO Frame.

PRG_CNTLx Behavior:

PRG_CNTL2, PRG_CNTL3 are used as HW_IL_LSB and HW_IL_MSB during the Initialize state (Hardware Interlock). PRG_CNTL1 will be set as default = TXRXIC_RSTn.

After Initialization, the user may assign/un-assign TXRXIC_RSTn function to PRG_CNTL1 and/or PRG_CNTL2 and/or PRG_CNTL3 using Registers A005h, A006h and A007h.

If TRXIC_RSTn is then asserted the signal integrity/loopback chips will be reset. For example, if the module is in "CDRs ON Mode" and the user asserts TRXIC_RSTn, this will cause a reset of the signal integrity chips. The module will revert back to "CDRs Bypass Mode", since "CDRs Bypass Mode" is the DEFAULT state of the Module.

Hardware Interlock

The Hardware Interlock provides for four different power consumption levels. The module shall compare the maximum power dissipation under vendor specified operating conditions to the host system cooling capacity value communicated via the Hardware Interlock.

Hardware Interlock Description		Power Class	Power Dissipation (W)
MSB	LSB		
0	0	1	≤ 3
0	1	2	≤ 6
1	0	3	≤ 9
1	1	≥ 4	>9

PRG_ALRMx Behavior

PRG_ALRMx behavior can be assigned using Registers A008, A009, A00A, per the CFP2 MSA definition. Note, however, that some alarm capabilities do not exist in our CFP2 SR10 module and therefore cannot be assigned to the PRG_ALRMx pins. This a list of the possible PRG_ALRMx assignments:

7:0 Alarm Source Code PRG_ALRMx; Selects, and assigns, an alarm source for PRG_ALRMx	
= 0: Not active, always de-asserted	NOT SUPPORTED
= 1: HIPWR_ON	SUPPORTED
= 2: Ready State	SUPPORTED
= 3: Fault State, MSA default setting	SUPPORTED
= 4: RX_ALRM = RX_LOS + Rx_NETWORK_LOL	SUPPORTED
= 5: TX_ALRM = TX_HOST_LOL	SUPPORTED
= 6: RX_NETWORK_LOL	SUPPORTED
= 7: TX_LOSF	NOT SUPPORTED
= 8: TX_HOST_LOL	SUPPORTED
= 9: OOA, Out of alignment	NOT SUPPORTED

Other and Unused Pins

REFCLKp, REFCLKn pins are not used in the AFBR-8422IDZ and can be left Not Connected (NC). These pins are internally terminated with a capacitor and resistor to ground internal to the CFP2 Module AFBR-8422IDZ.

Software Control/Status Indicators

Software feature sets for AFBR-8422IDZ are defined in the CFP Management Interface Specification (MIS), Version 2.2. Software features are accessible using the MDIO interface per the CFP MSA.

This CFP2 100GBASE-SR10 Module is less complex than other types of transceivers found in the CFP/CFP2 footprint; for example LR4-type modules. Therefore this module does not support many of the elaborate functions defined in the CFP MIS.

Examples of features not required, and therefore, not implemented for this CFP2 100GBASE-SR10 Module media are complex power on sequences related to managing internal laser cooling (section 4.1.2, 4.2 and 4.3), advanced host and network lane considerations related to electrical or optical multiplexers (section 4.9, 4.12), etc..

The CFP2 100GBASE-SR10 Module, AFBR-8422IDZ, provides digital diagnostic functionality for parameters of laser bias, laser optical power, received optical power, V_{CC} and temperature. It has variable host lane equalization.

Enable and Disable CDRs

All Tx CDRs and All Rx CDRs will be turned on with a single command to put the Transceiver into retimer mode. These CDRs cannot be enabled on a per individual channel basis. Furthermore, the user cannot separately turn on Tx CDRs or Rx CDRs.

The CFP2 module is in CDR Bypass, CPPI mode by default; the CDRs will be bypassed by default and 0x09h will be the value in Register A015 bits 7-0 (CPPI mode).

To enable all CDRs and enter retimer mode, the user must write value 0x01h to Register A015 bits 7-0.

Enable Network Lane Loopback (OLoop/OWrap)

The Network Lane Loopback will be disabled by default. To enable the Network Lane Loopback (Oloop/Owrap) write a value of '1' to bit 10 in Register A012.

Enable Host Lane Loopback (ELoop/EWrap)

The Host Lane Loopback will be disabled by default. To enable the Host Lane Loopback (Eloop/Ewrap) write a value of '1' to bit 10 in Register A014.

TX Squelch

Tx_Squelch turns off the laser on a per channel basis when there is no high-speed modulation on the electrical differential inputs on a per channel basis. This feature is enabled by default for all 10 Tx channels, which have the value '0', to bit 1 of registers A260h (channel 0) to A269h (channel 9).

RX Squelch

Rx_Squelch is based on OMA level of the incoming optical signal. Rx_Squelch triggers on loss of modulation (as opposed to a loss of average optical power). This feature is enabled by defaultfor all 10 Rx channels, which have value '0', to bit 0 of registers A260h (channel 0) to A269h (channel 9).

Rx LOS

Rx_Los is based on OMA level of the incoming optical signal. It triggers on loss of modulation (as opposed to a loss of average optical power). The threshold of Rx_Los is user programmable which is by writing value '1' to bit 8 of register A015. With this setting, Rx_Los is triggered by comparing the OMA level of the incoming optical signal against user defined value stored in A03C, A03D, A03E and A03F to generate Rx Alarm and Warning. Values set by host in register A03C ~ A03F should be in the range defined in Table 1: The Permissible Range for Host-Configured Receive Optical Power Threshold.

Password Protected Fields

MSA specifies the default **User** password value as 0101 1100h. This unlock read and write protection to the User NVR1, User NVR1 and CDB pages only in register 8800h, 8880h and AC00h.

Changing the password to 0000 0000h disables the password protection. Users can read and write to User NVR1, User NVR2 and CDB pages without entering a password.

The default **Vendor** password for Vendor NVR1 and Vendor NVR2 is 8101 1100 h. Entering the password provides read-only access to the Vendor NVR1 and Vendor NVR2 pages only in Registers 8400h and 8480h. Without entering correct password, user has no read access to those pages. The password is preset by the factory which can't not be changed at field.

Common Data Block (CDB)

CFP MSA MIS 2.2 allocates 1024 registers on A000h page as the CDB starting at AC00h and ending at AFFFh. AFBR-8422IDZ supports CDB Command Class 0 – System Operation; refer to Table 21 in CFP MSA MIS 2.2 r06a. CDB Command Class 1 – Register Access is not supported

The purpose of the CDB feature is to enable user to perform firmware update to the AFBR-8422IDZ via MDIO interface in the field.

Memory Map

Block Name	Hex Addr	Size	Access Type	8 Bits	Register Name	Value	Description	LSB Unit
NVR1 CFP	8000	1	Read Only	7-0	Module Identifier	11h	CFP2 Module Identifier	n/a
	8001	1	Read Only	7-6	Power Class	A0h	(10b bits 7-6) CFP2 Power Class 1 < 9 W	n/a
				5-4	Lane Ratio Type		(10b bits 5-4) Host to Network Lane Ratio Type n:n (10:10 parallel)	
				3-1	WDM type		(000b bits 3-1) Non-WDM Type	
				0	CLEI Presence		(0b bit 0) No CLEI code present	
	8002	1	Read Only	7-0	Connector Type	09h	MPO optical connector	n/a
	8003	1	Read Only	7-0	Ethernet Application	03h	Ethernet Application 100GE MMF 100GBASE-SR10	n/a
	8004	1	Read Only	7-0	Fibre Channel App	00h	undefined	n/a
	8005	1	Read Only	7-0	Copper Application	00h	undefined	n/a
	8006	1	Read Only	7-0	Sonet Application	00h	undefined	n/a
	8007	1	Read Only	7-0	OTN Application	00h	undefined	n/a
	8008	1	Read Only	7-0	Additional Rates	00h	Not supported	n/a
	8009	1	Read Only	7-4	Network Lanes	AAh	(Ah bits 7-4) Decimal Value = 10 [10 network optical lanes]	n/a
				3-0	Host Lanes		(Ah bits 3-0) Decimal Value = 10 [10 host electrical lanes]	n/a
	800A	1	Read Only	7-6	Media Type	4Ah	MMF (01b bits 7-6) for OM3/OM4.	n/a
				5	Directionality		0 b = Normal	
				4	Optical Muxing		0 b = WITHOUT optical Mux/Demux	
				3-0	Active Fibers per Connector		(Ah bits 3-0) Decimal Value = 10 [i.e., 10 TxRx lanes active per connector]	
	800B	1	Read Only	7-0	Max Network Lane Rate	38h	Decimal Value = 56 [i.e., 56 x 0.2 Gb/2 = 11.2 Gb/s lane rate]	0.2 Gb
	800C	1	Read Only	7-0	Max Host Lane Rate	38h	Decimal Value = 56 [i.e., 56 x 0.2 Gb/2 = 11.2 Gb/s lane rate]	0.2 Gb
	800D	1	Read Only	7-0	Max SM fiber length	00h	Undefined for MMF links	1 km
	800E	1	Read Only	7-0	Max MM OM3 fiber length	0Ah	Decimal Value = 10 [i.e., 10 x 10 m = 100 m maximum MM OM3 length] Maximum OM4 length is 150 m in register 8181.	10 m
	800F	1	Read Only	7-0	Max Cu cable length	00h	Undefined for MMF links	1 m
	8010	1	Read Only	7-0	Number Tx Fibers	0Ah	Decimal Value = 10 Active Transmit Fibers	n/a
	8011	1	Read Only	7-0	Number Tx Wavelengths	00h	Per MSA, 00h represents 850 nm MMF source. (Alt = 01h)	n/a
	8012	2	Read Only	7-0	Min Tx Wavelength (MSB 8012, LSB 8013)	0000h	Per MSA, 00h represents MMF source. (Alt = 8340h for Decimal Value = 33,600) [i.e., 33,600 x 0.025 nm = 840 nm]	.025 nm
	8014	2	Read Only	7-0	Max Tx Wavelength (MSB 8014, LSB 8015)	0000h	Per MSA, 00h represents MMF source. (Alt = 8660h for Decimal Value = 33,600) [i.e., 34,400 x 0.025 nm = 860 nm]	.025 nm
	8016	2	Read Only	7-0	Max Tx Optical Width (MSB 8016, LSB 8017)	0000h	Per MSA, 00h represents MMF source. (Alt = 028Ah for Decimal Value = 650) [i.e., 650 * .001 nm = 0.65 nm]	0.001 nm
	8018	1	Read Only	7-4	Laser Source Type	00h	(0000b bits 7-4) Per MSA for VCSEL source technology	n/a
				3-0	Tx Modulation Type		(0000b bits 0-3) DML - Direct modulation Tx technology	
	8019	1	Read Only	7-4	Tx Device Technology	04h	(0000b bits 7-4) No VOA, tunable, cooling, wavelength ctrl	n/a
				3-0	Detector Type, CDR Type		PIN detector (01b bits 3-2), CDR without EDC (0b bit 1)	
	801A	1	Read Only	7-6	Signal Modulation	40h	NRZ (01b bits 7-6)	n/a
				5-0	Signal Encoding		Non-PSK coding (0000b bits 5-0)	
	801B	1	Read Only	7-0	Max Output Power	11h	Decimal Value = 17 [i.e., 17 * 0.1 mW = 1.74 mW = +2.4 dBm]	0.1 mW
	801C	1	Read Only	7-0	Max Input Power	11h	Decimal Value = 17 [i.e., 17 * 0.1 mW = 1.74 mW = +2.4 dBm]	0.1 mW

Block Name	Hex Addr	Size	Access Type	8 Bits	Register Name	Value	Description	LSB Unit
NVR1 CFP	801D	1	Read Only	7-0	Max Power Consumption	2Dh	Decimal Value = 45 [i.e., 45 * 200 mW = 9 W]	200 mW
	801E	1	Read Only	7-0	LOW Power Consumption	64h	Decimal Value = 100 [i.e., 100 * 20 mW = 2 W]	20 mW
	801F	1	Read Only	7-0	Max Operating Case Temp	46h	[i.e., 70 * 1 °C = 70 °C]. Signed Two's compliment	1 °C
	8020	1	Read Only	7-0	Min Operating Case Temp	00h	[i.e., 0 * 1 °C = 0 °C]. Signed Two's compliment	1 °C
	8021	1	Read Only	7-0	Vendor Name	41h	ASCII "A"	n/a
	8022	1				56h	ASCII "V"	
	8023	1				41h	ASCII "A"	
	8024	1				47h	ASCII "G"	
	8025	1				4Fh	ASCII "O"	
	8026	1				20h	ASCII blank	
	8027	1				20h	ASCII blank	
	8028	1				20h	ASCII blank	
	8029	1				20h	ASCII blank	
	802A	1				20h	ASCII blank	
	802B	1				20h	ASCII blank	
	802C	1				20h	ASCII blank	
	802D	1				20h	ASCII blank	
	802E	1				20h	ASCII blank	
	802F	1				20h	ASCII blank	
	8030	1				20h	ASCII blank	
	8031	1	Read Only	7-0	Vendor OUI	00h	Avago OUI	n/a
	8032	1				17h	Avago OUI	
	8033	1				6Ah	Avago OUI	
	8034	1	Read Only	7-0	Vendor Part Number	41h	ASCII "A"	n/a
	8035	1				46h	ASCII "F"	
	8036	1				42h	ASCII "B"	
	8037	1				52h	ASCII "R"	
	8038	1				2Dh	ASCII "-"	
	8039	1				38h	ASCII "8"	
	803A	1				34h	ASCII "4"	
	803B	1				32h	ASCII "2"	
	803C	1				32h	ASCII "2"	
	803D	1				49h	ASCII "I"	
	803E	1				44h	ASCII "D"	
	803F	1				5Ah	ASCII "Z"	
	8040	1				20h	ASCII blank	
	8041	1				20h	ASCII blank	
	8042	1				20h	ASCII blank	
	8043	1				20h	ASCII blank	
	8044	1	Read Only	7-0	Vendor Serial Number			n/a
	8045	1						
	8046	1						
	8047	1						
	8048	1						
	8049	1						
	804A	1						
	804B	1						
	804C	1						
	804D	1						
	804E	1						
	804F	1						
	8050	1						
	8051	1						
	8052	1						
	8053	1						

Block Name	Hex Addr	Size	Access Type	8 Bits	Register Name	Value	Description	LSB Unit
NVR 1 CFP	8054	1	Read Only	7-0	Date Code			n/a
	8055	1						
	8056	1						
	8057	1						
	8058	1						
	8059	1						
	805A	1						
	805B	1						
	805C	1	Read Only	7-0	Lot Code	20h	ASCII Blank	n/a
	805D	1				20h	ASCII blank	
	805E	1	Read Only	7-0	CLEI Code	20h	ASCII blank	n/a
	805F	1				20h	ASCII blank	
	8060	1				20h	ASCII blank	
	8061	1				20h	ASCII blank	
	8062	1				20h	ASCII blank	
	8063	1				20h	ASCII blank	
	8064	1				20h	ASCII blank	
	8065	1				20h	ASCII blank	
	8066	1				20h	ASCII blank	
	8067	1				20h	ASCII Blank	
	8068	1	Read Only	7-0	CFP2 MSA HW Spec Rev	0Ah	Decimal Value = 10 [i.e., 10 * 0.1 rev = Revision 1.0]	n/a
	8069	1	Read Only	7-0	CFP MSA MIS Spec Rev	16h	Decimal Value = 22 [i.e., 22 * 0.1 rev = Revision 2.2]	n/a
	806A	2	Read Only	7-0	Module Hardware Revision			n/a
	806C	2	Read Only	7-0	Module Firmware Revision			n/a
	806E	1	Read Only	7-4	Reserved	0Ch	Reserved	n/a
				3	DDM Rx Opt PWR Monitor type		Rx Power measurement type (1b = Average Power)	
				2	DDM Tx Opt PWR Monitor type		Tx Power measurement type (1b = Average Power)	
				1-0	Reserved		Reserved	
	806F	1	Read Only	7-6	DDM Capability - AUX 2	03h	Auxiliary Monitor 2 (00b = Not Supported)	n/a
				5-4	DDM Capability - AUX 1		Auxiliary Monitor 1 (00b = Not Supported)	
				3	Reserved		Reserved	
				2	Transceiver SOA Bias Mon		Transceiver SOA Bias Current Monitor (0b = Not Supported)	
				1	Transceiver Vcc Monitor		Transceiver Vcc Voltage Monitor (1b = Supported)	
				0	Transceiver Temp Monitor		Transceiver Temperature Monitor (1b = Supported)	
	8070	1	Read Only	7-4	Reserved	0Eh	Reserved	n/a
				3	Network Lane Rx Opt PWR		Per Channel Rx Optical Power Monitor (1b = Supported)	
				2	Network Lane Tx BIAS		Per Channel Tx Laser Bias Monitor (1b = Supported)	
				1	Network Lane Tx Opt PWR		Per Channel Tx Optical Power Monitor (1b = Supported)	
				0	Network Lane Laser Temp		Per Channel Laser Temperature Monitor (0b = Not Supported)	

Block Name	Hex Addr	Size	Access Type	8 Bits	Register Name	Value	Description	LSB Unit
NVR 1 CFP	8071	1	Read Only	7	Host Lane Loop-back	B0h	Electrical Lane Tx,in to Rx,out Loopback (1b = Supported)	n/a
				6	Host Lane PRBS		Electrical Lane PRBS Generator (0b = Not Supported)	
				5	Host Lane EMPHASIS		Rx Output Emphasis Control (1b = Supported)	
				4	Network Lane Loop-back		Optical Lane Rx,in to Tx,out Loopback (1b = Supported)	
				3	Network Lane PRBS		Optical Lane Tx PRBS Generator (0b = Not Supported)	
				2	FEC Decision V threshold		FEC Decision Voltage Threshold (0b = not applicable)	
				1	FEC Decision Ph Threshold		FEC Decision Phase Threshold (0b = not applicable)	
				0	Unidirectional TXRX Modes		Uni-Directional Modes (0b = not applicable)	
	8072	1	Read Only	7-0	Maximum HIGH Power Up Time	03h	Decimal Value = 3 [i.e., 3 * 1 sec = 3 sec]	3 sec
	8073	1	Read Only	7-0	Maximum TX Turn On Time	03h	Decimal Value = 3 [i.e., 3 * 1 sec = 3 sec]	3 sec
	8074	1	Read Only	7-0	Host Lane Signal Specification	FFh	This is set to FFh and refer to address 81C7 for expanded capabilities. CPPI = 06h (CDR off) and CDRs on = 01h	n/a
	8075	1	Read Only	7-1	Reserved	00h	Reserved	n/a
				0	Heat Sink Type		Flat Top Heat Sink =0b.	
	8076	1	Read Only	7-0	Maximum TX Turn OFF Time	64h	Decimal Value = 100 [i.e., 100 * 1 ms = 100 ms]	1 ms
	8077	1	Read Only	7-0	Maximum HIGH Power DOWN Time	01h	Decimal Value = 1 [i.e., 1 * 1 sec = 1 sec]	1 sec
	8078	1	Read Only	7-6	Reserved	20h	Reserved	n/a
				5	Host lane EQ Control Function		1b = Supported	
				4	Active Decision Voltage/Phase Fnct		0b = Not supported	
				3	Rx FIFO Reset		0b = Not supported	
				2	Rx FIFO Auto Reset		0b = Not supported	
				1	Tx FIFO Reset		0b = Not supported	
				0	Tx FIFO Auto Reset		0b = Not supported	
	8079	1	Read Only	7	Tx MCLK Option 7	00h	0b = Not supported	n/a
				6	Tx MCLK Option 6		0b = Not supported	
				5	Tx MCLK Option 5		0b = Not supported	
				4	Tx MCLK Option 4		0b = Not supported	
				3	Reserved			
				2	Tx MCLK Option 2		0b = Not supported	
				1	Tx MCLK Option 1		0b = Not supported	
				0	Tx MCLK Monitor Option		0b = Not supported	
	807A	1	Read Only	7	Rx MCLK Option 7	00h	0b = Not supported	n/a
				6	Rx MCLK Option 6		0b = Not supported	
				5	Rx MCLK Option 5		0b = Not supported	
				4	Rx MCLK Option 4		0b = Not supported	
				3	Reserved			
				2	Rx MCLK Option 2		0b = Not supported	
				1	Rx MCLK Option 1		0b = Not supported	
				0	Rx MCLK Monitor Option		0b = Not supported	
	807B	1	Read Only	7-0	Module Firmware B Version	00h	Two address register format x.y with x at lower, y at higher.	n/a
	807C	1		7-0		00h		
	807D	1	Read Only	7-0	Max MDIO Ready Time	03h	3 sec = 03h. Max ready time due to software upgrade	03h
	807E	1	Read Only	7-6	Extended Power Class	20h	00b. Not needed. [See Address 8001 Bits 7-6 = 10b]	20h
				5	MDIO Port Address Scheme		1b = CFP2/CFP4 common MDIO port address scheme	
				4-0	Reserved			
	807F	1	Read Only	7-0	CFP NVR1 Checksum		CHECKSUM for 8000-807Eh inclusive	n/a

Block Name	Hex Addr	Size	Access Type	8 Bits	Register Name	Value	Description	LSB Unit
NVR 2 CFP	8080	2	Read Only	7-0	Module Temp High Alarm Threshold	4B00h	Module Temp High Alarm Threshold: 75 °C	1/256°
	8082	2	Read Only	7-0	Module Temp High Warning Threshold	4600h	Module Temp High Warning Threshold: 70 °C	
	8084	2	Read Only	7-0	Module Temp Low Warning Threshold	0000h	Module Temp Low Warning Threshold: 0 °C	
	8086	2	Read Only	7-0	Module Temp Low Alarm Threshold	FB00h	Module Temp Low Alarm Threshold: -5 °C	
	8088	2	Read Only	7-0	Module Vcc High Alarm Threshold	8DCCh	Module Vcc High Alarm Threshold: 3.63 V	0.1 mV
	808A	2	Read Only	7-0	Module Vcc High Warning Threshold	875Ah	Module Vcc High Warning Threshold: 3.465 V	
	808C	2	Read Only	7-0	Module Vcc Low Warning Threshold	7A75h	Module Vcc Low Warning Threshold: 3.315 V	
	808E	2	Read Only	7-0	Module Vcc Low Alarm Threshold	7404h	Module Vcc Low Alarm Threshold: 2.97 V	
	8090	2	Read Only	7-0	SOA threshold	00h	not supported	
	8092	2	Read Only	7-0	SOA threshold	00h	not supported	
	9094	2	Read Only	7-0	SOA threshold	00h	not supported	
	8096	2	Read Only	7-0	SOA threshold	00h	not supported	
	8098	2	Read Only	7-0	AUX1 threshold	00h	not supported	
	809A	2	Read Only	7-0	AUX1 threshold	00h	not supported	
	809C	2	Read Only	7-0	AUX1 threshold	00h	not supported	
	809E	2	Read Only	7-0	AUX1 threshold	00h	not supported	
	80A0	2	Read Only	7-0	AUX2 threshold	00h	not supported	
	80A2	2	Read Only	7-0	AUX2 threshold	00h	not supported	
	80A4	2	Read Only	7-0	AUX2 threshold	00h	not supported	
	80A6	2	Read Only	7-0	AUX2 threshold	00h	not supported	
	80A8	2	Read Only	7-0	Laser Bias High Alarm Threshold	1388h	Laser Bias High Alarm Threshold: 10 mA	2 µA
	80AA	2	Read Only	7-0	Laser Bias High Warning Threshold	128Eh	Laser Bias High Warning Threshold: 9.5 mA	
	80AC	2	Read Only	7-0	Laser Bias Low Warning Threshold	01F4h	Laser Bias Low Warning Threshold: 1 mA	
	80AE	2	Read Only	7-0	Laser Bias Low Alarm Threshold	00FAh	Laser Bias Low Alarm Threshold: 0.5 mA	
	80B0	2	Read Only	7-0	Laser PWR High Alarm Threshold	5575h	Laser PWR High Alarm Threshold: 3.4 dBm (Average Power)	0.1 µW
	80B2	2	Read Only	7-0	Laser PWR High Warning Threshold	43E2h	Laser PWR High Warning Threshold: 2.4 dBm (Average Power)	
	80B4	2	Read Only	7-0	Laser PWR Low Warning Threshold	06C9h	Laser PWR Low Warning Threshold: -7.6 dBm (Average Power)	
	80B6	2	Read Only	7-0	Laser PWR Low Alarm Threshold	0564h	Laser PWR Low Alarm Threshold: -8.6 dBm (Average Power)	
	80B8	2	Read Only	7-0	Laser Temp threshold	00h	not supported	
	80BA	2	Read Only	7-0	Laser Temp threshold	00h	not supported	
	80BC	2	Read Only	7-0	Laser Temp threshold	00h	not supported	
	80BE	2	Read Only	7-0	Laser Temp threshold	00h	not supported	
	80C0	2	Read Only	7-0	Receive PWR High Alarm Threshold	5575h	Receive PWR High Alarm Threshold: 3.4 dBm (Average Power)	0.1 µW
	80C2	2	Read Only	7-0	Receive PWR High Warning Threshold	43E2h	Receive PWR High Warning Threshold: 2.4 dBm (Average Power)	
	80C4	2	Read Only	7-0	Receive PWR Low Warning Threshold	0462h	Receive PWR Low Warning Threshold: -9.5 dBm (Average Power)	
	80C6	2	Read Only	7-0	Receive PWR Low Alarm Threshold	02C3h	Receive PWR Low Alarm Threshold: -11.5 dBm (Average Power)	

Block Name	Hex Addr	Size	Access Type	8 Bits	Register Name	Value	Description	LSB Unit
NVR 2 CFP	80C8	2	Read Only	7-0	Rx Laser Bias Current Alarm	00h	not supported	
	80CA	2	Read Only	7-0	Rx Laser Bias Current Warn	00h	not supported	
	80CC	2	Read Only	7-0	Rx Laser Bias Current Alarm	00h	not supported	
	80CE	2	Read Only	7-0	Rx Laser Bias Current Warn	00h	not supported	
	80DO	2	Read Only	7-0	Rx Laser Output Pwr Alarm	00h	not supported	
	80D2	2	Read Only	7-0	Rx Laser Output Pwr Warn	00h	not supported	
	80D4	2	Read Only	7-0	Rx Laser Output Pwr Alarm	00h	not supported	
	80D6	2	Read Only	7-0	Rx Laser Output Pwr Warn	00h	not supported	
	80D8	2	Read Only	7-0	Rx Laser Temperature Alarm	00h	not supported	
	80DA	2	Read Only	7-0	Rx Laser Temperature Warn	00h	not supported	
	80DC	2	Read Only	7-0	Rx Laser Temperature Alarm	00h	not supported	
	80DE	2	Read Only	7-0	Rx Laser Temperature Warn	00h	not supported	
	80EO	2	Read Only	7-0	Tx Modulator Bias Alarm	00h	not supported	
	80E2	2	Read Only	7-0	Tx Modulator Bias Warn	00h	not supported	
	80E4	2	Read Only	7-0	Tx Modulator Bias Alarm	00h	not supported	
	80E6	2	Read Only	7-0	Tx Modulator Bias Warn	00h	not supported	
	80E8	2	Read Only	7-0	Host RX Opt Pwr High Alarm	00h	not supported	
	80EA	2	Read Only	7-0	Host RX Opt Pwr High Warn	00h	not supported	
	80EC	2	Read Only	7-0	Host RX Opt Pwr Low Alarm	00h	not supported	
	80EE	2	Read Only	7-0	Host RX Opt Pwr Low Warn	00h	not supported	
	80F0	2	Read Only	7-0	Host RX Opt Pwr High Alarm	00h	not supported	
	80F2	2	Read Only	7-0	Host RX Opt Pwr High Warn	00h	not supported	
	80F4	2	Read Only	7-0	Host RX Opt Pwr Low Alarm	00h	not supported	
	80F6	2	Read Only	7-0	Host RX Opt Pwr Low Warn	00h	not supported	
	80F8	7	Read Only	7-0	Reserved	00h	not supported	
	80FF	1	Read Only	7-0	CFP NVR2 Checksum		CHECKSUM for 8080-80FEh inclusive	n/a

Block Name	Hex Addr	Size	Access Type	8 Bits	Register Name	Value	Description	LSB Unit
NVR 3 CFP	8100	32	Read Only	7-0	Rx Sensitivity Spec Network Lanes	00h	Not supported	0.01 dBm
	8120	32	Read Only	7-0	Tx Power Spec Network Lanes	00h	Not supported	0.01 dBm
	8140	32	Read Only	7-0	Measured ER Network Lanes	00h	Not supported	0.01 dB
	8160	32	Read Only	7-0	Path Penalty Network Lanes	00h	Not supported	0.01 dB

Block Name	Hex Addr	Size	Access Type	8 Bits	Register Name	Value	Description	LSB Unit
NVR 4 CFP	8180	1	Read Only	7-0	Checksum for NVR 3	00h	The 8-bit unsigned sum of all CFP NVR 3 contents from address 8100h through 817Fh, inclusive	
	8181	1	Read Only	7-0	Max MM OM4 fiber length	0Fh	Decimal Value = 15 [i.e., 15 x 10 m = 150 m max OM4 length] Max OM3 length is 100 m in register 800E.	10 m
	8182	2	Read Only	15-0	Extended Identifiers	0000h	Not supported	
	8184	2	Read Only	15-0	Extended Max Network Lane Rate	0000h	Not supported	
	8186	2	Read Only	15-0	Extended Max Power Consumption	0000h	Not supported	
	8188	2	Read Only	15-0	Extended Max Power Low Mode	0000h	Not supported	
	818A	2	Read Only	15-0	Tx/Rx Min Laser Frequency 1	0000h	Not supported	
	818C	2	Read Only	15-0	Tx/Rx Min Laser Frequency 2	0000h	Not supported	
	818E	2	Read Only	15-0	Tx/Rx Max Laser Frequency 1	0000h	Not supported	
	8190	2	Read Only	15-0	Tx/Rx Max Laser Frequency 2	0000h	Not supported	
	8192	2	Read Only	15-0	Rx Laser Fine Tune Freq Range	0000h	Not supported	
	8194	2	Read Only	15-0	Tx Laser Fine Tune Freq Range	0000h	Not supported	
	8196	2	Read Only	15-0	Laser Tuning Capabilities	0000h	Not supported	
	8198	8	Read Only	7-0	Reserved	00h	Not supported	
	81A0	8	Read Only	7-0	Network Lane n Vendor Specific	00h	Not supported	
	81A8	8	Read Only	7-0	Network Lane n Vendor Specific	00h	Not supported	
	81B0	8	Read Only	7-0	Network Lane n Vendor Specific	00h	Not supported	
	81B8	8	Read Only	7-0	Network Lane n Vendor Specific	00h	Not supported	
	81C0	6	Read Only	7-0	Reserved	00h	Not supported	
	81C6	1	Read Only	7-0	Host Lane Signal Mode Bit Map 1	00h	Not supported	
	81C7	1	Read Only	7	Host Lane Signal Mode Bit Map 0	41h	(0b bit 7) MLG1.0 not supported	
				6	[Reference Address 8074, A015]		(1b bit 6) CPPI Supported (Default, CDRs off)	
				5			(0b bit 5) CEI-28G-VSR not supported	
				4			(0b bit 4) CAUI-4f not supported	
				3			(0b bit 3) CAUI-4 not supported	
				2			(0b bit 2) SFI 5.2 not supported	
				1			(0b bit 1) XLAUI not supported	
				0			(1b bit 0) CAUI compatible supported (with CDRs on)	
	81C8	47	Read Only	7-0	Reserved	00h	Reserved	
	81FF	1	Read Only	7-0	CFP NVR 4 Checksum		The 8-bit unsigned sum of all CFP NVR 4 contents from address 8181h through 81FEh, inclusive	

Block Name	Hex Addr	Size	Access Type	8 Bits	Register Name	Value	Description	Initial Value
Reserved	8200-83FF	512	Read Only	7-0	Reserved			0000h

Block Name	Hex Addr	Size	Access Type	8 Bits	Register Name	Value	Description	Initial Value
Vendor NVR1	8400-847F	128	Mixed	7-0	Vendor NVR 1. Vendor Data Registers			0000h
Vendor NVR2	8480-84FF	128	Mixed	7-0	Vendor NVR 2. Vendor Data Registers			0000h

Vendor NVR 1 and Vendor NVR 2 tables are allocated for storing additional data that can be used by the vendor. These are non-volatile fields. These fields can only be read it if the vendor password has been inputted. Default vendor password is defined in the MSA. The user cannot write to these registers even with a vendor password (hardcoded at the factory).

Block Name	Hex Addr	Size	Access Type	8 Bits	Register Name	Value	Description	Initial Value
Reserved	8500-87FF	768	Read Only	7-0	Reserved			0000h

Block Name	Hex Addr	Size	Access Type	8 Bits	Register Name	Value	Description	Initial Value
User NVR1	8800-887F	128	Mixed	7-0	User NVR 1. User Data Registers			0000h
User NVR2	8880-88FF	128	Mixed	7-0	User NVR 2. User Data Registers			0000h

The User NVR 1 and User NVR 2 tables are allocated for module user to store data. User has the full read/write access to these tables. These registers are password accessible. Without an appropriate password, a read attempt shall return FFh.
Read – only with password, returns FFFF if no password given.
Write – only with same password. Once values have been written to these fields they are stored as non-volatile bytes.

Block Name	Hex Addr	Size	Access Type	8 Bits	Register Name	Value	Description	Initial Value
Reserved	8900-9FFF	5888	Read Only	7-0	Reserved			0000h

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 CFP	A000	2	Write Only	15-0	Password Entry	Password for module registers access control. Two word value. MSW is in the higher address. Reading these returns FFFFh. Password allows Non-Volatile Writes to 8800 [128 Bytes User Data Registers NVR1] 8880 [128 Bytes User Data Registers NVR2] AC00 [1024 Bytes Common Data Block] Upon inputting the correct Password, the user has the full read/write access to these registers. MSA specifies the default user password value as 0101 1100h. This unlocks the User NVR1, User NVR2 and CDB pages on in register 8800h, 8880h and AC00h. Vendor NVR1 and 2 has a different password than the User NVR; it is 8101 1100h. Entering the password provides read-only access to the Vendor NVR1 and Vendor NVR2 pages only in Registers 8400h and 8480h.	0000h 0000h
	A002-A003	2	Write Only	15-0	Password Change	New password entry. Two word value. MSW is in the lower address. Reading these returns FFFFh. The user password can be changed by writing the new value to the Password Change registers A002h and A003h after a password entry is successful. The new password value shall be stored and take effect only after writing the Save User Password command to register A004h.	0000h 0000h
	A004	1	Read Write	15-9	Reserved	Not Supported.	0000h
			Read Only	8-6	Reserved		
			Read Write	5	User Restore & Save Command	0= Restore User NVR Section, 1=Save User NVR Section See MSA section 4.10.2 "User NVR Restore and Save Functions" for proper operation	
			Read Only	4	Reserved		
			Read Only	3-2	Command Status	00b = Idle, 01b = Successful, 10b= In progress, 11 = Failed. See MSA section 4.10.2 "User NVR Restore and Save Functions" for proper operation	
			Read Write	1-0	Extended Commands	00b = No effect. 11b = Restore/Save User NVRs See MSA section 4.10.2 "User NVR Restore and Save Functions" for proper operation	

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 CFP	A005	1	Read Only	15-8	Reserved		0000h
			Read Write	7-0	PRG_CNTL3 Function Select	7:0 RW This multi-function input is used as HW_IL_MSB during the Initialize State and it can be programmed to other functions afterward. = 0: Assert/De-Assert of PRG_CNTL3 has no effect, = 1: Assign TRXIC_RSTn function to hardware pins PRG_CNTL3. When so assigned this pin uses the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, its soft counterpart Soft PRG_CNTL3 Control (A010h.12) uses an active high logic, that is, 1 = Assert (Reset). = 2-255: Reserved.	
	A006	1	Read Only	15-8	Reserved		0000h
			Read Write	7-0	PRG_CNTL2 Function Select	= 0: Assert/De-Assert of PRG_CNTL2 has no effect, = 1: Assign TRXIC_RSTn function to hardware pins PRG_CNTL2. When so assigned this pin uses the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, its soft counterpart Soft PRG_CNTL2 Control (A010h.12) uses an active high logic, that is, 1 = Assert (Reset). = 2-255: Reserved.	
	A007	1	Read Only	15-8	Reserved		0001h
			Read Write	7-0	PRG_CNTL1 Function Select	TRXIC_RSTn is the CFP MSA default function for PRG_CNTL1. = 0: Assert/De-Assert of PRG_CNTL1 has no effect, = 1: Assign TRXIC_RSTn function to hardware pins PRG_CNTL1. When so assigned this pin uses the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, its soft counterpart Soft PRG_CNTL1 Control (A010h.12) uses an active high logic, that is, 1 = Assert (Reset). = 2-255: Reserved.	
	A008	1	Read Only	15-8	Reserved		0003h
			Read Write	7-0	PRG_ALRM3 Function Source	7-0 Alarm Source Code PRG_ALRM3; Selects, and assigns, an alarm source for PRG_ALRM3 PRG_ALRM3 MSA default = MOD_FAULT Fault State = 0: Not active, always de-asserted, [NOT SUPPORTED] = 1: HIPWR_ON, [SUPPORTED] = 2: Ready State, [SUPPORTED] = 3: Fault State, MSA default setting, [SUPPORTED] = 4: RX_ALRM = RX_LOS + RX_NETWORK_LOL, [SUPPORTED WHEN CDR IS ENABLED] = 5: TX_ALRM = TX_HOST_LOL [SUPPORTED WHEN CDR IS ENABLED] = 6: RX_NETWORK_LOL, [SUPPORTED WHEN CDR IS ENABLED] = 7: TX_LOSF, [NOT SUPPORTED] = 8: TX_HOST_LOL, [SUPPORTED WHEN CDR IS ENABLED] = 9: OOA, Out of alignment, [NOT SUPPORTED]	

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 CFP	A009	1	Read Only	15-8	Reserved		0002h
			Read Write	7-0	PRG_ALRM2 Function Source	7:0 Alarm Source Code PRG_ALRM2; Selects, and assigns, an alarm source for PRG_ALRM2 PRG_ALRM2 MSA default = MOD_READY, Ready State (startup sequence done), = 0: Not active, always de-asserted,[NOT SUPPORTED] = 1: HIPWR_ON,[SUPPORTED] = 2: Ready State,[SUPPORTED] = 3: Fault State, MSA default setting,[SUPPORTED] = 4: RX_ALRM = RX_LOS + RX_NETWORK_LOL, [SUPPORTED WHEN CDR IS ENABLED] = 5: TX_ALRM = TX_HOST_LOL + TX_CMU_LOL, [SUPPORTED WHEN CDR IS ENABLED] = 6: RX_NETWORK_LOL, [SUPPORTED WHEN CDR IS ENABLED] = 7: TX_LOSF, [NOT SUPPORTED] = 8: TX_HOST_LOL, [SUPPORTED WHEN CDR IS ENABLED] = 9: OOA, Out of alignment, [NOT SUPPORTED]	
	A00A	1	Read Only	15-8	Reserved		0001h
			Read Write	7-0	PRG_ALRM1 Function Source	7:0 Alarm Source Code PRG_ALRM1; Selects, and assigns, an alarm source for PRG_ALRM1 PRG_ALRM1 MSA default = HIPWR_ON Module high-power-on indicator. = 0: Not active, always de-asserted, [NOT SUPPORTED] = 1: HIPWR_ON, [SUPPORTED] = 2: Ready State, [SUPPORTED] = 3: Fault State, MSA default setting, [SUPPORTED] = 4: RX_ALRM = RX_LOS + RX_NETWORK_LOL, [SUPPORTED WHEN CDR IS ENABLED] = 5: TX_ALRM = TX_HOST_LOL, [SUPPORTED WHEN CDR IS ENABLED] = 6: RX_NETWORK_LOL, [SUPPORTED WHEN CDR IS ENABLED] = 7: TX_LOSF, [NOT SUPPORTED] = 8: TX_HOST_LOL, [SUPPORTED WHEN CDR IS ENABLED] = 9: OOA, Out of alignment, [NOT SUPPORTED]	
	A00B	1	Read Only	15-3	Reserved		0000h
			Read Write	2-0	Bi-Directional Mode Select	Not supported.	
	A00C-A00F	4	Read Only	7-0	Reserved		0000h

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 CFP	A010	1	Read Write	15	Soft MOD_RST control	1= Assert (similar to pin 28)	0000h
				14	Soft MOD_LO_PWR control	1= Assert (similar to pin 26)	
				13	Soft Tx DIS Control (Global)	1= Assert (similar to pin 24)	
				12	Soft PRG_CNTL3 Control	Register bit for PRG_CNTL3 control function. 1: Assert	
				11	Soft PRG_CNTL2 Control	Register bit for PRG_CNTL2 control function. 1: Assert.	
				10	Soft PRG_CNTL1 Control	Register bit for PRG_CNTL1 control function. 1: Assert.	
				9	Soft GLB_ALRM Test	1=Assert to Generate a GLB_ALRM signal on the pin 29	
			Read Only	8-6	Reserved		
				5	Tx_DIS Pin Status (Global)	Echoes pin 24 (Transmit Disable)	
				4	MOD_LO_PWR Pin Status	Echoes pin 26 (Module Low Power Mode)	
				3	Soft PRG_CNTL3 Pin Status	Logical state of the PRG_CNTL3 pin. 1: Assert.	
				2	Soft PRG_CNTL2 Pin Status	Logical state of the PRG_CNTL2 pin. 1: Assert.	
				1	Soft PRG_CNTL1 Pin Status	Logical state of the PRG_CNTL1 pin. 1: Assert.	
				0	Reserved		
	A011	1	Read Only	15	Reserved		0000h
			Read Write	14	TX PRBS Generator Enable	Not supported	
				12-13	Tx PRBS Pattern Select	Not supported	
				11	Tx DeSkew Enable	Not supported	
				10	Tx FIFO Reset	Not supported	
				9	TX FIFO Auto Reset	Not supported	
				8	Tx Reset	Not supported	
				7-5	TX Module MCLK Control	Not supported	
			Read Only	4	Reserved		
			Read Write	3-1	TX Rate Select	Not supported	
				0	TX REF CLK Rate Select	Not supported	
	A012	1	Read Write	15	Active Decision Voltage/Phase Control	Not supported	0000h
				14	RX PRBS Checker Enable	Not supported	
				13-12	Rx PRBS Pattern Select	Not supported	
				11	Rx Lock RX Module CLK to REF CLK	Not supported	
				10	Network Lane Loopback (OWRAP)	0 = Normal Operation, 1 = Network lane OLoop/OWRAP Enable	
				9	RX FIFO Auto Reset	Not supported	
				8	Rx Reset	Not supported.	
				7-5	RX Module MCLK Control	Not supported	
				4	Rx FIFO Reset	Not supported	
				3-1	RX Rate Select (Host side)	Not supported	
				0	RX REF CLK Rate Select	Not supported	

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 CFP	A013	1	Read Write	15	Tx_Disable Lane 15 (Network Lane)	Not supported	0000h
				14	Tx_Disable Lane 14 (Network Lane)	Not supported	
				13	Tx_Disable Lane 13 (Network Lane)	Not supported	
				12	Tx_Disable Lane 12 (Network Lane)	Not supported	
				11	Tx_Disable Lane 11 (Network Lane)	Not supported	
				10	Tx_Disable Lane 10 (Network Lane)	0 = Laser Enabled, 1 = Laser Disabled (Laser turned OFF)	
				9	Tx_Disable Lane 9 (Network Lane)	0 = Laser Enabled, 1 = Laser Disabled (Laser turned OFF)	
				8	Tx_Disable Lane 8 (Network Lane)	0 = Laser Enabled, 1 = Laser Disabled (Laser turned OFF)	
				7	Tx_Disable Lane 7 (Network Lane)	0 = Laser Enabled, 1 = Laser Disabled (Laser turned OFF)	
				6	Tx_Disable Lane 6 (Network Lane)	0 = Laser Enabled, 1 = Laser Disabled (Laser turned OFF)	
				5	Tx_Disable Lane 5 (Network Lane)	0 = Laser Enabled, 1 = Laser Disabled (Laser turned OFF)	
				4	Tx_Disable Lane 4 (Network Lane)	0 = Laser Enabled, 1 = Laser Disabled (Laser turned OFF)	
				3	Tx_Disable Lane 3 (Network Lane)	0 = Laser Enabled, 1 = Laser Disabled (Laser turned OFF)	
				2	Tx_Disable Lane 2 (Network Lane)	0 = Laser Enabled, 1 = Laser Disabled (Laser turned OFF)	
				1	Tx_Disable Lane 1 (Network Lane)	0 = Laser Enabled, 1 = Laser Disabled (Laser turned OFF)	
				0	Tx_Disable Lane 0 (Network Lane)	0 = Laser Enabled, 1 = Laser Disabled (Laser turned OFF)	
	A014	1	Read Only	15	Reserved		0000h
			Read Write	14	Tx PRBS Checker Enable	Not supported	
				13	Tx PRBS Pattern 2	Not supported	
				12	Tx PRBS Pattern 1	Not supported	
				11	Tx PRBS Pattern 0	Not supported	
				10	Host Lane Loop-back enable (EWRAP)	0 = Normal Operation, 1 = Host lane ELoop/EWRAP Enable	
			Read Only	9-8	Reserved		
			Read Write	7	Rx PRBS Generator Enable	Not supported	
				6	Rx PRBS Pattern 2	Not supported	
				5	Rx PRBS Pattern 1	Not supported	
				4	Rx PRBS Pattern 0	Not supported	
			Read Only	3-0	Reserved		
	A015	1	Read Write	15	Enable Tx Network PRBS Modes	Not supported	0009h
				14	Enable Rx Network PRBS Modes	Not supported	
				13-12	MCLK Selection (CFP4)	Not supported	
				11	Tx Lane Offset Enable	Not supported	
				10	Rx Lane Offset Enable	Not supported	
				9	Rx PWR Monitor A/W Threshold Select	Not supported	
				8	Rx_Los Monitor A/W Threshold Select	Set to '1' which is programmable threshold. Host compares Rx A/D input OMA in register A2D0 (channel 0) to A2D9 (channel 9) with threshold values in A03C, A03D, A03E and A03F to generate Rx A/W. Values in these register is user programable and shall be in the range defined in Table 1 (Permissible Range for Host-Configured Receive Optical Power Threshold)	
				7-0	Electrical Interface Format Select [Reference Address 8074, 81C7]	01h = CDRs on 09h = CPPI (Default, CDRs off)	

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 CFP	A016	1	Read Only	15-9	Reserved		0000h
				8	High Power Down State	Transient. Not supported.	
				7	TX Turn Off State	Transient. Not supported	
				6	FAULT State (MOD_FAULT)	0b = No Fault. 1b = FAULT	
				5	READY State (MOD_READY)	0b = Not Ready. 1b = MODULE READY Realtime indicator. Module Fault can be caused by a Vcc Fault on internal indicator	
				4	TX Turn Off State	Transient. Not supported.	
				3	TX Off State	0b = Tx ON. 1b = Tx OFF (ie. Transmitters Disabled)	
				2	High Power Up State	Transient. Not supported.	
				1	Low Power State	0b = Full Operation. 1b = Low Power State Enabled	
				0	Initialize State.	Transient. Not supported.	
	A017	1	Read Only	15-0	Reserved		0000h
	A018	1	Read Only	15	GLB_ALRM Assertion Status	Echoes pin 29	0000h
				14	Host Lane FAULT/STATUS summary	Not supported	
				13	Network Lane FAULT/STATUS summary	Logic OR: Tx Opt OUT and Rx Opt IN Stages	
				12	Network Lane ALARM/WARNING Summary	Logic OR: Tx Opt OUT and Rx Opt IN Flags	
				11	Module ALARM/WARNING "2" Summary	Logic OR: All Alarm and Warning "2" Flags	
				10	Module ALARM/WARNING "1" Summary	Logic OR: All Alarm and Warning "1" Flags	
				9	Module FAULT Summary	Logic OR: All enabled inputs to Module FAULT	
				8	Module GENERAL STATUS summary	Logic OR: All enabled inputs to Module GEN STATUS	
				7	Module STATE summary	Logic OR: All enabled inputs to Module STATE	
				6-5	Reserved		
				4	CDB Command Completed	Logic OR: CDB status, complete successful or failed	
				3	Vendor Specific FAWS	Logic OR: All enable vendor specific FAWS	
				2-1	Reserved		
				0	Soft GLM_ALRM Test Status	Software GLB_ALRM Test bit Status	

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 CFP	A019	1	Read Only	15	Lane 15 Alarm & Warning Summary	Not supported	0000h
				14	Lane 14 Alarm & Warning Summary	Not supported	
				13	Lane 13 Alarm & Warning Summary	Not supported	
				12	Lane 12 Alarm & Warning Summary	Not supported	
				11	Lane 11 Alarm & Warning Summary	Not supported	
				10	Lane 10 Alarm & Warning Summary	Logic OR of enabled bits of Network Lane Alarms/Warnings	
				9	Lane 9 Alarm & Warning Summary	Logic OR of enabled bits of Network Lane Alarms/Warnings	
				8	Lane 8 Alarm & Warning Summary	Logic OR of enabled bits of Network Lane Alarms/Warnings	
				7	Lane 7 Alarm & Warning Summary	Logic OR of enabled bits of Network Lane Alarms/Warnings	
				6	Lane 6 Alarm & Warning Summary	Logic OR of enabled bits of Network Lane Alarms/Warnings	
				5	Lane 5 Alarm & Warning Summary	Logic OR of enabled bits of Network Lane Alarms/Warnings	
				4	Lane 4 Alarm & Warning Summary	Logic OR of enabled bits of Network Lane Alarms/Warnings	
				3	Lane 3 Alarm & Warning Summary	Logic OR of enabled bits of Network Lane Alarms/Warnings	
				2	Lane 2 Alarm & Warning Summary	Logic OR of enabled bits of Network Lane Alarms/Warnings	
				1	Lane 1 Alarm & Warning Summary	Logic OR of enabled bits of Network Lane Alarms/Warnings	
				0	Lane 0 Alarm & Warning Summary	Logic OR of enabled bits of Network Lane Alarms/Warnings	

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 CFP	A01A	1	Read Only	15	Lane 15 Network Lane FAULT & STATUS	Not supported	0000h
				14	Lane 14 Network Lane FAULT & STATUS	Not supported	
				13	Lane 13 Network Lane FAULT & STATUS	Not supported	
				12	Lane 12 Network Lane FAULT & STATUS	Not supported	
				11	Lane 11 Network Lane FAULT & STATUS	Not supported	
				10	Lane 10 Network Lane FAULT & STATUS	Logic OR of enabled bits of Network Lane FAULT & STATUS	
				9	Lane 9 Network Lane FAULT & STATUS	Logic OR of enabled bits of Network Lane FAULT & STATUS	
				8	Lane 8 Network Lane FAULT & STATUS	Logic OR of enabled bits of Network Lane FAULT & STATUS	
				7	Lane 7 Network Lane FAULT & STATUS	Logic OR of enabled bits of Network Lane FAULT & STATUS	
				6	Lane 6 Network Lane FAULT & STATUS	Logic OR of enabled bits of Network Lane FAULT & STATUS	
				5	Lane 5 Network Lane FAULT & STATUS	Logic OR of enabled bits of Network Lane FAULT & STATUS	
				4	Lane 4 Network Lane FAULT & STATUS	Logic OR of enabled bits of Network Lane FAULT & STATUS	
				3	Lane 3 Network Lane FAULT & STATUS	Logic OR of enabled bits of Network Lane FAULT & STATUS	
				2	Lane 2 Network Lane FAULT & STATUS	Logic OR of enabled bits of Network Lane FAULT & STATUS	
				1	Lane 1 Network Lane FAULT & STATUS	Logic OR of enabled bits of Network Lane FAULT & STATUS	
				0	Lane 0 Network Lane FAULT & STATUS	Logic OR of enabled bits of Network Lane FAULT & STATUS	
	A01B	1	Read Only	15	Lane 15 Host Lane FAULT & STATUS	Not supported	0000h
				14	Lane 14 Host Lane FAULT & STATUS	Not supported	
				13	Lane 13 Host Lane FAULT & STATUS	Not supported	
				12	Lane 12 Host Lane FAULT & STATUS	Not supported	
				11	Lane 11 Host Lane FAULT & STATUS	Not supported	
				10	Lane 10 Host Lane FAULT & STATUS	Not supported	
				9	Lane 9 Host Lane FAULT & STATUS	Not supported	
				8	Lane 8 Host Lane FAULT & STATUS	Not supported	
				7	Lane 7 Host Lane FAULT & STATUS	Not supported	
				6	Lane 6 Host Lane FAULT & STATUS	Not supported	
				5	Lane 5 Host Lane FAULT & STATUS	Not supported	
				4	Lane 4 Host Lane FAULT & STATUS	Not supported	
				3	Lane 3 Host Lane FAULT & STATUS	Not supported	
				2	Lane 2 Host Lane FAULT & STATUS	Not supported	
				1	Lane 1 Host Lane FAULT & STATUS	Not supported	
				0	Lane 0 Host Lane FAULT & STATUS	Not supported	
	A01C	1	Read Only	15-0	Reserved		0000h
	A01D	1	Read Only	15-14	Reserved		0000h
				13	HW_Interlock Status	0 = Safe to use Module, 1= Hotter than System Cooling	
				12-11	Reserved		
				10	LOSS of REF_CLK Input Alarm	Not supported	
				9	TX_JITTER_PLL_LOL Alarm	Not supported	
				8	TX_CMU_LOL Alarm	Not supported	
				7	TX_LOSF Alarm	Not supported	
				6	TX_HOST_LOL Alarm	Supported, only when CDR is enabled	
				5	RX_LOS Alarm	0 = Normal, 1 = RxLOS Logic OR all Network Lane RX LOS	
				4	RX_NETWORK_LOL Alarm	Supported, only when CDR is enabled	
				3	Out of Alignment Alarm (Host Lane Skew)	Not supported	
				2	Reserved		
				1	HI_PWR_ON Status	0= Lower Power Mode, 1= Module in HI PWR MODE	
				0	Reserved		

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 CFP	A01E	1	Read Only	15-7	Reserved		0000h
				6	PLD or FLASH Initialization FAULT Alarm	Not supported	
				5	Power Supply FAULT Alarm	0=Normal, 1= Asserted: Internal power regulators declares fault status	
				4-2	Reserved		
				1	CFP Checksum FAULT Alarm	0 =Normal, 1 = Asserted	
				0	Reserved		
	A01F		Read Only	15-12	Reserved		0000h
				11	Module Temperature HIGH Alarm	0 =Normal, 1 = Asserted	
				10	Module Temperature HIGH Warning	0 =Normal, 1 = Asserted	
				9	Module Temperature LOW Warning	0 =Normal, 1 = Asserted	
				8	Module Temperature LOW Alarm	0 =Normal, 1 = Asserted	
				7	Module Vcc HIGH Alarm	0 =Normal, 1 = Asserted	
				6	Module Vcc HIGH Warning	0 =Normal, 1 = Asserted	
				5	Module Vcc LOW Warning	0 =Normal, 1 = Asserted	
				4	Module Vcc LOW Alarm	0 =Normal, 1 = Asserted	
				3	Module SOA HIGH Alarm	Not supported	
				2	Module SOA HIGH Warning	Not supported	
				1	Module SOA LOW Warning	Not supported	
				0	Module SOA LOW Alarm	Not Supported	
	A020		Read Only	15-8	Reserved		0000h
				7	Module AUX1 HIGH Alarm	Not supported	
				6	Module AUX1 HIGH Warning	Not supported	
				5	Module AUX1 LOW Warning	Not supported	
				4	Module AUX1 LOW Alarm	Not Supported	
				3	Module AUX2 HIGH Alarm	Not supported	
				2	Module AUX2 HIGH Warning	Not supported	
				1	Module AUX2 LOW Warning	Not supported	
				0	Module AUX2 LOW Alarm	Not Supported	
	A021	1	Read Only	15-0	Reserved		0000h
	A022	1	Read/COR	15-9	Reserved		0000h
				8	HI_PWR_DOWN Status latched	Transient. Not supported.	
				7	TX_TURN_OFF Status latched	Transient. Not supported	
				6	FAULT Status latched	0b = No Fault. 1b = FAULT	
				5	READY Status latched	0b = Not Ready. 1b = MODULE READY	
				4	TX_TURN_ON Status Latched	Transient. Not supported.	
				3	TX_OFF Status Latched	0b = Tx ON. 1b = Tx OFF (ie. Transmitters Disabled)	
				2	HI_PWR_UP Status Latched	Transient. Not supported.	
				1	LOW PWR Status latched	0b = Full Operation. 1b = Low Power State Enabled	
				0	Initialize Status latched	Transient. Not supported.	

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 CFP	A023	1	Read/COR	15-14	Reserved		0000h
				13	HW_Interlock Status latched	0 = Safe to use Module, 1= Hotter than System Cooling	
				12-11	Reserved		
				10	LOSS of REF_CLK Alarm latched	Not supported	
				9	TX_JITTER_PLL_LOL Alarm latched	Not supported	
				8	TX_CMU_LOL Alarm latched	Not supported	
				7	TX_LOSF Alarm latched	Not supported	
				6	TX_HOST_LOL Alarm latched	Supported, only when CDR is enabled	
				5	RX_LOS Alarm latched	0 = Normal, 1 = Latched. Note: Set to 1 on any change (0->1 or 1->0) of RxLOS	
				4	RX_NETWORK_LOL Alarm latched	Supported, only when CDR is enabled	
				3	Out of Alignment Alarm (Host Skew) latched	Not supported	
				2-0	Reserved		
	A024	1	Read/COR	15-7	Reserved		0000h
				6	PLD or FLASH Init FAULT Alarm latched	Not supported	
				5	Power Supply FAULT Alarm Latched	0=Normal, 1= Asserted: Logic OR of V_{CC} Alarm High & Low	
				4-2	Reserved		
				1	CFP Checksum FAULT Alarm Latched	0 =Normal, 1 = Asserted	
				0	Reserved		
	A025		Read/COR	15-12	Reserved		0000h
				11	Module Temperature HIGH Alarm Latched	0 =Normal, 1 = Asserted	
				10	Module Temperature HIGH Warning Latched	0 =Normal, 1 = Asserted	
				9	Module Temperature LOW Warning Latched	0 =Normal, 1 = Asserted	
				8	Module Temperature LOW Alarm Latched	0 =Normal, 1 = Asserted	
				7	Module Vcc HIGH Alarm Latched	0 =Normal, 1 = Asserted	
				6	Module Vcc HIGH Warning Latched	0 =Normal, 1 = Asserted	
				5	Module Vcc LOW Warning Latched	0 =Normal, 1 = Asserted	
				4	Module Vcc LOW Alarm Latched	0 =Normal, 1 = Asserted	
				3	Module SOA HIGH Alarm Latched	Not supported	
				2	Module SOA HIGH Warning Latched	Not supported	
				1	Module SOA LOW Warning Latched	Not supported	
				0	Module SOA LOW Alarm Latched	Not Supported	
	A026		Read/COR	15-8	Reserved		0000h
				7	Module AUX1 HIGH Alarm Latched	Not supported	
				6	Module AUX1 HIGH Warning Latched	Not supported	
				5	Module AUX1 LOW Warning Latched	Not supported	
				4	Module AUX1 LOW Alarm Latched	Not Supported	
				3	Module AUX2 HIGH Alarm Latched	Not supported	
				2	Module AUX2 HIGH Warning Latched	Not supported	
				1	Module AUX2 LOW Warning Latched	Not supported	
				0	Module AUX2 LOW Alarm Latched	Not Supported	
	A027	1	Read/COR	15-0	Optional Vendor Specific FAWS Latch	Not Supported	0000h

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 CFP	A028	1	Read Only	15-9	Reserved		006Ah
			Read Write	8	HI_PWR_DOWN (enable to GLB_ALRM)	Transient. Not supported.	
				7	TX_TURN_OFF (enable to GLB_ALRM)	Transient. Not supported	
				6	FAULT enable (enable to GLB_ALRM)	0b = No Fault. 1b = FAULT	
				5	READY enable (enable to GLB_ALRM)	0b = Not Ready. 1b = MODULE READY	
				4	TX_TURN_ON (enable to GLB_ALRM)	Transient. Not supported.	
				3	FAULT enable (enable to GLB_ALRM)	0b = No Fault. 1b = FAULT	
				2	HI_PWR_UP (enable to GLB_ALRM)	Transient. Not supported.	
				1	LO_PWR enable (enable to GLB_ALRM)	0b = Full Operation. 1b = Low Power State Enabled	
				0	Initialize enable (enable to GLB_ALRM)	Transient. Not supported.	
	A029	1	Read Write	15	GLB_ALRM Master Enable	0=disable, 1=enable	A020h
			Read Only	14	Reserved		
			Read Write	13	HW_Interlock Enable to GLB_ALRM	0=disable, 1=enable	
			Read Only	12-11	Reserved		
			Read Write	10	LOSS of REF_CLK (enable to GLB_ALRM)	Not supported	
				9	TX_JITTER_PLL_LOL (enable GLB_ALRM)	Not supported	
				8	TX_CMU_LOL Alarm (enable GLB_ALRM)	Not supported	
				7	TX_LOSF Alarm (enable to GLB_ALRM)	Not supported	
				6	TX_HOST_LOL Alarm (enable GLB_ALRM)	Supported, only when CDR is enabled	
				5	RX_LOS (enable to GLB_ALRM)	0=disable, 1=enable	
				4	RX_NETWORK_LOL A (enable GLB_ALRM)	Supported, only when CDR is enabled	
				3	Out of Alignment (enable to GLB_ALRM)	Not supported	
			Read Only	0-2	Reserved		
	A02A	1	Read Only	15-7	Reserved		0022h
			Read Write	6	PLD FLASH Init FAULT (enable GLB_ALRM)	Not supported	
				5	Power Supply FAULT (enable GLB_ALRM)	0=disable, 1=enable	
			Read Only	4-2	Reserved		
			Read Write	1	CFP Checksum FAULT (enable GLB_ALRM)	0=disable, 1=enable	
			Read Only	0	Reserved		
	A02B	1	Read Only	15-12	Reserved		0FF0h
				11	Module Temp HIGH Alarm (enable to GLB_ALRM)	0=disable, 1=enable	
				10	Module Temp HIGH Warning (enable to GLB_ALRM)	0=disable, 1=enable	
				9	Module Temp LOW Warning (enable to GLB_ALRM)	0=disable, 1=enable	
				8	Module Temp LOW Alarm (enable to GLB_ALRM)	0=disable, 1=enable	
				7	Module Vcc HIGH Alarm (enable to GLB_ALRM)	0=disable, 1=enable	
				6	Module Vcc HIGH Warning (enable to GLB_ALRM)	0=disable, 1=enable	
				5	Module Vcc LOW Warning (enable to GLB_ALRM)	0=disable, 1=enable	
				4	Module Vcc LOW Alarm (enable to GLB_ALRM)	0=disable, 1=enable	
				3	Module SOA HIGH Alarm (enable to GLB_ALRM)	Not supported	
				2	Module SOA HIGH Warning (enable to GLB_ALRM)	Not supported	
				1	Module SOA LOW Warning (enable to GLB_ALRM)	Not supported	
				0	Module SOA LOW Alarm (enable to GLB_ALRM)	Not Supported	
	A02C	1	Read Only	15-8	Reserved		0000h
				7	Module AUX1 HIGH Alarm (enable to GLB_ALRM)	Not supported	
				6	Module AUX1 HIGH Warning (enable to GLB_ALRM)	Not supported	
				5	Module AUX1 LOW Warning (enable to GLB_ALRM)	Not supported	
				4	Module AUX1 LOW Alarm (enable to GLB_ALRM)	Not Supported	
				3	Module AUX2 HIGH Alarm (enable to GLB_ALRM)	Not supported	
				2	Module AUX2 HIGH Warning (enable to GLB_ALRM)	Not supported	
				1	Module AUX2 LOW Warning (enable to GLB_ALRM)	Not supported	
				0	Module AUX2 LOW Alarm (enable to GLB_ALRM)	Not Supported	

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 CFP	A02D	1	Read Write	15-0	Optional Vendor Specific FAWS Enable	Not Supported	0000h
	A02E	1	Read Only	15-0	Reserved		0000h
	A02F	1	Read Only	15-0	Module Temperature Monitor A/D Value	Range -40/125 °C. Accuracy ± 3 °C. Resolution 1/256 °C.	0000h
	A030	1	Read Only	15-0	Module VCC Monitor A/D Value	Range 0 to 6.55 V. Accuracy ± 3%. Resolution 0.1 mV.	0000h
	A031	1	Read Only	15-0	Module SOA Bias Current A/D Value	Not supported	0000h
	A032	1	Read Only	15-0	Module AUX1 Monitor A/D Value	Not supported	0000h
	A033	1	Read Only	15-0	Module AUX2 Monitor A/D Value	Not supported	0000h
	A034	4	Read Only	15-0	Reserved		00h
	A038	1	Read Only	15-10	Network Lane PRBS Data Count Exponent	Not supported	0000h
				0-9	Network Lane PRBS Data Count Mantissa	Not supported	
	A039	1	Read Only	15-10	Host Lane PRBS Data Count Exponent	Not supported	0000h
				0-9	Host Lane PRBS Data Count Mantissa	Not supported	
	A03A	70	Read Only	15-0	Reserved		0000h
	A03C	1	Read Write	15-0	Host Configured Rx Opt Power Hi Alarm Thresh	Supported	0000h
	A03D	1	Read Write	15-0	Host Configured Rx Opt Power Hi Warn Thresh	Supported	0000h
	A03E	1	Read Write	15-0	Host Configured Rx Opt Power Lo Alarm Thresh	Supported	0000h
	A03F	1	Read Write	15-0	Host Configured Rx Opt Power Lo Warn Thresh	Supported	0000h
	A040	64	Read Only	7-0	Reserved	Not supported	00h

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 MLG	A080 - A0FF	128	Mixed		MLG Volatile Registers	MLG Not supported	0000h

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 Network Lanes	A200	1	Read Only	15	Lane 0: Laser Bias High Alarm Flag	0 = Normal, 1 = Flag Asserted	00h
				14	Lane 0: Laser Bias High Warning Flag	0 = Normal, 1 = Flag Asserted	
				13	Lane 0: Laser Bias Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				12	Lane 0: Laser Bias Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
				11	Lane 0: Laser PWR High Alarm Flag	0 = Normal, 1 = Flag Asserted	
				10	Lane 0: Laser PWR High Warning Flag	0 = Normal, 1 = Flag Asserted	
				9	Lane 0: Laser PWR Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				8	Lane 0: Laser PWR Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
				7	Lane 0: Laser Temp High Alarm Flag	Not supported	
				6	Lane 0: Laser Temp High Warning Flag	Not supported	
				5	Lane 0: Laser Temp Low Warning Flag	Not supported	
				4	Lane 0: Laser Temp Low Alarm Flag	Not supported	
				3	Lane 0: Rx PWR High Alarm Flag	0 = Normal, 1 = Flag Asserted	
				2	Lane 0: Rx PWR High Warning Flag	0 = Normal, 1 = Flag Asserted	
				1	Lane 0: Rx PWR Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				0	Lane 0: Rx PWR Low Alarm Flag	0 = Normal, 1 = Flag Asserted	

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 Network Lanes	A201	1	Read Only	15	Lane 1: Laser Bias High Alarm Flag	0 = Normal, 1 = Flag Asserted	00h
				14	Lane 1: Laser Bias High Warning Flag	0 = Normal, 1 = Flag Asserted	
				13	Lane 1: Laser Bias Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				12	Lane 1: Laser Bias Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
				11	Lane 1: Laser PWR High Alarm Flag	0 = Normal, 1 = Flag Asserted	
				10	Lane 1: Laser PWR High Warning Flag	0 = Normal, 1 = Flag Asserted	
				9	Lane 1: Laser PWR Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				8	Lane 1: Laser PWR Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
				7	Lane 1: Laser Temp High Alarm Flag	Not supported	
				6	Lane 1: Laser Temp High Warning Flag	Not supported	
				5	Lane 1: Laser Temp Low Warning Flag	Not supported	
				4	Lane 1: Laser Temp Low Alarm Flag	Not supported	
				3	Lane 1: RX PWR High Alarm Flag	0 = Normal, 1 = Flag Asserted	
				2	Lane 1: RX PWR High Warning Flag	0 = Normal, 1 = Flag Asserted	
				1	Lane 1: RX PWR Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				0	Lane 1: RX PWR Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
	A202	1	Read Only	15	Lane 2: Laser Bias High Alarm Flag	0 = Normal, 1 = Flag Asserted	00h
				14	Lane 2: Laser Bias High Warning Flag	0 = Normal, 1 = Flag Asserted	
				13	Lane 2: Laser Bias Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				12	Lane 2: Laser Bias Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
				11	Lane 2: Laser PWR High Alarm Flag	0 = Normal, 1 = Flag Asserted	
				10	Lane 2: Laser PWR High Warning Flag	0 = Normal, 1 = Flag Asserted	
				9	Lane 2: Laser PWR Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				8	Lane 2: Laser PWR Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
				7	Lane 2: Laser Temp High Alarm Flag	Not supported	
				6	Lane 2: Laser Temp High Warning Flag	Not supported	
				5	Lane 2: Laser Temp Low Warning Flag	Not supported	
				4	Lane 2: Laser Temp Low Alarm Flag	Not supported	
				3	Lane 2: RX PWR High Alarm Flag	0 = Normal, 1 = Flag Asserted	
				2	Lane 2: RX PWR High Warning Flag	0 = Normal, 1 = Flag Asserted	
				1	Lane 2: RX PWR Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				0	Lane 2: RX PWR Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
	A203	1	Read Only	15	Lane 3: Laser Bias High Alarm Flag	0 = Normal, 1 = Flag Asserted	00h
				14	Lane 3: Laser Bias High Warning Flag	0 = Normal, 1 = Flag Asserted	
				13	Lane 3: Laser Bias Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				12	Lane 3: Laser Bias Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
				11	Lane 3: Laser PWR High Alarm Flag	0 = Normal, 1 = Flag Asserted	
				10	Lane 3: Laser PWR High Warning Flag	0 = Normal, 1 = Flag Asserted	
				9	Lane 3: Laser PWR Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				8	Lane 3: Laser PWR Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
				7	Lane 3: Laser Temp High Alarm Flag	Not supported	
				6	Lane 3: Laser Temp High Warning Flag	Not supported	
				5	Lane 3: Laser Temp Low Warning Flag	Not supported	
				4	Lane 3: Laser Temp Low Alarm Flag	Not supported	
				3	Lane 3: RX PWR High Alarm Flag	0 = Normal, 1 = Flag Asserted	
				2	Lane 3: RX PWR High Warning Flag	0 = Normal, 1 = Flag Asserted	
				1	Lane 3: RX PWR Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				0	Lane 3: RX PWR Low Alarm Flag	0 = Normal, 1 = Flag Asserted	

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 Network Lanes	A204	1	Read Only	15	Lane 4: Laser Bias High Alarm Flag	0 = Normal, 1 = Flag Asserted	0000h
				14	Lane 4: Laser Bias High Warning Flag	0 = Normal, 1 = Flag Asserted	
				13	Lane 4: Laser Bias Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				12	Lane 4: Laser Bias Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
				11	Lane 4: Laser PWR High Alarm Flag	0 = Normal, 1 = Flag Asserted	
				10	Lane 4: Laser PWR High Warning Flag	0 = Normal, 1 = Flag Asserted	
				9	Lane 4: Laser PWR Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				8	Lane 4: Laser PWR Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
				7	Lane 4: Laser Temp High Alarm Flag	Not supported	
				6	Lane 4: Laser Temp High Warning Flag	Not supported	
				5	Lane 4: Laser Temp Low Warning Flag	Not supported	
				4	Lane 4: Laser Temp Low Alarm Flag	Not supported	
				3	Lane 4: RX PWR High Alarm Flag	0 = Normal, 1 = Flag Asserted	
				2	Lane 4: RX PWR High Warning Flag	0 = Normal, 1 = Flag Asserted	
				1	Lane 4: RX PWR Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				0	Lane 4: RX PWR Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
	A205	1	Read Only	15	Lane 5: Laser Bias High Alarm Flag	0 = Normal, 1 = Flag Asserted	0000h
				14	Lane 5: Laser Bias High Warning Flag	0 = Normal, 1 = Flag Asserted	
				13	Lane 5: Laser Bias Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				12	Lane 5: Laser Bias Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
				11	Lane 5: Laser PWR High Alarm Flag	0 = Normal, 1 = Flag Asserted	
				10	Lane 5: Laser PWR High Warning Flag	0 = Normal, 1 = Flag Asserted	
				9	Lane 5: Laser PWR Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				8	Lane 5: Laser PWR Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
				7	Lane 5: Laser Temp High Alarm Flag	Not supported	
				6	Lane 5: Laser Temp High Warning Flag	Not supported	
				5	Lane 5: Laser Temp Low Warning Flag	Not supported	
				4	Lane 5: Laser Temp Low Alarm Flag	Not supported	
				3	Lane 5: RX PWR High Alarm Flag	0 = Normal, 1 = Flag Asserted	
				2	Lane 5: RX PWR High Warning Flag	0 = Normal, 1 = Flag Asserted	
				1	Lane 5: RX PWR Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				0	Lane 5: RX PWR Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
	A206	1	Read Only	15	Lane 6: Laser Bias High Alarm Flag	0 = Normal, 1 = Flag Asserted	0000h
				14	Lane 6: Laser Bias High Warning Flag	0 = Normal, 1 = Flag Asserted	
				13	Lane 6: Laser Bias Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				12	Lane 6: Laser Bias Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
				11	Lane 6: Laser PWR High Alarm Flag	0 = Normal, 1 = Flag Asserted	
				10	Lane 6: Laser PWR High Warning Flag	0 = Normal, 1 = Flag Asserted	
				9	Lane 6: Laser PWR Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				8	Lane 6: Laser PWR Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
				7	Lane 6: Laser Temp High Alarm Flag	Not supported	
				6	Lane 6: Laser Temp High Warning Flag	Not supported	
				5	Lane 6: Laser Temp Low Warning Flag	Not supported	
				4	Lane 6: Laser Temp Low Alarm Flag	Not supported	
				3	Lane 6: RX PWR High Alarm Flag	0 = Normal, 1 = Flag Asserted	
				2	Lane 6: RX PWR High Warning Flag	0 = Normal, 1 = Flag Asserted	
				1	Lane 6: RX PWR Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				0	Lane 6: RX PWR Low Alarm Flag	0 = Normal, 1 = Flag Asserted	

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 Network Lanes	A207	1	Read Only	15	Lane 7: Laser Bias High Alarm Flag	0 = Normal, 1 = Flag Asserted	0000h
				14	Lane 7: Laser Bias High Warning Flag	0 = Normal, 1 = Flag Asserted	
				13	Lane 7: Laser Bias Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				12	Lane 7: Laser Bias Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
				11	Lane 7: Laser PWR High Alarm Flag	0 = Normal, 1 = Flag Asserted	
				10	Lane 7: Laser PWR High Warning Flag	0 = Normal, 1 = Flag Asserted	
				9	Lane 7: Laser PWR Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				8	Lane 7: Laser PWR Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
				7	Lane 7: Laser Temp High Alarm Flag	Not supported	
				6	Lane 7: Laser Temp High Warning Flag	Not supported	
				5	Lane 7: Laser Temp Low Warning Flag	Not supported	
				4	Lane 7: Laser Temp Low Alarm Flag	Not supported	
				3	Lane 7: RX PWR High Alarm Flag	0 = Normal, 1 = Flag Asserted	
				2	Lane 7: RX PWR High Warning Flag	0 = Normal, 1 = Flag Asserted	
				1	Lane 7: RX PWR Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				0	Lane 7: RX PWR Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
	A208	1	Read Only	15	Lane 8: Laser Bias High Alarm Flag	0 = Normal, 1 = Flag Asserted	0000h
				14	Lane 8: Laser Bias High Warning Flag	0 = Normal, 1 = Flag Asserted	
				13	Lane 8: Laser Bias Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				12	Lane 8: Laser Bias Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
				11	Lane 8: Laser PWR High Alarm Flag	0 = Normal, 1 = Flag Asserted	
				10	Lane 8: Laser PWR High Warning Flag	0 = Normal, 1 = Flag Asserted	
				9	Lane 8: Laser PWR Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				8	Lane 8: Laser PWR Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
				7	Lane 8: Laser Temp High Alarm Flag	Not supported	
				6	Lane 8: Laser Temp High Warning Flag	Not supported	
				5	Lane 8: Laser Temp Low Warning Flag	Not supported	
				4	Lane 8: Laser Temp Low Alarm Flag	Not supported	
				3	Lane 8: RX PWR High Alarm Flag	0 = Normal, 1 = Flag Asserted	
				2	Lane 8: RX PWR High Warning Flag	0 = Normal, 1 = Flag Asserted	
				1	Lane 8: RX PWR Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				0	Lane 8: RX PWR Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
	A209	1	Read Only	15	Lane 9: Laser Bias High Alarm Flag	0 = Normal, 1 = Flag Asserted	0000h
				14	Lane 9: Laser Bias High Warning Flag	0 = Normal, 1 = Flag Asserted	
				13	Lane 9: Laser Bias Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				12	Lane 9: Laser Bias Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
				11	Lane 9: Laser PWR High Alarm Flag	0 = Normal, 1 = Flag Asserted	
				10	Lane 9: Laser PWR High Warning Flag	0 = Normal, 1 = Flag Asserted	
				9	Lane 9: Laser PWR Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				8	Lane 9: Laser PWR Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
				7	Lane 9: Laser Temp High Alarm Flag	Not supported	
				6	Lane 9: Laser Temp High Warning Flag	Not supported	
				5	Lane 9: Laser Temp Low Warning Flag	Not supported	
				4	Lane 9: Laser Temp Low Alarm Flag	Not supported	
				3	Lane 9: RX PWR High Alarm Flag	0 = Normal, 1 = Flag Asserted	
				2	Lane 9: RX PWR High Warning Flag	0 = Normal, 1 = Flag Asserted	
				1	Lane 9: RX PWR Low Warning Flag	0 = Normal, 1 = Flag Asserted	
				0	Lane 9: RX PWR Low Alarm Flag	0 = Normal, 1 = Flag Asserted	
	A20A	1	Read Only	15-0	Lane 10: Network Lane Alarm/Warning Flags	Not supported	0000h
	A20B	1	Read Only	15-0	Lane 11: Network Lane Alarm/Warning Flags	Not supported	0000h
	A20C	1	Read Only	15-0	Lane 12: Network Lane Alarm/Warning Flags	Not supported	0000h
	A20D	1	Read Only	15-0	Lane 13: Network Lane Alarm/Warning Flags	Not supported	0000h
	A20E	1	Read Only	15-0	Lane 14: Network Lane Alarm/Warning Flags	Not supported	0000h
	A20F	1	Read Only	15-0	Lane 15: Network Lane Alarm/Warning Flags	Not supported	0000h

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 Network Lanes	A210	1	Read Only	15-13	Lane 0: TEC, Wavelength, APD Faults	Not supported	0000h
				12-8	Reserved		
				7-6	Lane 0: TX_LOL Fault	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 0: Rx_LOS	0 = Normal, 1 = Flag Asserted	
				3-2	Lane 0: Rx_LOL Fault	Supported, only when CDR is enabled	
				1-0	Reserved		
	A211	1	Read Only	15-13	Lane 1: TEC, Wavelength, APD Faults	Not supported	00000h
				12-8	Reserved		
				7-6	Lane 1: TX_LOL Fault	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 1: Rx_LOS	0 = Normal, 1 = Flag Asserted	
				3-2	Lane 1: Rx_LOL Fault	Supported, only when CDR is enabled	
				1-0	Reserved		
	A212	1	Read Only	15-13	Lane 2: TEC, Wavelength, APD Faults	Not supported	0000h
				12-8	Reserved		
				7-6	Lane 2: TX_LOL Fault	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 2: Rx_LOS	0 = Normal, 1 = Flag Asserted	
				3-2	Lane 2: Rx_LOL Fault	Supported, only when CDR is enabled	
				1-0	Reserved		
	A213	1	Read Only	15-13	Lane 3: TEC, Wavelength, APD Faults	Not supported	0000h
				12-8	Reserved		
				7-6	Lane 3: TX_LOL Fault	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 3: Rx_LOS	0 = Normal, 1 = Flag Asserted	
				3-2	Lane 3: Rx_LOL Fault	Supported, only when CDR is enabled	
				1-0	Reserved		
	A214	1	Read Only	15-13	Lane 4: TEC, Wavelength, APD Faults	Not supported	0000h
				12-8	Reserved		
				7-6	Lane 4: TX_LOL Fault	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 4: Rx_LOS	0 = Normal, 1 = Flag Asserted	
				3-2	Lane 4: Rx_LOL Fault	Supported, only when CDR is enabled	
				1-0	Reserved		
	A215	1	Read Only	15-13	Lane 5: TEC, Wavelength, APD Faults	Not supported	0000h
				12-8	Reserved		
				7-6	Lane 5: TX_LOL Fault	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 5: Rx_LOS	0 = Normal, 1 = Flag Asserted	
				3-2	Lane 5: Rx_LOL Fault	Supported, only when CDR is enabled	
				1-0	Reserved		
	A216	1	Read Only	15-13	Lane 6: TEC, Wavelength, APD Faults	Not supported	0000h
				12-8	Reserved		
				7-6	Lane 6: TX_LOL Fault	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 6: Rx_LOS	0 = Normal, 1 = Flag Asserted	
				3-2	Lane 6: Rx_LOL Fault	Supported, only when CDR is enabled	
				1-0	Reserved		
	A217	1	Read Only	15-13	Lane 7: TEC, Wavelength, APD Faults	Not supported	0000h
				12-8	Reserved		
				7-6	Lane 7: TX_LOL Fault	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 7: Rx_LOS	0 = Normal, 1 = Flag Asserted	
				3-2	Lane 7: Rx_LOL Fault	Supported, only when CDR is enabled	
				1-0	Reserved		

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 Network Lanes	A218	1	Read Only	15-13	Lane 8: TEC, Wavelength, APD Faults	Not supported	0000h
				12-8	Reserved		
				7-6	Lane 8: TX_LOL Fault	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 8: Rx_LOS	0 = Normal, 1 = Flag Asserted	
				3-2	Lane 8: Rx_LOL Fault	Supported, only when CDR is enabled	
				1-0	Reserved		
	A219	1	Read Only	15-13	Lane 9: TEC, Wavelength, APD Faults	Not supported	0000h
				12-8	Reserved		
				7-6	Lane 9: TX_LOL Fault	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 9: Rx_LOS	0 = Normal, 1 = Flag Asserted	
				3-2	Lane 9: Rx_LOL Fault	Supported, only when CDR is enabled	
				1-0	Reserved		
	A21A	1	Read Only	15-0	Lane 10: Network Lane Fault Status	Not supported	0000h
	A21B	1	Read Only	15-0	Lane 11: Network Lane Fault Status	Not supported	0000h
	A21C	1	Read Only	15-0	Lane 12: Network Lane Fault Status	Not supported	0000h
	A21D	1	Read Only	15-0	Lane 13: Network Lane Fault Status	Not supported	0000h
	A21E	1	Read Only	15-0	Lane 14: Network Lane Fault Status	Not supported	0000h
	A21F	1	Read Only	15-0	Lane 15: Network Lane Fault Status	Not supported	0000h
	A220	1	Read/COR	15	Lane 0: Laser Bias High Alarm Latch	0 = Normal, 1 = Enable Asserted	0000h
				14	Lane 0: Laser Bias High Warning Latch	0 = Normal, 1 = Enable Asserted	
				13	Lane 0: Laser Bias Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				12	Lane 0: Laser Bias Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
				11	Lane 0: Laser PWR High Alarm Latch	0 = Normal, 1 = Enable Asserted	
				10	Lane 0: Laser PWR High Warning Latch	0 = Normal, 1 = Enable Asserted	
				9	Lane 0: Laser PWR Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				8	Lane 0: Laser PWR Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
				7	Lane 0: Laser Temp High Alarm Latch	Not supported	
				6	Lane 0: Laser Temp High Warning Latch	Not supported	
				5	Lane 0: Laser Temp Low Warning Latch	Not supported	
				4	Lane 0: Laser Temp Low Alarm Latch	Not supported	
				3	Lane 0: RX PWR High Alarm Latch	0 = Normal, 1 = Enable Asserted	
				2	Lane 0: RX PWR High Warning Latch	0 = Normal, 1 = Enable Asserted	
				1	Lane 0: RX PWR Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				0	Lane 0: RX PWR Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
	A221	1	Read/COR	15	Lane 1: Laser Bias High Alarm Latch	0 = Normal, 1 = Enable Asserted	0000h
				14	Lane 1: Laser Bias High Warning Latch	0 = Normal, 1 = Enable Asserted	
				13	Lane 1: Laser Bias Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				12	Lane 1: Laser Bias Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
				11	Lane 1: Laser PWR High Alarm Latch	0 = Normal, 1 = Enable Asserted	
				10	Lane 1: Laser PWR High Warning Latch	0 = Normal, 1 = Enable Asserted	
				9	Lane 1: Laser PWR Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				8	Lane 1: Laser PWR Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
				7	Lane 1: Laser Temp High Alarm Latch	Not supported	
				6	Lane 1: Laser Temp High Warning Latch	Not supported	
				5	Lane 1: Laser Temp Low Warning Latch	Not supported	
				4	Lane 1: Laser Temp Low Alarm Latch	Not supported	
				3	Lane 1: RX PWR High Alarm Latch	0 = Normal, 1 = Enable Asserted	
				2	Lane 1: RX PWR High Warning Latch	0 = Normal, 1 = Enable Asserted	
				1	Lane 1: RX PWR Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				0	Lane 1: RX PWR Low Alarm Latch	0 = Normal, 1 = Enable Asserted	

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 Network Lanes	A222	1	Read/COR	15	Lane 2: Laser Bias High Alarm Latch	0 = Normal, 1 = Enable Asserted	0000h
				14	Lane 2: Laser Bias High Warning Latch	0 = Normal, 1 = Enable Asserted	
				13	Lane 2: Laser Bias Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				12	Lane 2: Laser Bias Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
				11	Lane 2: Laser PWR High Alarm Latch	0 = Normal, 1 = Enable Asserted	
				10	Lane 2: Laser PWR High Warning Latch	0 = Normal, 1 = Enable Asserted	
				9	Lane 2: Laser PWR Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				8	Lane 2: Laser PWR Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
				7	Lane 2: Laser Temp High Alarm Latch	Not supported	
				6	Lane 2: Laser Temp High Warning Latch	Not supported	
				5	Lane 2: Laser Temp Low Warning Latch	Not supported	
				4	Lane 2: Laser Temp Low Alarm Latch	Not supported	
				3	Lane 2: RX PWR High Alarm Latch	0 = Normal, 1 = Enable Asserted	
				2	Lane 2: RX PWR High Warning Latch	0 = Normal, 1 = Enable Asserted	
				1	Lane 2: RX PWR Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				0	Lane 2: RX PWR Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
	A223	1	Read/COR	15	Lane 3: Laser Bias High Alarm Latch	0 = Normal, 1 = Enable Asserted	0000h
				14	Lane 3: Laser Bias High Warning Latch	0 = Normal, 1 = Enable Asserted	
				13	Lane 3: Laser Bias Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				12	Lane 3: Laser Bias Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
				11	Lane 3: Laser PWR High Alarm Latch	0 = Normal, 1 = Enable Asserted	
				10	Lane 3: Laser PWR High Warning Latch	0 = Normal, 1 = Enable Asserted	
				9	Lane 3: Laser PWR Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				8	Lane 3: Laser PWR Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
				7	Lane 3: Laser Temp High Alarm Latch	Not supported	
				6	Lane 3: Laser Temp High Warning Latch	Not supported	
				5	Lane 3: Laser Temp Low Warning Latch	Not supported	
				4	Lane 3: Laser Temp Low Alarm Latch	Not supported	
				3	Lane 3: RX PWR High Alarm Latch	0 = Normal, 1 = Enable Asserted	
				2	Lane 3: RX PWR High Warning Latch	0 = Normal, 1 = Enable Asserted	
				1	Lane 3: RX PWR Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				0	Lane 3: RX PWR Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
	A224	1	Read/COR	15	Lane 4: Laser Bias High Alarm Latch	0 = Normal, 1 = Enable Asserted	0000h
				14	Lane 4: Laser Bias High Warning Latch	0 = Normal, 1 = Enable Asserted	
				13	Lane 4: Laser Bias Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				12	Lane 4: Laser Bias Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
				11	Lane 4: Laser PWR High Alarm Latch	0 = Normal, 1 = Enable Asserted	
				10	Lane 4: Laser PWR High Warning Latch	0 = Normal, 1 = Enable Asserted	
				9	Lane 4: Laser PWR Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				8	Lane 4: Laser PWR Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
				7	Lane 4: Laser Temp High Alarm Latch	Not supported	
				6	Lane 4: Laser Temp High Warning Latch	Not supported	
				5	Lane 4: Laser Temp Low Warning Latch	Not supported	
				4	Lane 4: Laser Temp Low Alarm Latch	Not supported	
				3	Lane 4: RX PWR High Alarm Latch	0 = Normal, 1 = Enable Asserted	
				2	Lane 4: RX PWR High Warning Latch	0 = Normal, 1 = Enable Asserted	
				1	Lane 4: RX PWR Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				0	Lane 4: RX PWR Low Alarm Latch	0 = Normal, 1 = Enable Asserted	

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 Network Lanes	A225	1	Read/COR	15	Lane 5: Laser Bias High Alarm Latch	0 = Normal, 1 = Enable Asserted	0000h
				14	Lane 5: Laser Bias High Warning Latch	0 = Normal, 1 = Enable Asserted	
				13	Lane 5: Laser Bias Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				12	Lane 5: Laser Bias Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
				11	Lane 5: Laser PWR High Alarm Latch	0 = Normal, 1 = Enable Asserted	
				10	Lane 5: Laser PWR High Warning Latch	0 = Normal, 1 = Enable Asserted	
				9	Lane 5: Laser PWR Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				8	Lane 5: Laser PWR Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
				7	Lane 5: Laser Temp High Alarm Latch	Not supported	
				6	Lane 5: Laser Temp High Warning Latch	Not supported	
				5	Lane 5: Laser Temp Low Warning Latch	Not supported	
				4	Lane 5: Laser Temp Low Alarm Latch	Not supported	
				3	Lane 5: RX PWR High Alarm Latch	0 = Normal, 1 = Enable Asserted	
				2	Lane 5: RX PWR High Warning Latch	0 = Normal, 1 = Enable Asserted	
				1	Lane 5: RX PWR Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				0	Lane 5: RX PWR Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
	A226	1	Read/COR	15	Lane 6: Laser Bias High Alarm Latch	0 = Normal, 1 = Enable Asserted	0000h
				14	Lane 6: Laser Bias High Warning Latch	0 = Normal, 1 = Enable Asserted	
				13	Lane 6: Laser Bias Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				12	Lane 6: Laser Bias Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
				11	Lane 6: Laser PWR High Alarm Latch	0 = Normal, 1 = Enable Asserted	
				10	Lane 6: Laser PWR High Warning Latch	0 = Normal, 1 = Enable Asserted	
				9	Lane 6: Laser PWR Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				8	Lane 6: Laser PWR Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
				7	Lane 6: Laser Temp High Alarm Latch	Not supported	
				6	Lane 6: Laser Temp High Warning Latch	Not supported	
				5	Lane 6: Laser Temp Low Warning Latch	Not supported	
				4	Lane 6: Laser Temp Low Alarm Latch	Not supported	
				3	Lane 6: RX PWR High Alarm Latch	0 = Normal, 1 = Enable Asserted	
				2	Lane 6: RX PWR High Warning Latch	0 = Normal, 1 = Enable Asserted	
				1	Lane 6: RX PWR Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				0	Lane 6: RX PWR Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
	A227	1	Read/COR	15	Lane 7: Laser Bias High Alarm Latch	0 = Normal, 1 = Enable Asserted	0000h
				14	Lane 7: Laser Bias High Warning Latch	0 = Normal, 1 = Enable Asserted	
				13	Lane 7: Laser Bias Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				12	Lane 7: Laser Bias Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
				11	Lane 7: Laser PWR High Alarm Latch	0 = Normal, 1 = Enable Asserted	
				10	Lane 7: Laser PWR High Warning Latch	0 = Normal, 1 = Enable Asserted	
				9	Lane 7: Laser PWR Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				8	Lane 7: Laser PWR Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
				7	Lane 7: Laser Temp High Alarm Latch	Not supported	
				6	Lane 7: Laser Temp High Warning Latch	Not supported	
				5	Lane 7: Laser Temp Low Warning Latch	Not supported	
				4	Lane 7: Laser Temp Low Alarm Latch	Not supported	
				3	Lane 7: RX PWR High Alarm Latch	0 = Normal, 1 = Enable Asserted	
				2	Lane 7: RX PWR High Warning Latch	0 = Normal, 1 = Enable Asserted	
				1	Lane 7: RX PWR Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				0	Lane 7: RX PWR Low Alarm Latch	0 = Normal, 1 = Enable Asserted	

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 Network Lanes	A228	1	Read/COR	15	Lane 8: Laser Bias High Alarm Latch	0 = Normal, 1 = Enable Asserted	0000h
				14	Lane 8: Laser Bias High Warning Latch	0 = Normal, 1 = Enable Asserted	
				13	Lane 8: Laser Bias Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				12	Lane 8: Laser Bias Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
				11	Lane 8: Laser PWR High Alarm Latch	0 = Normal, 1 = Enable Asserted	
				10	Lane 8: Laser PWR High Warning Latch	0 = Normal, 1 = Enable Asserted	
				9	Lane 8: Laser PWR Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				8	Lane 8: Laser PWR Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
				7	Lane 8: Laser Temp High Alarm Latch	Not supported	
				6	Lane 8: Laser Temp High Warning Latch	Not supported	
				5	Lane 8: Laser Temp Low Warning Latch	Not supported	
				4	Lane 8: Laser Temp Low Alarm Latch	Not supported	
				3	Lane 8: RX PWR High Alarm Latch	0 = Normal, 1 = Enable Asserted	
				2	Lane 8: RX PWR High Warning Latch	0 = Normal, 1 = Enable Asserted	
				1	Lane 8: RX PWR Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				0	Lane 8: RX PWR Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
	A229	1	Read/COR	15	Lane 9: Laser Bias High Alarm Latch	0 = Normal, 1 = Enable Asserted	0000h
				14	Lane 9: Laser Bias High Warning Latch	0 = Normal, 1 = Enable Asserted	
				13	Lane 9: Laser Bias Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				12	Lane 9: Laser Bias Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
				11	Lane 9: Laser PWR High Alarm Latch	0 = Normal, 1 = Enable Asserted	
				10	Lane 9: Laser PWR High Warning Latch	0 = Normal, 1 = Enable Asserted	
				9	Lane 9: Laser PWR Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				8	Lane 9: Laser PWR Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
				7	Lane 9: Laser Temp High Alarm Latch	Not supported	
				6	Lane 9: Laser Temp High Warning Latch	Not supported	
				5	Lane 9: Laser Temp Low Warning Latch	Not supported	
				4	Lane 9: Laser Temp Low Alarm Latch	Not supported	
				3	Lane 9: RX PWR High Alarm Latch	0 = Normal, 1 = Enable Asserted	
				2	Lane 9: RX PWR High Warning Latch	0 = Normal, 1 = Enable Asserted	
				1	Lane 9: RX PWR Low Warning Latch	0 = Normal, 1 = Enable Asserted	
				0	Lane 9: RX PWR Low Alarm Latch	0 = Normal, 1 = Enable Asserted	
	A22A	1	Read/COR	15-0	Lane 10: Network Lane Alarm/Warning Latch	Not supported	0000h
	A22B	1	Read/COR	15-0	Lane 11: Network Lane Alarm/Warning Latch	Not supported	0000h
	A22C	1	Read/COR	15-0	Lane 12: Network Lane Alarm/Warning Latch	Not supported	0000h
	A22D	1	Read/COR	15-0	Lane 13: Network Lane Alarm/Warning Latch	Not supported	0000h
	A22E	1	Read/COR	15-0	Lane 14: Network Lane Alarm/Warning Latch	Not supported	0000h
	A22F	1	Read/COR	15-0	Lane 15: Network Lane Alarm/Warning Latch	Not supported	0000h
	A230	1	Read/COR	15-13	Lane 0: TEC, APD, λ Fault Latch	Not supported	0000h
				12-8	Reserved		
				7-6	Lane 0: TX_LOL Fault Latch	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 0: Rx_LOS Latch	0 = Normal, 1 = Flag Asserted	
				3-2	Lane 0: RX_LOL Fault Latch	Supported, only when CDR is enabled	
				1-0	Reserved		
	A231	1	Read/COR	15-13	Lane 1: TEC, APD, λ Fault Latch	Not supported	0000h
				12-8	Reserved		
				7-6	Lane 1: TX_LOL Fault Latch	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 1: Rx_LOS Latch	0 = Normal, 1 = Flag Asserted	
				3-2	Lane 1: RX_LOL Fault Latch	Supported, only when CDR is enabled	
				1-0	Reserved		

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 Network Lanes	A232	1	Read/COR	15-13	Lane 2: TEC, APD, λ Fault Latch	Not supported	0000h
				12-8	Reserved		
				7-6	Lane 2: TX_LOL Fault Latch	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 2: Rx_LOS Latch	0 = Normal, 1 = Flag Asserted	
				3-2	Lane 2: RX_LOL Fault Latch	Supported, only when CDR is enabled	
				1-0	Reserved		
	A233	1	Read/COR	15-13	Lane 3: TEC, APD, λ Fault Latch	Not supported	0000h
				12-8	Reserved		
				7-6	Lane 3: TX_LOL Fault Latch	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 3: Rx_LOS Latch	0 = Normal, 1 = Flag Asserted	
				3-2	Lane 3: RX_LOL Fault Latch	Supported, only when CDR is enabled	
				1-0	Reserved		
	A234	1	Read/COR	15-13	Lane 4: TEC, APD, λ Fault Latch	Not supported	0000h
				12-8	Reserved		
				7-6	Lane 4: TX_LOL Fault Latch	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 4: Rx_LOS Latch	0 = Normal, 1 = Flag Asserted	
				3-2	Lane 4: RX_LOL Fault Latch	Supported, only when CDR is enabled	
				1-0	Reserved		
	A235	1	Read/COR	15-13	Lane 5: TEC, APD, λ Fault Latch	Not supported	0000h
				12-8	Reserved		
				7-6	Lane 5: TX_LOL Fault Latch	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 5: Rx_LOS Latch	0 = Normal, 1 = Flag Asserted	
				3-2	Lane 5: RX_LOL Fault Latch	Supported, only when CDR is enabled	
				1-0	Reserved		
	A236	1	Read/COR	15-13	Lane 6: TEC, APD, λ Fault Latch	Not supported	0000h
				12-8	Reserved		
				7-6	Lane 6: TX_LOL Fault Latch	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 6: Rx_LOS Latch	0 = Normal, 1 = Flag Asserted	
				3-2	Lane 6: RX_LOL Fault Latch	Supported, only when CDR is enabled	
				1-0	Reserved		
	A237	1	Read/COR	15-13	Lane 7: TEC, APD, λ Fault Latch	Not supported	0000h
				12-8	Reserved		
				7-6	Lane 7: TX_LOL Fault Latch	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 7: Rx_LOS Latch	0 = Normal, 1 = Flag Asserted	
				3-2	Lane 7: RX_LOL Fault Latch	Supported, only when CDR is enabled	
				1-0	Reserved		
	A238	1	Read/COR	15-13	Lane 8: TEC, APD, λ Fault Latch	Not supported	0000h
				12-8	Reserved		
				7-6	Lane 8: TX_LOL Fault Latch	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 8: Rx_LOS Latch	0 = Normal, 1 = Flag Asserted	
				3-2	Lane 8: RX_LOL Fault Latch	Supported, only when CDR is enabled	
				1-0	Reserved		

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 Network Lanes	A239	1	Read/COR	15-13	Lane 9: TEC, APD, λ Fault Latch	Not supported	0000h
				12-8	Reserved		
				7-6	Lane 9: TX_LOL Fault Latch	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 9: Rx_LOS Latch	0 = Normal, 1 = Flag Asserted	
				3-2	Lane 9: RX_LOL Fault Latch	Supported, only when CDR is enabled	
				1-0	Reserved		
	A23A	1	Read/COR	15-0	Lane 10: Network Lane Fault Status Latch	Not supported	0000h
	A23B	1	Read/COR	15-0	Lane 11: Network Lane Fault Status Latch	Not supported	0000h
	A23C	1	Read/COR	15-0	Lane 12: Network Lane Fault Status Latch	Not supported	0000h
	A23D	1	Read/COR	15-0	Lane 13: Network Lane Fault Status Latch	Not supported	0000h
	A23E	1	Read/COR	15-0	Lane 14: Network Lane Fault Status Latch	Not supported	0000h
	A23F	1	Read/COR	15-0	Lane 15: Network Lane Fault Status Latch	Not supported	0000h
	A240	1	Read Write	15	Lane 0: Laser Bias High Alarm Enable	0 = Normal, 1 = Enable Asserted	FF0Fh
				14	Lane 0: Laser Bias High Warning Enable	0 = Normal, 1 = Enable Asserted	
				13	Lane 0: Laser Bias Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				12	Lane 0: Laser Bias Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
				11	Lane 0: Laser PWR High Alarm Enable	0 = Normal, 1 = Enable Asserted	
				10	Lane 0: Laser PWR High Warning Enable	0 = Normal, 1 = Enable Asserted	
				9	Lane 0: Laser PWR Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				8	Lane 0: Laser PWR Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
				7	Lane 0: Laser Temp High Alarm Enable	Not supported	
				6	Lane 0: Laser Temp High Warning Enable	Not supported	
				5	Lane 0: Laser Temp Low Warning Enable	Not supported	
				4	Lane 0: Laser Temp Low Alarm Enable	Not supported	
				3	Lane 0: RX PWR High Alarm Enable	0 = Normal, 1 = Enable Asserted	
				2	Lane 0: RX PWR High Warning Enable	0 = Normal, 1 = Enable Asserted	
				1	Lane 0: RX PWR Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				0	Lane 0: RX PWR Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
	A241	1	Read Write	15	Lane 1: Laser Bias High Alarm Enable	0 = Normal, 1 = Enable Asserted	FF0Fh
				14	Lane 1: Laser Bias High Warning Enable	0 = Normal, 1 = Enable Asserted	
				13	Lane 1: Laser Bias Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				12	Lane 1: Laser Bias Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
				11	Lane 1: Laser PWR High Alarm Enable	0 = Normal, 1 = Enable Asserted	
				10	Lane 1: Laser PWR High Warning Enable	0 = Normal, 1 = Enable Asserted	
				9	Lane 1: Laser PWR Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				8	Lane 1: Laser PWR Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
				7	Lane 1: Laser Temp High Alarm Enable	Not supported	
				6	Lane 1: Laser Temp High Warning Enable	Not supported	
				5	Lane 1: Laser Temp Low Warning Enable	Not supported	
				4	Lane 1: Laser Temp Low Alarm Enable	Not supported	
				3	Lane 1: RX PWR High Alarm Enable	0 = Normal, 1 = Enable Asserted	
				2	Lane 1: RX PWR High Warning Enable	0 = Normal, 1 = Enable Asserted	
				1	Lane 1: RX PWR Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				0	Lane 1: RX PWR Low Alarm Enable	0 = Normal, 1 = Enable Asserted	

Bloc Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 Network Lanes	A242	1	Read Write	15	Lane 2: Laser Bias High Alarm Enable	0 = Normal, 1 = Enable Asserted	FF0Fh
				14	Lane 2: Laser Bias High Warning Enable	0 = Normal, 1 = Enable Asserted	
				13	Lane 2: Laser Bias Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				12	Lane 2: Laser Bias Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
				11	Lane 2: Laser PWR High Alarm Enable	0 = Normal, 1 = Enable Asserted	
				10	Lane 2: Laser PWR High Warning Enable	0 = Normal, 1 = Enable Asserted	
				9	Lane 2: Laser PWR Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				8	Lane 2: Laser PWR Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
				7	Lane 2: Laser Temp High Alarm Enable	Not supported	
				6	Lane 2: Laser Temp High Warning Enable	Not supported	
				5	Lane 2: Laser Temp Low Warning Enable	Not supported	
				4	Lane 2: Laser Temp Low Alarm Enable	Not supported	
				3	Lane 2: RX PWR High Alarm Enable	0 = Normal, 1 = Enable Asserted	
				2	Lane 2: RX PWR High Warning Enable	0 = Normal, 1 = Enable Asserted	
				1	Lane 2: RX PWR Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				0	Lane 2: RX PWR Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
	A243	1	Read Write	15	Lane 3: Laser Bias High Alarm Enable	0 = Normal, 1 = Enable Asserted	FF0Fh
				14	Lane 3: Laser Bias High Warning Enable	0 = Normal, 1 = Enable Asserted	
				13	Lane 3: Laser Bias Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				12	Lane 3: Laser Bias Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
				11	Lane 3: Laser PWR High Alarm Enable	0 = Normal, 1 = Enable Asserted	
				10	Lane 3: Laser PWR High Warning Enable	0 = Normal, 1 = Enable Asserted	
				9	Lane 3: Laser PWR Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				8	Lane 3: Laser PWR Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
				7	Lane 3: Laser Temp High Alarm Enable	Not supported	
				6	Lane 3: Laser Temp High Warning Enable	Not supported	
				5	Lane 3: Laser Temp Low Warning Enable	Not supported	
				4	Lane 3: Laser Temp Low Alarm Enable	Not supported	
				3	Lane 3: RX PWR High Alarm Enable	0 = Normal, 1 = Enable Asserted	
				2	Lane 3: RX PWR High Warning Enable	0 = Normal, 1 = Enable Asserted	
				1	Lane 3: RX PWR Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				0	Lane 3: RX PWR Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
	A244	1	Read Write	15	Lane 4: Laser Bias High Alarm Enable	0 = Normal, 1 = Enable Asserted	FF0Fh
				14	Lane 4: Laser Bias High Warning Enable	0 = Normal, 1 = Enable Asserted	
				13	Lane 4: Laser Bias Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				12	Lane 4: Laser Bias Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
				11	Lane 4: Laser PWR High Alarm Enable	0 = Normal, 1 = Enable Asserted	
				10	Lane 4: Laser PWR High Warning Enable	0 = Normal, 1 = Enable Asserted	
				9	Lane 4: Laser PWR Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				8	Lane 4: Laser PWR Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
				7	Lane 4: Laser Temp High Alarm Enable	Not supported	
				6	Lane 4: Laser Temp High Warning Enable	Not supported	
				5	Lane 4: Laser Temp Low Warning Enable	Not supported	
				4	Lane 4: Laser Temp Low Alarm Enable	Not supported	
				3	Lane 4: RX PWR High Alarm Enable	0 = Normal, 1 = Enable Asserted	
				2	Lane 4: RX PWR High Warning Enable	0 = Normal, 1 = Enable Asserted	
				1	Lane 4: RX PWR Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				0	Lane 4: RX PWR Low Alarm Enable	0 = Normal, 1 = Enable Asserted	

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 Network Lanes	A245	1	Read Write	15	Lane 5: Laser Bias High Alarm Enable	0 = Normal, 1 = Enable Asserted	FF0Fh
				14	Lane 5: Laser Bias High Warning Enable	0 = Normal, 1 = Enable Asserted	
				13	Lane 5: Laser Bias Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				12	Lane 5: Laser Bias Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
				11	Lane 5: Laser PWR High Alarm Enable	0 = Normal, 1 = Enable Asserted	
				10	Lane 5: Laser PWR High Warning Enable	0 = Normal, 1 = Enable Asserted	
				9	Lane 5: Laser PWR Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				8	Lane 5: Laser PWR Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
				7	Lane 5: Laser Temp High Alarm Enable	Not supported	
				6	Lane 5: Laser Temp High Warning Enable	Not supported	
				5	Lane 5: Laser Temp Low Warning Enable	Not supported	
				4	Lane 5: Laser Temp Low Alarm Enable	Not supported	
				3	Lane 5: RX PWR High Alarm Enable	0 = Normal, 1 = Enable Asserted	
				2	Lane 5: RX PWR High Warning Enable	0 = Normal, 1 = Enable Asserted	
				1	Lane 5: RX PWR Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				0	Lane 5: RX PWR Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
	A246	1	Read Write	15	Lane 6: Laser Bias High Alarm Enable	0 = Normal, 1 = Enable Asserted	FF0Fh
				14	Lane 6: Laser Bias High Warning Enable	0 = Normal, 1 = Enable Asserted	
				13	Lane 6: Laser Bias Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				12	Lane 6: Laser Bias Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
				11	Lane 6: Laser PWR High Alarm Enable	0 = Normal, 1 = Enable Asserted	
				10	Lane 6: Laser PWR High Warning Enable	0 = Normal, 1 = Enable Asserted	
				9	Lane 6: Laser PWR Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				8	Lane 6: Laser PWR Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
				7	Lane 6: Laser Temp High Alarm Enable	Not supported	
				6	Lane 6: Laser Temp High Warning Enable	Not supported	
				5	Lane 6: Laser Temp Low Warning Enable	Not supported	
				4	Lane 6: Laser Temp Low Alarm Enable	Not supported	
				3	Lane 6: RX PWR High Alarm Enable	0 = Normal, 1 = Enable Asserted	
				2	Lane 6: RX PWR High Warning Enable	0 = Normal, 1 = Enable Asserted	
				1	Lane 6: RX PWR Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				0	Lane 6: RX PWR Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
	A247	1	Read Write	15	Lane 7: Laser Bias High Alarm Enable	0 = Normal, 1 = Enable Asserted	FF0Fh
				14	Lane 7: Laser Bias High Warning Enable	0 = Normal, 1 = Enable Asserted	
				13	Lane 7: Laser Bias Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				12	Lane 7: Laser Bias Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
				11	Lane 7: Laser PWR High Alarm Enable	0 = Normal, 1 = Enable Asserted	
				10	Lane 7: Laser PWR High Warning Enable	0 = Normal, 1 = Enable Asserted	
				9	Lane 7: Laser PWR Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				8	Lane 7: Laser PWR Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
				7	Lane 7: Laser Temp High Alarm Enable	Not supported	
				6	Lane 7: Laser Temp High Warning Enable	Not supported	
				5	Lane 7: Laser Temp Low Warning Enable	Not supported	
				4	Lane 7: Laser Temp Low Alarm Enable	Not supported	
				3	Lane 7: RX PWR High Alarm Enable	0 = Normal, 1 = Enable Asserted	
				2	Lane 7: RX PWR High Warning Enable	0 = Normal, 1 = Enable Asserted	
				1	Lane 7: RX PWR Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				0	Lane 7: RX PWR Low Alarm Enable	0 = Normal, 1 = Enable Asserted	

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 Network Lanes	A248	1	Read Write	15	Lane 8: Laser Bias High Alarm Enable	0 = Normal, 1 = Enable Asserted	FF0Fh
				14	Lane 8: Laser Bias High Warning Enable	0 = Normal, 1 = Enable Asserted	
				13	Lane 8: Laser Bias Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				12	Lane 8: Laser Bias Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
				11	Lane 8: Laser PWR High Alarm Enable	0 = Normal, 1 = Enable Asserted	
				10	Lane 8: Laser PWR High Warning Enable	0 = Normal, 1 = Enable Asserted	
				9	Lane 8: Laser PWR Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				8	Lane 8: Laser PWR Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
				7	Lane 8: Laser Temp High Alarm Enable	Not supported	
				6	Lane 8: Laser Temp High Warning Enable	Not supported	
				5	Lane 8: Laser Temp Low Warning Enable	Not supported	
				4	Lane 8: Laser Temp Low Alarm Enable	Not supported	
				3	Lane 8: RX PWR High Alarm Enable	0 = Normal, 1 = Enable Asserted	
				2	Lane 8: RX PWR High Warning Enable	0 = Normal, 1 = Enable Asserted	
				1	Lane 8: RX PWR Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				0	Lane 8: RX PWR Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
	A249	1	Read Write	15	Lane 9: Laser Bias High Alarm Enable	0 = Normal, 1 = Enable Asserted	FF0Fh
				14	Lane 9: Laser Bias High Warning Enable	0 = Normal, 1 = Enable Asserted	
				13	Lane 9: Laser Bias Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				12	Lane 9: Laser Bias Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
				11	Lane 9: Laser PWR High Alarm Enable	0 = Normal, 1 = Enable Asserted	
				10	Lane 9: Laser PWR High Warning Enable	0 = Normal, 1 = Enable Asserted	
				9	Lane 9: Laser PWR Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				8	Lane 9: Laser PWR Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
				7	Lane 9: Laser Temp High Alarm Enable	Not supported	
				6	Lane 9: Laser Temp High Warning Enable	Not supported	
				5	Lane 9: Laser Temp Low Warning Enable	Not supported	
				4	Lane 9: Laser Temp Low Alarm Enable	Not supported	
				3	Lane 9: RX PWR High Alarm Enable	0 = Normal, 1 = Enable Asserted	
				2	Lane 9: RX PWR High Warning Enable	0 = Normal, 1 = Enable Asserted	
				1	Lane 9: RX PWR Low Warning Enable	0 = Normal, 1 = Enable Asserted	
				0	Lane 9: RX PWR Low Alarm Enable	0 = Normal, 1 = Enable Asserted	
	A24A	1	Read Only	15-0	Lane 10: Alarm/Warning Enable	Not supported	0000h
	A24B	1	Read Only	15-0	Lane 11: Alarm/Warning Enable	Not supported	0000h
	A24C	1	Read Only	15-0	Lane 12: Alarm/Warning Enable	Not supported	0000h
	A24D	1	Read Only	15-0	Lane 13: Alarm/Warning Enable	Not supported	0000h
	A24E	1	Read Only	15-0	Lane 14: Alarm/Warning Enable	Not supported	0000h
	A24F	1	Read Only	15-0	Lane 15: Alarm/Warning Enable	Not supported	0000h
	A250	1	Read Write	15-13	Lane 0: TEC, Wavelength, APD Fault	Not supported	0010h
				12-8	Reserved		
				7-6	Lane 0: TX_LOL Fault Enables	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 0: Rx_LOS Enable	0 = Normal, 1 = Enable Asserted	
				3	Lane 0: Rx_LOL Enable	Supported, only when CDR is enabled	
				2	Lane 0: Fault Enable	Not supported	
				1-0	Reserved		

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 Network Lanes	A251	1	Read Write	15-13	Lane 1: TEC, Wavelength, APD Fault	Not supported	0010h
				12-8	Reserved		
				7-6	Lane 1: TX_LOL Fault Enable	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 1: Rx_LOS Enable	0 = Normal, 1 = Enable Asserted	
				3	Lane 1: Rx_LOL Enable	Supported, only when CDR is enabled	
				2	Lane 1: Fault Enable	Not supported	
				1-0	Reserved		
	A252	1	Read Write	15-13	Lane 2: TEC, Wavelength, APD Fault Enables	Not supported	0010h
				12-8	Reserved		
				7-6	Lane 2: TX_LOL Fault Enable	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 2: Rx_LOS Enable	0 = Normal, 1 = Enable Asserted	
				3	Lane 2: Rx_LOL Enable	Supported, only when CDR is enabled	
				2	Lane 2: Fault Enable	Not supported	
				1-0	Reserved		
	A253	1	Read Write	15-13	Lane 3: TEC, Wavelength, APD Fault	Not supported	0010h
				12-8	Reserved		
				7-6	Lane 3: TX_LOL Fault Enable	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 3: Rx_LOS Enable	0 = Normal, 1 = Enable Asserted	
				3	Lane 3: Rx_LOL Enable	Supported, only when CDR is enabled	
				2	Lane 3: Fault Enable	Not supported	
				1-0	Reserved		
	A254	1	Read Write	15-13	Lane 4: TEC, Wavelength, APD Fault	Not supported	0010h
				12-8	Reserved		
				7-6	Lane 4: TX_LOL Fault Enable	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 4: Rx_LOS Enable	0 = Normal, 1 = Enable Asserted	
				3	Lane 4: Rx_LOL Enable	Supported, only when CDR is enabled	
				2	Lane 4: Fault Enable	Not supported	
				1-0	Reserved		
	A255	1	Read Write	15-13	Lane 5: TEC, Wavelength, APD Fault	Not supported	0010h
				12-8	Reserved		
				7-6	Lane 5: TX_LOL Fault Enable	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 5: Rx_LOS Enable	0 = Normal, 1 = Enable Asserted	
				3	Lane5: Rx_LOL Enable	Supported, only when CDR is enabled	
				2	Lane 5: Fault Enable	Not supported	
				1-0	Reserved		
	A256	1	Read Write	15-13	Lane 6: TEC, Wavelength, APD Fault	Not supported	0010h
				12-8	Reserved		
				7-6	Lane 6: TX_LOL Fault Enable	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 6: Rx_LOS Enable	0 = Normal, 1 = Enable Asserted	
				3	Lane 6: Rx_LOL Enable	Supported, only when CDR is enabled	
				2	Lane 6: Fault Enable	Not supported	
				1-0	Reserved		

| Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 Network Lanes	A257	1	Read Write	15-13	Lane 7: TEC, Wavelength, APD Fault	Not supported	0010h
				12-8	Reserved		
				7-6	Lane 7: TX_LOL Fault Enable	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 7: Rx_LOS Enable	0 = Normal, 1 = Enable Asserted	
				3	Lane 7: Rx_LOL Enable	Supported, only when CDR is enabled	
				2	Lane 7: Fault Enable	Not supported	
				1-0	Reserved		
	A258	1	Read Write	15-13	Lane 8: TEC, Wavelength, APD Fault Enables	Not supported	0010h
				12-8	Reserved		
				7-6	Lane 8: TX_LOL Fault Enable	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 8: Rx_LOS Enable	0 = Normal, 1 = Enable Asserted	
				3	Lane 8: Rx_LOL Enable	Supported, only when CDR is enabled	
				2	Lane 8: Fault Enable	Not supported	
				1-0	Reserved		
	A259	1	Read Only	15-13	Lane 9: TEC, Wavelength, APD Fault Enables	Not supported	0010h
				12-8	Reserved		
				7-6	Lane 9: TX_LOL Fault Enable	Supported, only when CDR is enabled	
				5	Reserved		
				4	Lane 9: Rx_LOS Enable	0 = Normal, 1 = Enable Asserted	
				3	Lane 9: Rx_LOL Enable	Supported, only when CDR is enabled	
				2	Lane 9: Fault Enable	Not supported	
				1-0	Reserved		
	A25A	1	Read Only	15-0	Lane 10: Extra Alarm/Warning Flag Enable	Not supported	0000h
	A25B	1	Read Only	15-0	Lane 11: Extra Alarm/Warning Flag Enable	Not supported	0000h
	A25C	1	Read Only	15-0	Lane 12: Extra Alarm/Warning Flag Enable	Not supported	0000h
	A25D	1	Read Only	15-0	Lane 13: Extra Alarm/Warning Flag Enable	Not supported	0000h
	A25E	1	Read Only	15-0	Lane 14: Extra Alarm/Warning Flag Enable	Not supported	0000h
	A25F	1	Read Only	15-0	Lane 15: Extra Alarm/Warning Flag Enable	Not supported	0000h
	A260 to A269	10	Read only	15-2	Reserved		0000h
			Read Write	1	Tx_Squelch Control	Default value is '0' which is Tx_Squelch enabled; A260 to A269 is channel 0 to channel 9 respectively. It can be disabled on per channel basis by writing value '1' to bit 1 of A260 (channel 0) ~ A269 (channel 9)	
			Read Write	0	Rx_Squelch Control	Default value is '0' which is Rx_Squelch enabled; A260 to A269 is channel 0 to channel 9 respectively. It can be disabled on per channel basis by writing value '1' to bit 0 of A260 (channel 0) ~ A269 (channel 9) Disable Tx/Rx_Squelch function is intended for engineering test purpose. Operating the transceiver module in this mode is not recommended and shall be avoid	
	A26A	22	Read Only	15-0	Reserved		0000h

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 2 Network Lanes	A280	16	Read Only	15-0	Network Lane FEC Controls	Not supported	0000h
	A290	16	Read Only	15-0	Network Lane PRBS Rx Error Count	Not supported	0000h
	A2A0	1	Read Only	15-0	Lane 0: TX Bias Current Monitor A/D Value	Range 0 - 131 mA. Accuracy ± 10%. Resolution 2 μA.	0000h
	A2A1			15-0	Lane 1: TX Bias Current Monitor A/D Value	Range 0 - 131 mA. Accuracy ± 10%. Resolution 2 μA.	0000h
	A2A2			15-0	Lane 2: TX Bias Current Monitor A/D Value	Range 0 - 131 mA. Accuracy ± 10%. Resolution 2 μA.	0000h
	A2A3			15-0	Lane 3: TX Bias Current Monitor A/D Value	Range 0 - 131 mA. Accuracy ± 10%. Resolution 2 μA.	0000h
	A2A4			15-0	Lane 4: TX Bias Current Monitor A/D Value	Range 0 - 131 mA. Accuracy ± 10%. Resolution 2 μA.	0000h
	A2A5			15-0	Lane 5: TX Bias Current Monitor A/D Value	Range 0 - 131 mA. Accuracy ± 10%. Resolution 2 μA.	0000h
	A2A6			15-0	Lane 6: TX Bias Current Monitor A/D Value	Range 0 - 131 mA. Accuracy ± 10%. Resolution 2 μA.	0000h
	A2A7			15-0	Lane 7: TX Bias Current Monitor A/D Value	Range 0 - 131 mA. Accuracy ± 10%. Resolution 2 μA.	0000h
	A2A8			15-0	Lane 8: TX Bias Current Monitor A/D Value	Range 0 - 131mA. Accuracy ± 10%. Resolution 2 μA.	0000h
	A2A9			15-0	Lane 9: TX Bias Current Monitor A/D Value	Range 0 - 131 mA. Accuracy ± 10%. Resolution 2 μA.	0000h
	A2AA	1	Read Only	15-0	Lane 10: TX Bias Current Monitor A/D Value	Not supported	0000h
	A2AB	1	Read Only	15-0	Lane 11: TX Bias Current Monitor A/D Value	Not supported	0000h
	A2AC	1	Read Only	15-0	Lane 12: TX Bias Current Monitor A/D Value	Not supported	0000h
	A2AD	1	Read Only	15-0	Lane 13: TX Bias Current Monitor A/D Value	Not supported	0000h
	A2AE	1	Read Only	15-0	Lane 14: TX Bias Current Monitor A/D Value	Not supported	0000h
	A2AF	1	Read Only	15-0	Lane 15: TX Bias Current Monitor A/D Value	Not supported	0000h
	A2B0	1	Read Only	15-0	Lane 0: Tx Optical PWR Monitor A/D Value	Range 0 to 6.5 mW. Accuracy ± 2 dB. Resolution 0.1 μW. Average Power.	0000h
	A2B1			15-0	Lane 1: Tx Optical PWR Monitor A/D Value	Range 0 to 6.5 mW. Accuracy ± 2 dB. Resolution 0.1 μW. Average Power.	0000h
	A2B2			15-0	Lane 2: Tx Optical PWR Monitor A/D Value	Range 0 to 6.5 mW. Accuracy ± 2 dB. Resolution 0.1 μW. Average Power.	0000h
	A2B3			15-0	Lane 3: Tx Optical PWR Monitor A/D Value	Range 0 to 6.5 mW. Accuracy ± 2 dB. Resolution 0.1 μW. Average Power.	0000h
	A2B4			15-0	Lane 4: Tx Optical PWR Monitor A/D Value	Range 0 to 6.5 mW. Accuracy ± 2 dB. Resolution 0.1 μW. Average Power.	0000h
	A2B5			15-0	Lane 5: Tx Optical PWR Monitor A/D Value	Range 0 to 6.5 mW. Accuracy ± 2 dB. Resolution 0.1 μW. Average Power.	0000h
	A2B6			15-0	Lane 6: Tx Optical PWR Monitor A/D Value	Range 0 to 6.5 mW. Accuracy ± 2 dB. Resolution 0.1 μW. Average Power.	0000h
	A2B7			15-0	Lane 7: Tx Optical PWR Monitor A/D Value	Range 0 to 6.5 mW. Accuracy ± 2 dB. Resolution 0.1 μW. Average Power.	0000h
	A2B8			15-0	Lane 8: Tx Optical PWR Monitor A/D Value	Range 0 to 6.5 mW. Accuracy ± 2 dB. Resolution 0.1 μW. Average Power.	0000h
	A2B9			15-0	Lane 9: Tx Optical PWR Monitor A/D Value	Range 0 to 6.5 mW. Accuracy ± 2 dB. Resolution 0.1 μW. Average Power.	0000h
	A2BA	1	Read Only	15-0	Lane 10: Tx Optical PWR Monitor A/D Value	Not supported	0000h
	A2BB	1	Read Only	15-0	Lane 11: Tx Optical PWR Monitor A/D Value	Not supported	0000h
	A2BC	1	Read Only	15-0	Lane 12: Tx Optical PWR Monitor A/D Value	Not supported	0000h
	A2BD	1	Read Only	15-0	Lane 13: Tx Optical PWR Monitor A/D Value	Not supported	0000h
	A2BE	1	Read Only	15-0	Lane 14: Tx Optical PWR Monitor A/D Value	Not supported	0000h
	A2BF	1	Read Only	15-0	Lane 15: Tx Optical PWR Monitor A/D Value	Not supported	0000h
	A2C0	16	Read Only	15-0	Network Lane Tx Laser Temperature A/D	Not supported	0000h

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 2 Network Lanes (Cont.)	A2D0	1	Read Only	15-0	Lane 0: Rx Optical PWR Monitor A/D Value	Range 0 to 6.5 mW. Accuracy ± 2 dB. Resolution 0.1 μW. Average Power.	0000h
	A2D1			15-0	Lane 1: Rx Optical PWR Monitor A/D Value	Range 0 to 6.5 mW. Accuracy ± 2 dB. Resolution 0.1 μW. Average Power.	0000h
	A2D2			15-0	Lane 2: Rx Optical PWR Monitor A/D Value	Range 0 to 6.5 mW. Accuracy ± 2 dB. Resolution 0.1 μW. Average Power.	0000h
	A2D3			15-0	Lane 3: Rx Optical PWR Monitor A/D Value	Range 0 to 6.5 mW. Accuracy ± 2 dB. Resolution 0.1 μW. Average Power.	0000h
	A2D4			15-0	Lane 4: Rx Optical PWR Monitor A/D Value	Range 0 to 6.5 mW. Accuracy ± 2 dB. Resolution 0.1 μW. Average Power.	0000h
	A2D5			15-0	Lane 5: Rx Optical PWR Monitor A/D Value	Range 0 to 6.5 mW. Accuracy ± 2 dB. Resolution 0.1 μW. Average Power.	0000h
	A2D6			15-0	Lane 6: Rx Optical PWR Monitor A/D Value	Range 0 to 6.5 mW. Accuracy ± 2 dB. Resolution 0.1 μW. Average Power.	0000h
	A2D7			15-0	Lane 7: Rx Optical PWR Monitor A/D Value	Range 0 to 6.5 mW. Accuracy ± 2 dB. Resolution 0.1 μW. Average Power.	0000h
	A2D8			15-0	Lane 8: Rx Optical PWR Monitor A/D Value	Range 0 to 6.5 mW. Accuracy ± 2 dB. Resolution 0.1 μW. Average Power.	0000h
	A2D9			15-0	Lane 9: Rx Optical PWR Monitor A/D Value	Range 0 to 6.5 mW. Accuracy ± 2 dB. Resolution 0.1 μW. Average Power.	0000h
	A2DA	1	Read Only	15-0	Lane 10: Rx Optical PWR Monitor A/D Value	Not supported	0000h
	A2DB	1	Read Only	15-0	Lane 11: Rx Optical PWR Monitor A/D Value	Not supported	0000h
	A2DC	1	Read Only	15-0	Lane 12: Rx Optical PWR Monitor A/D Value	Not supported	0000h
	A2DD	1	Read Only	15-0	Lane 13: Rx Optical PWR Monitor A/D Value	Not supported	0000h
	A2DE	1	Read Only	15-0	Lane 14: Rx Optical PWR Monitor A/D Value	Not supported	0000h
	A2DF	1	Read Only	15-0	Lane 15: Rx Optical PWR Monitor A/D Value	Not supported	0000h
	A2E0	32	Read Only	15-0	Reserved		0000h

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 3 Network Lanes	A300 - A3FF	128	Mixed	15-0	Optional Network Lane VR 3 Registers	Not supported	0000h

Block Name	Hex Addr	Size	Access Type	16 Bits	Register Name	Description	Initial Value
VR 1 Host Lanes	A400	16	Read Only	15-0	Host Lane FAWS Registers	Not supported	0000h
	A410	16	Read, COR	15-0	Host Lane FAWS Registers - Latched	Not supported	0000h
	A420	16	Read Write	15-0	Host Lane FAWS Registers - Enable	Not supported	0000h
	A430	16	Read Only	15-0	Host Lane PRBS Tx Error Count	Not supported	0000h
	A440	1	Read Write	15	Lane 0: Host Lane EQ Control Mode	1b = Fixed in manual mode	D807h
			Read Write	14-8	Lane 0: Host Lane Equalization Value		
			Read Only	7-4	Reserved	Not supported	
			Read Write	3-0	Lane 0: Host Lane Pre/De Emphasis Value		
	A441	1	Read Only	15	Lane 1: Host Lane EQ Control Mode	1b = Fixed in manual mode	D807h
			Read Write	14-8	Lane 1: Host Lane Equalization Value		
			Read Only	7-4	Reserved	Not supported	
			Read Write	3-0	Lane 1: Host Lane Pre/De Emphasis Value		
	A442	1	Read Only	15	Lane 2: Host Lane EQ Control	1b = Fixed in manual mode	D807h
			Read Write	14-8	Lane 2: Host Lane Equalization		
			Read Only	7-4	Reserved	Not supported	
			Read Write	3-0	Lane 2: Host Lane Pre/De Emphasis		
	A443	1	Read Only	15	Lane 3: Host Lane EQ Control	1b = Fixed in manual mode	D807h
			Read Write	14-8	Lane 3: Host Lane Equalization		
			Read Only	7-4	Reserved	Not supported	
			Read Write	3-0	Lane 3: Host Lane Pre/De Emphasis		
	A444	1	Read Only	15	Lane 4: Host Lane EQ Control	1b = Fixed in manual mode	D807h
			Read Write	14-8	Lane 4: Host Lane Equalization		
			Read Only	7-4	Reserved	Not supported	
			Read Write	3-0	Lane 4: Host Lane Pre/De Emphasis		
	A445	1	Read Only	15	Lane 5: Host Lane EQ Control	1b = Fixed in manual mode	D807h
			Read Write	14-8	Lane 5: Host Lane Equalization		
			Read Only	7-4	Reserved	Not supported	
			Read Write	3-0	Lane 5: Host Lane Pre/De Emphasis		
	A446	1	Read Only	15	Lane 6: Host Lane EQ Control	1b = Fixed in manual mode	D807h
			Read Write	14-8	Lane 6: Host Lane Equalization		
			Read Only	7-4	Reserved	Not supported	
			Read Write	3-0	Lane 6: Host Lane Pre/De Emphasis		
	A447	1	Read Only	15	Lane 7: Host Lane EQ Control	1b = Fixed in manual mode	D807h
			Read Write	14-8	Lane 7: Host Lane Equalization		
			Read Only	7-4	Reserved	Not supported	
			Read Write	3-0	Lane 7: Host Lane Pre/De Emphasis		
	A448	1	Read Only	15	Lane 8: Host Lane EQ Control	1b = Fixed in manual mode	D807h
			Read Write	14-8	Lane 8: Host Lane Equalization		
			Read Only	7-4	Reserved	Not supported	
			Read Write	3-0	Lane 8: Host Lane Pre/De Emphasis		
	A449	1	Read Only	15	Lane 9: Host Lane EQ Control	1b = Fixed in manual mode	D807h
			Read Write	14-8	Lane 9: Host Lane Equalization		
			Read Only	7-4	Reserved	Not supported	
			Read Write	3-0	Lane 9: Host Lane Pre/De Emphasis		
	A44A	1	Read Only	15-0	Lane 10: Host Lane Pre/De Emphasis	Not supported	00h
	A44B	1	Read Only	15-0	Lane 11: Host Lane Pre/De Emphasis	Not supported	00h
	A44C	1	Read Only	15-0	Lane 12: Host Lane Pre/De Emphasis	Not supported	00h
	A44D	1	Read Only	15-0	Lane 13: Host Lane Pre/De Emphasis	Not supported	00h
	A44E	1	Read Only	15-0	Lane 14: Host Lane Pre/De Emphasis	Not supported	00h
	A44F	1	Read Only	15-0	Lane 15: Host Lane Pre/De Emphasis	Not supported	00h
	A450	48	Read Only	15-0	Reserved		
Common Data Block	AC00 to AFFF	1024	Read Write	15-0	Common Data Block Registers	Supported	00h

Case Temperature Definition
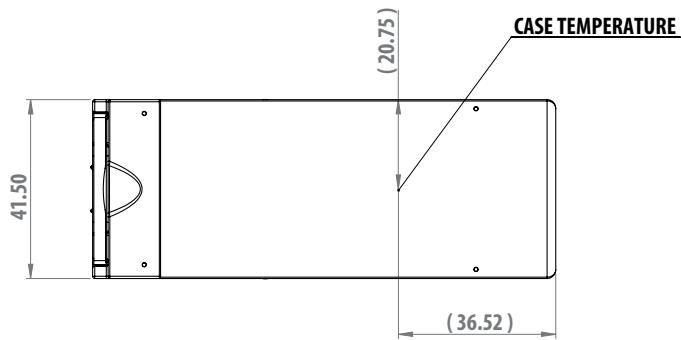
CFP2 Mechanical Outline

Bail Latch Color is Beige with one center black band to indicate 10G/fiber operation, 100GE-SR10 compliance and 100 m OM3 Multi-Mode fiber (150 m OM4) capability
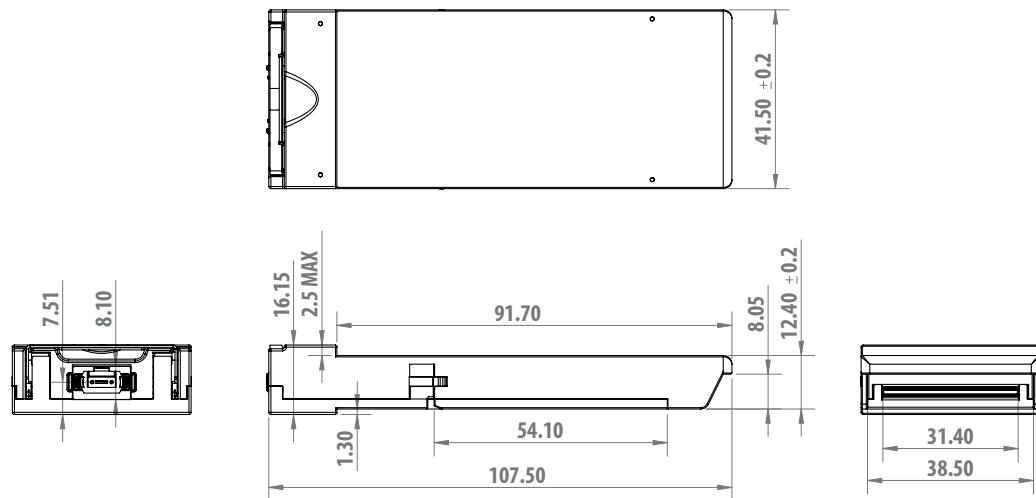
ALL DIMENSIONS ARE IN MM

CFP2 Module Insertion, Extraction Forces

Parameter	Maximum	Unit	Notes
Maximum Insertion Force	80	N	Without Heat Sink
Maximum Extraction Force	50	N	Without Heat Sink
Minimum Retention Force	90	N	No damage to module below 90 N
Minimum Cage Retention Force	180	N	No damage to cage latch below 180 N

Table 1. Permissible Range for Host-Configured Receive Optical Power Threshold

Address (Hex)	Description	Raw data (dBm)	Value (Hex)
80E8	Host configured receive optical power high alarm permissible minimum threshold (mW)	1.74	0043
80E9	(dBm)	2.4	00E2
80EA	Host configured receive optical power high warning permissible minimum threshold	1.38	0035
80EB	(dBm)	1.4	00EB
80EC	Host configured receive optical power low warning permissible minimum threshold (mW)	0.09	0003
80ED	(dBm)	-10.5	007B
80EE	Host configured receive optical power low alarm permissible minimum threshold (mW)	0.06	0002
80EF	(dBm)	-12.5	0032
80F0	Host configured receive optical power high alarm permissible maximum threshold (mW)	2.75	006B
80F1	(dBm)	4.4	0096
80F2	Host configured receive optical power high warning permissible maximum threshold (mW)	2.19	0055
80F3	(dBm)	3.4	0075
80F4	Host configured receive optical power low warning permissible maximum threshold (mW)	0.14	0005
80F5	(dBm)	-8.5	0084
80F6	Host configured receive optical power low alarm permissible maximum threshold (mW)	0.09	0003
80F7	(dBm)	-10.5	007B

Note:
Host-programmed A/W levels should be constrained as:
- High Alarm Level > High Warning Level
- Low Alarm Level < Low Warning Level
(Accordingly, the warning for High or Low will be asserted if the alarm for High or Low is asserted.)

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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