

74LVC2G08-Q100

Dual 2-input AND gate

Rev. 3 — 28 January 2019

Product data sheet

1. General description

The 74LVC2G08-Q100 provides a 2-input AND gate function.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of the 74LVC2G08-Q100 as a translator in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant outputs for interfacing with 5 V logic
- High noise immunity
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8-B/JESD36 (2.7 V to 3.6 V)
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V ($C = 200$ pF, $R = 0$ Ω)
- Multiple package options

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|------------------|-------------------|--------|---|----------|
| | Temperature range | Name | Description | |
| 74LVC2G08DP-Q100 | -40 °C to +125 °C | TSSOP8 | plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm | SOT505-2 |
| 74LVC2G08DC-Q100 | -40 °C to +125 °C | VSSOP8 | plastic very thin shrink small outline package; 8 leads; body width 2.3 mm | SOT765-1 |
| 74LVC2G08GS-Q100 | -40 °C to +125 °C | XSON8 | extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1.0 x 0.35 mm | SOT1203 |

4. Marking

Table 2. Marking codes

| Type number | Marking code ^[1] |
|------------------|-----------------------------|
| 74LVC2G08DP-Q100 | V08 |
| 74LVC2G08DC-Q100 | V08 |
| 74LVC2G08GS-Q100 | VE |

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

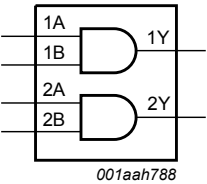


Fig. 1. Logic symbol

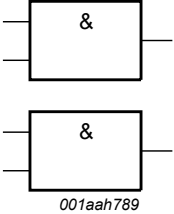


Fig. 2. IEC logic symbol

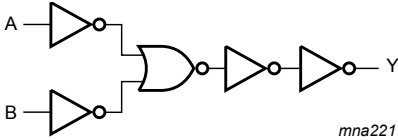


Fig. 3. Logic diagram (one gate)

6. Pinning information

6.1. Pinning

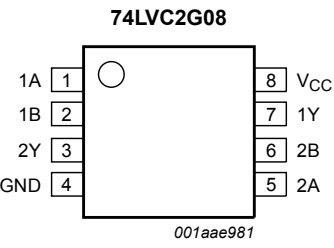


Fig. 4. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

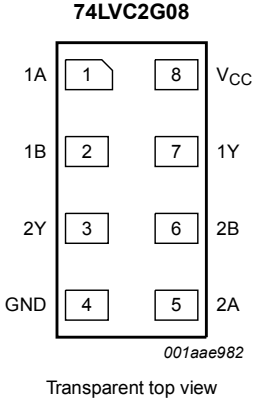


Fig. 5. Pin configuration SOT1203 (XSON8)

6.2. Pin description

Table 3. Pin description

| Symbol | Pin | Description |
|-----------------|-----|----------------|
| 1A | 1 | data input |
| 1B | 2 | data input |
| 2Y | 3 | data output |
| GND | 4 | ground (0 V) |
| 2A | 5 | data input |
| 2B | 6 | data input |
| 1Y | 7 | data output |
| V _{CC} | 8 | supply voltage |

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

| Input | | Output |
|-------|----|--------|
| nA | nB | nY |
| L | X | L |
| X | L | L |
| H | H | H |

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|--|----------|-----------------------|------|
| V _{CC} | supply voltage | | -0.5 | +6.5 | V |
| V _I | input voltage | | [1] -0.5 | +6.5 | V |
| V _O | output voltage | Active mode | [1] -0.5 | V _{CC} + 0.5 | V |
| | | Power-down mode; V _{CC} = 0 V | [1] -0.5 | +6.5 | V |
| I _{IK} | input clamping current | V _I < 0 V | -50 | - | mA |
| I _{OK} | output clamping current | V _O < 0 V or V _O > V _{CC} | - | ±50 | mA |
| I _O | output current | V _O = 0 V to V _{CC} | - | ±50 | mA |
| I _{CC} | supply current | | - | 100 | mA |
| I _{GND} | ground current | | -100 | - | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| P _{tot} | total power dissipation | T _{amb} = -40 °C to +125 °C | [2] - | 300 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly at 2.5 mW/K.
 For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly at 8 mW/K.
 For XSON8 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Operating conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|-------------------------------------|---------------------------------|------|----------|------|
| V_{CC} | supply voltage | | 1.65 | 5.5 | V |
| V_I | input voltage | | 0 | 5.5 | V |
| V_O | output voltage | Active mode | 0 | V_{CC} | V |
| | | Power-down mode; $V_{CC} = 0$ V | 0 | 5.5 | V |
| T_{amb} | ambient temperature | | -40 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 1.65$ V to 2.7 V | - | 20 | ns/V |
| | | $V_{CC} = 2.7$ V to 5.5 V | - | 10 | ns/V |

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---------------------------|--|----------------------|-----------|----------------------|---------|
| $T_{amb} = -40$ °C to $+85$ °C | | | | | | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 1.65$ V to 1.95 V | $0.65 \times V_{CC}$ | - | - | V |
| | | $V_{CC} = 2.3$ V to 2.7 V | 1.7 | - | - | V |
| | | $V_{CC} = 2.7$ V to 3.6 V | 2.0 | - | - | V |
| | | $V_{CC} = 4.5$ V to 5.5 V | $0.7 \times V_{CC}$ | - | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 1.65$ V to 1.95 V | - | - | $0.35 \times V_{CC}$ | V |
| | | $V_{CC} = 2.3$ V to 2.7 V | - | - | 0.7 | V |
| | | $V_{CC} = 2.7$ V to 3.6 V | - | - | 0.8 | V |
| | | $V_{CC} = 4.5$ V to 5.5 V | - | - | $0.3 \times V_{CC}$ | V |
| V_{OH} | HIGH-level output voltage | $V_I = V_{IH}$ or V_{IL} | | | | |
| | | $I_O = -100$ μ A; $V_{CC} = 1.65$ V to 5.5 V | $V_{CC} - 0.1$ | - | - | V |
| | | $I_O = -4$ mA; $V_{CC} = 1.65$ V | 1.2 | 1.53 | - | V |
| | | $I_O = -8$ mA; $V_{CC} = 2.3$ V | 1.9 | 2.13 | - | V |
| | | $I_O = -12$ mA; $V_{CC} = 2.7$ V | 2.2 | 2.50 | - | V |
| | | $I_O = -24$ mA; $V_{CC} = 3.0$ V | 2.3 | 2.60 | - | V |
| | | $I_O = -32$ mA; $V_{CC} = 4.5$ V | 3.8 | 4.10 | - | V |
| V_{OL} | LOW-level output voltage | $V_I = V_{IH}$ or V_{IL} | | | | |
| | | $I_O = 100$ μ A; $V_{CC} = 1.65$ V to 5.5 V | - | - | 0.1 | V |
| | | $I_O = 4$ mA; $V_{CC} = 1.65$ V | - | 0.08 | 0.45 | V |
| | | $I_O = 8$ mA; $V_{CC} = 2.3$ V | - | 0.14 | 0.3 | V |
| | | $I_O = 12$ mA; $V_{CC} = 2.7$ V | - | 0.19 | 0.4 | V |
| | | $I_O = 24$ mA; $V_{CC} = 3.0$ V | - | 0.37 | 0.55 | V |
| $I_O = 32$ mA; $V_{CC} = 4.5$ V | - | 0.43 | 0.55 | V | | |
| I_I | input leakage current | $V_I = 5.5$ V or GND; $V_{CC} = 0$ V to 5.5 V | - | ± 0.1 | ± 1 | μ A |
| I_{OFF} | power-off leakage current | V_I or $V_O = 5.5$ V; $V_{CC} = 0$ V | - | ± 0.1 | ± 2 | μ A |
| I_{CC} | supply current | $V_I = 5.5$ V or GND; $V_{CC} = 1.65$ V to 5.5 V; $I_O = 0$ A | - | 0.1 | 4 | μ A |

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---------------------------|---|----------------------|--------|----------------------|---------------|
| ΔI_{CC} | additional supply current | per pin; $V_I = V_{CC} - 0.6 \text{ V}$; $I_O = 0 \text{ A}$; $V_{CC} = 2.3 \text{ V to } 5.5 \text{ V}$ | - | 5 | 500 | μA |
| C_i | input capacitance | | - | 2.5 | - | pF |
| $T_{\text{amb}} = -40 \text{ }^\circ\text{C to } +125 \text{ }^\circ\text{C}$ | | | | | | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | $0.65 \times V_{CC}$ | - | - | V |
| | | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 1.7 | - | - | V |
| | | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ | 2.0 | - | - | V |
| | | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | $0.7 \times V_{CC}$ | - | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | - | - | $0.35 \times V_{CC}$ | V |
| | | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | - | - | 0.7 | V |
| | | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ | - | - | 0.8 | V |
| | | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ | - | - | $0.3 \times V_{CC}$ | V |
| V_{OH} | HIGH-level output voltage | $V_I = V_{IH} \text{ or } V_{IL}$ | | | | |
| | | $I_O = -100 \mu\text{A}$; $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$ | $V_{CC} - 0.1$ | - | - | V |
| | | $I_O = -4 \text{ mA}$; $V_{CC} = 1.65 \text{ V}$ | 0.95 | - | - | V |
| | | $I_O = -8 \text{ mA}$; $V_{CC} = 2.3 \text{ V}$ | 1.7 | - | - | V |
| | | $I_O = -12 \text{ mA}$; $V_{CC} = 2.7 \text{ V}$ | 1.9 | - | - | V |
| | | $I_O = -24 \text{ mA}$; $V_{CC} = 3.0 \text{ V}$ | 2.0 | - | - | V |
| | | $I_O = -32 \text{ mA}$; $V_{CC} = 4.5 \text{ V}$ | 3.4 | - | - | V |
| V_{OL} | LOW-level output voltage | $V_I = V_{IH} \text{ or } V_{IL}$ | | | | |
| | | $I_O = 100 \mu\text{A}$; $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$ | - | - | 0.1 | V |
| | | $I_O = 4 \text{ mA}$; $V_{CC} = 1.65 \text{ V}$ | - | - | 0.70 | V |
| | | $I_O = 8 \text{ mA}$; $V_{CC} = 2.3 \text{ V}$ | - | - | 0.45 | V |
| | | $I_O = 12 \text{ mA}$; $V_{CC} = 2.7 \text{ V}$ | - | - | 0.60 | V |
| | | $I_O = 24 \text{ mA}$; $V_{CC} = 3.0 \text{ V}$ | - | - | 0.80 | V |
| | | $I_O = 32 \text{ mA}$; $V_{CC} = 4.5 \text{ V}$ | - | - | 0.80 | V |
| I_I | input leakage current | $V_I = 5.5 \text{ V or GND}$; $V_{CC} = 0 \text{ V to } 5.5 \text{ V}$ | - | - | ± 1 | μA |
| I_{OFF} | power-off leakage current | $V_I \text{ or } V_O = 5.5 \text{ V}$; $V_{CC} = 0 \text{ V}$ | - | - | ± 2 | μA |
| I_{CC} | supply current | $V_I = 5.5 \text{ V or GND}$; $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$; $I_O = 0 \text{ A}$ | - | - | 4 | μA |
| ΔI_{CC} | additional supply current | per pin; $V_I = V_{CC} - 0.6 \text{ V}$; $I_O = 0 \text{ A}$; $V_{CC} = 2.3 \text{ V to } 5.5 \text{ V}$ | - | - | 500 | μA |

[1] All typical values are measured at $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|-----------------|-------------------------------|---|------------------|--------|-----|-------------------|------|------|
| | | | Min | Typ[1] | Max | Min | Max | |
| t _{pd} | propagation delay | nA, nB to nY; see Fig. 6 [2] | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 1.0 | 3.2 | 9.0 | 1.0 | 11.3 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 0.5 | 2.2 | 5.1 | 0.5 | 6.4 | ns |
| | | V _{CC} = 2.7 V | 1.0 | 2.5 | 5.3 | 1.0 | 6.7 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 0.5 | 2.1 | 4.7 | 0.5 | 5.9 | ns |
| | | V _{CC} = 4.5 V to 5.5 V | 0.5 | 1.7 | 3.8 | 0.5 | 4.8 | ns |
| C _{PD} | power dissipation capacitance | per gate; V _I = GND to V _{CC} [3] | - | 14.4 | - | - | - | pF |

[1] Typical values are measured at nominal V_{CC} and at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

∑(C_L × V_{CC}² × f_o) = sum of outputs.

11.1. Waveforms and test circuit

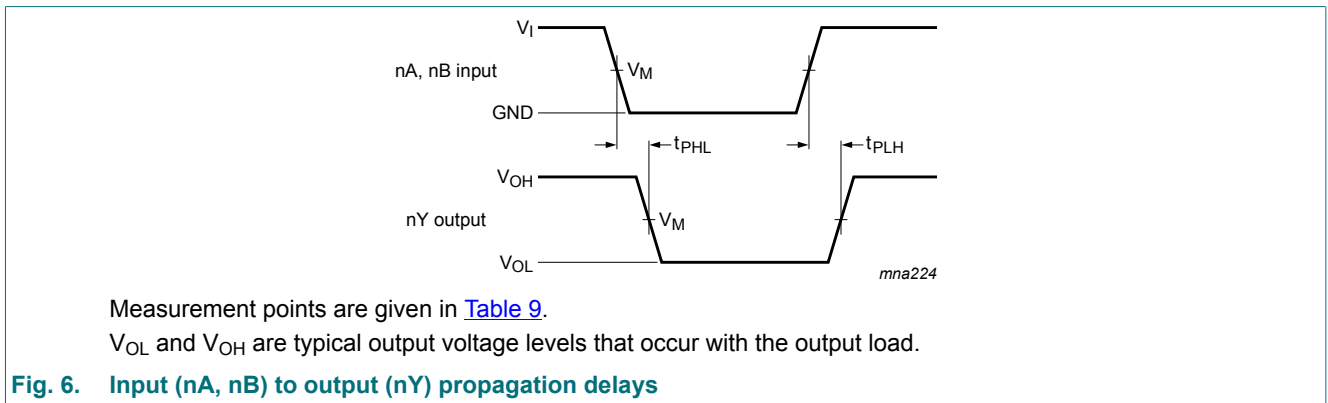


Table 9. Measurement points

| Supply voltage | Input | Output |
|------------------|---------------------|---------------------|
| V_{CC} | V_M | V_M |
| 1.65 V to 1.95 V | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ |
| 2.3 V to 2.7 V | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ |
| 2.7 V | 1.5 V | 1.5 V |
| 3.0 V to 3.6 V | 1.5 V | 1.5 V |
| 4.5 V to 5.5 V | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ |

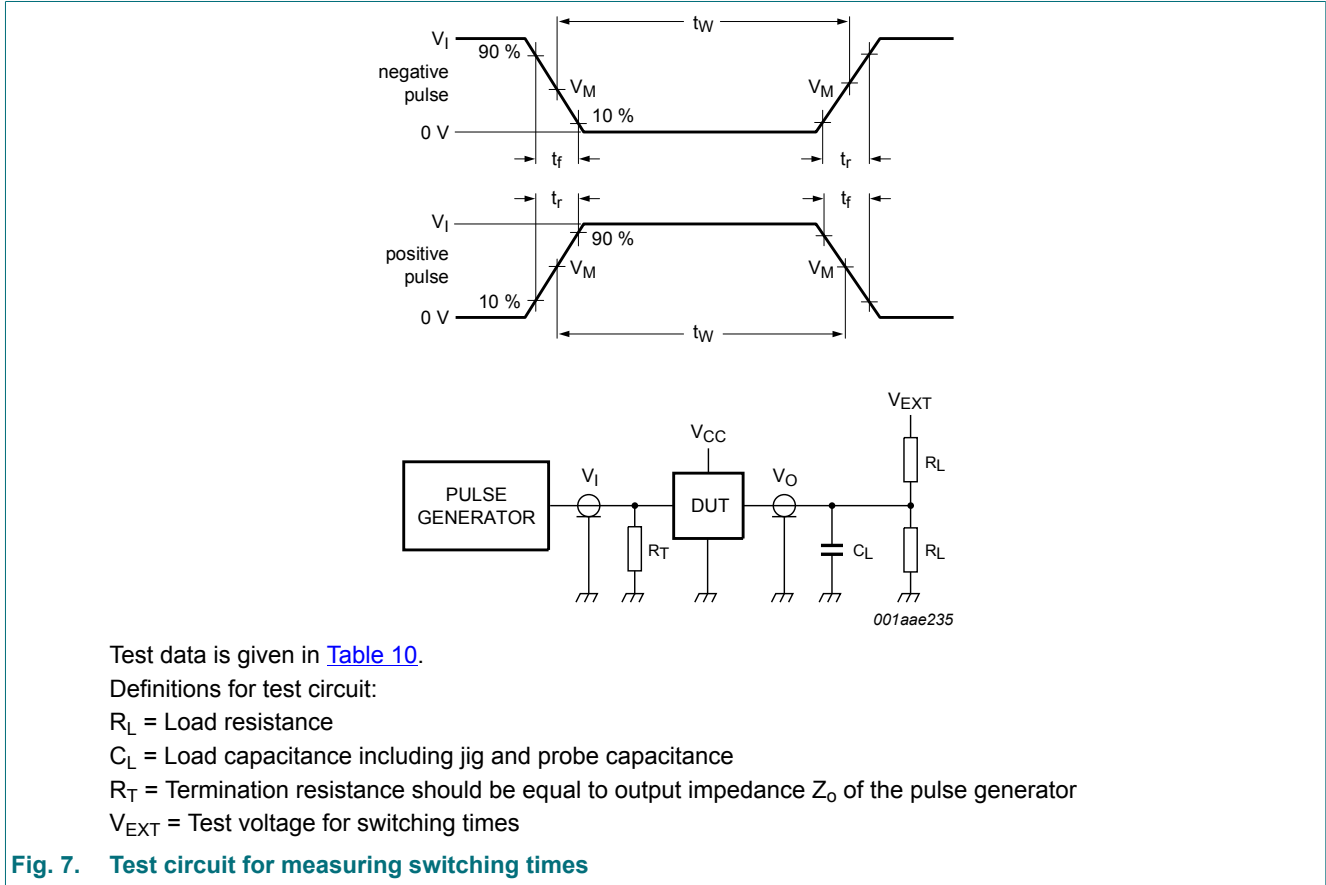


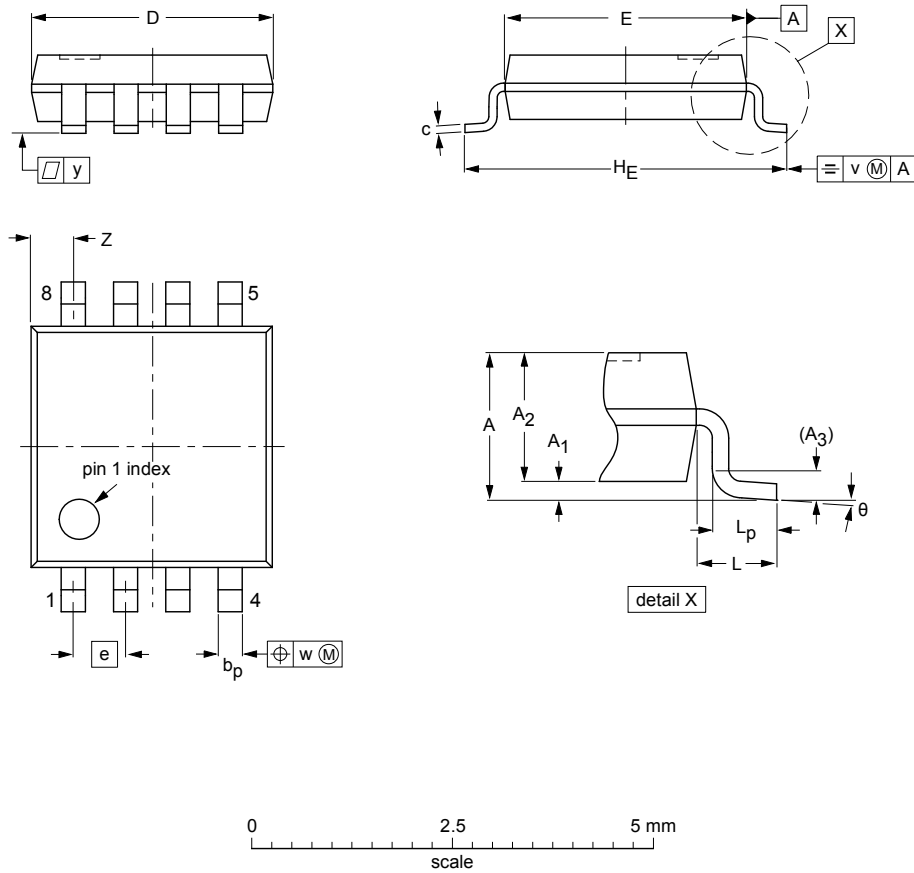
Fig. 7. Test circuit for measuring switching times

Table 10. Test data

| Supply voltage | Input | Load | V_{EXT} |
|------------------|----------|-------|--------------------|
| V_{CC} | V_I | C_L | t_{PLH}, t_{PHL} |
| 1.65 V to 1.95 V | V_{CC} | 30 pF | open |
| 2.3 V to 2.7 V | V_{CC} | 30 pF | open |
| 2.7 V | 2.7 V | 50 pF | open |
| 3.0 V to 3.6 V | 2.7 V | 50 pF | open |
| 4.5 V to 5.5 V | V_{CC} | 50 pF | open |

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | v | w | y | Z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|-----|----------------|-----|------|-----|------------------|----------|
| mm | 1.1 | 0.15 0.00 | 0.95 0.75 | 0.25 | 0.38 0.22 | 0.18 0.08 | 3.1 2.9 | 3.1 2.9 | 0.65 | 4.1 3.9 | 0.5 | 0.47 0.33 | 0.2 | 0.13 | 0.1 | 0.70 0.35 | 8° 0° |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|-------|--|---------------------|------------|
| | IEC | JEDEC | JEITA | | | |
| SOT505-2 | | --- | | | | 02-01-16 |

Fig. 8. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1



Dimensions (mm are the original dimensions)

| Unit | A _{max.} | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽²⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|-------------------|----------------|----------------|----------------|----------------|------|------------------|------------------|-----|----------------|-----|----------------|------|-----|------|-----|------------------|----|
| max | 0.15 | 0.85 | | | 0.27 | 0.23 | 2.1 | 2.4 | | 3.2 | | 0.40 | 0.21 | | | | 0.4 | 8° |
| mm | nom | 1 | | 0.12 | | | | | 0.5 | | 0.4 | | | 0.2 | 0.08 | 0.1 | | |
| | min | | 0.00 | 0.60 | 0.17 | 0.08 | 1.9 | 2.2 | | 3.0 | | 0.15 | 0.19 | | | | 0.1 | 0° |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

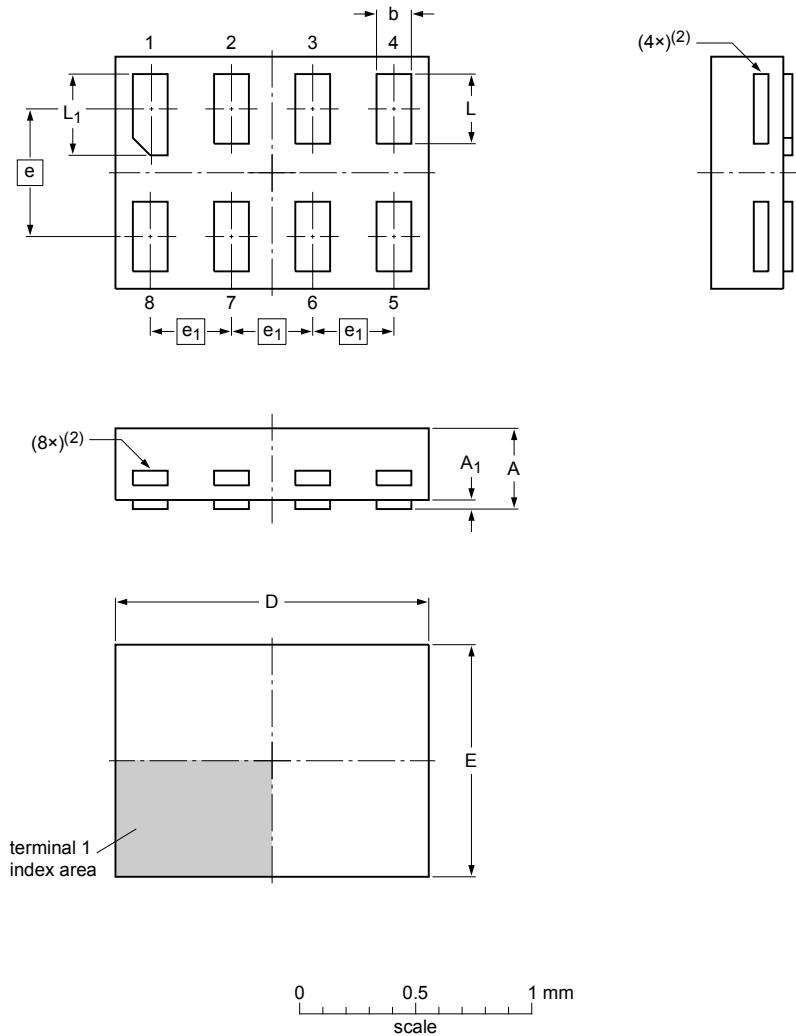
sot765-1_po

| Outline version | References | | | European projection | Issue date |
|-----------------|------------|--------|-------|---------------------|-------------------|
| | IEC | JEDEC | JEITA | | |
| SOT765-1 | | MO-187 | | | 07-06-02-16-05-31 |

Fig. 9. Package outline SOT765-1 (VSSOP8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1.0 x 0.35 mm

SOT1203



Dimensions

| Unit | A ⁽¹⁾ | A ₁ | b | D | E | e | e ₁ | L | L ₁ |
|------|------------------|----------------|------|------|------|------|----------------|------|----------------|
| mm | max 0.35 | 0.04 | 0.20 | 1.40 | 1.05 | | | 0.35 | 0.40 |
| | nom | | 0.15 | 1.35 | 1.00 | 0.55 | 0.35 | 0.30 | 0.35 |
| | min | | 0.12 | 1.30 | 0.95 | | | 0.27 | 0.32 |

Note

- Including plating thickness.
- Visible depending upon used manufacturing technology.

sot1203_po

| Outline version | References | | | | European projection | Issue date |
|-----------------|------------|-------|-------|--|---------------------|------------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT1203 | | | | | | -10-04-02- 10-04-06 |

Fig. 10. Package outline SOT1203 (XSON8)

13. Abbreviations

Table 11. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MIL | Military |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 12. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|--------------------|--|--------------------|---------------|--------------------|
| 74LVC2G08_Q100 v.3 | 20190128 | Product data sheet | - | 74LVC2G08_Q100 v.2 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Added type number 74LVC2G08GS-Q100 (SOT1203/XSON8). | | | |
| 74LVC2G08_Q100 v.2 | 20161214 | Product data sheet | - | 74LVC2G08_Q100 v.1 |
| Modifications: | <ul style="list-style-type: none"> Table 7: The maximum limits for leakage current and supply current have changed. | | | |
| 74LVC2G08_Q100 v.1 | 20130626 | Product data sheet | - | - |

15. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

Definitions

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