

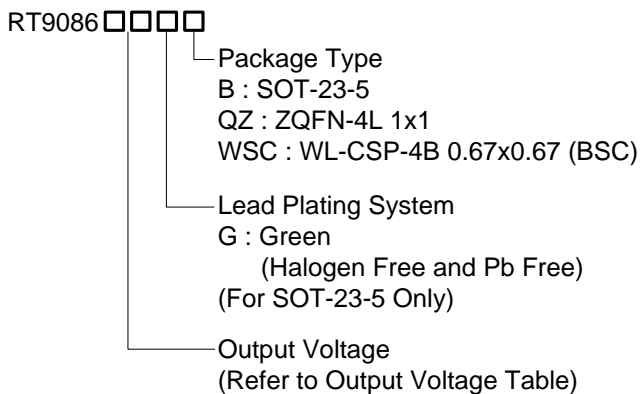
250mA, Ultra-Low Noise, Low Quiescent Current, LDO Regulator

General Description

The RT9086 is a high performance positive low dropout (LDO) regulator designed for applications requiring very low dropout voltage and ultra-high Power Supply Ripple Rejection (PSRR) low noise, low quiescent current that can supply up to 250mA output current. The input voltage range is from 2.2V to 5.5V. The device is designed to work with a 1 μ F input and a 1 μ F output ceramic capacitor (no separate noise bypass capacitor is required).

The RT9086 features a precise 2% output regulation over line, load, and temperature variations in WL-CSP-4B 0.67x0.67 (BSC) package. The output voltage is available from 1.2V to 4.5V in 25mV steps.

Ordering Information

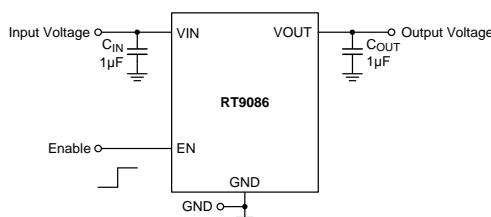


Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Simplified Application Circuit



Features

- Input Voltage Range : 2.2V to 5.5V
- Adjustable Output Voltage : 1.2V to 4.5V
- PSRR
 - ▶ 85dB @ 1kHz (20mA)
 - ▶ 80dB @ 10kHz (20mA)
- Output Current : 250mA
- Very Low Dropout : 120mV
- Very Low I_Q (Enabled) : 16 μ A
- Virtually Zero I_Q (Disable) : < 1 μ A
- Very Low I_G (Enabled) : 16 μ A
- Start-up Time : 80 μ s
- -40°C to 125°C Operating Junction Temperature Range
- Excellent Noise Immunity
- Fast Response Overload and Line Transient
- Stable with a 1 μ F Input and Output Ceramic Capacitors
- Accurate Output Voltage 2% Overload, Line, Process, and Temperature Variations
- Over-Current Protection
- Over-Temperature Protection

Applications

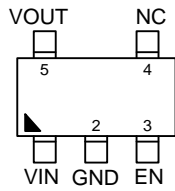
- Mobile Phones, Tablets
- Digital Cameras and Audio Devices
- Portable and Battery-Powered Equipment
- Portable Medical Equipment
- Smart Meters
- IP Cameras
- Drones
- Telecom/Networking Cards
- Wireless Infrastructures
- Medical Equipments

Marking Information

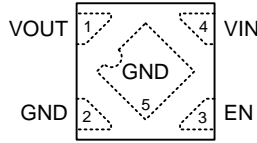
For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Pin Configuration

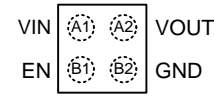
(TOP VIEW)



SOT-23-5



ZQFN-4L 1x1



WL-CSP-4B 0.67x0.67 (BSC)

Functional Pin Description

Pin No.			Pin Name	Pin Function
SOT-23-5	ZQFN-4L 1x1	WL-CSP-4B 0.67x0.67		
1	4	A1	VIN	Supply input. A minimum of 1 μ F ceramic capacitor should be placed as close as possible to this pin for better noise rejection.
2	2	B2	GND	Common ground.
3	3	B1	EN	Enable control input. Connecting this pin to logic high enables the regulator or driving this pin low puts it into shutdown mode. EN can be connected to GND if not used.
4	--	--	NC	No internal connection.
5	1	A2	VOUT	Output of the regulator. Decouple this pin to GND with at least 1 μ F for stability.
--	5 (Exposed Pad)	--	GND	Thermal pad for ZQFN-4L 1x1 package, connect to GND.

RT9086 Output Voltage Table

V_{OUT} = 1.2V to 1.575V	
V_{OUT}	Output Voltage Code
1.2	12
1.225	1A
1.25	1B
1.275	1C
1.3	13
1.325	1D
1.35	1E
1.375	1F
1.4	14
1.425	1G
1.45	1H
1.475	1J
1.5	15
1.525	1K
1.55	1M
1.575	1N

V_{OUT} = 1.6V to 1.975V	
V_{OUT}	Output Voltage Code
1.6	16
1.625	1P
1.65	1Q
1.675	1R
1.7	17
1.725	1S
1.75	1T
1.775	1U
1.8	18
1.825	1V
1.85	1W
1.875	1Y
1.9	19
1.925	1Z
1.95	2A
1.975	2B

V_{OUT} = 2V to 2.375V	
V_{OUT}	Output Voltage Code
2	20
2.025	2C
2.05	2D
2.075	2E
2.1	21
2.125	2F
2.15	2G
2.175	2H
2.2	22
2.225	2J
2.25	2K
2.275	2M
2.3	23
2.325	2N
2.35	2P
2.375	2Q

V_{OUT} = 2.4V to 2.775V	
V_{OUT}	Output Voltage Code
2.4	24
2.425	2R
2.45	2S
2.475	2T
2.5	25
2.525	2U
2.55	2V
2.575	2W
2.6	26
2.625	2Y
2.65	2Z
2.675	3A
2.7	27
2.725	3B
2.75	3C
2.775	3D

V_{OUT} = 2.8V to 3.175V	
V_{OUT}	Output Voltage Code
2.8	28
2.825	3E
2.85	3F
2.875	3G
2.9	29
2.925	3H
2.95	3J
2.975	3K
3	30
3.025	3M
3.05	3N
3.075	3P
3.1	31
3.125	3Q
3.15	3R
3.175	3S

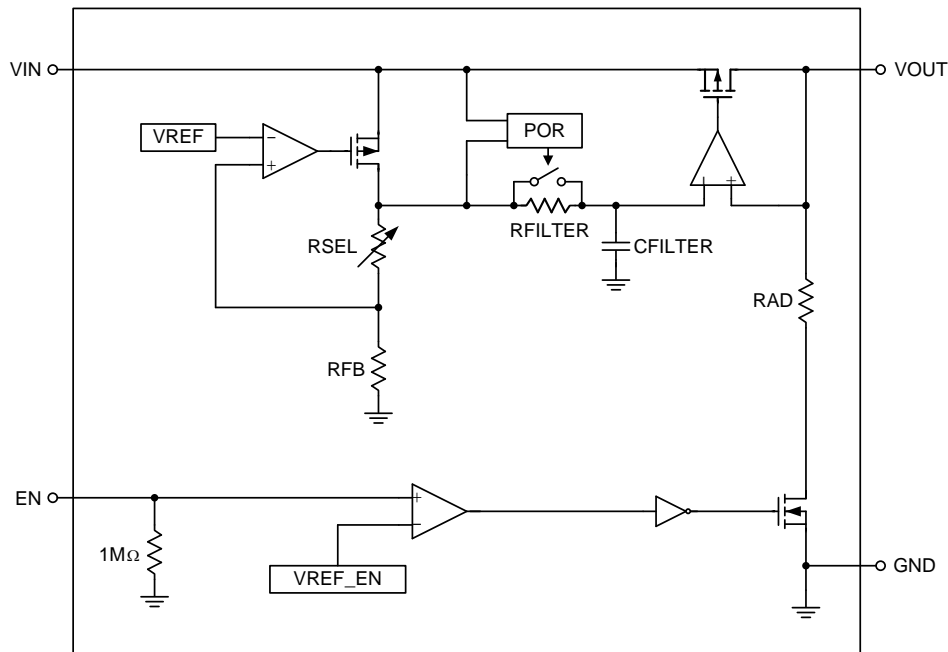
V_{OUT} = 3.2V to 3.575V	
V_{OUT}	Output Voltage Code
3.2	32
3.225	3T
3.25	3U
3.275	3V
3.3	33
3.325	3W
3.35	3Y
3.375	3Z
3.4	34
3.425	4A
3.45	4B
3.475	4C
3.5	35
3.525	4D
3.55	4E
3.575	4F

V _{OUT} = 3.6V to 3.975V	
V _{OUT}	Output Voltage Code
3.6	36
3.625	4G
3.65	4H
3.675	4J
3.7	37
3.725	4K
3.75	4M
3.775	4N
3.8	38
3.825	4P
3.85	4Q
3.875	4R
3.9	39
3.925	4S
3.95	4T
3.975	4U

V _{OUT} = 4V to 4.375V	
V _{OUT}	Output Voltage Code
4	40
4.025	4V
4.05	4W
4.075	4Y
4.1	41
4.125	4Z
4.15	5A
4.175	5B
4.2	42
4.225	5C
4.25	5D
4.275	5E
4.3	43
4.325	5F
4.35	5G
4.375	5H

V _{OUT} = 4.4V to 4.5V	
V _{OUT}	Output Voltage Code
4.4	44
4.425	5J
4.45	5K
4.475	5M
4.5	45

Functional Block Diagram



Operation

Basic Operation

The RT9086 is a high performance positive low dropout (LDO) regulator designed for applications requiring very low dropout voltage, ultra-high Power Supply Ripple Rejection (PSRR), low noise and low quiescent current that can supply up to 250mA output current. The input voltage range is from 2.2V to 5.5V. The RT9086 features a precise 2% output regulation over line, load, and temperature variations. The output voltage is available from 1.2V to 4.5V in 25mV steps. The minimum required output capacitance for stable operation is 1μF (X5R or X7R) effective capacitance after consideration of the temperature and voltage coefficient of the capacitor.

Enable and Shutdown Operation

The RT9086 goes into shutdown mode when the EN pin is in a logic low condition. In this condition, the pass transistor, error amplifier, and bandgap are all turned off, reducing the supply current to only 1μA (max.). If the shutdown mode is not required, the EN pin can be directly tied to VIN pin to keep the LDO on.

Over-Temperature Protection (OTP)

The over-temperature protection function will turn off the P-MOSFET when the junction temperature exceeds 160°C (typ.), and the output current exceeds 250mA. Once the junction temperature cools down by approximately 26°C (typ.), the regulator will automatically resume operation.

Current Limit Protection

The RT9086 provides current limit function to prevent the device from damages during overload or shorted-circuit condition. This current is detected by an internal sensing transistor.

Error Amplifier

The Error Amplifier compares the internal reference voltage with the output feedback voltage from the internal divider, and controls the Gate voltage of P-MOSFET to support good line regulation and load regulation at output voltage.

Output Automatic Discharge

The RT9086 output employs an internal 10Ω (typ.) pulldown resistance to discharge the output when the EN pin is low, and the device is disabled.

Absolute Maximum Ratings (Note 1)

- VIN, EN to GND ----- -0.3V to 6V
- VOUT to GND ----- -0.3V to 6V
- Power Dissipation, PD @ TA = 25°C
 - SOT-23-5 ----- 0.45W
 - ZQFN-4L 1x1 ----- 1.07W
 - WL-CSP-4B 0.67x0.67 (BSC) ----- 0.46W
- Package Thermal Resistance (Note 2)
 - SOT-23-5, θJA ----- 218.1°C/W
 - SOT-23-5, θJC ----- 28.5°C/W
 - ZQFN-4L 1x1, θJA ----- 92.7°C/W
 - ZQFN-4L 1x1, θJC ----- 62.3°C/W
 - WL-CSP-4B 0.67x0.67 (BSC), θJA ----- 214.9°C/W
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)
 - HBM (Human Body Model) ----- 2kV

Recommended Operating Conditions (Note 4)

- Input Voltage Range ----- 2.2V to 5.5V
- Output Current ----- 0mA to 250mA
- Ambient Temperature Range ----- -40°C to 85°C
- Junction Temperature Range ----- -40°C to 125°C

Electrical Characteristics

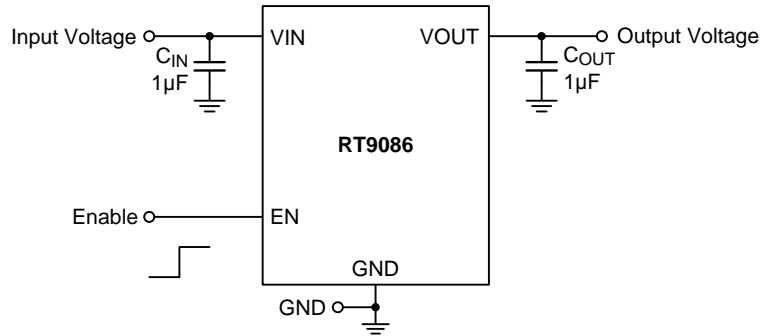
(VIN = VOUT + 1V, VEN = 1.2V, IOUT = 1mA, CIN = 1μF, COUT = 1μF, TA = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage	VIN	VIN = VOUT + 1V	2.2	--	5.5	V
Output Voltage Accuracy (Note 5)	VOUT_ACC	VIN = (VOUT + 1V) to 5.5V, IOUT = 1 mA to 250mA, package : WL-CSP-4B 0.67x0.67 (BSC)	-2	--	2	%VOUT
		VIN = (VOUT + 1V) to 5.5V, IOUT = 1 mA to 250mA, package : SOT-23-5 and ZQFN-4L 1x1	-3	--	3	
Line Regulation	VOUT_LineReg	VIN = (VOUT + 1V) to 5.5V, IOUT = 1mA	--	0.02	--	%/V
Load Regulation	VOUT_LoadReg	IOUT = 1mA to 250mA	--	0.001	--	%/mA
LOAD Current	IOUT	Operation in stable and regulated output voltage	0	--	250	mA
Maximum Output Current	IOUT_MAX		250	--	--	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Current (Note 6)	I _Q	V _{EN} = 1.2V, I _{OUT} = 0mA	--	16	25	μA
		V _{EN} = 1.2V, I _{OUT} = 250mA (Note 7)	--	300	425	
		V _{EN} = 0.3V (Disable)	--	0.2	1	
Ground Current (Note 8)	I _G	V _{EN} = 1.2V, I _{OUT} = 0mA	--	16	--	μA
Dropout Voltage (Note 9)	V _{DROP}	V _{OUT} ≥ 2.2V, I _{OUT} = 100mA	--	50	--	mV
		V _{OUT} ≥ 2.2V, I _{OUT} = 250mA (SOT-23-5 and WL-CSP-4B 0.67x0.67 (BSC) package)	--	120	200	
		V _{OUT} ≥ 2.2V, I _{OUT} = 250mA (ZQFN-4L 1x1 package)	--	--	250	
Power Supply Rejection Ratio (Note 7)	PSRR	f = 100Hz, I _{OUT} = 20mA	--	88	--	dB
		f = 1kHz, I _{OUT} = 20mA	--	85	--	
		f = 10kHz, I _{OUT} = 20mA	--	80	--	
		f = 100kHz, I _{OUT} = 20mA	--	60	--	
Output Noise Voltage (Note 7)	e _N	BW = 10Hz to 100kHz, I _{OUT} = 1mA	--	10	--	μV _{rms}
		BW = 10Hz to 100kHz, I _{OUT} = 250mA	--	6.5	--	
Output Automatic Discharge Pulldown Resistance	R _{AD}	V _{EN} < 0.3V	--	10	--	Ω
EN Pin Logic Input Threshold						
Low Input Threshold	V _{IL}	V _{IN} = 2.2 to 5.5V, V _{EN} falling until the output is disabled	--	--	0.4	V
High Input Threshold	V _{IH}	V _{IN} = 2.2 to 5.5V, V _{EN} rising until the output is enabled	1.2	--	--	V
Input Current at EN PIN	I _{EN}	V _{EN} = 5.5V and V _{IN} = 5.5V	--	5.5	--	μA
		V _{EN} = 0V and V _{IN} = 5.5V	--	0.001	--	
Transient Characteristics						
Line Transient (Note 7)	ΔV _{OUT_Line}	V _{IN} = V _{OUT} + 1V to V _{OUT} + 1.6V in 30μs	-1	--	--	mV
		V _{IN} = V _{OUT} + 1.6V to V _{OUT} + 1V in 30μs	--	--	1	
Load Transient (Note 7)	ΔV _{OUT_Load}	I _{OUT} = 1mA to 250mA in 10μs	-40	--	--	mV
		I _{OUT} = 250mA to 1mA in 10μs	--	--	40	
Overshoot on Start-Up	ΔV _{OUT_Startup}	Stated as a percentage of V _{OUT(NOM)}	--	--	5	%
Start-Up Time	t _{start}	From V _{EN} > V _{IH} to V _{OUT} = 95% of V _{OUT}	--	80	150	μs
Protection						
Short Circuit Current Limit	I _{SC}	Temp = 25°C	250	500	--	mA
Thermal Shutdown	T _{SD}		--	160	--	°C
Thermal Hysteresis	T _{SD_H}		--	26	--	°C

- Note 1.** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
- Note 2.** θ_{JA} is measured under natural convection (still air) at $T_A = 25^\circ\text{C}$ with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the top of the package.
- Note 3.** Devices are ESD sensitive.
- Note 4.** The device is not guaranteed to function outside its operating conditions.
- Note 5.** Maximum available load $I_{OUT_SUPPORT}$ with different V_{IN} due to thermal consideration refers to the curves at Typical Operating Characteristics.
- Note 6.** Quiescent current is defined here as the difference in current between the input voltage source and the load at V_{OUT} .
- Note 7.** This specification is guaranteed by design.
- Note 8.** Ground current is defined here as the total current flowing to ground as a result of all input voltages applied to the device.
- Note 9.** Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100mV below its nominal value.

Typical Application Circuit

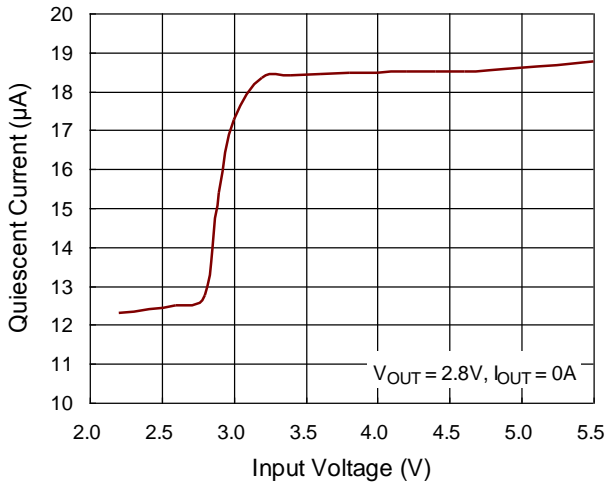


BOM List

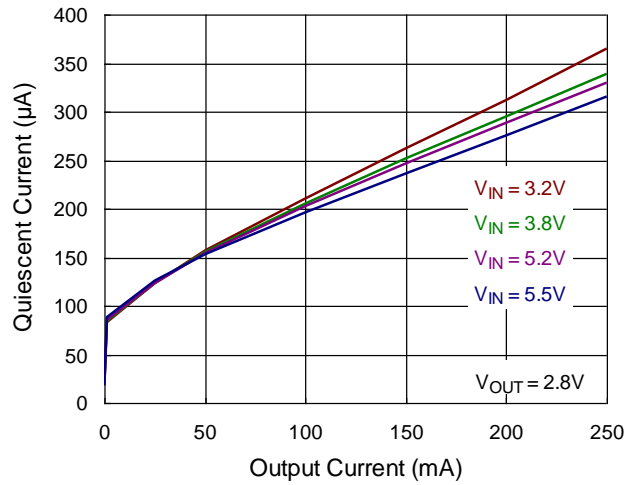
Reference	Part Number	Value	Package	Manufacturer
C _{IN} , C _{OUT}	GRM155R61A105KE01	1µF/10V/X5R	0402	MURATA

Typical Operating Characteristics

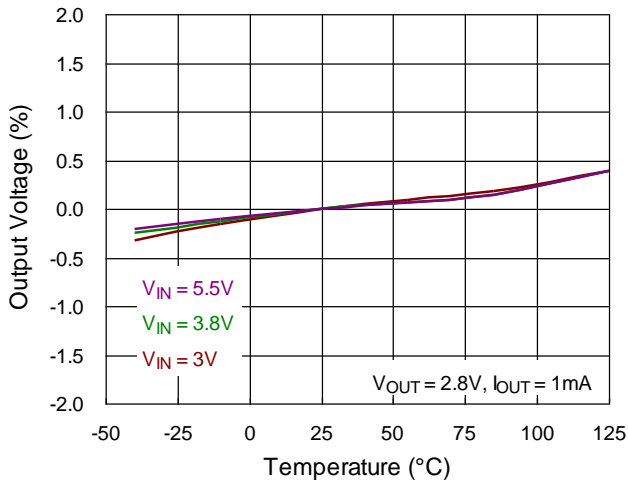
Quiescent Current vs. Input Voltage



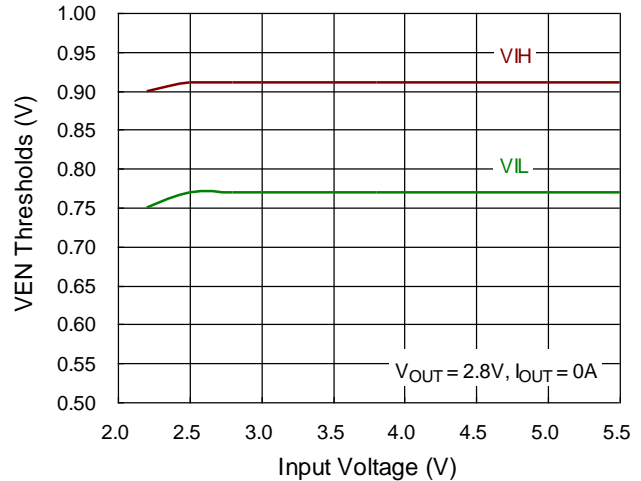
Quiescent Current vs. Output Current



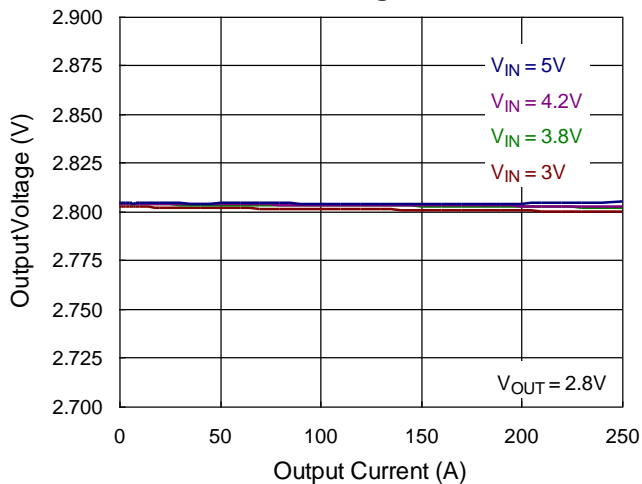
Output Voltage vs. Temperature



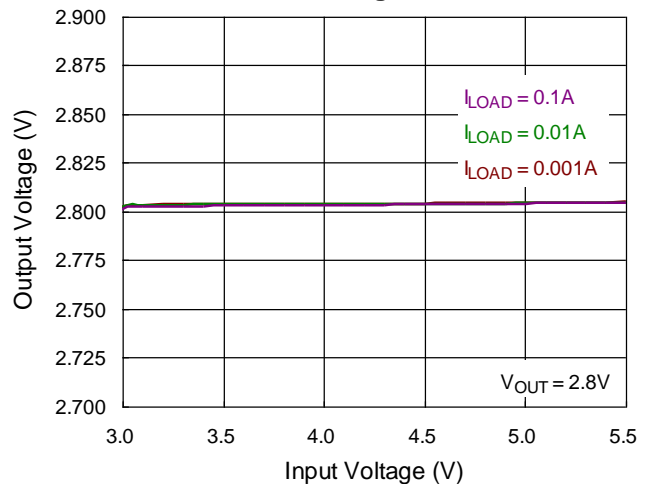
VEN Thresholds vs. Input Voltage



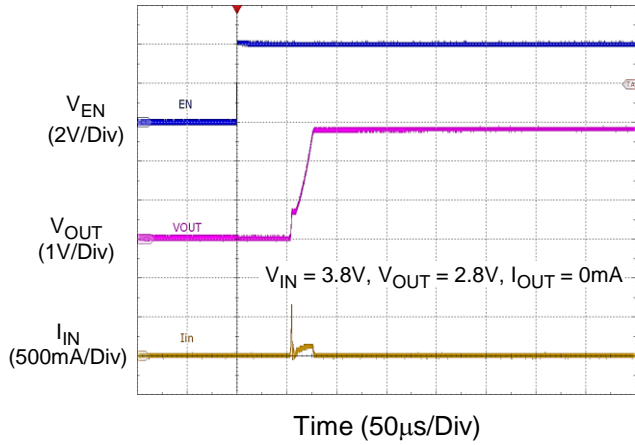
Load Regulation



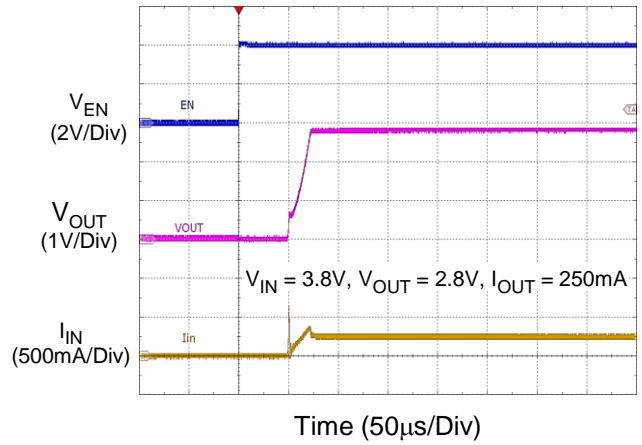
Line Regulation



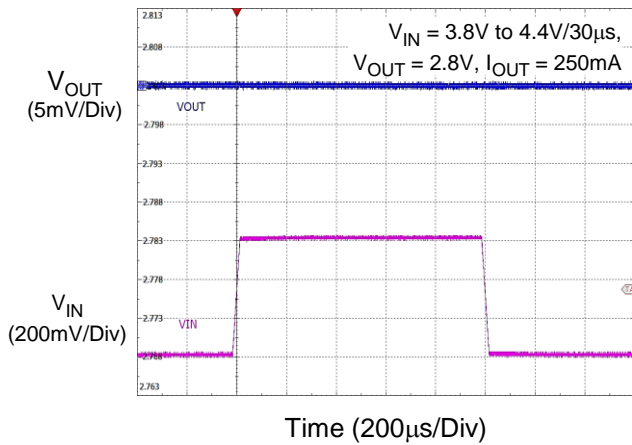
Inrush Current



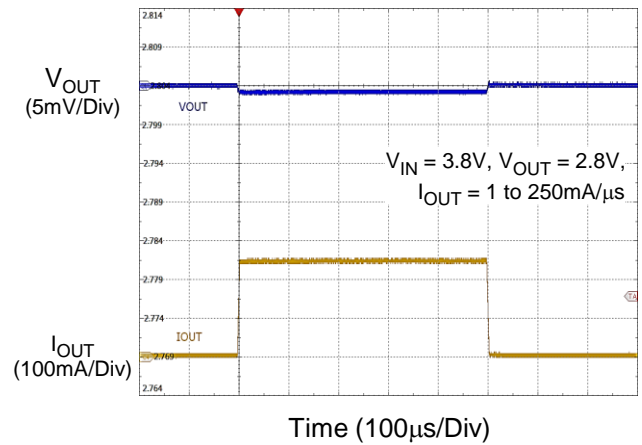
Power On from EN



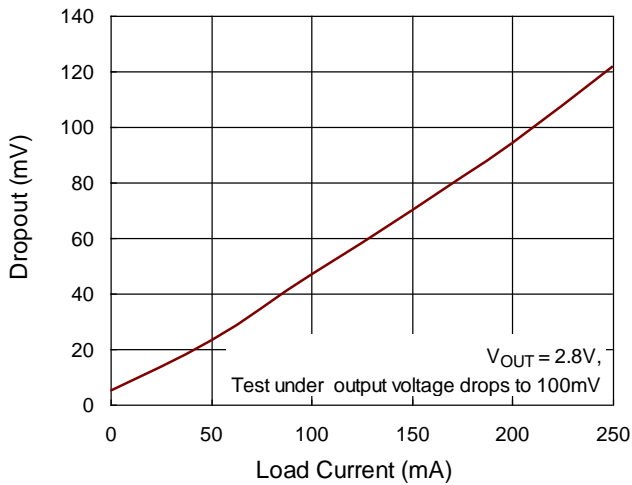
Line Transient



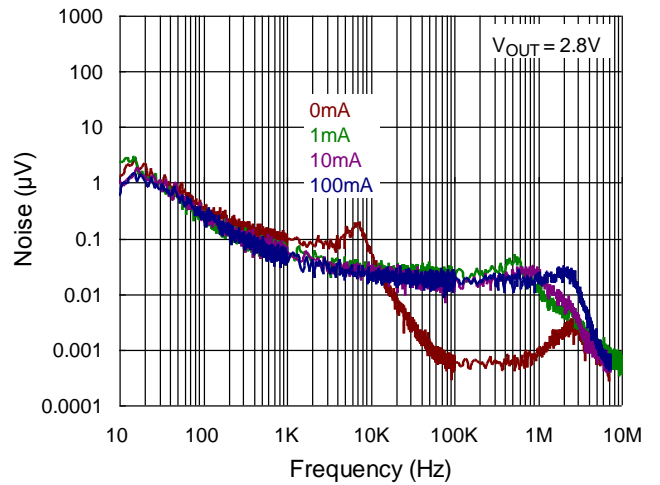
Load Transient

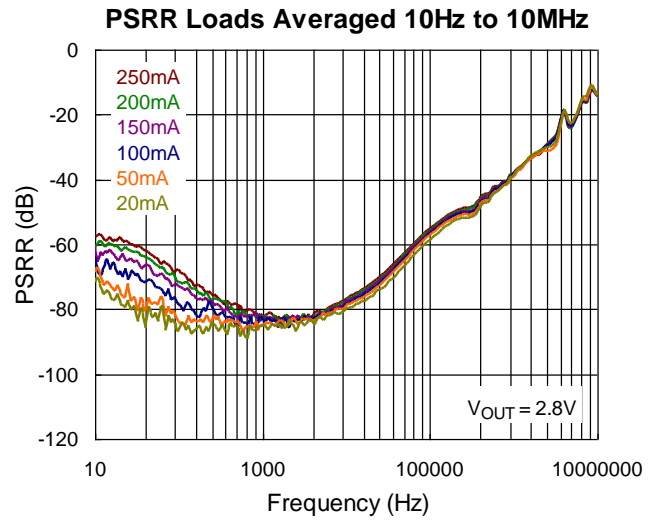
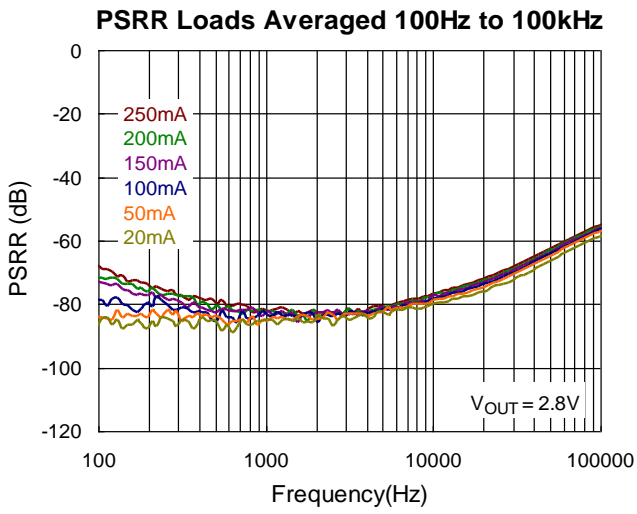


Dropout vs. Load Current



Noise Density Test





Application Information

Like any low dropout linear regulator, the RT9086's external input and output capacitors must be properly selected for stability and performance. Use a 1 μ F (X5R or X7R) or larger input capacitor and place it close to the IC's VIN and GND pins. Output capacitor effective capacitance larger than 1 μ F (X5R or X7R) requirement may be used. Place the output capacitor close to the IC's VOUT and GND pins. Increasing capacitance and decreasing ESR can improve the circuit's PSRR and line transient response.

Chip Enable Operation

The RT9086 EN pin internal resistor is 1M Ω to GND. The EN pin is the chip enable input. Pull the EN pin low (< 0.4V) will shutdown the device. During shutdown mode, the RT9086 quiescent current drops to lower than 1 μ A. Drive the EN pin to high (> 1.2V, < 5.5V) will turn on the device again.

Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at specific output current. The dropout voltage V_{DROP} also can be expressed as the voltage drop on the pass-FET at specific output current (I_{RATED}) while the pass-FET is fully operating at ohmic region and the pass-FET can be characterized as an resistance $R_{DS(ON)}$. Thus the dropout voltage can be defined as ($V_{DROP} = V_{VIN} - V_{VOUT} = R_{DS(ON)} \times I_{RATED}$). For normal operation, the suggested LDO operating range is ($V_{VIN} > V_{VOUT} + V_{DROP}$) for good transient response and PSRR ability. Vice versa, while operating at the ohmic region will degrade these performance severely. Output discharge Automatically The RT9086 output employs an internal 10 Ω pull-down resistance to discharge the output When EN pin is low, and the device is disabled.

C_{IN} and C_{OUT} Selection

Like any low dropout regulator, the external capacitors of the RT9086 must be carefully selected for regulator stability and performance. Using a capacitor of at least 1 μ F (X5R or X7R) is suitable. The input capacitor must be located at a distance of no more than 1cm from the

input pin of the chip. Any good quality ceramic capacitor can be used. However, a capacitor with larger value and lower ESR (Equivalent Series Resistance) is recommended since it will provide better PSRR and line transient response.

The RT9086 is designed specifically to work with low ESR ceramic output capacitor for space saving and performance consideration. Using a ceramic capacitor with capacitance of at least 1 μ F (X5R or X7R) on the RT9086 output ensures stability.

Minimum Operating Input Voltage (V_{IN})

The RT9086 does not include any dedicated UVLO circuitry. The RT9086 internal circuitry is not fully functional until VIN is at least 2.2V. The output voltage is not regulated until VIN has reached at least the greater of 2.2 V or (VOUT + V_{DROP}).

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA} , is highly package dependent. For a SOT-23-5 package, the thermal resistance, θ_{JA} , is 218.1°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. For a ZQFN-4L 1x1 package, the thermal resistance, θ_{JA} , is 92.7°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. For a WL-CSP-4B 0.67x0.67

(BSC) package, the thermal resistance, θ_{JA} , is 214.9°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated as below :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (218.1^\circ\text{C/W}) = 0.45\text{W for a SOT-23-5 package.}$$

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (92.7^\circ\text{C/W}) = 1.07\text{W for a ZQFN-4L 1x1 package.}$$

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (214.9^\circ\text{C/W}) = 0.46\text{W for a WL-CSP-4B 0.67x0.67 (BSC) package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA} . The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

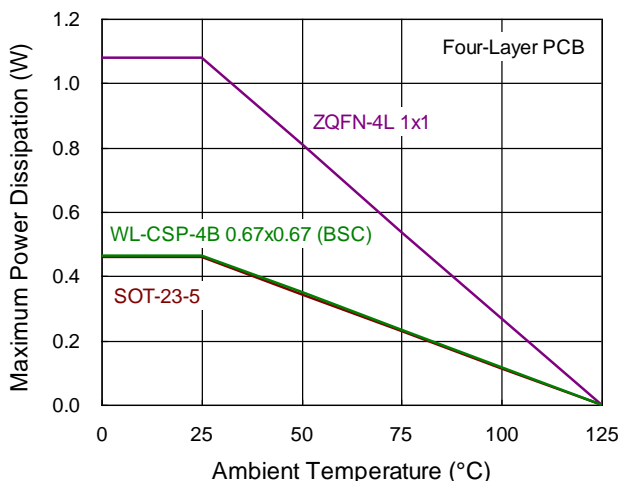


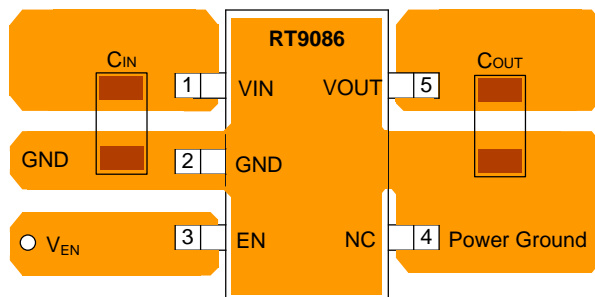
Figure 1. Derating Curve of Maximum Power Dissipation

Layout Considerations

The dynamic performance of the RT9086 is dependent on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the RT9086.

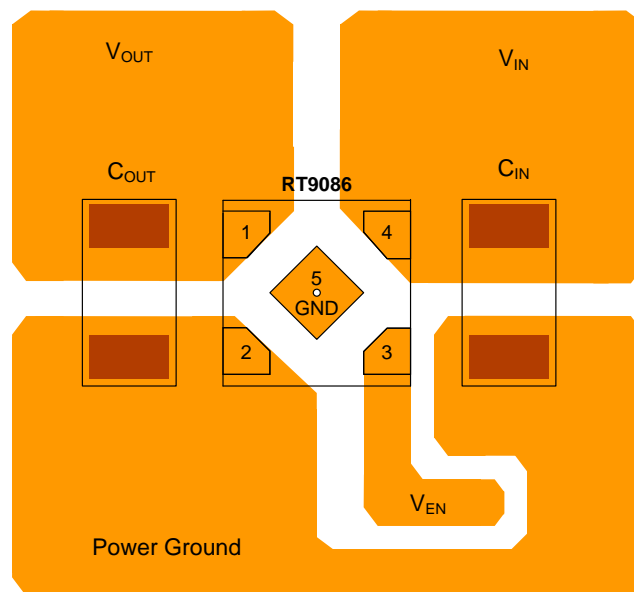
Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the RT9086, and as close to the package as is practical. The ground connections for C_{IN} and C_{OUT} must be back to the RT9086 ground pin using as wide and short a copper trace as is practical.

Connections using long trace lengths, narrow trace widths, and/or connections through vias must be avoided. These add parasitic inductances and resistance that results in inferior performance especially during transient conditions.



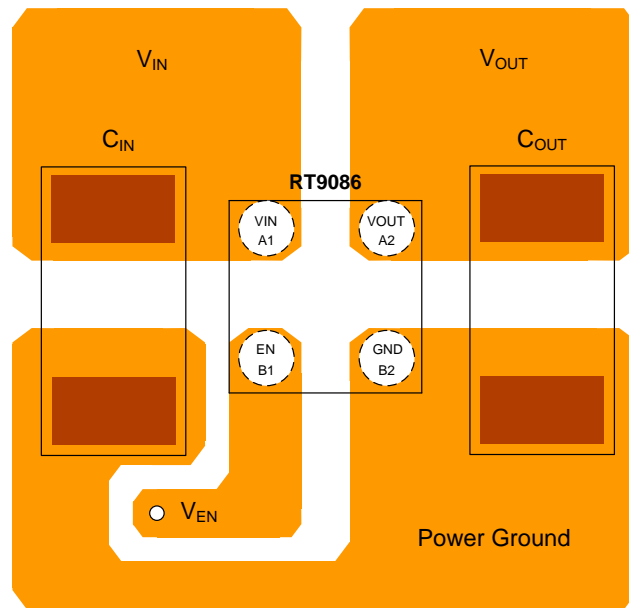
GND Pin (2) connect to second layer ground path by Via to increase cooling area directly.

Figure 2. SOT-23-5 Layout Guide



GND Pad (2) and (5) connect to second layer ground path by Via to increase cooling area directly.

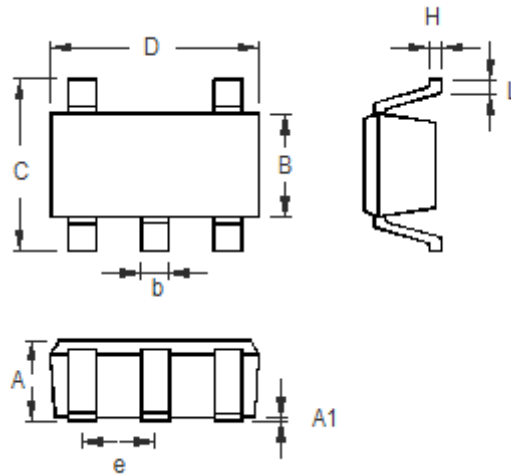
Figure 3. ZQFN-4L 1x1 Layout Guide



GND ball (B2) connect to second layer ground path by Via to increase cooling area directly.

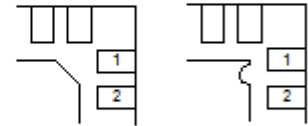
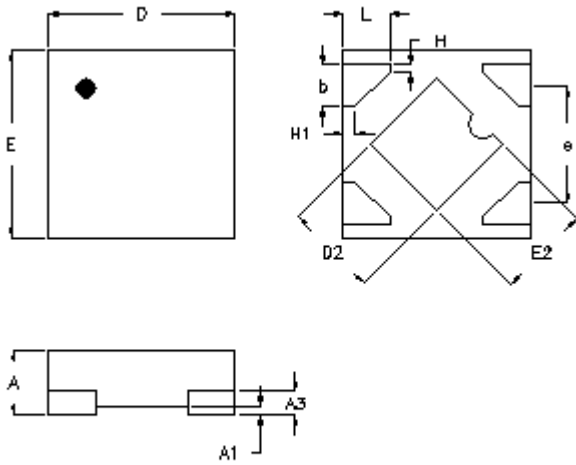
Figure 4. WL-CSP-4B 0.67x0.67 (BSC) Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-5 Surface Mount Package



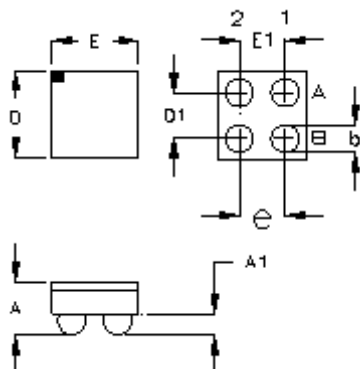
DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.300	0.400	0.012	0.016
A1	0.000	0.050	0.000	0.002
A3	0.117	0.162	0.005	0.006
b	0.175	0.275	0.007	0.011
D	0.900	1.100	0.035	0.043
D2	0.450	0.550	0.018	0.022
E	0.900	1.100	0.035	0.043
E2	0.450	0.550	0.018	0.022
e	0.625		0.025	
L	0.200	0.300	0.008	0.012
H	0.039		0.002	
H1	0.064		0.003	

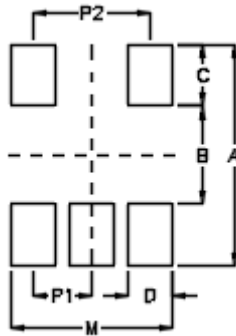
Z-Type 4L QFN 1x1 Package



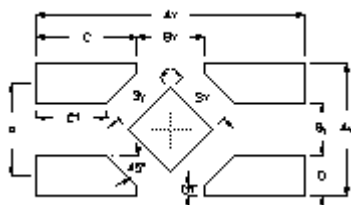
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.355	0.445	0.014	0.018
A1	0.135	0.165	0.005	0.006
b	0.190	0.230	0.007	0.009
D	0.630	0.710	0.025	0.028
D1	0.350		0.014	
E	0.630	0.710	0.025	0.028
E1	0.350		0.014	
e	0.350		0.014	

4B WL-CSP 0.67x0.67 Package (BSC)

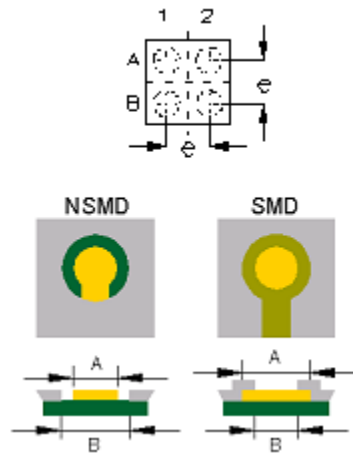
Footprint Information



Package	Number of Pin	Footprint Dimension (mm)							Tolerance
		P1	P2	A	B	C	D	M	
TSOT-25/TSOT-25(FC)/SOT-25	5	0.95	1.90	3.60	1.60	1.00	0.70	2.60	±0.10



Package	Number of Pin	Footprint Dimension (mm)											Tolerance
		P	Ax	Ay	Bx	By	C	C1	D	D1	Sx	Sy	
U/X/ZQFN1x1-4	4	0.625	1.800	0.900	0.450	0.350	0.675	0.474	0.275	0.074	0.400	0.400	±0.050



Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP0.67x0.67-4(BSC)	4	NSMD	0.350	0.200	0.300	±0.025
		SMD		0.230	0.200	

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City
 Hsinchu, Taiwan, R.O.C.
 Tel: (8863)5526789

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