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MAX98390

Boosted Class-D Amplifier with Integrated Dynamic Speaker Management

General Description

The MAX98390 is a high-efficiency mono Class-D DSM smart amplifier that features an integrated boost converter, integrated Dynamic Speaker Management™, and FET scaling for higher-efficiency at low output power.

The maximum boost converter output voltage is programmable from 6.5V to 10V in 0.125V increments from a battery voltage as low as 2.65V. The boost converter supports bypass mode for lower quiescent current and improved mid-power efficiency as well as envelope tracking which automatically adjusts the output voltage for maximum efficiency. The boosted supply efficiently delivers up to 6.2W at 10% THD+N into a 4Ω load.

Integrated IV sense and Dynamic Speaker Management allows louder, fuller audio while protecting the speaker against damage and improving sound quality.

The PCM interface supports I²S, left-justified, and 16-channel TDM formats as a slave or master device with I²C control. Either BCLK or MCLK can be used as the internal clock source providing system level flexibility.

Thermal and other status data can also be read from the I²C interface.

Patented active emissions limiting edge rate and overshoot control circuitry minimizes EMI and eliminates the need for output filtering found in traditional Class-D devices.

A flexible brownout-detection engine (BDE) can be programmed to initiate various current limiting, signal limiting, and clip functions to prevent dips in battery voltage. Threshold, hysteresis, and attack-and-release rates are programmable.

The IC is available in a 0.4mm pitch, 36-bump wafer-level package. It is specified over the extended -40°C to +85°C temperature range.

Applications

- Smartphones
- Tablets
- Notebook Computers
- Single Li-ion Cell Devices
- IoT Devices
- Toys

Benefits and Features

- Integrated Speaker Current and Voltage Sense Requires no External Components
- Integrated Programmable 10V Boost Converter
 - Bypass Mode
 - Envelope Tracking
- Integrated Dynamic Speaker Management
 - Thermal Protection
 - Excursion Protection
 - Low-Frequency Extension
 - 8-Band Parametric Equalizer
 - Dynamic Range Compression
 - Perceptual Power Reduction
 - Debuzzer
 - Stereo Bass Management
- Ultra-Low Noise Floor
 - 9μV Output Noise
 - 117dB Dynamic Range
- Low Distortion—0.01% THD+N
- Output Power at 1% THD+N
 - 5.1W into 8Ω, V_{BAT} = 4.3V
 - 5.1W into 4Ω, V_{BAT} = 4.3V
- Output Power at 10% THD+N
 - 6.2W into 8Ω, V_{BAT} = 4.3V
 - 6.2W into 4Ω, V_{BAT} = 4.3V
- System Efficiency
 - 82% at 1.2W into 8Ω, V_{BAT} = 3.7V
 - 86% at 0.45W into 8Ω, V_{BAT} = 3.7V
- Dynamic Speaker Output FET Scaling
- 2.65V to 5.5V Battery Voltage Range
- I²S/16-Channel TDM and I²C Interfaces
- Class-D Edge Rate Control Enables Filterless Operation
- Advanced Brownout-Protection Engine
- Extensive Click-and-Pop Suppression
- Robust Short-Circuit and Thermal Protection
- Space-Saving, 36-Bump WLP Package (6.3mm², 0.4mm Pitch)

Ordering Information appears at end of data sheet.

Dynamic Speaker Management is a trademark of Maxim Integrated Products, Inc.

Simplified Block Diagram

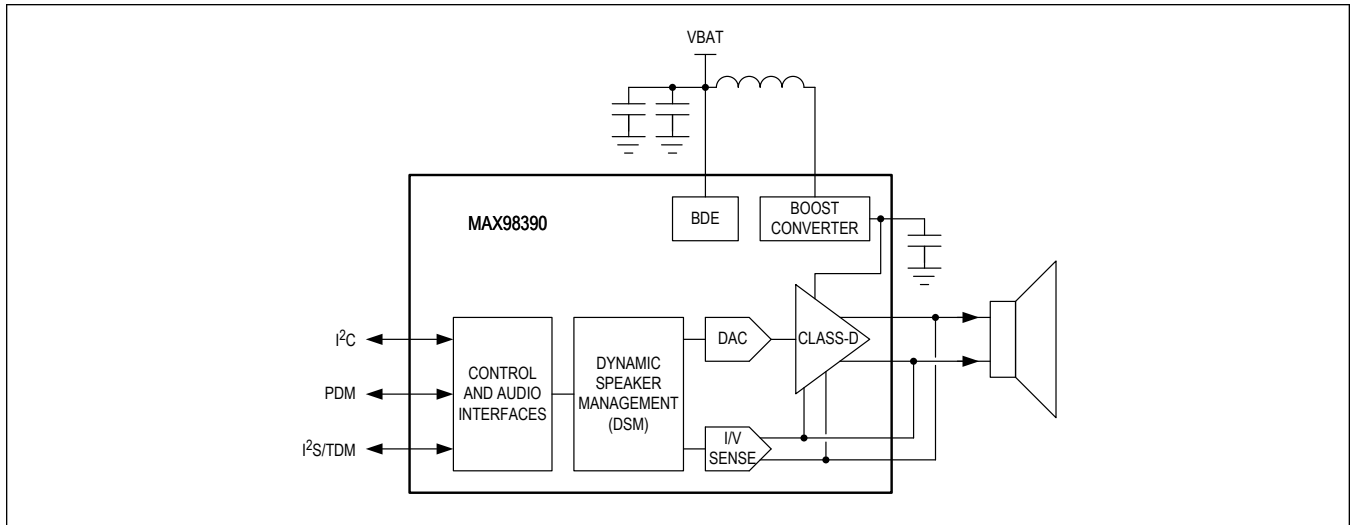


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Absolute Maximum Ratings

| | | | |
|---|----------------------|--|-----------------|
| VBAT to PGND..... | -0.3V to 6V | Short-Circuit Duration Between OUTP, OUTN, and GND..... | Continuous |
| PVDD to PGND (Note 1)..... | -0.3V to 12V | Short-Circuit Duration Between OUTP, OUTN, and PVDD..... | Continuous |
| DVDD to GND..... | -0.3V to 2.15V | Junction Temperature..... | +150°C |
| OUTP, OUTN to PGND..... | -0.3V to PVDD + 0.3V | Operating Temperature Range..... | -40°C to +85°C |
| LX to PGND..... | -0.3V to PVDD + 0.3V | Storage Temperature Range..... | -65°C to +150°C |
| VSNSP, VSNSN to PGND..... | -0.3V to 12V | Soldering Temperature (reflow)..... | +260°C |
| SDA, SCL, ADDR1, ADDR2 to GND..... | -0.3V to 5V | | |
| PGND to GND..... | -0.3V to 0.3V | | |
| All other digital pins to GND..... | -0.3V to DVDD + 0.3V | | |
| Short-Circuit Duration Between OUTP and OUTN..... | Continuous | | |

Note 1: When supplying PVDD externally, care must be taken to ensure PVDD is applied only when VBAT is present and the device is enabled. See the [Supplying PVDD Externally](#) section for the required sequence.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

36 WLP

| | |
|--|--|
| Package Code | W362G2+1 |
| Outline Number | 21-100287 |
| Land Pattern Number | Refer to Application Note 1891 |
| Thermal Resistance, Four-Layer Board: | |
| Junction to Ambient (θ_{JA}) | 46.2°C/W |
| Junction to Case (θ_{JC}) | N/A |

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

($V_{VBAT} = 3.7V$, $V_{DVDD} = 1.8V$, $V_{GND} = 0V$, $V_{PGND} = 0V$, $V_{PVDD} = 10V$ (BST_VOUT = 11100b), $L_1 = 1\mu H$, $C_{VBAT} = 10\mu F + 0.1\mu F + 10\mu F$, $C_{PVDD} = 0.1\mu F + 10\mu F + 10\mu F$, $C_{DVDD} = 0.1\mu F$, $C_{VREFC} = 1\mu F$, $R_{VREFC} = 30\Omega$, Amplifier Volume = +0dB (DSM_VOL_CTRL = 0xA0), $Z_{SPK} = \infty$ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, PCM_MSTR_MODE = 00b, $f_S = 48kHz$, $f_{BCLK} = 3.072MHz$, BST_BYP_MODE = 00b (automatic), AMP_FET_SCALE_MODE = 00b (automatic), DSP_GLOBAL_EN = 0, $T_A = T_{MIN}$ to T_{MAX} , typical values are at $T_A = +25^\circ C$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------------|------------|------------|------|-----|------|-------|
| SYSTEM | | | | | | |
| Power-Supply Voltage Range | V_{VBAT} | | 2.65 | | 5.5 | V |
| | V_{DVDD} | | 1.71 | | 1.89 | |

Electrical Characteristics (continued)

($V_{VBAT} = 3.7V$, $V_{DVDD} = 1.8V$, $V_{GND} = 0V$, $V_{PGND} = 0V$, $V_{PVDD} = 10V$ (BST_VOUT = 11100b), $L_1 = 1\mu H$, $C_{VBAT} = 10\mu F + 0.1\mu F + 10\mu F$, $C_{PVDD} = 0.1\mu F + 10\mu F + 10\mu F$, $C_{DVDD} = 0.1\mu F$, $C_{VREFC} = 1\mu F$, $R_{VREFC} = 30\Omega$, Amplifier Volume = +0dB (DSM_VOL_CTRL = 0xA0), $Z_{SPK} = \infty$ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, PCM_MSTR_MODE = 00b, $f_S = 48kHz$, $f_{BCLK} = 3.072MHz$, BST_BYP_MODE = 00b (automatic), AMP_FET_SCALE_MODE = 00b (automatic), DSP_GLOBAL_EN = 0, $T_A = T_{MIN}$ to T_{MAX} , typical values are at $T_A = +25^\circ C$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------|-------------------|--|-----|------|-----|-------|
| Quiescent Current | I _{VBAT} | $T_A = +25^\circ C$, IV sense on, AMP_FET_SCALE_MODE = 00b (FET scaling enabled), BST_BYP_MODE = 00b (boost bypass enabled), DSP_GLOBAL_EN = 0, POWER_GATING_EN = 0 | | 2.6 | 2.8 | |
| | | $T_A = +25^\circ C$, $Z_{SPK} = 4\Omega + 33\mu H$, IV sense on, AMP_FET_SCALE_MODE = 00b (FET scaling enabled), BST_BYP_MODE = 00b (boost bypass enabled), DSP_GLOBAL_EN = 1, all DSP blocks enabled, POWER_GATING_EN = 1 | | 2.7 | 2.9 | |
| | | $T_A = +25^\circ C$, $Z_{SPK} = 4\Omega + 33\mu H$, IV sense on, AMP_FET_SCALE_MODE = 00b (FET scaling enabled), BST_BYP_MODE = 00b (boost bypass enabled), DSP_GLOBAL_EN = 1, all DSP blocks enabled, POWER_GATING_EN = 0 | | 3.0 | 3.3 | |
| | | $T_A = +25^\circ C$, $Z_{SPK} = 4\Omega + 33\mu H$, IV sense on, AMP_FET_SCALE_MODE = 00b (FET scaling enabled), BST_BYP_MODE = 00b (boost bypass enabled), DSP_GLOBAL_EN = 0, POWER_GATING_EN = 0, $V_{VBAT} = 4.2V$ | | 2.95 | 3.2 | mA |
| | I _{DVDD} | $T_A = +25^\circ C$, IV sense on, AMP_FET_SCALE_MODE = 00b (FET scaling enabled), BST_BYP_MODE = 00b (boost bypass enabled), DSP_GLOBAL_EN = 0, POWER_GATING_EN = 0 | | 4.8 | 5.2 | |
| | | $T_A = +25^\circ C$, $Z_{SPK} = 4\Omega + 33\mu H$, IV sense on, AMP_FET_SCALE_MODE = 00b (FET scaling enabled), BST_BYP_MODE = 00b (boost bypass enabled), DSP_GLOBAL_EN = 1, all DSP blocks enabled, POWER_GATING_EN = 1 | | 2.7 | 2.8 | |
| | | $T_A = +25^\circ C$, $Z_{SPK} = 4\Omega + 33\mu H$, IV sense on, AMP_FET_SCALE_MODE = 00b (FET scaling enabled), BST_BYP_MODE = 00b (boost bypass enabled), DSP_GLOBAL_EN = 1, all DSP blocks enabled, POWER_GATING_EN = 0 | | 7.2 | 7.5 | |

Electrical Characteristics (continued)

($V_{VBAT} = 3.7V$, $V_{DVDD} = 1.8V$, $V_{GND} = 0V$, $V_{PGND} = 0V$, $V_{PVDD} = 10V$ (BST_VOUT = 11100b), $L_1 = 1\mu H$, $C_{VBAT} = 10\mu F + 0.1\mu F + 10\mu F$, $C_{PVDD} = 0.1\mu F + 10\mu F + 10\mu F$, $C_{DVDD} = 0.1\mu F$, $C_{VREFC} = 1\mu F$, $R_{VREFC} = 30\Omega$, Amplifier Volume = +0dB (DSM_VOL_CTRL = 0xA0), $Z_{SPK} = \infty$ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, PCM_MSTR_MODE = 00b, $f_S = 48kHz$, $f_{BCLK} = 3.072MHz$, BST_BYP_MODE = 00b (automatic), AMP_FET_SCALE_MODE = 00b (automatic), DSP_GLOBAL_EN = 0, $T_A = T_{MIN}$ to T_{MAX} , typical values are at $T_A = +25^\circ C$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------------------|----------------------|---|-----|------|-----|---------|
| Software Shutdown Supply Current | I_{VBAT} (SHDN_SW) | EN = 0, no MCLK/BCLK/LRCLK/DIN transitions, $T_A = +25^\circ C$ | | 0.4 | 1 | μA |
| | I_{DVDD} (SHDN_SW) | EN = 0, no MCLK/BCLK/LRCLK/DIN transitions, $T_A = +25^\circ C$ | | 8.4 | 13 | |
| Hardware Shutdown Supply Current | I_{VBAT} (SHDN_HW) | $\overline{RESET} = 0$, $T_A = +25^\circ C$ | | 0.35 | 1 | μA |
| | I_{DVDD} (SHDN_HW) | $\overline{RESET} = 0$, $T_A = +25^\circ C$ | | | 1 | |
| System Efficiency | η | $P_{OUT} = 1.2W$, $f = 1kHz$, $Z_{SPK} = 8\Omega + 33\mu H$ | | 82 | | % |
| | | $P_{OUT} = 1.2W$, $f = 1kHz$, $Z_{SPK} = 8\Omega + 33\mu H$, $V_{VBAT} = 4.3V$ | | 83 | | |
| | | $P_{OUT} = 0.45W$, $f = 1kHz$, $Z_{SPK} = 8\Omega + 33\mu H$, boost bypassed, 1/4 size output FETs | | 86 | | |
| Turn-On Time | t_{ON} | Time from EN active to Class-D amplifier on, SPK_SPEEDUP = 0, DSM_VOL_RMP_UP_BYP = 0 | | 3.7 | 10 | ms |
| | | Time from EN active to Class-D amplifier on, SPK_SPEEDUP = 1, DSM_VOL_RMP_UP_BYP = 1 | | 750 | | μs |
| BOOST CONVERTER | | | | | | |
| Soft-Start Time | t_{STR} | | | 1.4 | | ms |
| LX leakage current | I_{LX_LEAK} | $T_A = +25^\circ C$, LX from 0V to 4.5V | -1 | 0 | +1 | μA |
| Startup Input Current Limit | $I_{STARTUP}$ | | | 0.5 | | A |
| Minimum Peak Input Current Limit | I_{LX_MIN} | At minimum programmed setting | | 0 | | A |
| Maximum Peak Input Current Value | I_{LX_MAX} | Maximum usable programmed limit, $2.65V \leq V_{VBAT} \leq 2.85V$ | | 2.8 | | A |
| | I_{LX_MAX} | Maximum usable programmed limit, $2.85V < V_{VBAT} \leq 5.5V$ | | 4.1 | | |
| Input Current-Limit Step | | From 1A to 4.1A | | 50 | | mA |
| Switching Frequency | f_{SW} | Speaker driving signal or skip mode disabled | 2.1 | 2.3 | 2.5 | MHz |

Electrical Characteristics (continued)

($V_{VBAT} = 3.7V$, $V_{DVDD} = 1.8V$, $V_{GND} = 0V$, $V_{PGND} = 0V$, $V_{PVDD} = 10V$ (BST_VOUT = 11100b), $L_1 = 1\mu H$, $C_{VBAT} = 10\mu F + 0.1\mu F + 10\mu F$, $C_{PVDD} = 0.1\mu F + 10\mu F + 10\mu F$, $C_{DVDD} = 0.1\mu F$, $C_{VREFC} = 1\mu F$, $R_{VREFC} = 30\Omega$, Amplifier Volume = +0dB (DSM_VOL_CTRL = 0xA0), $Z_{SPK} = \infty$ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, PCM_MSTR_MODE = 00b, $f_S = 48kHz$, $f_{BCLK} = 3.072MHz$, BST_BYP_MODE = 00b (automatic), AMP_FET_SCALE_MODE = 00b (automatic), DSP_GLOBAL_EN = 0, $T_A = T_{MIN}$ to T_{MAX} , typical values are at $T_A = +25^\circ C$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------------|----------------|---|------------|---------|------------|-------|
| Skip-Mode Frequency | $f_{SW-SKIP}$ | Quiescent speaker and skip mode enabled, Mode 1 | | 58 | | kHz |
| | $f_{SW-SKIP}$ | Quiescent speaker and skip mode enabled, Mode 2 | | 66 | | |
| | $f_{SW-SKIP}$ | Quiescent speaker and skip mode enabled, Mode 3 | | 340 | | |
| Efficiency | η_{BOOST} | $I_{OUT} = 0.4A$, $V_{VBAT} = 4.3V$ | | 90 | | % |
| Boost Clock Phase | Φ_{BOOST} | Relative to LRCLK, BST_PHASE = 000 | | 3 | | ° |
| | | Relative to LRCLK, BST_PHASE = 001 | | 71 | | |
| | | Relative to LRCLK, BST_PHASE = 010 | | 140 | | |
| | | Relative to LRCLK, BST_PHASE = 011 | | 208 | | |
| Output Voltage | V_{PVDD} | Max setting, across specified V_{VBAT} operating range, boost on (not bypassed) | 9.5 | 10 | 10.27 | V |
| | | Min setting, across specified V_{VBAT} operating range, boost on (not bypassed) | 6.3 | 6.5 | 6.7 | |
| Output Voltage Step Size | | | 0.09 | 0.125 | 0.16 | V |
| Absolute Output Voltage Accuracy | | ENV_TRACKER_EN = 0, $V_{VBAT} = 3.5V$ and 4.5V, BST_VOUT set to 6.5V, 8.5V, and 10V, relative to nominal | -3 | | +3 | % |
| Relative Output Voltage Accuracy | | ENV_TRACKER_EN = 0, $V_{VBAT} = 3.5V$ to 4.5V, relative to V_{PVDD} at $V_{VBAT} = 3.7V$, any output voltage setting | | ± 1 | | % |
| Boost Load Regulation | | $0mA \leq I_{LOAD} \leq 1100mA$. DC | | -3 | | %/A |
| Overvoltage Protection | OVP | | | 10.5 | | V |
| DAC | | | | | | |
| Gain Error | | | | 1 | | % |
| Full-Scale Output Voltage | | | | 2.16 | | Vpk |
| DAC / DIGITAL FILTER (Note 4) | | | | | | |
| Valid Sample Rates | f_S | | 8 | | 48 | kHz |
| Passband | f_{PLP} | Ripple < δ_P | 0.45 f_S | | | Hz |
| | | Droop < 3dB | 0.46 f_S | | | |
| Passband Ripple | δ_P | $f < f_{PLP}$, referenced to signal level at 1kHz | -0.1 | | +0.1 | dB |
| Stopband | f_{SLP} | Attenuation > δ_S | | | 0.49 f_S | Hz |
| Stopband Attenuation | δ_S | $f > f_{SLP}$ | 75 | | | dB |

Electrical Characteristics (continued)

($V_{VBAT} = 3.7V$, $V_{DVDD} = 1.8V$, $V_{GND} = 0V$, $V_{PGND} = 0V$, $V_{PVDD} = 10V$ (BST_VOUT = 11100b), $L_1 = 1\mu H$, $C_{VBAT} = 10\mu F + 0.1\mu F + 10\mu F$, $C_{PVDD} = 0.1\mu F + 10\mu F + 10\mu F$, $C_{DVDD} = 0.1\mu F$, $C_{VREFC} = 1\mu F$, $R_{VREFC} = 30\Omega$, Amplifier Volume = +0dB (DSM_VOL_CTRL = 0xA0), $Z_{SPK} = \infty$ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, PCM_MSTR_MODE = 00b, $f_S = 48kHz$, $f_{BCLK} = 3.072MHz$, BST_BYP_MODE = 00b (automatic), AMP_FET_SCALE_MODE = 00b (automatic), DSP_GLOBAL_EN = 0, $T_A = T_{MIN}$ to T_{MAX} , typical values are at $T_A = +25^\circ C$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|----------|---|------|---------|-----|---------------|
| Group Delay | | $f = f_{PLP}$ | | 27 | | samples |
| | | $f = 1kHz$ | | 5 | | |
| DAC / DIGITAL DC BLOCKING FILTER (Note 4) | | | | | | |
| Corner Frequency | f_c | $f_S = 8kHz$ | | 0.312 | | Hz |
| | | $f_S = 48kHz$ | | 1.872 | | |
| SPEAKER AMPLIFIER | | | | | | |
| Output Offset Voltage | V_{OS} | $T_A = +25^\circ C$, $Z_{SPK} = 8\Omega + 33\mu H$ or $4\Omega + 33\mu H$, DRE_EN = 0 | -3 | ± 1 | +3 | mV |
| Click-and-Pop Level | K_{CP} | Peak voltage, A-weighted, 32 samples per second; digital audio inputs have zero-code input, $Z_{SPK} = 8\Omega + 33\mu H$ or $4\Omega + 33\mu H$, out of software shutdown (EN changed from 0 to 1), AMP_FET_SCALE_MODE = 00b (FET scaling enabled), BST_BYP_MODE = 00b (boost bypass enabled) | | -63 | | dBV |
| | | Peak voltage, A-weighted, 32 samples per second; digital audio inputs have zero-code input, $Z_{SPK} = 8\Omega + 33\mu H$ or $4\Omega + 33\mu H$, into software shutdown (EN changed from 1 to 0), AMP_FET_SCALE_MODE = 00b (FET scaling enabled), BST_BYP_MODE = 00b (boost bypass enabled) | | -66 | | |
| Dynamic Range | DNR | LRCLK = 48kHz, 24 or 32 bits, -60dBFS 1kHz output signal, normalized to full-scale (THD+N = 1%), $Z_{SPK} = 8\Omega + 33\mu H$, A-weighted, $T_A = +25^\circ C$ | | 117 | | dB |
| | | LRCLK = 48kHz, 24 or 32 bits, -60dBFS 1kHz output signal, normalized to full-scale (THD+N = 1%), $Z_{SPK} = 8\Omega + 33\mu H$, unweighted, $T_A = +25^\circ C$ | | 112 | | |
| Output Noise | e_{Nd} | $Z_{SPK} = 8\Omega + 33\mu H$ or $4\Omega + 33\mu H$, DRE enabled, A-weighted | | 9 | | μV_{RMS} |
| Power-Supply Input Range | PVDD | Guaranteed by Class-D PSRR test | 2.65 | | 10 | V |

Electrical Characteristics (continued)

($V_{VBAT} = 3.7V$, $V_{DVDD} = 1.8V$, $V_{GND} = 0V$, $V_{PGND} = 0V$, $V_{PVDD} = 10V$ (BST_VOUT = 11100b), $L_1 = 1\mu H$, $C_{VBAT} = 10\mu F + 0.1\mu F + 10\mu F$, $C_{PVDD} = 0.1\mu F + 10\mu F + 10\mu F$, $C_{DVDD} = 0.1\mu F$, $C_{VREFC} = 1\mu F$, $R_{VREFC} = 30\Omega$, Amplifier Volume = +0dB (DSM_VOL_CTRL = 0xA0), $Z_{SPK} = \infty$ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, PCM_MSTR_MODE = 00b, $f_S = 48kHz$, $f_{BCLK} = 3.072MHz$, BST_BYP_MODE = 00b (automatic), AMP_FET_SCALE_MODE = 00b (automatic), DSP_GLOBAL_EN = 0, $T_A = T_{MIN}$ to T_{MAX} , typical values are at $T_A = +25^\circ C$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-----------|--|-----|------|-----|-------|
| Output Power | P_{OUT} | $V_{VBAT} = 4.3V$, $f = 1kHz$, THD+N $\leq 1\%$, $I_{LIM} = 4.1A$, $Z_{SPK} = 8\Omega + 33\mu H$ | | 5.1 | | W |
| | | $V_{VBAT} = 4.3V$, $f = 1kHz$, THD+N $\leq 1\%$, $I_{LIM} = 4.1A$, $Z_{SPK} = 4\Omega + 33\mu H$ | | 5.1 | | |
| | | $V_{VBAT} = 4.3V$, $f = 1kHz$, THD+N $\leq 10\%$, $I_{LIM} = 4.1A$, $Z_{SPK} = 8\Omega + 33\mu H$ | | 6.2 | | |
| | | $V_{VBAT} = 4.3V$, $f = 1kHz$, THD+N $\leq 10\%$, $I_{LIM} = 4.1A$, $Z_{SPK} = 4\Omega + 33\mu H$ | | 6.2 | | |
| Total Harmonic Distortion + Noise | THD+N | $f = 1kHz$, $P_{OUT} = 1W$, $Z_{SPK} = 8\Omega + 33\mu H$, $T_A = +25^\circ C$ | | 0.01 | | % |
| | | $f = 1kHz$, $P_{OUT} = 1.5W$, $Z_{SPK} = 4\Omega + 33\mu H$, $T_A = +25^\circ C$ | | 0.01 | | |
| Intermodulation Distortion | IMD | 5.5kHz/6.5kHz, 1:1, $V_{OUT} = 2V_{pk}$, $Z_{SPK} = 8\Omega + 33\mu H$ | | 79 | | dB |
| VBAT Power-Supply Rejection Ratio (VBAT to Speaker Amplifier) | PSRR | Boost on, no input signal, $Z_{SPK} = \infty$, DC, $V_{PVDD} = 6.5V$ to $10V$ | | 111 | | dB |
| | | Boost on, no input signal, $Z_{SPK} = 8\Omega + 33\mu H$ or $4\Omega + 33\mu H$, AC, $f = 217Hz$, V_{VBAT} ripple = $500mV_{pp}$ | | 113 | | |
| | | Boost on, no input signal, $Z_{SPK} = 8\Omega + 33\mu H$ or $4\Omega + 33\mu H$, AC, $f = 1kHz$, V_{VBAT} ripple = $500mV_{pp}$ | | 107 | | |
| | | Boost on, no input signal, $Z_{SPK} = 8\Omega + 33\mu H$ or $4\Omega + 33\mu H$, AC, $f = 10kHz$, V_{VBAT} ripple = $500mV_{pp}$ | | 77 | | |
| | | Boost bypassed, no input signal, $Z_{SPK} = \infty$, DC, $V_{VBAT} = 2.65V$ to $5.5V$ | | 89 | | |
| | | Boost bypassed, no input signal, $Z_{SPK} = 8\Omega + 33\mu H$ or $4\Omega + 33\mu H$, AC, $f = 217Hz$, V_{VBAT} ripple = $500mV_{pp}$ | | 86 | | |
| | | Boost bypassed, no input signal, $Z_{SPK} = 8\Omega + 33\mu H$ or $4\Omega + 33\mu H$, AC, $f = 1kHz$, V_{VBAT} ripple = $500mV_{pp}$ | | 85 | | |
| | | Boost bypassed, no input signal, $Z_{SPK} = 8\Omega + 33\mu H$ or $4\Omega + 33\mu H$, AC, $f = 10kHz$, V_{VBAT} ripple = $500mV_{pp}$ | | 64 | | |
| DVDD Power-Supply Rejection Ratio (DVDD to Speaker Amplifier) | PSRR | No input signal, $Z_{SPK} = 8\Omega + 33\mu H$ or $4\Omega + 33\mu H$, AC, $f = 1kHz$, V_{DVDD} ripple = $100mV_{pp}$ | | 90 | | dB |
| Output Switching Frequency | f_S | 48kHz related sample rates | 640 | 646 | 670 | kHz |
| | | 44.1kHz related sample rates | | 639 | | |

Electrical Characteristics (continued)

($V_{VBAT} = 3.7V$, $V_{DVDD} = 1.8V$, $V_{GND} = 0V$, $V_{PGND} = 0V$, $V_{PVDD} = 10V$ (BST_VOUT = 11100b), $L_1 = 1\mu H$, $C_{VBAT} = 10\mu F + 0.1\mu F + 10\mu F$, $C_{PVDD} = 0.1\mu F + 10\mu F + 10\mu F$, $C_{DVDD} = 0.1\mu F$, $C_{VREFC} = 1\mu F$, $R_{VREFC} = 30\Omega$, Amplifier Volume = +0dB (DSM_VOL_CTRL = 0xA0), $Z_{SPK} = \infty$ between OUP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, PCM_MSTR_MODE = 00b, $f_S = 48kHz$, $f_{BCLK} = 3.072MHz$, BST_BYP_MODE = 00b (automatic), AMP_FET_SCALE_MODE = 00b (automatic), DSP_GLOBAL_EN = 0, $T_A = T_{MIN}$ to T_{MAX} , typical values are at $T_A = +25^\circ C$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------|---|------------|------------|------------|------------|
| Current Limit | I_{LIM} | | | 4.5 | | A |
| Output Stage On-Resistance | R_{ON} | PMOS + NMOS (full H-bridge) | 240 | 400 | 500 | m Ω |
| Output Stage On-Resistance Matching | | OUP PMOS + OUTN NMOS vs. OUP NMOS + OUTN PMOS | | 25 | | m Ω |
| Amplifier Short-Circuit Autoreset | | Amplifier outputs exceed output current limit | | 100 | | μs |
| MEASUREMENT ADC | | | | | | |
| Resolution | | | | 8 | | Bits |
| VBAT Measurement Voltage Range | | | 2.65 | | 5.5 | V |
| VBAT Measurement Accuracy | | $T_A = +25^\circ C$ | -37.5 | | +37.5 | mV |
| | | Across specified T_A range | -45 | | +45 | |
| PVDD Measurement Voltage Range | | | 6 | | 11 | V |
| PVDD Measurement Accuracy | | | -100 | | +100 | mV |
| Temperature Measurement Accuracy | | $T_A = +25^\circ C$ to $+150^\circ C$ | | ± 8 | | $^\circ C$ |
| BROWNOUT-DETECTION ENGINE (BDE) | | | | | | |
| BDE Gain Attack Delay Time to Gain Change | | Measurement ADC sampling VBAT at 512kHz | | 7 | | μs |
| BDE Gain Attack Delay Time to Interrupt | | Measurement ADC sampling VBAT at 512kHz | | 5 | | μs |
| DIGITAL I/O / INPUT—DIN, BCLK, LRCLK, MCLK, ICC, WDT | | | | | | |
| Input Voltage High | V_{IH} | | 0.7 x DVDD | | | V |
| Input Voltage Low | V_{IL} | | | | 0.3 x DVDD | V |
| Input Hysteresis | V_{hyst} | | | 0.2 x DVDD | | V |
| Input Leakage Current | | | -1 | | 3.5 | μA |
| Input Capacitance | C_{IN} | DIN, MCLK | | 3 | | pF |
| | | BCLK, LRCLK, ICC | | 14 | | |
| DIGITAL I/O / INPUT—RESET, ADDR1, ADDR2 | | | | | | |
| Input Voltage High | V_{IH} | | 0.7 x DVDD | | | V |
| Input Voltage Low | V_{IL} | | | | 0.3 x DVDD | V |

Electrical Characteristics (continued)

($V_{VBAT} = 3.7V$, $V_{DVDD} = 1.8V$, $V_{GND} = 0V$, $V_{PGND} = 0V$, $V_{PVDD} = 10V$ (BST_VOUT = 11100b), $L_1 = 1\mu H$, $C_{VBAT} = 10\mu F + 0.1\mu F + 10\mu F$, $C_{PVDD} = 0.1\mu F + 10\mu F + 10\mu F$, $C_{DVDD} = 0.1\mu F$, $C_{VREFC} = 1\mu F$, $R_{VREFC} = 30\Omega$, Amplifier Volume = +0dB (DSM_VOL_CTRL = 0xA0), $Z_{SPK} = \infty$ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, PCM_MSTR_MODE = 00b, $f_S = 48kHz$, $f_{BCLK} = 3.072MHz$, BST_BYP_MODE = 00b (automatic), AMP_FET_SCALE_MODE = 00b (automatic), DSP_GLOBAL_EN = 0, $T_A = T_{MIN}$ to T_{MAX} , typical values are at $T_A = +25^\circ C$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---------------|--|-----------------------|------------------|-----------------------|-------------------|
| Input Leakage Current | | | -1 | | +1 | μA |
| Input Capacitance | C_{IN} | | | 3 | | pF |
| DIGITAL I/O / OUTPUT—DOUT, BCLK, LRCLK, ICC | | | | | | |
| Output Voltage High | V_{OH} | $I_{OH} = 4mA$, normal-drive mode | | $V_{DVDD} - 0.3$ | | V |
| Output Voltage Low | V_{OL} | $I_{OL} = 4mA$, normal-drive mode | | | 0.3 | V |
| Output Current | I_{OH} | Highest-drive mode | | 16 | | mA |
| | | High-drive mode | | 12 | | |
| | | Normal-drive mode | | 8 | | |
| | | Reduced-drive mode | | 4 | | |
| DIGITAL I/O / INPUT—SDA, SCL | | | | | | |
| Input Voltage High | V_{IH} | | $0.7 \times V_{DVDD}$ | | | V |
| Input Voltage Low | V_{IL} | | | | $0.3 \times V_{DVDD}$ | V |
| Input Hysteresis | V_{HYST} | | | 200 | | mV |
| Input Capacitance | C_{IN} | | | 10 | | pF |
| Input High Leakage Current | | $T_A = +25^\circ C$, input high | -1 | | +1 | μA |
| Input Low Leakage Current | | $T_A = +25^\circ C$, input low | -1 | | +1 | μA |
| DIGITAL I/O / OUTPUT—SDA, IRQ | | | | | | |
| Output Low Voltage | V_{OL} | $I_{SINK} = 4mA$ | | | 0.4 | V |
| Output High Leakage Current | I_{OH} | $T_A = +25^\circ C$ | -1 | | +1 | μA |
| PCM INTERFACE TIMING | | | | | | |
| LRCLK Frequency | f_{LRCLK} | | 8 | | 48 | kHz |
| Maximum MDLL Source Clock Low-Frequency Jitter | | Maximum allowable jitter before -20dBFS, 20kHz input has 1dB reduction in THD+N; RMS jitter $\leq 40kHz$, DRE enabled | | 0.2 | | ns _{RMS} |
| Maximum MDLL Source Clock High-Frequency Jitter | | Maximum allowable jitter before -60dBFS, 20kHz input has 1dB reduction in THD+N; RMS jitter $> 40kHz$, DRE enabled | | 1 | | ns _{RMS} |
| PCM INTERFACE TIMING / MASTER MODE—LRCLK, BCLK, DIN | | | | | | |
| BCLK Inactive Edge to LRCLK Delay | $t_{CLKSYNC}$ | | | | 25 | ns |

Electrical Characteristics (continued)

($V_{VBAT} = 3.7V$, $V_{DVDD} = 1.8V$, $V_{GND} = 0V$, $V_{PGND} = 0V$, $V_{PVDD} = 10V$ (BST_VOUT = 11100b), $L_1 = 1\mu H$, $C_{VBAT} = 10\mu F + 0.1\mu F + 10\mu F$, $C_{PVDD} = 0.1\mu F + 10\mu F + 10\mu F$, $C_{DVDD} = 0.1\mu F$, $C_{VREFC} = 1\mu F$, $R_{VREFC} = 30\Omega$, Amplifier Volume = +0dB (DSM_VOL_CTRL = 0xA0), $Z_{SPK} = \infty$ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, PCM_MSTR_MODE = 00b, $f_S = 48kHz$, $f_{BCLK} = 3.072MHz$, BST_BYP_MODE = 00b (automatic), AMP_FET_SCALE_MODE = 00b (automatic), DSP_GLOBAL_EN = 0, $T_A = T_{MIN}$ to T_{MAX} , typical values are at $T_A = +25^\circ C$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---------------|----------------------------------|-----|-----|------|-------|
| DIN to BCLK Active Edge Setup Time | t_{SETUP} | | 4 | | | ns |
| DIN to BCLK Active Edge Hold Time | t_{HOLD} | | 4 | | | ns |
| BCLK or LRCLK Rise and Fall Times | t_r, t_f | $C_L = 30pF$, normal-drive mode | | 5 | | ns |
| PCM INTERFACE TIMING / SLAVE MODE—LRCLK, BCLK, DIN | | | | | | |
| BCLK Cycle Time | t_{BCLK} | | 65 | | | ns |
| BCLK Duty Cycle | DC | | 45 | | 55 | % |
| LRCLK to BCLK Active Edge Setup Time | $t_{SYNCSET}$ | | 4 | | | ns |
| LRCLK to BCLK Active Edge Hold Time | $t_{SYNHOLD}$ | | 4 | | | ns |
| DIN to BCLK Active Edge Setup Time | t_{SETUP} | | 4 | | | ns |
| DIN to BCLK Active Edge Hold Time | t_{HOLD} | | 4 | | | ns |
| PCM INTERFACE TIMING / DOUT | | | | | | |
| BCLK Inactive Edge to DOUT Delay | t_{CLKTX} | | | | 20 | ns |
| BCLK Active Edge to DOUT Hi-Z Delay | t_{Hi-Z} | | 4 | | 24 | ns |
| BCLK Inactive Edge to DOUT Active Delay | t_{ACTV} | | 0 | | 20 | ns |
| PCM INTERFACE TIMING / INTERCHIP COMMUNICATION—ICC | | | | | | |
| ICC to BCLK Active Edge Setup Time | t_{SETUP} | | 4 | | | ns |
| ICC to BCLK Active Edge Hold Time | t_{HOLD} | | 4 | | | ns |
| BCLK Inactive Edge to ICC Delay | t_{CLKTX} | | | | 20 | ns |
| BCLK Active Edge to ICC Hi-Z Delay | t_{Hi-Z} | | 4 | | 24 | ns |
| BCLK Inactive Edge to ICC Active Delay | t_{ACTV} | | 0 | | 20 | ns |
| I²C TIMING | | | | | | |
| Serial Clock Frequency | f_{SCL} | | 0 | | 1000 | kHz |

Electrical Characteristics (continued)

($V_{VBAT} = 3.7V$, $V_{DVDD} = 1.8V$, $V_{GND} = 0V$, $V_{PGND} = 0V$, $V_{PVDD} = 10V$ (BST_VOUT = 11100b), $L_1 = 1\mu H$, $C_{VBAT} = 10\mu F + 0.1\mu F + 10\mu F$, $C_{PVDD} = 0.1\mu F + 10\mu F + 10\mu F$, $C_{DVDD} = 0.1\mu F$, $C_{VREFC} = 1\mu F$, $R_{VREFC} = 30\Omega$, Amplifier Volume = +0dB (DSM_VOL_CTRL = 0xA0), $Z_{SPK} = \infty$ between OUP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, PCM_MSTR_MODE = 00b, $f_S = 48kHz$, $f_{BCLK} = 3.072MHz$, BST_BYP_MODE = 00b (automatic), AMP_FET_SCALE_MODE = 00b (automatic), DSP_GLOBAL_EN = 0, $T_A = T_{MIN}$ to T_{MAX} , typical values are at $T_A = +25^\circ C$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------------|--|---------------|-----|-----|---------|
| Bus Free Time Between STOP and START Conditions | t_{BUF} | | 0.5 | | | μs |
| Hold Time (Repeated) START Condition | $t_{HD,STA}$ | | 0.26 | | | μs |
| SCL Pulse-Width Low | t_{LOW} | | 0.5 | | | μs |
| SCL Pulse-Width High | t_{HIGH} | | 0.26 | | | μs |
| Setup Time for a Repeated START Condition | $t_{SU,STA}$ | | 0.26 | | | μs |
| Data Hold Time | $t_{HD,DAT}$ | | 0 | | 900 | ns |
| Data Setup Time | $t_{SU,DAT}$ | | 50 | | | ns |
| SDA and SCL Receiving Rise Time | t_R | C_B in pF | 20 + $0.1C_B$ | | 120 | ns |
| SDA and SCL Receiving Fall Time | t_F | C_B in pF | 20 + $0.1C_B$ | | 120 | ns |
| SDA Transmitting Fall Time | t_F | $V_{DVDD} = 1.71V$ | 20 | | 120 | ns |
| Setup Time for STOP Condition | $t_{SU,STO}$ | | 0.26 | | | μs |
| Bus Capacitance | C_B | | | | 550 | pF |
| Pulse Width of Suppressed Spike | t_{SP} | | 0 | | 50 | ns |
| RESET TIMING | | | | | | |
| Minimum \overline{RESET} Low Time | t_{RESET_LOW} | Minimum low time for \overline{RESET} to ensure device shutdown, $T_A = +25^\circ C$ (Note 3) | | 0.1 | 1 | μs |
| Release from \overline{RESET} | t_{I2C_READY} | Time from rising edge of \overline{RESET} to I ² C communication available, $T_A = +25^\circ C$ | | | 0.9 | ms |

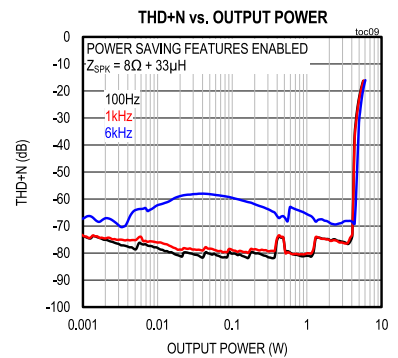
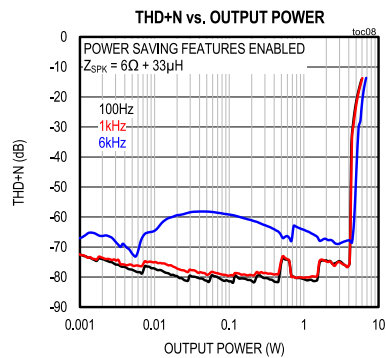
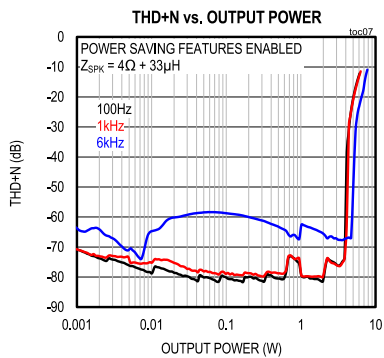
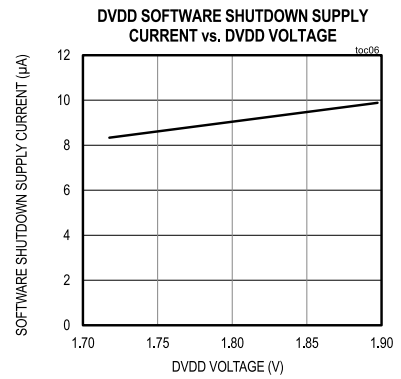
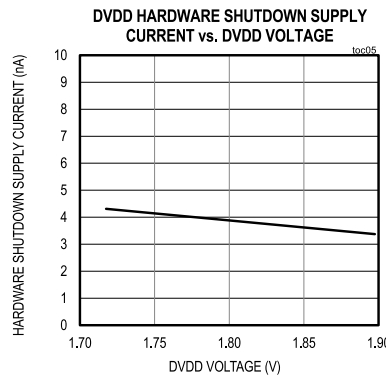
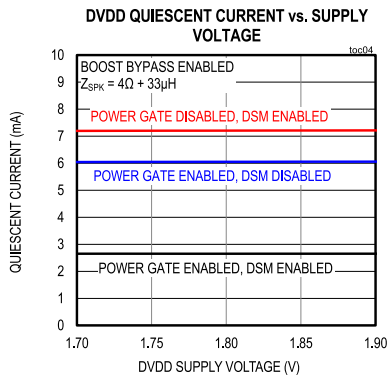
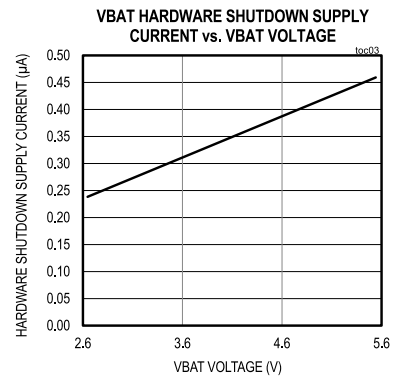
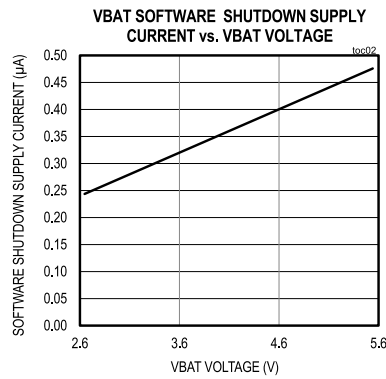
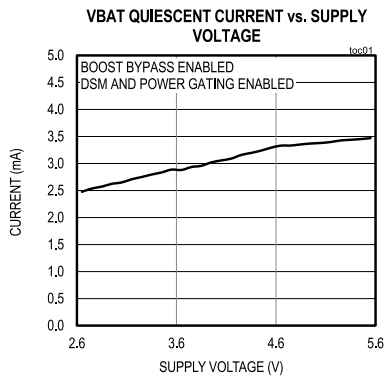
Note 2: Limits are 100% tested at $T_A = +25^\circ C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 3: Min/max limits are based bench data at $T_A = +25^\circ C$, are not guaranteed, and are for informational purpose only.

Note 4: Digital filter performance is invariant over temperature and production tested at $T_A = +25^\circ C$.

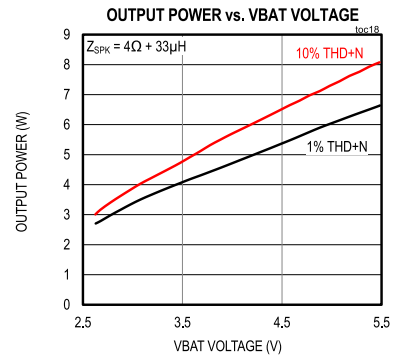
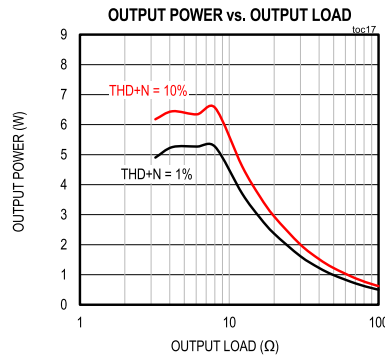
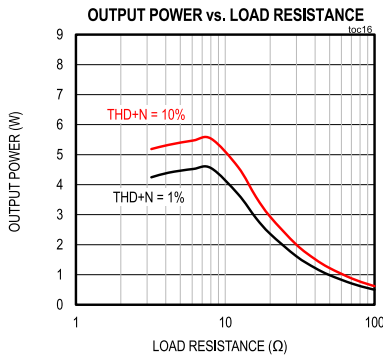
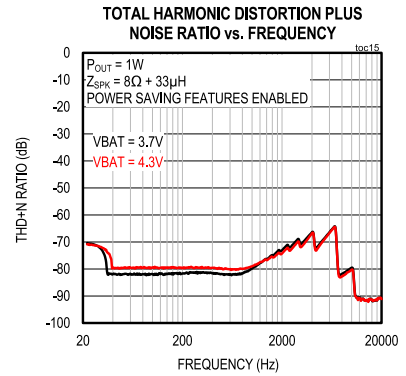
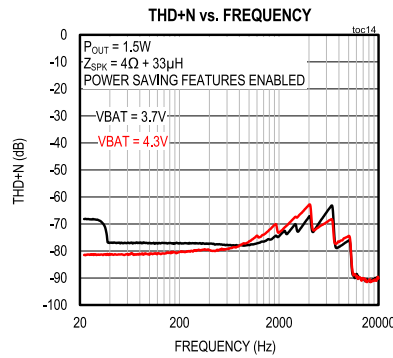
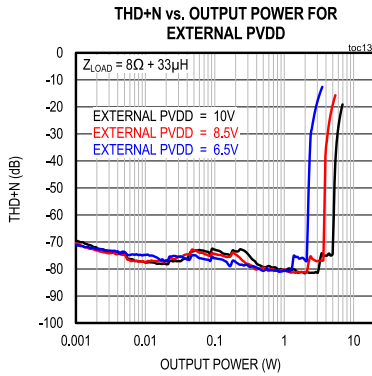
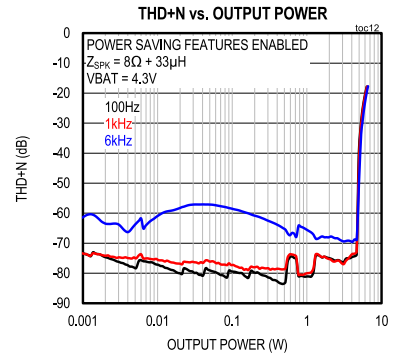
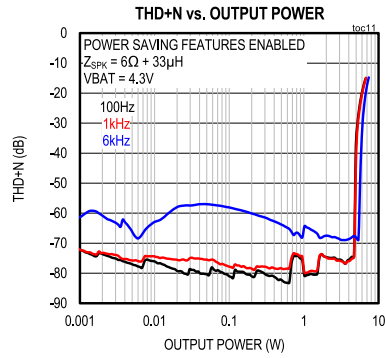
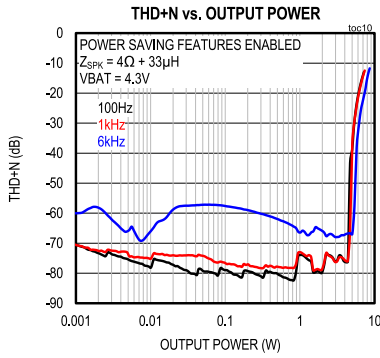
Typical Operating Characteristics

($V_{VBAT} = 3.7V$, $V_{DVDD} = 1.8V$, $V_{GND} = 0V$, $V_{PGND} = 0V$, $V_{PVDD} = 10V$ (BST_VOUT = 11100b), $L_1 = 1\mu H$, $C_{VBAT} = 10\mu F + 0.1\mu F + 10\mu F$, $C_{PVDD} = 0.1\mu F + 10\mu F + 10\mu F$, $C_{DVDD} = 0.1\mu F$, $C_{VREFC} = 1\mu F$, $R_{VREFC} = 30\Omega$, Amplifier Volume = +0dB (DSM_VOL_CTRL = 0xA0), $Z_{SPK} = \infty$ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, PCM_MSTR_MODE = 00b, $f_S = 48kHz$, $f_{BCLK} = 3.072MHz$, BST_BYP_MODE = 00b (automatic), AMP_FET_SCALE_MODE = 00b (automatic), DSP_GLOBAL_EN = 0, $T_A = +25^\circ C$)



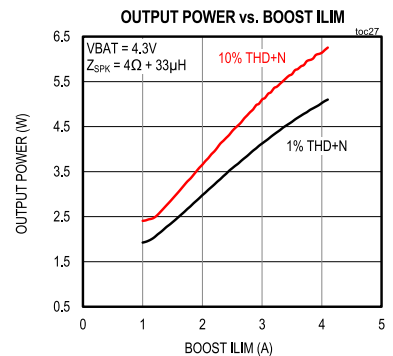
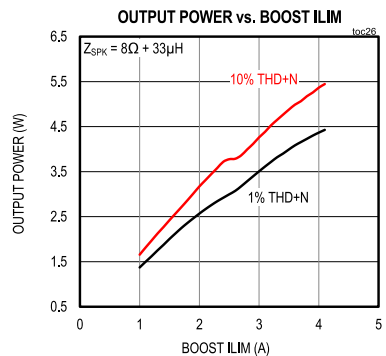
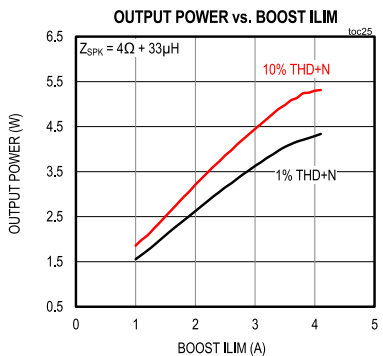
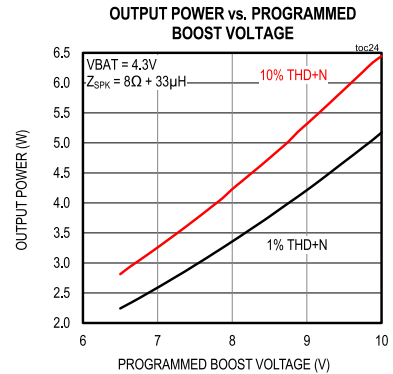
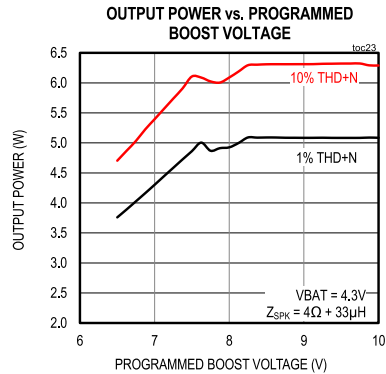
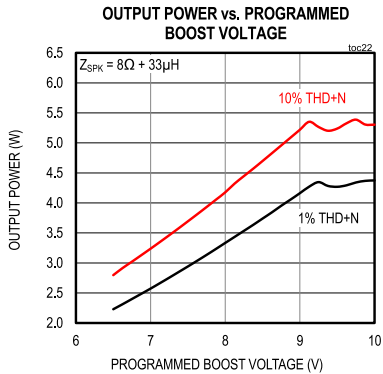
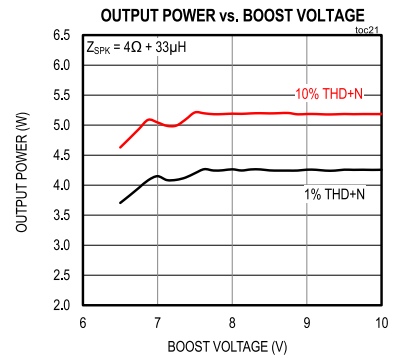
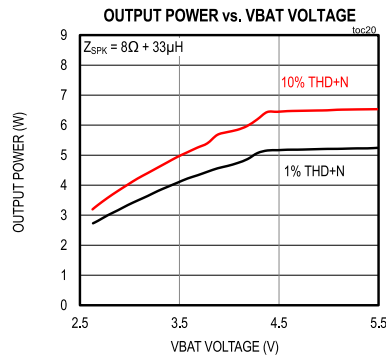
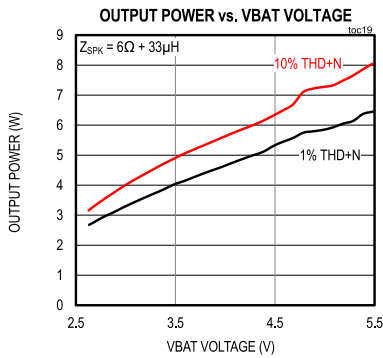
Typical Operating Characteristics (continued)

($V_{VBAT} = 3.7V$, $V_{DVDD} = 1.8V$, $V_{GND} = 0V$, $V_{PGND} = 0V$, $V_{PVDD} = 10V$ (BST_VOUT = 11100b), $L_1 = 1\mu H$, $C_{VBAT} = 10\mu F + 0.1\mu F + 10\mu F$, $C_{PVDD} = 0.1\mu F + 10\mu F + 10\mu F$, $C_{DVDD} = 0.1\mu F$, $C_{VREFC} = 1\mu F$, $R_{VREFC} = 30\Omega$, Amplifier Volume = +0dB (DSM_VOL_CTRL = 0xA0), $Z_{SPK} = \infty$ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, PCM_MSTR_MODE = 00b, $f_S = 48kHz$, $f_{BCLK} = 3.072MHz$, BST_BYP_MODE = 00b (automatic), AMP_FET_SCALE_MODE = 00b (automatic), DSP_GLOBAL_EN = 0, $T_A = +25^\circ C$)



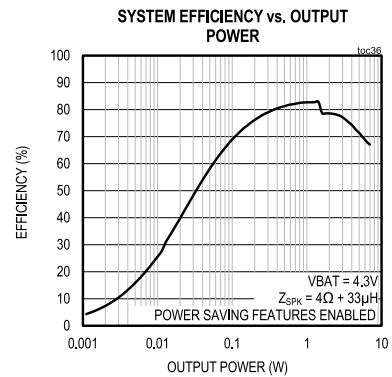
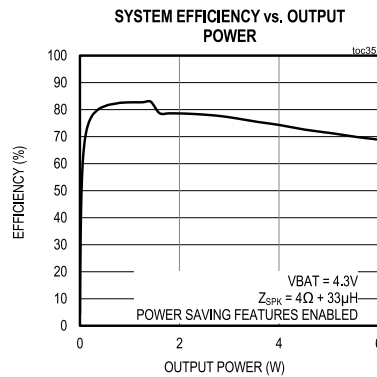
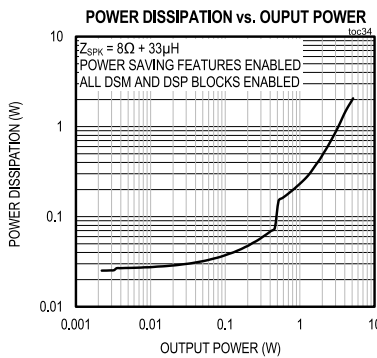
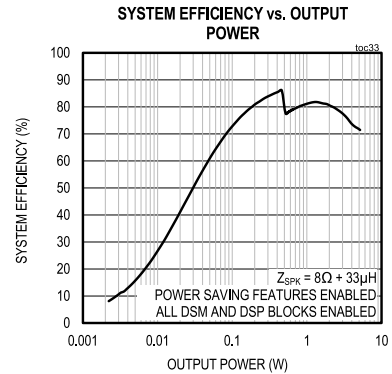
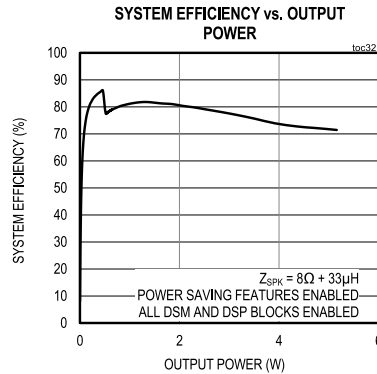
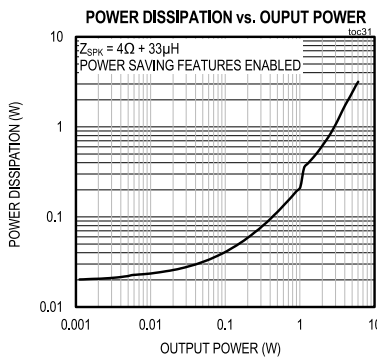
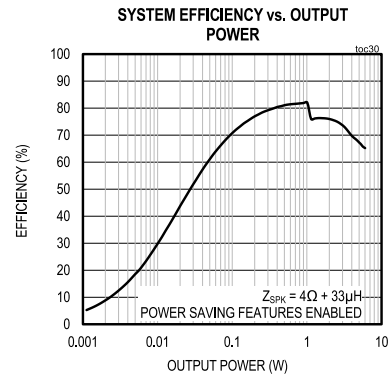
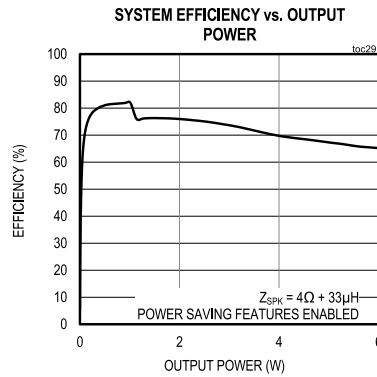
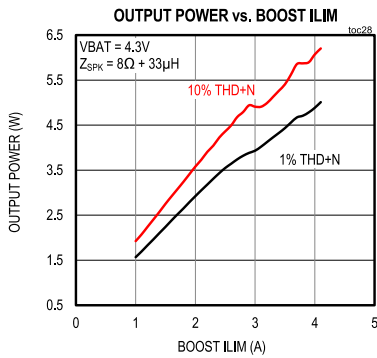
Typical Operating Characteristics (continued)

($V_{VBAT} = 3.7V$, $V_{DVDD} = 1.8V$, $V_{GND} = 0V$, $V_{PGND} = 0V$, $V_{PVDD} = 10V$ (BST_VOUT = 11100b), $L_1 = 1\mu H$, $C_{VBAT} = 10\mu F + 0.1\mu F + 10\mu F$, $C_{PVDD} = 0.1\mu F + 10\mu F + 10\mu F$, $C_{DVDD} = 0.1\mu F$, $C_{VREFC} = 1\mu F$, $R_{VREFC} = 30\Omega$, Amplifier Volume = +0dB (DSM_VOL_CTRL = 0xA0), $Z_{SPK} = \infty$ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, PCM_MSTR_MODE = 00b, $f_S = 48kHz$, $f_{BCLK} = 3.072MHz$, BST_BYP_MODE = 00b (automatic), AMP_FET_SCALE_MODE = 00b (automatic), DSP_GLOBAL_EN = 0, $T_A = +25^\circ C$)



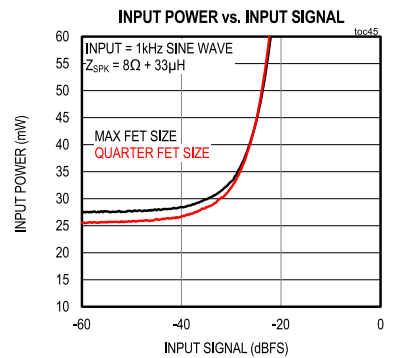
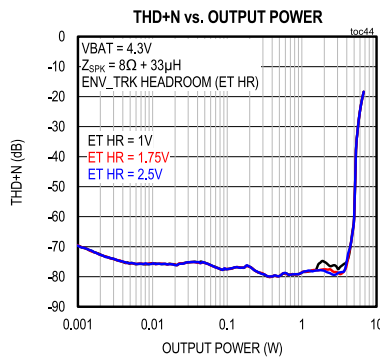
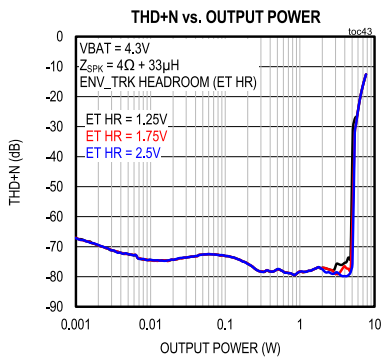
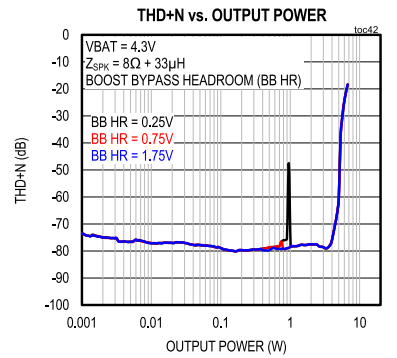
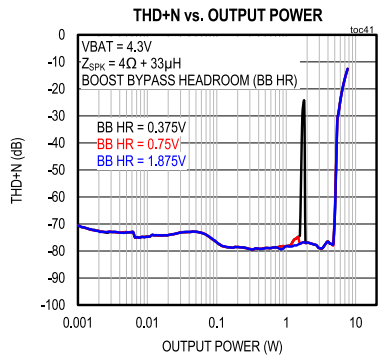
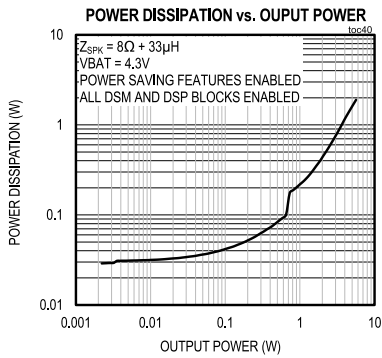
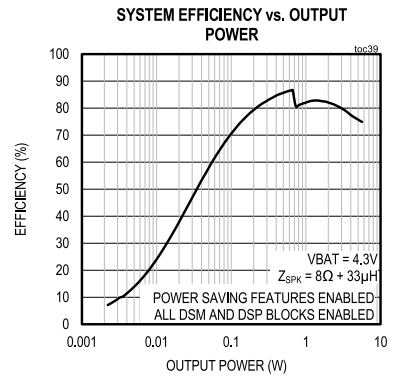
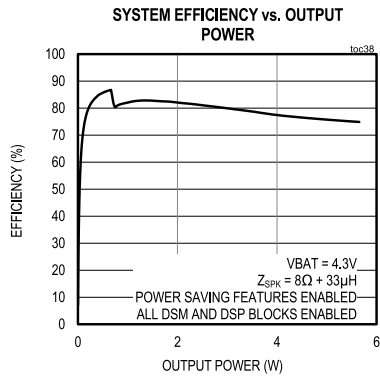
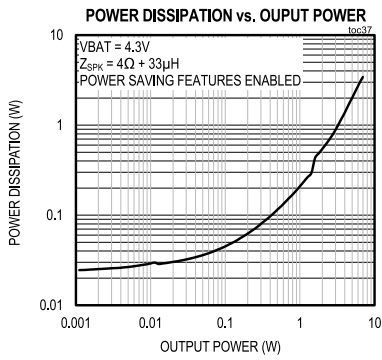
Typical Operating Characteristics (continued)

($V_{BAT} = 3.7V$, $V_{DVDD} = 1.8V$, $V_{GND} = 0V$, $V_{PGND} = 0V$, $V_{PVDD} = 10V$ (BST_VOUT = 11100b), $L_1 = 1\mu H$, $C_{VBAT} = 10\mu F + 0.1\mu F + 10\mu F$, $C_{PVDD} = 0.1\mu F + 10\mu F + 10\mu F$, $C_{DVDD} = 0.1\mu F$, $C_{VREFC} = 1\mu F$, $R_{VREFC} = 30\Omega$, Amplifier Volume = +0dB (DSM_VOL_CTRL = 0xA0), $Z_{SPK} = \infty$ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, PCM_MSTR_MODE = 00b, $f_S = 48kHz$, $f_{BCLK} = 3.072MHz$, BST_BYP_MODE = 00b (automatic), AMP_FET_SCALE_MODE = 00b (automatic), DSP_GLOBAL_EN = 0, $T_A = +25^\circ C$)



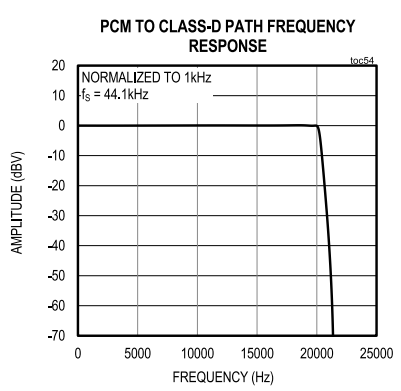
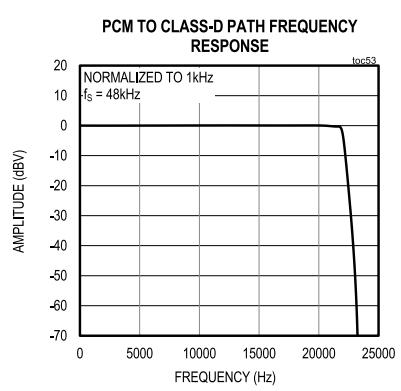
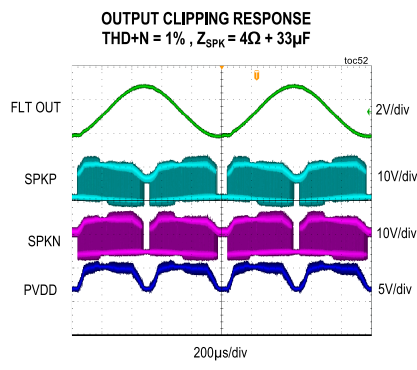
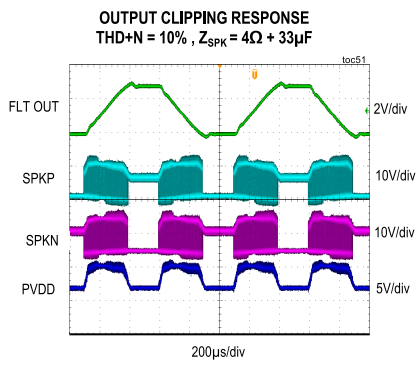
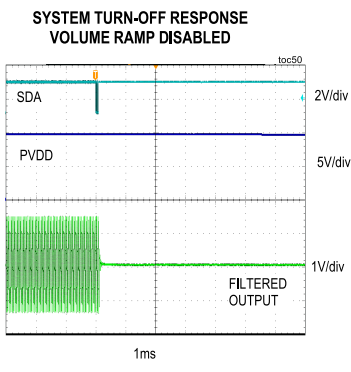
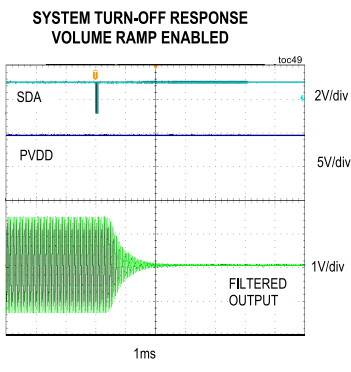
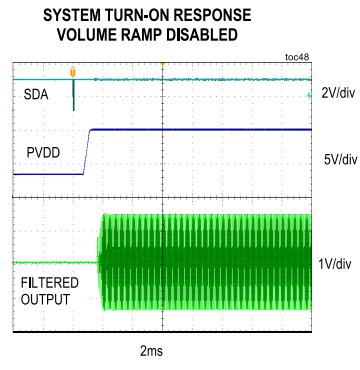
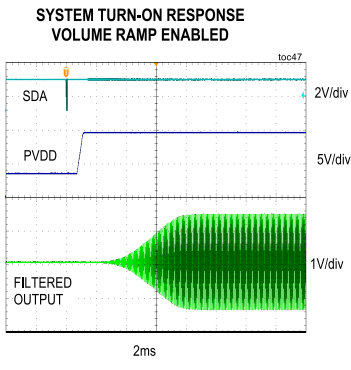
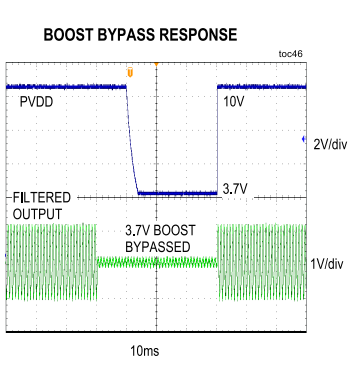
Typical Operating Characteristics (continued)

($V_{BAT} = 3.7V$, $V_{DVDD} = 1.8V$, $V_{GND} = 0V$, $V_{PGND} = 0V$, $V_{PVDD} = 10V$ (BST_VOUT = 11100b), $L_1 = 1\mu H$, $C_{VBAT} = 10\mu F + 0.1\mu F + 10\mu F$, $C_{PVDD} = 0.1\mu F + 10\mu F + 10\mu F$, $C_{DVDD} = 0.1\mu F$, $C_{VREFC} = 1\mu F$, $R_{VREFC} = 30\Omega$, Amplifier Volume = +0dB (DSM_VOL_CTRL = 0xA0), $Z_{SPK} = \infty$ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, PCM_MSTR_MODE = 00b, $f_S = 48kHz$, $f_{BCLK} = 3.072MHz$, BST_BYP_MODE = 00b (automatic), AMP_FET_SCALE_MODE = 00b (automatic), DSP_GLOBAL_EN = 0, $T_A = +25^\circ C$)



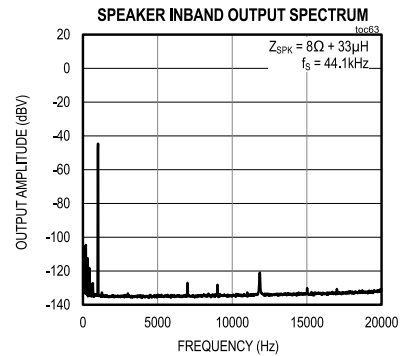
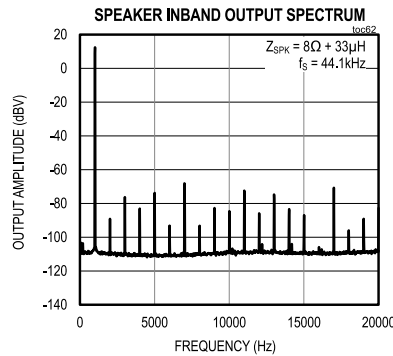
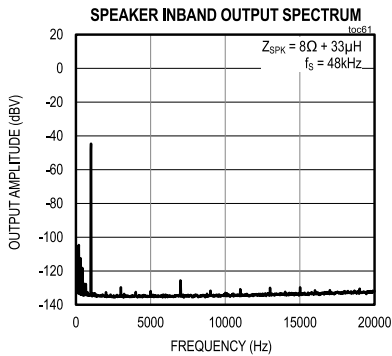
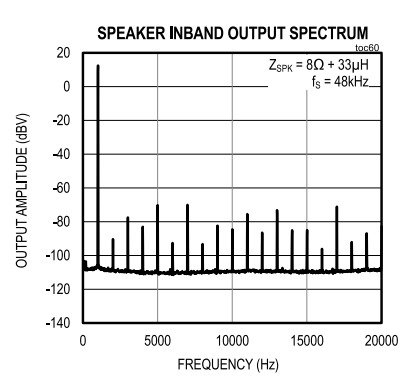
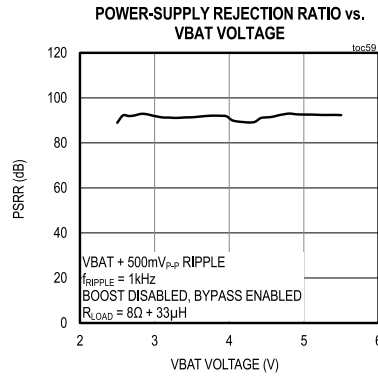
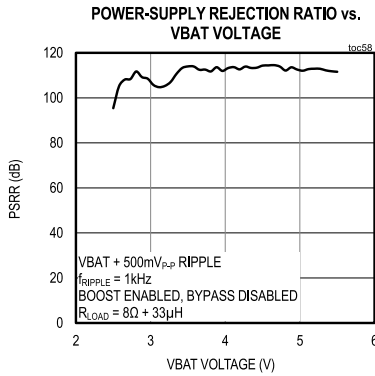
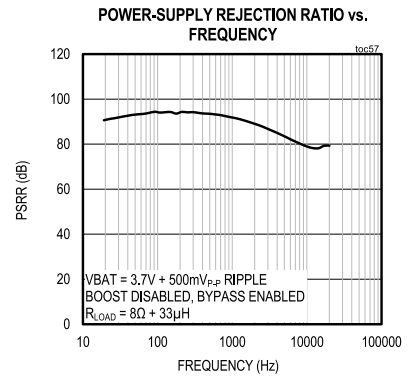
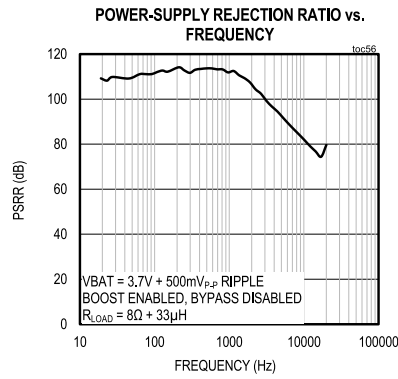
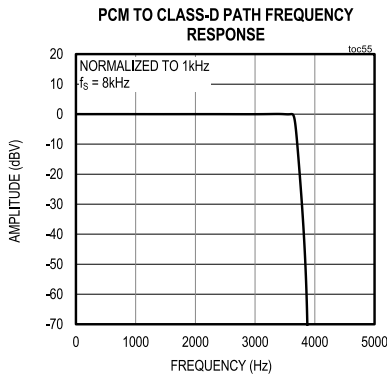
Typical Operating Characteristics (continued)

($V_{BAT} = 3.7V$, $V_{DVDD} = 1.8V$, $V_{GND} = 0V$, $V_{PGND} = 0V$, $V_{PVDD} = 10V$ (BST_VOUT = 11100b), $L_1 = 1\mu H$, $C_{VBAT} = 10\mu F + 0.1\mu F + 10\mu F$, $C_{PVDD} = 0.1\mu F + 10\mu F + 10\mu F$, $C_{DVDD} = 0.1\mu F$, $C_{VREFC} = 1\mu F$, $R_{VREFC} = 30\Omega$, Amplifier Volume = +0dB (DSM_VOL_CTRL = 0xA0), $Z_{SPK} = \infty$ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, PCM_MSTR_MODE = 00b, $f_S = 48kHz$, $f_{BCLK} = 3.072MHz$, BST_BYP_MODE = 00b (automatic), AMP_FET_SCALE_MODE = 00b (automatic), DSP_GLOBAL_EN = 0, $T_A = +25^\circ C$)



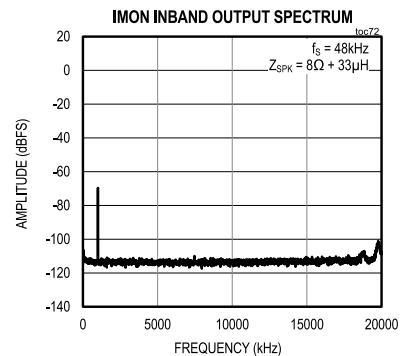
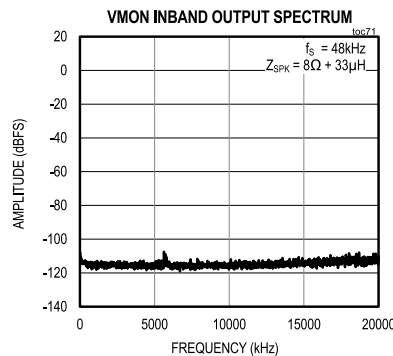
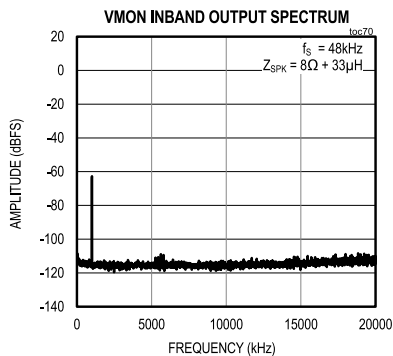
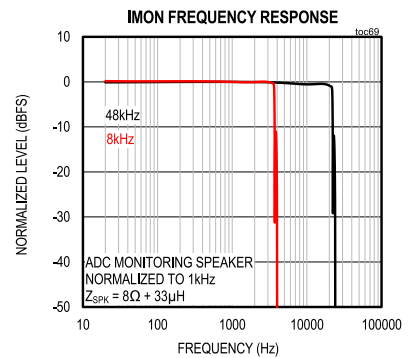
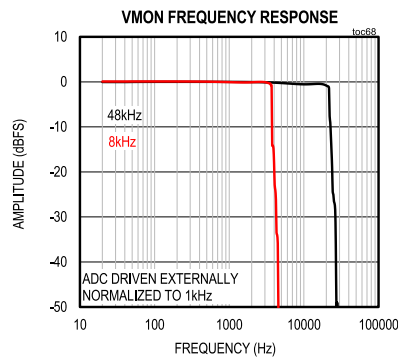
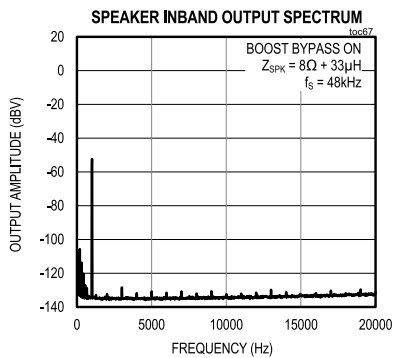
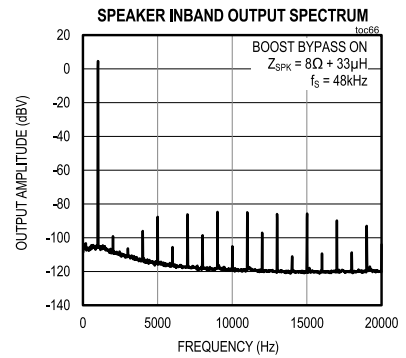
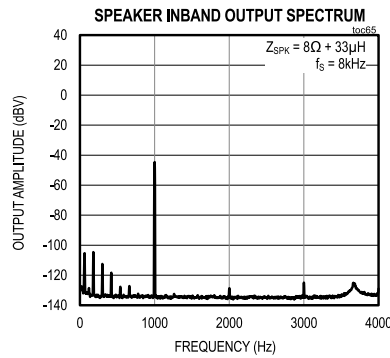
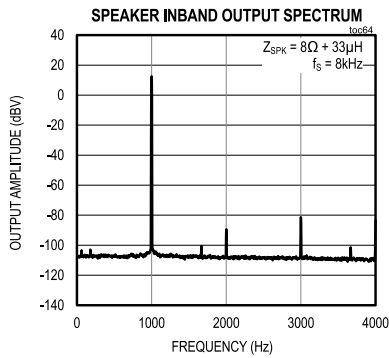
Typical Operating Characteristics (continued)

($V_{VBAT} = 3.7V$, $V_{DVDD} = 1.8V$, $V_{GND} = 0V$, $V_{PGND} = 0V$, $V_{PVDD} = 10V$ (BST_VOUT = 11100b), $L_1 = 1\mu H$, $C_{VBAT} = 10\mu F + 0.1\mu F + 10\mu F$, $C_{PVDD} = 0.1\mu F + 10\mu F + 10\mu F$, $C_{DVDD} = 0.1\mu F$, $C_{VREFC} = 1\mu F$, $R_{VREFC} = 30\Omega$, Amplifier Volume = +0dB (DSM_VOL_CTRL = 0xA0), $Z_{SPK} = \infty$ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, PCM_MSTR_MODE = 00b, $f_S = 48kHz$, $f_{BCLK} = 3.072MHz$, BST_BYP_MODE = 00b (automatic), AMP_FET_SCALE_MODE = 00b (automatic), DSP_GLOBAL_EN = 0, $T_A = +25^\circ C$)



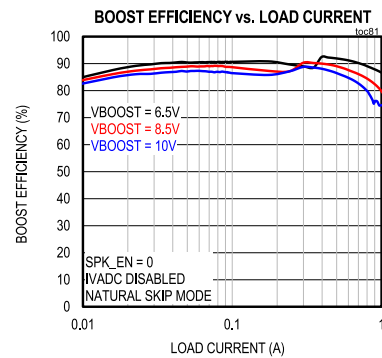
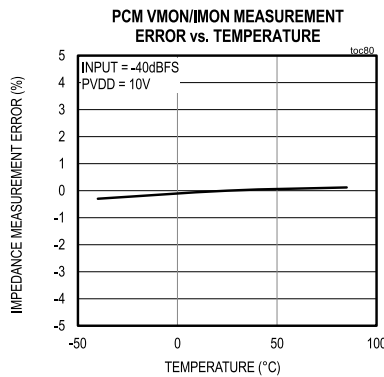
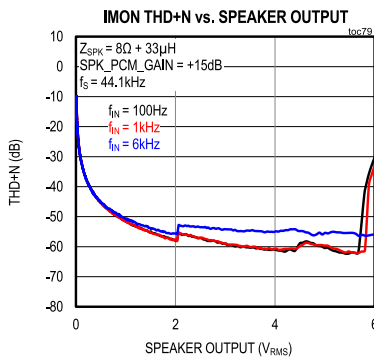
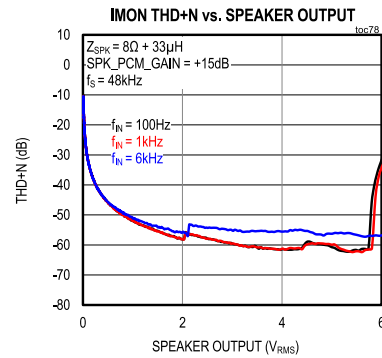
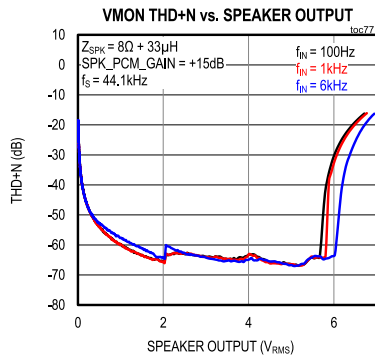
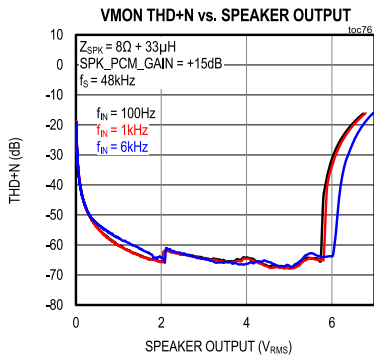
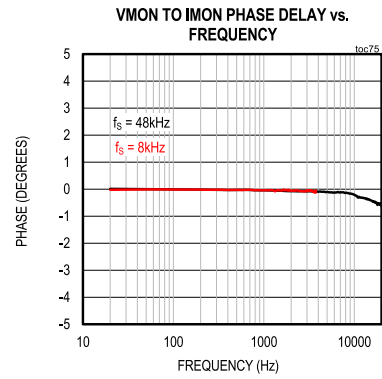
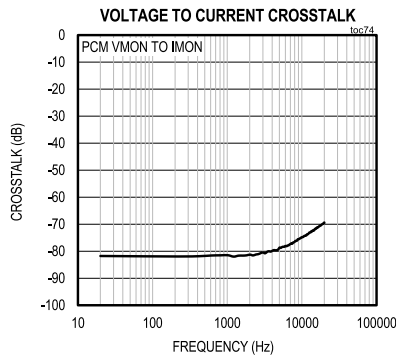
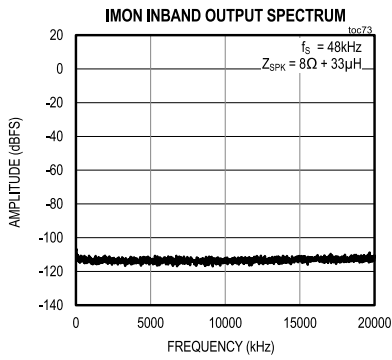
Typical Operating Characteristics (continued)

($V_{BAT} = 3.7V$, $V_{DVDD} = 1.8V$, $V_{GND} = 0V$, $V_{PGND} = 0V$, $V_{PVDD} = 10V$ (BST_VOUT = 11100b), $L_1 = 1\mu H$, $C_{VBAT} = 10\mu F + 0.1\mu F + 10\mu F$, $C_{PVDD} = 0.1\mu F + 10\mu F + 10\mu F$, $C_{DVDD} = 0.1\mu F$, $C_{VREFC} = 1\mu F$, $R_{VREFC} = 30\Omega$, Amplifier Volume = +0dB (DSM_VOL_CTRL = 0xA0), $Z_{SPK} = \infty$ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, PCM_MSTR_MODE = 00b, $f_s = 48kHz$, $f_{BCLK} = 3.072MHz$, BST_BYP_MODE = 00b (automatic), AMP_FET_SCALE_MODE = 00b (automatic), DSP_GLOBAL_EN = 0, $T_A = +25^\circ C$)



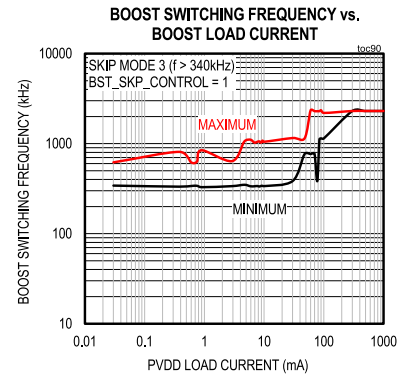
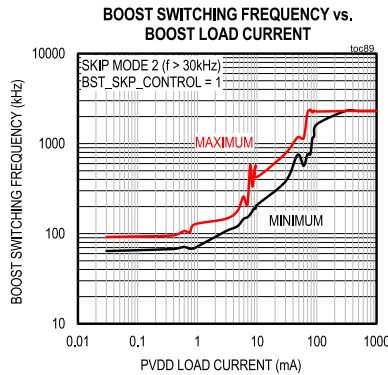
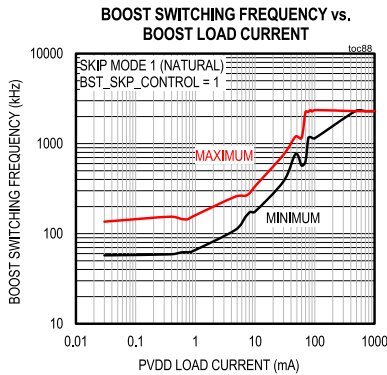
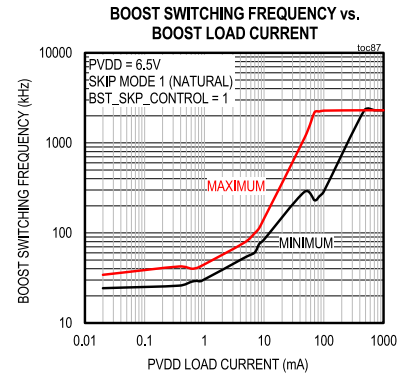
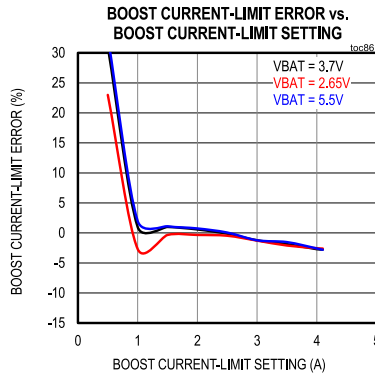
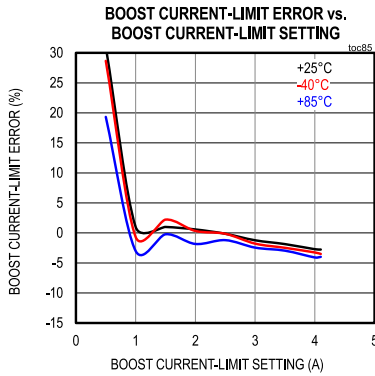
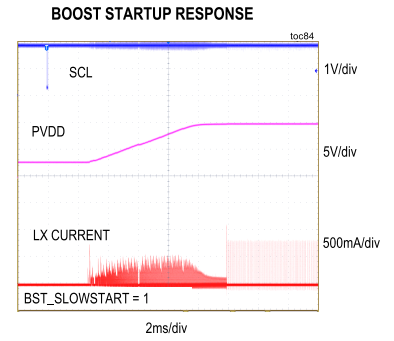
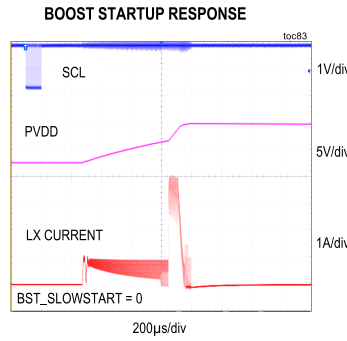
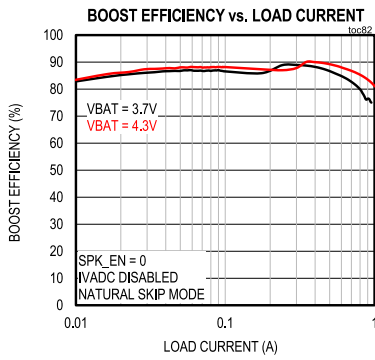
Typical Operating Characteristics (continued)

($V_{VBAT} = 3.7V$, $V_{DVDD} = 1.8V$, $V_{GND} = 0V$, $V_{PGND} = 0V$, $V_{PVDD} = 10V$ (BST_VOUT = 11100b), $L_1 = 1\mu H$, $C_{VBAT} = 10\mu F + 0.1\mu F + 10\mu F$, $C_{PVDD} = 0.1\mu F + 10\mu F + 10\mu F$, $C_{DVDD} = 0.1\mu F$, $C_{VREFC} = 1\mu F$, $R_{VREFC} = 30\Omega$, Amplifier Volume = +0dB (DSM_VOL_CTRL = 0xA0), $Z_{SPK} = \infty$ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, PCM_MSTR_MODE = 00b, $f_S = 48kHz$, $f_{BCLK} = 3.072MHz$, BST_BYP_MODE = 00b (automatic), AMP_FET_SCALE_MODE = 00b (automatic), DSP_GLOBAL_EN = 0, $T_A = +25^\circ C$)



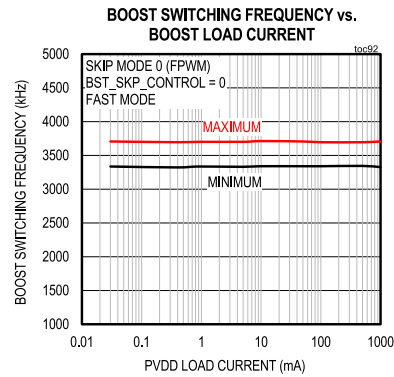
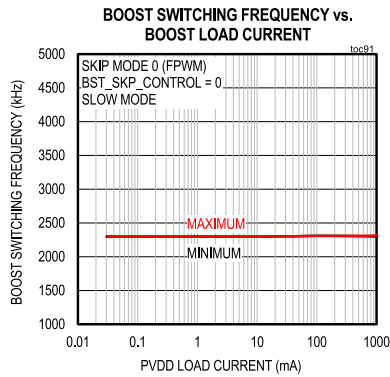
Typical Operating Characteristics (continued)

($V_{BAT} = 3.7V$, $V_{DVDD} = 1.8V$, $V_{GND} = 0V$, $V_{PGND} = 0V$, $V_{PVDD} = 10V$ (BST_VOUT = 11100b), $L_1 = 1\mu H$, $C_{VBAT} = 10\mu F + 0.1\mu F + 10\mu F$, $C_{PVDD} = 0.1\mu F + 10\mu F + 10\mu F$, $C_{DVDD} = 0.1\mu F$, $C_{VREFC} = 1\mu F$, $R_{VREFC} = 30\Omega$, Amplifier Volume = +0dB (DSM_VOL_CTRL = 0xA0), $Z_{SPK} = \infty$ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, PCM_MSTR_MODE = 00b, $f_S = 48kHz$, $f_{BCLK} = 3.072MHz$, BST_BYP_MODE = 00b (automatic), AMP_FET_SCALE_MODE = 00b (automatic), DSP_GLOBAL_EN = 0, $T_A = +25^\circ C$)



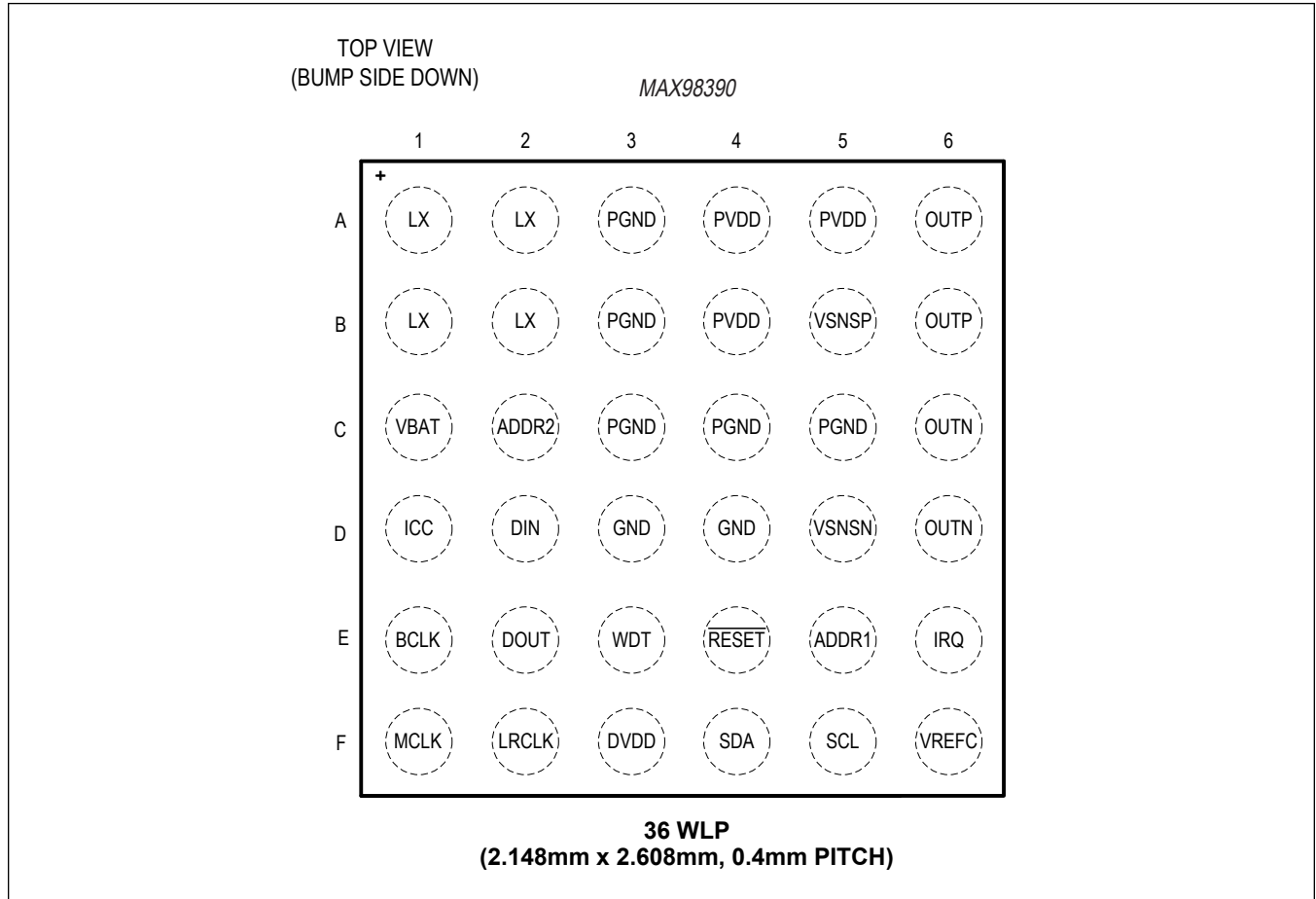
Typical Operating Characteristics (continued)

($V_{VBAT} = 3.7V$, $V_{DVDD} = 1.8V$, $V_{GND} = 0V$, $V_{PGND} = 0V$, $V_{PVDD} = 10V$ (BST_VOUT = 11100b), $L_1 = 1\mu H$, $C_{VBAT} = 10\mu F + 0.1\mu F + 10\mu F$, $C_{PVDD} = 0.1\mu F + 10\mu F + 10\mu F$, $C_{DVDD} = 0.1\mu F$, $C_{VREFC} = 1\mu F$, $R_{VREFC} = 30\Omega$, Amplifier Volume = +0dB (DSM_VOL_CTRL = 0xA0), $Z_{SPK} = \infty$ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, PCM_MSTR_MODE = 00b, $f_S = 48kHz$, $f_{BCLK} = 3.072MHz$, BST_BYP_MODE = 00b (automatic), AMP_FET_SCALE_MODE = 00b (automatic), DSP_GLOBAL_EN = 0, $T_A = +25^\circ C$)



Pin Configuration

36 WLP



Pin Description

| PIN | NAME | FUNCTION | REF SUPPLY | TYPE |
|--------|------|---|------------|--------|
| C1 | VBAT | Battery Voltage Input. V _{BAT} supplies the boost converter and other analog circuit blocks. Bypass V _{BAT} to GND with C _{VBAT1} and C _{VBAT2} , and to PGND with C _{VBAT3} . | — | Supply |
| F3 | DVDD | Digital Interface Logic Reference. Used for PCM interface, I ² C interface, and all digital I/O. In addition, powers the internal core supply regulator. Bypass to GND with 0.1µF capacitor. | — | Supply |
| D3, D4 | GND | Analog and Digital Ground. Connect to common ground plane of the application. | — | Supply |

Pin Description (continued)

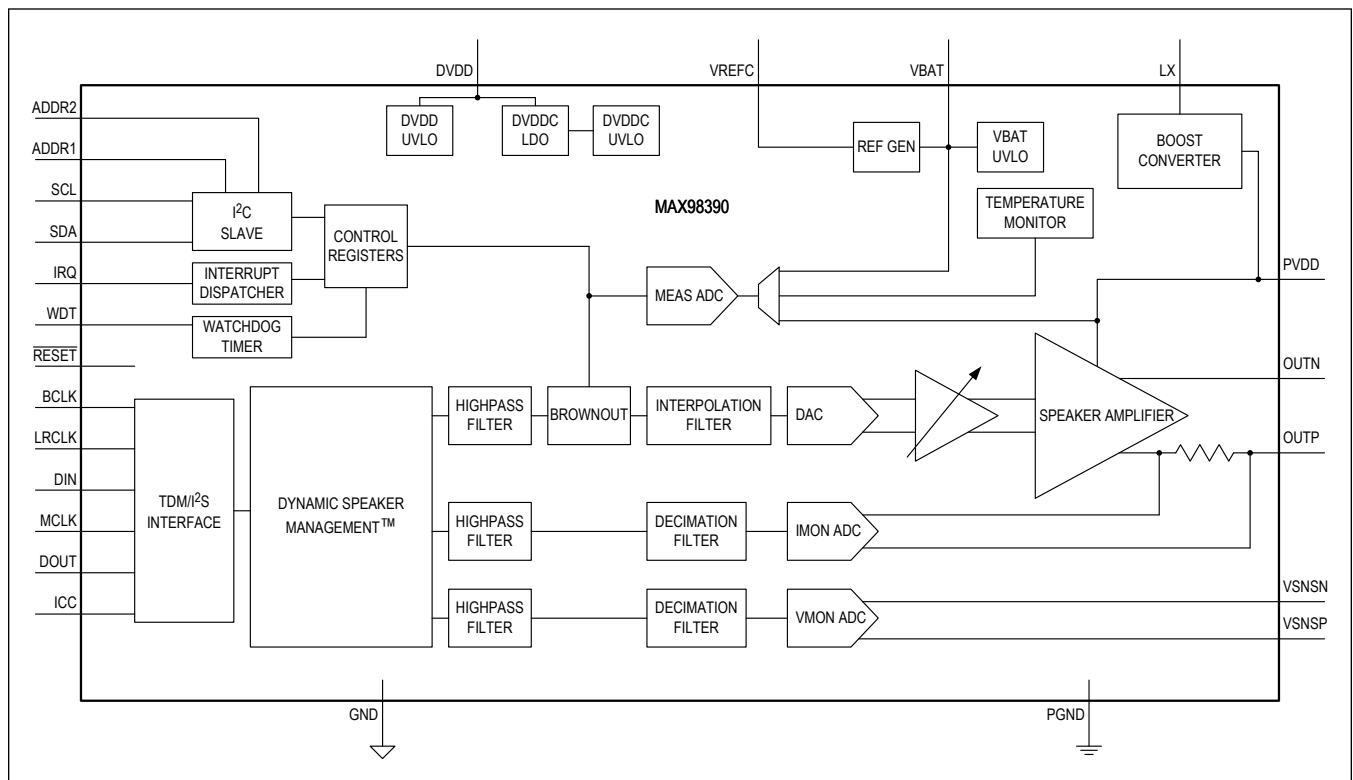
| PIN | NAME | FUNCTION | REF SUPPLY | TYPE |
|--------------------|---------------------------|--|------------|----------------------------|
| A4, A5, B4 | PVDD | Power Amplifier Supply and Boost Converter Output. PVDD supplies the Class-D power amplifier. In most applications, the PVDD pin is used to decouple the on-chip boost converter output using a 10 μ F capacitor and a 0.1 μ F capacitor to PGND. Note that LX is internally connected to the boost converter output, and therefore the PVDD pin, by a forward diode connection. When PVDD is supplied externally, the pin should be decoupled as required by the application. | — | Supply |
| A3, B3, C3, C4, C5 | PGND | Power Ground. Grounding for the boost converter and Class-D amplifier. Connect all PGND bumps together as close as possible to the IC. | — | Supply |
| A1, A2, B1, B2 | LX | Boost Inductor Switching Connection. LX is the drain of the boost switching MOSFET. Connect LX to the side of the inductor opposite VBAT. LX is internally connected to PVDD by the body diode of the boost high side switching MOSFET. | PVDD | Supply |
| F1 | MCLK | Optional Master Clock Input. Connect a 6MHz, 11.2896MHz, 12MHz, or 12.288MHz clock. Internally pulled down to GND through a 1M Ω resistor. | DVDD | Digital Input |
| E1 | BCLK | PCM Interface Bit Clock Input/Output. Internally pulled down to GND through a 1M Ω resistor. | DVDD | Digital I/O |
| F2 | LRCLK | PCM Interface Left-Right Clock Input/Output. LRCLK is the audio sample rate clock and determines whether audio data is routed to the left or right channel. In TDM mode, LRCLK is a frame sync pulse. Internally pulled down to GND through a 1M Ω resistor. | DVDD | Digital I/O |
| D2 | DIN | PCM Interface Data Input. Internally pulled down to GND through a 1M Ω resistor. | DVDD | Digital I/O |
| E2 | DOUT | PCM Interface Data Out | DVDD | Digital Output |
| F4 | SDA | I ² C-Compatible Serial-Data Input/Output. Connect a 1.5k Ω pullup resistor to DVDD for full output swing. | DVDD | Digital I/O (Open Drain) |
| F5 | SCL | I ² C-Compatible Serial-Clock Input. Connect a 1.5k Ω pullup resistor to DVDD for full output swing. | DVDD | Digital Input (Open Drain) |
| E6 | IRQ | Interrupt Output. See the IRQ Pin Configuration section for details. | DVDD | Digital Output |
| E4 | $\overline{\text{RESET}}$ | Hardware reset (active-low). Resets all digital portions of the device to default values. | DVDD | Digital Input |
| E5 | ADDR1 | Address Select 1. Used to select I ² C slave address. | DVDD | Digital Input |
| C2 | ADDR2 | Address Select 2. Used to select I ² C slave address. | DVDD | Digital Input |
| F6 | VREFC | Internal Bias. Connect to a 30 Ω resistor in series with a 1 μ F capacitor to GND. | VBAT | Analog Output |

Pin Description (continued)

| PIN | NAME | FUNCTION | REF SUPPLY | TYPE |
|--------|-------|--|------------|---------------|
| E3 | WDT | Watchdog Timer Input. WDT monitors the edge-to-edge period of an input watchdog timer signal. If the watchdog timer signal period is greater than the programmed timeout length then the audio path is disabled. Internally pulled down to GND through a 1MΩ resistor. | DVDD | Digital Input |
| D1 | ICC | Inter-Chip Communication Data I/O. Optionally allows multiple devices to communicate with each other in order to provide a consistent brownout response. Internally pulled down to GND through a 1MΩ resistor. | DVDD | Digital I/O |
| A6, B6 | OUTP | Speaker Amplifier Positive Output | PVDD | Analog Output |
| C6, D6 | OUTN | Speaker Amplifier Negative Output | PVDD | Analog Output |
| D5 | VSNSN | Voltage Sense Negative Input. Connect to the negative terminal of the loudspeaker as close as possible. | PVDD | Analog Input |
| B5 | VSNSP | Voltage Sense Positive Input. Connect to the positive terminal of the loudspeaker as close as possible. | PVDD | Analog Input |

Functional Diagram

MAX98390



Detailed Description

The MAX98390 is a high-efficiency mono Class-D DSM smart amplifier that features an integrated boost converter, integrated Dynamic Speaker Management, and FET scaling for higher-efficiency at low output power.

The maximum boost converter output voltage is programmable from 6.5V to 10V in 0.125V increments from a battery voltage as low as 2.65V. The boost converter supports bypass mode for lower quiescent current and improved mid power efficiency as well as envelope tracking which automatically adjusts the output voltage for maximum efficiency. The boosted supply efficiently delivers up to 6.2W at 10% THD+N into a 4Ω load.

Integrated IV sense and Dynamic Speaker Management allows louder, fuller audio while protecting the speaker against damage and improving sound quality.

The PCM interface supports I²S, left-justified, and 16-channel TDM formats as a slave or master device with I²C control. Either BCLK or MCLK can be used as the internal clock source providing system level flexibility.

Thermal and other status data can also be read from the I²C interface.

Patented active emissions limiting edge rate and overshoot control circuitry minimizes EMI and eliminates the need for output filtering found in traditional Class-D devices.

A flexible brownout-detection engine (BDE) can be programmed to initiate various current limiting, signal limiting and clip functions, based on battery voltage status. Threshold, hysteresis, and attack and release rates are programmable.

The IC is available in a 0.4mm pitch, 36-bump WLP package. It is specified over the extended -40°C to +85°C temperature range.

Integrated Dynamic Speaker Management (DSM)

Integrated DSM increases the loudness (sound pressure level or SPL) and bass response to maximize the performance of the audio subsystem with industry leading efficiency. DSM senses the voltage and current at the speaker and uses patented Maxim algorithms to unlock the full potential of the speaker. The DSM Path is enabled by setting DSP_GLOBAL_EN to 1.

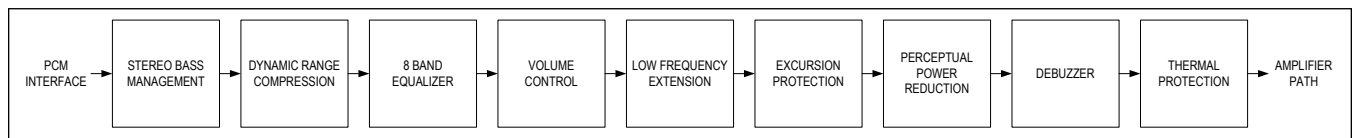


Figure 1. DSM Path

DSM Sound Studio

For more information on tuning DSM and programming DSM registers, see the *DSM Sound Studio* software that is included with the MAX98390 Evaluation System.

Thermal and Excursion Protection

By protecting speakers against overheating and over-excursion, DSM delivers twice the loudness and significantly deeper bass response.

DSMs thermal and excursion protection use the current and voltage feedback to monitor the speaker and ensure that the speaker is protected against damage.

DSM actively measures the speaker's load current and voltage and compares this against its DC resistance at a known temperature. The temperature coefficient of copper is then used to calculate speaker coil temperature. This ensures that the maximum power handling of a speaker can be utilized while not being exceeded.

Excursion is defined as the distance the diaphragm of the speaker moves during playback. If the diaphragm moves too far, this can lead to speaker damage. The DSM algorithm protects against over-excursion ensuring that the speaker

never exceeds its excursion limit.

Thermal protection is enabled by setting `THERMAL_PROT_EN = 1`.

Excursion protection is enabled by setting `EXCURSION_PROT_EN = 1`.

Low-Frequency Extension

DSM's ability to protect against overheating and over-excursion enables DSM to significantly extend a speaker's bass response below the resonant frequency.

Low-frequency extension is enabled by setting `BASS_EXT_EN = 1`.

Perceptual Power Reduction (PPR)

Maxim's patented PPR increases system efficiency by 10% to 25% (depending on audio content and speaker design) with no loss to audio fidelity. The PPR algorithm leverages the knowledge of the speaker response and human hearing response (also known as "equal loudness contour"). Using this information, the DSM algorithm is able to apply a dynamic, adaptive algorithm to filter the content that either the speaker cannot reproduce or that the listener cannot hear. For additional power savings in low-power modes, increasing the aggressiveness of PPR further decreases power consumption with a slight impact to audio fidelity.

PPR is enabled by setting `PPR_EN = 1`.

Stereo Bass Management

In a stereo system, lower frequencies are sent to both channels to maximize bass response while maintaining a stereo image in mid and high frequencies. Stereo bass management ensures that the phase shift due to left vs. right highpass filters do not result in cancelling frequencies.

Stereo bass management is enabled by setting `STEREO_BASS_EN` to 1.

Note that when `DSP_GLOBAL_EN = 0` and `EN = 1`, `STEREO_BASS_EN` must not be set to 1.

Debuzzer

Some speaker designs can produce an audible buzz at higher output levels. The debuzzer maximizes the SPL that the speaker can deliver without buzzing.

The debuzzer is enabled by setting `DEBUZZER_EN = 1`.

Dynamic Range Compression

Dynamic range compression attenuates loud signals and amplifies low signals. This ensures that the listener is not jarred by loud sounds like guns firing or blaring advertisements while still being able to hear softer sounds like footsteps or a quiet voice.

Dynamic range compression is enabled by setting `WBDRC_EN = 1`.

Note that RMS signal levels for compression thresholds (`DRC_COMP_THRESH`), noise gate thresholds (`DRC_NG_THRESH`), attack time (`DRC_ATK`), and release time (`DRC_RLS`) are continually approximated. The approximated RMS values for threshold levels may vary by up to ± 1 dB from the expected RMS value at 1kHz. The variation of the approximated RMS value increases as the input frequency decreases and/or the amplitude decreases. Furthermore, attack and release times can vary depending on dynamics and frequency content of the input signal.

Equalizer

The DSM path features eight individually programmable digital biquad filters.

The coefficients should be programmed before the equalizers are enabled. The transfer function for each band is defined as:

$$H(z) = \frac{B_0 + B_1z^{-1} + B_2z^{-2}}{1 + A_1z^{-1} + A_2z^{-2}}$$

The coefficients are stored using a two's complement format where the first 4 bits (DSM_EQ_BQy_Bz[23:20]) are the integer portion and the next 20 bits (DSM_EQ_BQy_Bz[19:0]) are the fractional portion (which results in an approximate +8 to -8 range for each coefficient).

For example, if the sample rate is 48kHz, a 1kHz highpass filter with a Q of 0.707 could be implemented in biquad number 5 with the coefficients in [Table 1](#).

Table 1. Coefficients for 1kHz Highpass Filter

| COEFFICIENT NAME | COEFFICIENT VALUE (dec) | DSM_EQ_BQ5_Bn[23:16] (hex) | DSM_EQ_BQ5_Bn[15:8] (hex) | DSM_EQ_BQ5_Bn[7:0] (hex) |
|------------------|-------------------------|----------------------------|---------------------------|--------------------------|
| B ₀ | 0.911575317 | 0E | 95 | D0 |
| B ₁ | -1.823149681 | E2 | D4 | 61 |
| B ₂ | 0.911575317 | 0E | 95 | D0 |
| A ₁ | -1.815318108 | E2 | F4 | 75 |
| A ₂ | 0.830982208 | 0D | 4B | B4 |

To read and write EQ registers, both EN and SPK_EN must be 0.

The EQ section is enabled by setting EQ8_EN to 1.

When enabled, all eight biquads are active. If a filter is not used, its coefficients should be programmed to:

- DSM_EQ_BQm_B0 = 0x100000
- DSM_EQ_BQm_B1 = 0x000000
- DSM_EQ_BQm_B2 = 0x000000
- DSM_EQ_BQm_A1 = 0x000000
- DSM_EQ_BQm_A2 = 0x000000

Reading and Writing DSM Registers

Both EN and SPK_EN must be 0 when reading and writing to register addresses 0x2100 to 0x23F3.

When writing to any of the three byte coefficients like the equalizer, the bytes must be written consecutively starting from [7:0], then [15:8], and [23:16] last. For example, to program DSM_EQ_BQ1_B2, follow these steps:

1. Write to DSM_EQ_BQ1_B2[7:0] (address 0x2131)
2. Write to DSM_EQ_BQ1_B2[15:8] (address 0x2132)
3. Write to DSM_EQ_BQ1_B2[23:16] (address 0x2133)

Note that the three byte coefficients are not initialized at power-on so they must be configured by the host whenever power is applied.

Interrupts

The device supports programmable interrupts for sending feedback to the host about events that have occurred on-chip. If IRQ_EN is 1, interrupts are output on the IRQ pin.

Each interrupt source has the following bits:

- *_RAW—Raw signal which is only high for as long as the source of the interrupt exists. For example, BOOSTCURRLIM_RAW is high while a short circuit is detected at the boost output. Note that a high state can be difficult to catch with an I²C read. This bit is included for diagnostic purposes and is not expected to be read in normal use. This bit is read-only.
- *_STATE—Set to 1 whenever a rising edge occurs on the associated *_RAW bit. For example, BOOSTCURRLIM_STATE goes high when a short circuit is initially detected at the boost output. It stays high until BOOSTCURRLIM_CLR or a power-on reset (for example when RST is set to 1) is asserted. This bit is read-only.
- *_FLAG—Maskable version of *_STATE. The *_FLAG bits from all interrupt sources are ORed together to generate IRQ. This bit is read-only.
- *_EN—Enable (unmask) bit for *_FLAG. This bit is read/write.
- *_CLR—Clears *_STATE and *_FLAG by writing a 1. Writing a 0 has no effect. This bit is write only.

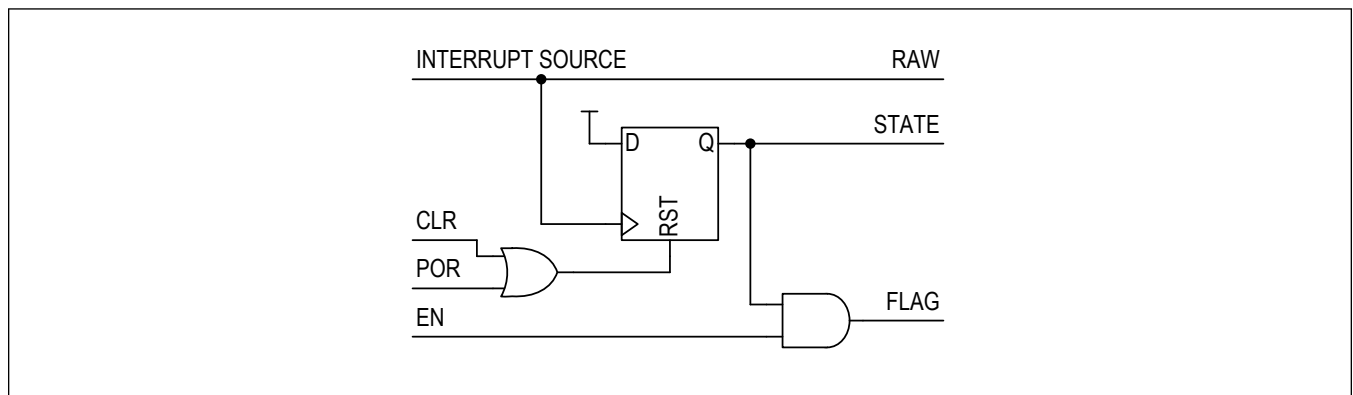


Figure 2. Interrupt Logic

IRQ Pin Configuration

IRQ_MODE controls the drive mode of IRQ. If IRQ_MODE is 0, the pin acts as an open-drained output and requires an external pullup resistor. If IRQ_MODE is 1, IRQ acts as a CMOS output.

IRQ_POL controls the polarity of IRQ. When IRQ_POL is 0, IRQ is low when any of the interrupt FLAG bits are high (i.e., active-low). When IRQ_POL is 1, IRQ is high when any of the interrupt FLAG bits are high (i.e., active-high).

Interrupt Sources

Table 2 lists the possible interrupt sources. For more information, see the [Register Details](#).

Table 2. Interrupt Sources

| NAME | DESCRIPTION |
|------------------------------|---|
| Thermal Shutdown Start Event | Indicates when the thermal-shutdown threshold has been exceeded. |
| Thermal Shutdown End Event | Indicates that the die temperature was previously above the thermal-shutdown threshold and has now dropped below the thermal-shutdown threshold minus the hysteresis setting. |
| Thermal Warning Start Event | Indicates when the thermal-warning threshold has been exceeded. |

Table 2. Interrupt Sources (continued)

| NAME | DESCRIPTION |
|---------------------------------|---|
| Thermal Warning End Event | Indicates that the die temperature was previously above the thermal-warning threshold and has now dropped below the thermal-warning threshold minus the hysteresis setting. |
| BDE Level 4 Event | Indicates that the BDE has transitioned into level 4. |
| BDE Level Change Event | Indicates that the BDE has transitioned between thresholds. |
| BDE Active Start Event | Indicates that the BDE is active. |
| BDE Active End Event | Indicates that the BDE is no longer active. |
| Boost UVLO Event | Indicates that the boost output has dropped below the minimum allowed voltage. |
| Speaker Overcurrent Event | Indicates that the speaker amplifier current limit has been exceeded. |
| Power Up Fail Event | Indicates when the device has not successfully completed power-up. |
| Power Up Done Event | Indicates when the device has completed power-up successfully. |
| Power Down Done Event | Indicates when the device has completed power-down. |
| Boost Input Current Limit Event | Indicates that the boost input current limit has been reached. |
| Watchdog Fail Event | Indicates that the watchdog timer has expired. |
| Watchdog Warning Event | Indicates that the software mode watchdog timer has exceeded 75%. |
| Data Monitor Event | Indicates that the data monitor has detected DC in the input signal. |
| Frame Error Recovery Event | Indicates that the device has recovered from a frame error. |
| Frame Error Event | Indicates that the ratio of BCLKs to LRCLKs does not match the PCM_BSEL/MSEL setting. |
| LRCLK Rate Error Recovery Event | Indicates that the device has recovered from a LRCLK rate error. |
| LRCLK Rate Error Event | Indicates that the LRCLK rate does not match the SPK_SR setting. |
| BCLK Rate Error Recovery Event | Indicates that the device has recovered from a BCLK rate error. |
| BCLK Rate Error Event | Indicates that the BCLK rate does not match the SPK_SR and PCM_xSEL settings. |

Boost Converter

The device features a boost converter that increases the supply voltage from VBAT to generate PVDD, which powers the Class-D amplifier. The boost converter output voltage is programmable and can be set in a range from 6.5V to 10V in 0.125V increments, using the BST_VOUT register. The boost converter output voltage should only be programmed when the device is in software shutdown.

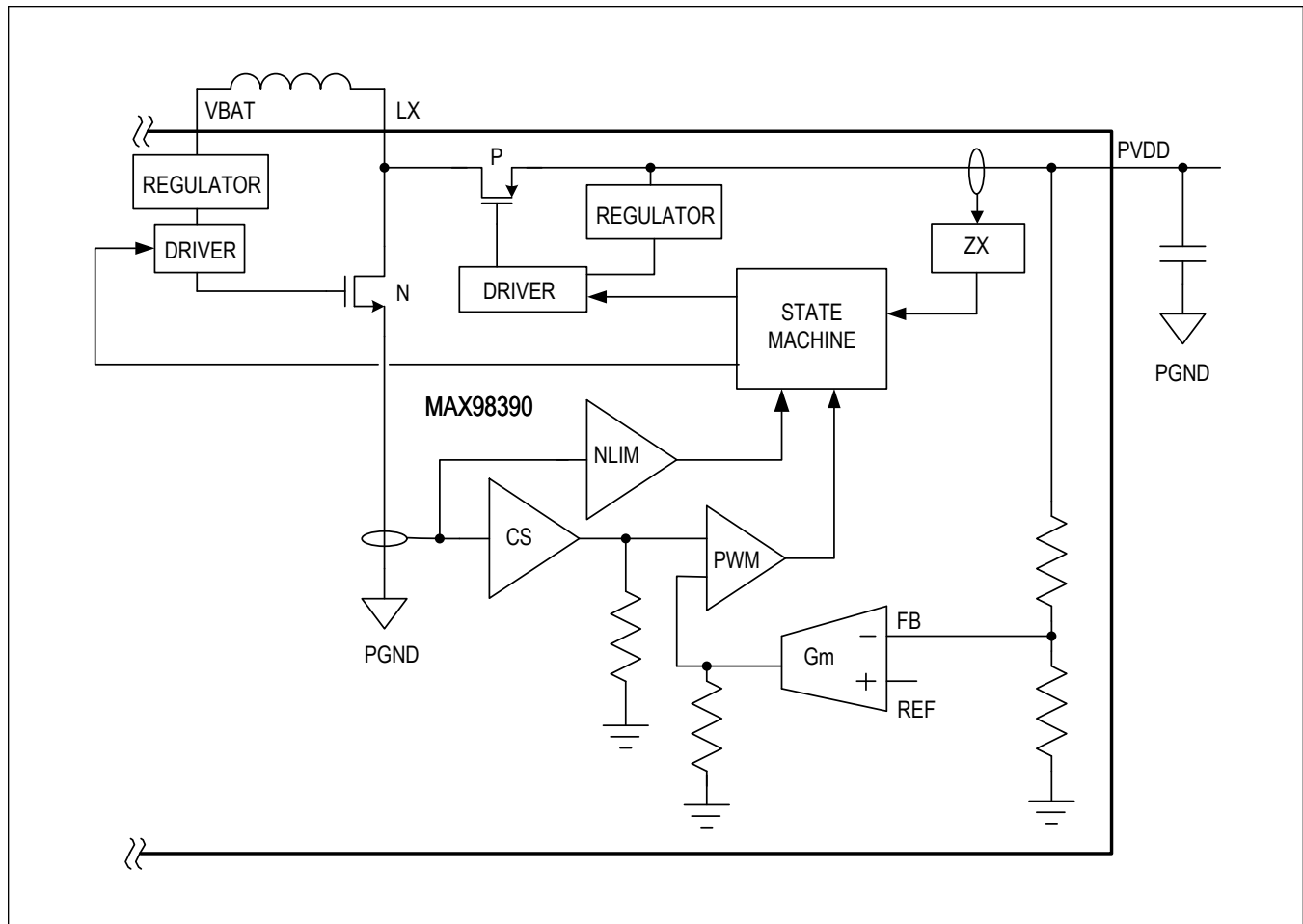


Figure 3. Boost Converter Block Diagram

Soft-Start

The device features a soft-start sequence to minimize inrush current and voltage overshoot on power-up. In shutdown, VBAT is connected to PVDD through a diode that charges PVDD to approximately 700mV below VBAT. When the IC is enabled, the soft-start ramps PVDD to its final value in a fixed time while maintaining a current limit of $I_{STARTUP}$ (see the [Electrical Characteristics](#) table). Maximum load current is available after the soft-start is completed.

For $C_{PVDD} \leq 100\mu\text{F}$, the default soft-start time of approximately t_{STR} should be expected. If $C_{PVDD} > 100\mu\text{F}$, the soft-start time should be increased to approximately 12ms by setting BST_SLOWSTART to 1. This extra time is necessary to allow the boost output to reach the final output value without the sudden inrush-current spike that would otherwise occur after t_{STR} .

Boost Output Undervoltage Lockout

The boost output undervoltage-lockout circuit compares the voltage at PVDD to VBAT to ensure that PVDD is high enough for the boost converter LX to PVDD FET to be turned on. If the voltage is insufficient, the undervoltage-lockout circuit causes the speaker output to become Hi-Z.

Boost Overvoltage Protection

The boost overvoltage protection circuit is activated when V_{PVDD} exceeds 10.5V. The circuit activates an internal 100 Ω pulldown resistor on PVDD to prevent V_{PVDD} from exceeding the absolute maximum rating on PVDD.

Programmable Boost Input Current Limit

The boost input current limit can be programmed using `BST_ILIM` to 0A, 0.5A, and between 1A to 4.1A in 50mA steps.

Note that `BST_ILIM` settings above 2.8A can be used only when V_{VBAT} is greater than 2.85V. If V_{VBAT} is likely to fall to less than 2.85V, the brownout-detection engine (BDE) can be used to automatically configure the `BST_ILIM` to a setting of 2.8A or lower.

Also note that boost input current limit does not function during boost-bypass mode.

Boost-Clock Phase

The phase of the boost converter can be altered to avoid overloading the supply when two or more devices are drawing heavy load current. When two or more devices are used, heavy loads can overload the supply source if the boost converters are switching in phase. The boost switching frequency can be phase shifted with respect to `LRCLK` to reduce the peak current draw from the supply source. There are four phase settings controlled by `BST_PHASE`.

Boost-Skip Mode

The device features different boost-skip modes (selectable with `BST_SKIPLOAD`) to achieve reduced power consumption from the boost converter block. When a skip mode is enabled, the boost converter switching frequency is reduced when no boost load current is needed. The reduced switching frequency greatly reduces the boost's idle power consumption.

There are two different boost-skip modes that can be chosen with varying levels of power consumption. Skip mode can also be disabled at the cost of increased idle power consumption.

Supplying PVDD Externally

The speaker amplifier can be directly powered at `PVDD` with an external supply in the range of 6.5V to 10V. Powering the speaker amplifier externally bypasses the boost converter and its associated losses.

To supply `PVDD` externally:

1. Depopulate the boost converter inductor (optional)
2. Apply V_{VBAT} and V_{DVDD}
3. Set V_{PVDD} to the same voltage as V_{VBAT}
4. Load desired register settings (these settings should include `BST_BYP_MODE = 0x02` and `EXT_PVDD_EN = 0x01`)
5. Set `EN = 1`
6. Ramp V_{PVDD} from V_{VBAT} to 10V (or desired voltage) with > 1.5ms rise time

To exit external `PVDD` mode:

1. Ramp V_{PVDD} from 10V down to V_{VBAT} with > 1.5ms fall time
2. Set `EN = 0`

Boost Envelope Tracker

The boost envelope tracker can dynamically adjust the boost output voltage according to the amplifier output's signal swing requirements in order to maximize efficiency.

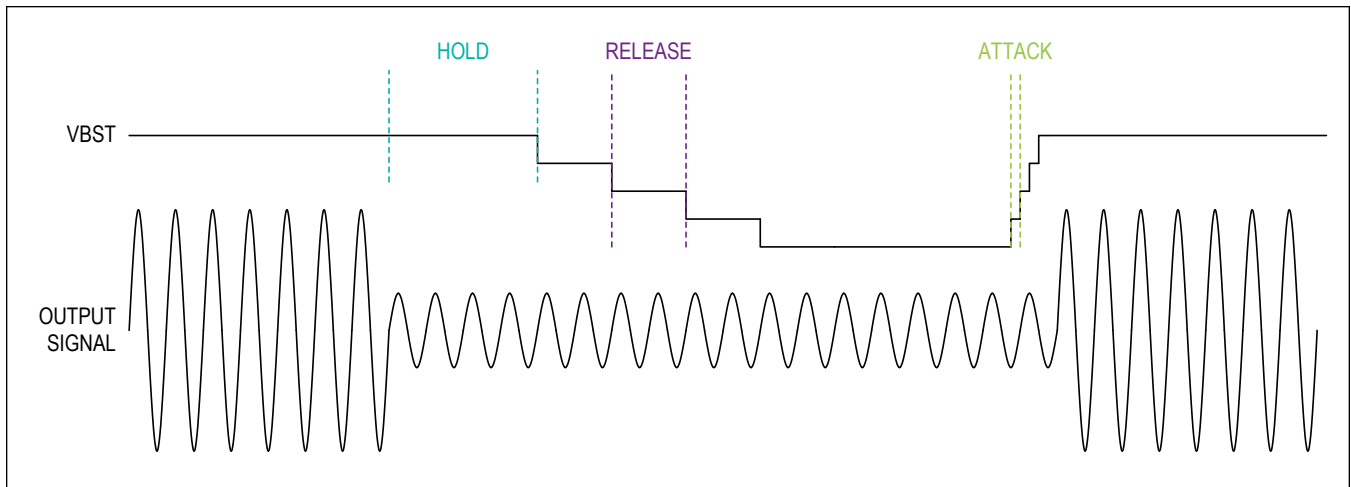


Figure 4. Boost Envelope Tracker

The envelope tracker monitors the input data to the DSP signal path using a peak-detect circuit. The envelope tracker is aware of the path gain and therefore knows the peak output signal from the device based on the input data it is monitoring. Using this information and accounting for the headroom programmed in `ENV_TRACKER_BST_VOUT_HEADROOM`, the envelope tracker can override the programmed value for the boost converter to use a lower voltage setting. The minimum voltage the envelope tracker can set the boost output is 6.5V, while the maximum voltage is defined by the `BST_VOUT` setting.

When the envelope tracker detects a fall in the output signal level, it first waits for the hold period as controlled by `ENV_TRACKER_HOLD_TIME`. If the output signal remains low enough for the boost output to be lowered, it is lowered at the release rate defined by `ENV_TRACKER_RLS_RATE` and `ENV_TRACKER_RLS_RATE_SCALE`. When the envelope tracker detects a rise in the output signal level that requires a rise in the boost output voltage, it immediately ramps up the boost converter output at the fastest possible attack rate.

The envelope tracker is enabled using `ENV_TRACKER_EN`. When enabled, the target boost output voltage setting current requested by the envelope tracker can be readback using `ENV_TRACKER_BST_VOUT_RD`.

Automatic Boost Bypass

Boost-bypass mode can dynamically turn off the boost according to the amplifier output's signal swing requirements in order to maximize efficiency.

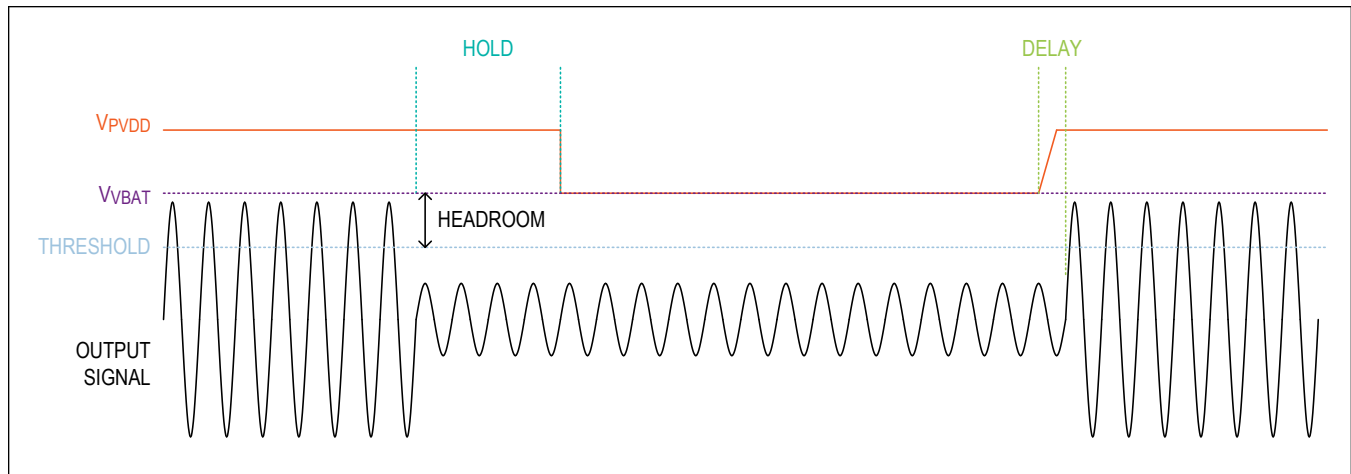


Figure 5. Boost Bypass

Automatic boost bypass monitors the input data to the DSP signal path using a peak-detect circuit. Automatic boost bypass is aware of the path gain and therefore knows the peak output signal from the device based on the input data it is monitoring. Using this information and accounting for the headroom programmed in `BST_BYP_HEADROOM`, the boost converter can automatically enter bypass mode to save power. In bypass mode, the boost stops switching and internally shorts VBAT to PVDD. While in bypass mode, boost output undervoltage lockout is disabled.

If the Class-D amplifier's output amplitude falls below the boost-bypass threshold for the hold period as controlled by `BST_BYP_HOLD_TIME`, the boost enters bypass mode. When the output amplitude rises above the boost-bypass threshold, the boost converter automatically turns on to support the higher output amplitude.

The boost-bypass threshold changes along with the battery voltage and is defined by V_{VBAT} minus the boost-bypass headroom. The boost-bypass headroom is controlled by the `BST_BYP_HEADROOM` register.

To enable automatic boost bypass, set the `BST_BYP_MODE` register to 00b or 11b. To disable automatic boost bypass and force the boost on while the amplifier is enabled, set `BST_BYP_MODE` to 10b. To force the boost into bypass mode regardless of the Class-D amplifier's output amplitude, set `BST_BYP_MODE` to 01b.

While `BST_BYP_MODE` is set to 00b or 11b, the measurement ADC is forced to a high rate so that the boost-bypass block can respond quickly to rapidly changing VBAT levels. The registers below are internally overridden with the values shown. The host can still read and write these registers, but the values are ignored.

- `MEAS_ADC_BASE_DIV` = 0x0023 (Measurement ADC sample rate = $12.288\text{MHz}/(35 + 1) = 341\text{kHz}$)
- `MEAS_ADC_CH0_EN` = 1 (Measurement ADC V_{VBAT} channel enable)
- `MEAS_ADC_CH0_DIV` = 0x00 (Measurement ADC battery voltage sample rate = $341\text{kHz}/(0 + 1) = 341\text{kHz}$)
- `MEAS_ADC_CH2_DIV` = 0x07 (Measurement ADC temperature sample rate = $341\text{kHz}/(7 + 1) = 42\text{kHz}$)

Also, while `BST_BYP_MODE` is set to 00b or 11b, the boost-bypass block internally bypasses the measurement ADC V_{VBAT} channel filter for fast response times. The `MEAS_ADC_CH0_FILT_EN` register still controls whether the BDE block and `MEAS_ADC_CH0_DATA` register contains filtered or unfiltered V_{VBAT} data.

Notes:

- Do not disable the measurement ADC while in boost-bypass mode.
- Soft-start and `I_STARTUP` do not apply when the boost turns on due to automatic boost bypass.
- The speed at which the boost voltage rises is proportional to the boost input current limit set by `BST_ILIM` or the BDE. If the boost voltage does not rise quickly enough, momentary output clipping can occur. Also see the [Delay for Envelope Tracker and Automatic Boost Bypass](#) section.

Delay for Envelope Tracker and Automatic Boost Bypass

To avoid the potential for clipping the output signal as the boost output rises, there is a programmable delay in the signal path controlled by ENV_BYP_DELAY. This allows the boost converter time to increase the output voltage before it is required to output larger signals. Table 3 shows the recommended settings for each sample rate to guarantee no clipping assuming the worst-case rise (6.5V to 10V) at the minimum boost input current-limit setting (1A) and the specified 10 μ F + 10 μ F + 0.1 μ F PVDD output capacitors shown in the [Recommended External Components](#) section. Higher current-limit settings mean faster response for the boost converter, so smaller delay settings can be used. Higher output capacitance (up to a maximum of 100 μ F) means slower response for the boost converter, so larger delay settings should be used. If using a boost output capacitance greater than 100 μ F, the envelope tracker should be disabled.

Table 3. Recommended Delay Settings

| SAMPLE RATE (kHz) | RECOMMENDED DELAY |
|-------------------|-------------------|
| 8 to 11.025 | 1 sample |
| 16 to 24 | 2 samples |
| 32 to 48 | 4 samples |

Host Fault Handling

The device has several methods of detecting a host fault and preventing unwanted signals from being passed to the amplifier output.

Clock Monitor

In PCM slave mode, the clock monitor can disable the device if BCLK and LRCLK inputs are invalid. The clock monitor is enabled by setting CMON_EN to 1.

Note that it is not valid to enable the clock monitor (CMON_EN = 1) while the PCM interface is in master mode (PCM_MSTR_MODE = 11). The clock monitor should only be used while in slave mode.

If SPK_EN, IVADC_I_EN, and IVADC_V_EN are all 0, or if EN is 0, then the clock monitor is not enabled and does not generate interrupts regardless of the state of CMON_EN.

The clock monitor can respond to a loss and reapplication of clock in two ways:

1. When CMON_AUTORESTART_EN is set to 0 and a clock error is detected, it generates an interrupt (BCLK_ERR_*, LRCLK_ERR_*, or FRAME_ERR_*) and disables the device by setting EN to 0. The host is required to write EN to 1 to restart the device. A *_RECOVER_* interrupt is NOT generated when a valid clock is reapplied.
2. When CMON_AUTORESTART_EN is set to 1 and a clock error is detected, it generates an interrupt (BCLK_ERR_*, LRCLK_ERR_*, or FRAME_ERR_*) and disables the device internally. When a valid clock is re-applied, it generates an interrupt (BCLK_RECOVER_*, LRCLK_RECOVER_*, or FRAME_RECOVER_*) and the device restarts automatically. The value of EN remains 1 throughout.

For best pop performance, DIN should be 0 when clocks are stopped or started.

BCLK and LRCLK Rate Detection

When the clock monitor is enabled, BCLK and LRCLK frequencies are compared against the frequency set by the combination of PCM_BSEL (or PCM_MSEL) and SPK_SR.

Clock rate errors are counted when BCLK or LRCLK frequencies stray from the programmed value.

CMON_ERRTOL sets the number of consecutive LRCLK periods with either BCLK or LRCLK rate errors before the device is disabled and an interrupt is generated. If CMON_AUTORESTART_EN = 1, CMON_ERRTOL also sets the number of consecutive frames with no errors needed for automatic restart to occur.

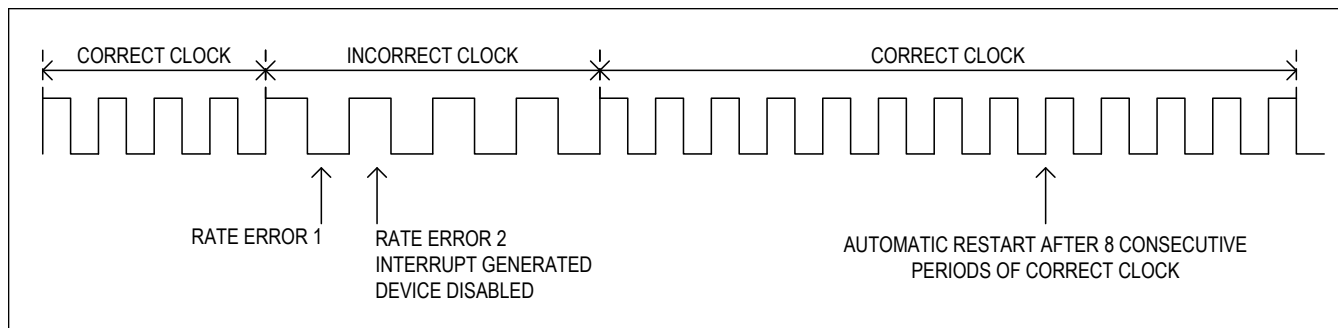


Figure 6. Clock Monitor LRCLK Rate Error Example with $CMON_ERRTOL = 0x1$

PCM Framing Error Detection

When the clock monitor is enabled, the number of BCLK periods per LRCLK period are compared against the quantity set by PCM_BSEL (or PCM_MSEL).

$CMON_BSELTOL$ sets the number of consecutive errors before the device is disabled and an interrupt is generated. If $CMON_AUTORESTART_EN = 1$, $CMON_BSELTOL$ also sets the number of consecutive frames with no errors needed for automatic restart to occur.

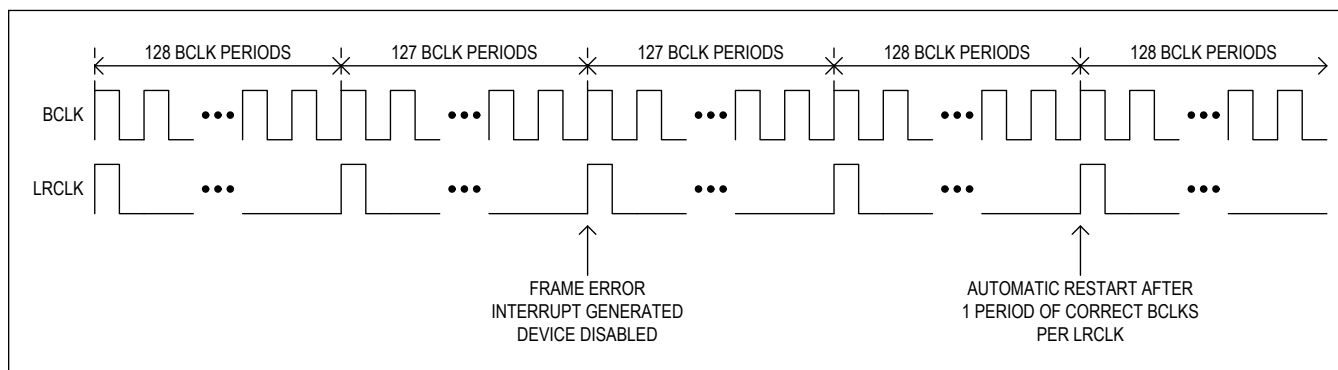


Figure 7. Clock Monitor Framing Error Example in TDM Mode with $PCM_BSEL = 0x6$ (128 BCLKs per LRCLK) and $CMON_BSELTOL = 0x0$

Input Data Monitor

The device provides an optional input data monitor that is enabled by setting $DMON_MAG_EN$ to 1 for the data magnitude monitor or $DMON_STUCK_EN$ to 1 for the data stuck monitor. While enabled, the data monitor is active while EN is 1. The block monitors the audio input and automatically enters software shutdown if a data magnitude or data stuck error is detected. When a data error is detected, a $DMON_ERR_*$ interrupt is generated, the device goes into software shutdown, and EN is cleared to 0.

A data magnitude error is detected if the signal magnitude (positive or negative) is above the threshold set by $DMON_MAG_THRESH$ for longer than the time defined by the $DMON_DURATION$ register.

A data stuck error is detected if the signal repeats a fixed value with a magnitude (positive or negative) that is above the threshold set by $DMON_STUCK_THRESH$ for longer than the time defined by the $DMON_DURATION$ register.

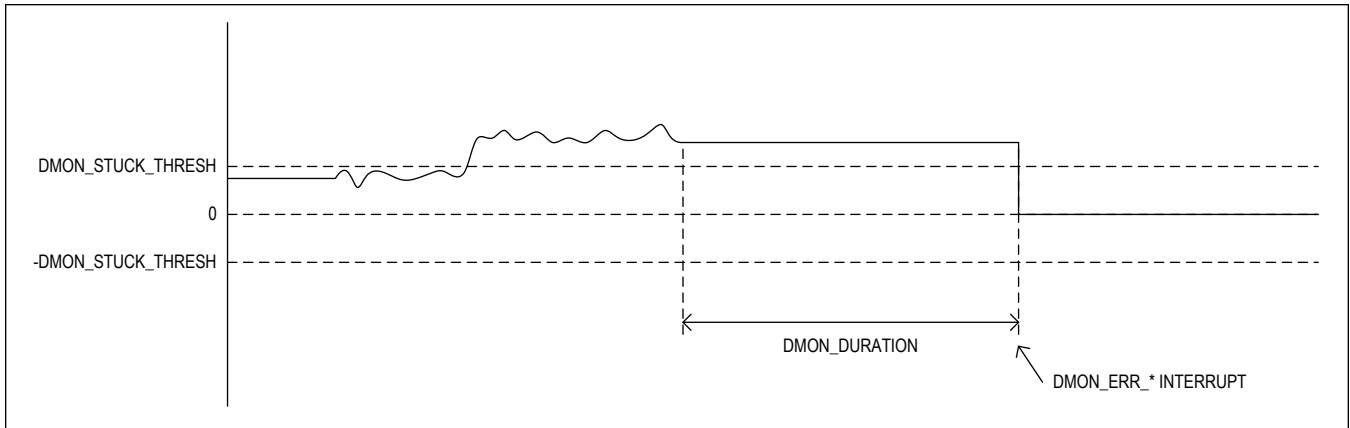


Figure 8. Data Stuck Error Example

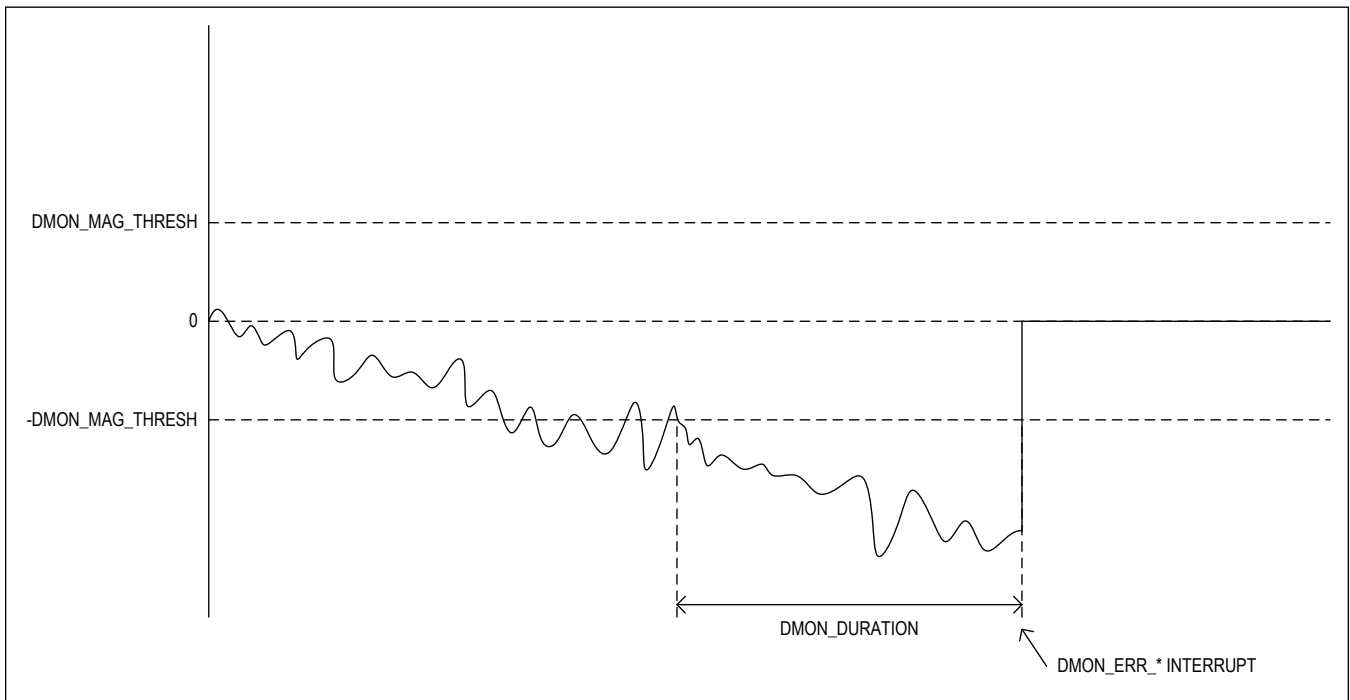


Figure 9. Data Magnitude Error Example

Watchdog Timer

The device features a watchdog timer to protect the speaker in the event the host suffers a critical failure and is unresponsive. The watchdog timer supports two modes, hardware or software, controlled by WDT_MODE.

Software Mode

When WDT_MODE is set to 0, the watchdog timer is in software mode. When enabled, the watchdog timer must be continually reset by the host for the audio path to remain active.

The watchdog-timer-reset event is triggered by writing the value 0xE9 to WDT_SW_RESET. Four timeout periods are available, controlled by WDT_TO_SEL: 100ms, 500ms, 1000ms, and 2000ms. The software watchdog generates a warning interrupt (WATCHDOGWARN_*) when the internal counter is at approximately 75%. This can be used by

software to enable an event-driven reset, rather than having to run an internal counter of its own.

If the host does not reset the watchdog timer before the timeout period expires, the device goes into the software-shutdown state and generates an interrupt (WATCHDOGFAIL_*). In addition, if the host writes any value other than 0xE9 to the WDT_SW_RST register, the device immediately goes into software shutdown and generates a WATCHDOGFAIL_* interrupt.

To reactivate the audio path after a software watchdog-timeout event, reset the watchdog timer and set EN to 1.

The watchdog-timer function is enabled and disabled using WDT_EN.

Hardware Mode

When WDT_MODE is set to 1, the watchdog timer is in hardware mode. When enabled, the watchdog timer monitors the edge-to-edge period of the signal at the WDT pin.

Four timeout periods are available, controlled by WDT_TO_SEL: 5ms, 10ms, 35ms, and 50ms. The hardware watchdog generates a warning interrupt (WATCHDOGWARN_*) when the internal counter is at approximately 75%. If the period of the watchdog-timer signal exceeds the watchdog-timer-period setting, the device goes into the software-shutdown state and generates an interrupt (WATCHDOGFAIL_*).

To reactivate the audio path after a hardware-watchdog-timeout event, the host must provide a valid watchdog-timer signal input OR disable the watchdog circuit AND set EN to 1.

The watchdog timer function is enabled and disabled using WDT_EN.

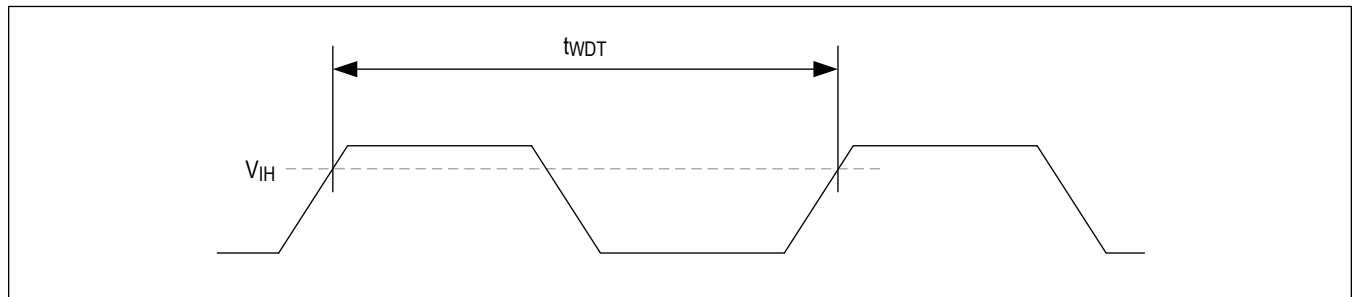


Figure 10. Watchdog Timer Period

PCM Interface

PCM Master/Slave Modes and MCLK

The PCM_MSTR_MODE bitfield configures the PCM interface for slave or master mode.

In slave mode, BCLK and LRCLK are supplied by the host and PCM_CLK_SOURCE determines whether MCLK or BCLK is used to derive internal clocks.

In master mode, the host provides a clock to MCLK. The device uses this to derive BCLK and LRCLK and supplies these to the host. If the PCM interface is configured for master mode, MCLK must be provided and the PCM_MCLK_RATE register configured to match the frequency of MCLK. If the PCM interface is in slave mode and PCM_CLK_SOURCE is set to 0, PCM_MCLK_RATE is ignored. In order to ensure phase alignment, any slave MAX98390 devices connected to the master should be powered up and fully configured along with CMON_AUTORESTART_EN set to 1 before the master is enabled. PCM_CLK_SOURCE must be set to 1 in master mode.

[Table 4](#) shows when the PCM output clocks are enabled.

Table 4. PCM Output Clock Control

| EN | PCM_RX_CHm_EN OR PCM_TX_CHm_EN | PCM_MSTR_MODE[1:0] | BCLK | LRCLK | NOTES |
|----|--------------------------------|--------------------|---------|---------|--------------------|
| 0 | 0 | — | Hi-Z | Hi-Z | Device disabled |
| 1 | 0 | — | Hi-Z | Hi-Z | Interface disabled |
| 1 | 1 | 00 | Hi-Z | Hi-Z | Slave mode |
| 1 | 1 | 11 | Enabled | Enabled | Master mode |

Interface Formats—All Modes

The PCM interface supports slave and master mode I²S, left-justified, and TDM data. The operating mode is selected by the PCM_FORMAT register.

Data is clocked in and out with BCLK. The PCM_BCLKEDGE bit selects either the rising or falling edge of BCLK as active for clocking data in and out on DIN and DOUT respectively.

LRCLK delimits data frames. The PCM_CHANSEL bit selects whether a rising edge on LRCLK or a falling edge on LRCLK is active, indicating the start of a frame. The LRCLK active edge always aligns with a BCLK inactive edge.

The SPK_SR register sets the frequency of LRCLK and the sample rate of the Class-D amplifier path.

PCM Clock Ratio Configuration

The BCLK rate is the PCM interface sample rate (SPK_SR) multiplied by the BCLKs per LRCLK (PCM_BSEL). The BCLK rate must not exceed $1/t_{BCLK}$ (see the [Electrical Characteristics](#) section).

The device supports a range of BCLK to LRCLK clock ratios ranging from 32 to 512. In slave mode with PCM_CLK_SOURCE = 0, PCM_BSEL must be set by the host to match the number of BCLKs per LRCLK being sent. In master mode, or slave mode with PCM_CLK_SOURCE = 1, PCM_MSEL sets the number of BCLKs per LRCLK.

Table 5. PCM_MSTR_MODE and PCM_CLK_SOURCE Configuration

| PCM_MSTR_MODE | PCM_CLK_SOURCE | MASTER OR SLAVE MODE | INTERNAL CLOCKS DERIVED FROM | BCLKs PER LRCLK SET BY |
|---------------|----------------|----------------------|------------------------------|------------------------|
| 00 | 0 | Slave | BCLK | PCM_BSEL |
| 00 | 1 | Slave | MCLK | PCM_MSEL |
| 11 | 1 | Master | MCLK | PCM_MSEL |
| 11 | 1 | Reserved | Reserved | Reserved |
| 01 or 10 | x | Reserved | Reserved | Reserved |

[Table 6](#), [Table 7](#), [Table 8](#), and [Table 9](#) show the supported BCLKs per LRCLK settings for given SPK_SR settings.

Table 6. Supported Clock Settings in Slave Mode with PCM_CLK_SOURCE = 0

| | | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | PCM_BSEL [3:0] (bin) |
|--------------------|---|------|------|------|------|------|------|------|------|------|------|----------------------|
| | | 32 | 48 | 64 | 96 | 128 | 192 | 256 | 320 | 384 | 512 | BCLKs PER LRCLK |
| 0000 | 8 | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | |
| 0001 | 11.025 | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | |
| 0010 | 12 | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | |
| 0011 | 16 | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | |
| 0100 | 22.05 | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | |
| 0101 | 24 | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | |
| 0110 | 32 | Y | Y | Y | Y | Y | Y | Y | Y | Y | N | |
| 0111 | 44.1 | Y | Y | Y | Y | Y | Y | Y | Y | N | N | |
| 1000 | 48 | Y | Y | Y | Y | Y | Y | Y | Y | N | N | |
| SPK_SR [3:0] (bin) | PCM INTERFACE SAMPLE RATE (LRCLK) (kHz) | | | | | | | | | | | |

Table 7. Supported Clock Settings in Master Mode or Slave Mode with PCM_CLK_SOURCE = 1 and MCLK = 12.0000MHz

| MCLK Rate: 12.0000MHz | | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1010 | 1011 | PCM_MSEL [3:0] (bin) |
|-----------------------|---|------|------|------|------|------|------|------|------|------|----------------------|
| | | 32 | 48 | 64 | 96 | 128 | 192 | 256 | 384 | 512 | BCLKs PER LRCLK |
| 0000 | 8 | Y | Y | Y | Y | Y | Y | Y | Y | Y | |
| 0001 | 11.025 | Y | N | Y | N | Y | N | Y | N | Y | |
| 0010 | 12 | Y | N | Y | N | Y | N | Y | N | Y | |
| 0011 | 16 | Y | Y | Y | Y | Y | Y | Y | Y | N | |
| 0100 | 22.05 | Y | N | Y | N | Y | N | Y | N | N | |
| 0101 | 24 | Y | N | Y | N | Y | N | Y | N | N | |
| 0110 | 32 | Y | Y | Y | Y | Y | Y | N | N | N | |
| 0111 | 44.1 | Y | N | Y | N | Y | N | N | N | N | |
| 1000 | 48 | Y | N | Y | N | Y | N | N | N | N | |
| SPK_SR [3:0] (bin) | PCM INTERFACE SAMPLE RATE (LRCLK) (kHz) | | | | | | | | | | |

Table 8. Supported Clock Settings in Master Mode or Slave Mode with PCM_CLK_SOURCE = 1 and MCLK = 11.2896MHz

| MCLK Rate: 11.2896MHz | | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1010 | 1011 | PCM_MSEL [3:0] (bin) |
|-----------------------|---|------|------|------|------|------|------|------|------|------|----------------------|
| | | 32 | 48 | 64 | 96 | 128 | 192 | 256 | 384 | 512 | BCLKs PER LRCLK |
| 0000 | 8 | N | N | N | N | N | N | N | N | N | |
| 0001 | 11.025 | Y | Y | Y | Y | Y | Y | Y | Y | Y | |
| 0010 | 12 | N | N | N | N | N | N | N | N | N | |
| 0011 | 16 | N | N | N | N | N | N | N | N | N | |
| 0100 | 22.05 | Y | Y | Y | Y | Y | Y | Y | N | N | |
| 0101 | 24 | N | N | N | N | N | N | Y | N | N | |
| 0110 | 32 | N | N | N | N | N | N | N | N | N | |
| 0111 | 44.1 | Y | Y | Y | Y | Y | N | N | N | N | |
| 1000 | 48 | N | N | N | N | N | N | N | N | N | |
| SPK_SR [3:0] (bin) | PCM INTERFACE SAMPLE RATE (LRCLK) (kHz) | | | | | | | | | | |

Table 9. Supported Clock Settings in Master Mode or Slave Mode with PCM_CLK_SOURCE = 1 and MCLK = 12.2880MHz

| MCLK Rate: 12.288MHz | | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1010 | 1011 | PCM_MSEL [3:0] (bin) |
|----------------------|---|------|------|------|------|------|------|------|------|------|----------------------|
| | | 32 | 48 | 64 | 96 | 128 | 192 | 256 | 384 | 512 | BCLKs PER LRCLK |
| 0000 | 8 | Y | Y | Y | Y | Y | Y | Y | Y | Y | |
| 0001 | 11.025 | N | N | N | N | N | N | N | N | N | |
| 0010 | 12 | Y | Y | Y | Y | Y | Y | Y | Y | Y | |
| 0011 | 16 | Y | Y | Y | Y | Y | Y | Y | Y | N | |
| 0100 | 22.05 | N | N | N | N | N | N | N | N | N | |
| 0101 | 24 | Y | Y | Y | Y | Y | Y | Y | N | N | |
| 0110 | 32 | Y | Y | Y | Y | Y | Y | N | N | N | |
| 0111 | 44.1 | N | N | N | N | N | N | N | N | N | |
| 1000 | 48 | Y | Y | Y | Y | Y | N | N | N | N | |
| SPK_SR [3:0] (bin) | PCM INTERFACE SAMPLE RATE (LRCLK) (kHz) | | | | | | | | | | |

I²S and Left-Justified Modes

I²S and left-justified formats support two channels. LRCLK duty cycle is 50%. Channel 0 starts after the active LRCLK edge and channel 1 starts after the inactive edge.

The BCLK to LRCLK ratio (PCM_BSEL or PCM_MSEL) must be configured to be twice the desired channel length. The data word size is configurable to 16-, 24-, or 32-bits in length (PCM_CHANSZ), but must be programmed to be less than or equal to the channel length. If the resulting channel length exceeds the configured data word size, then the data input LSBs are truncated and the data output LSBs are padded with either zero or Hi-Z data based on the PCM_TX_CHm_HIZ

setting. The PCM_TX_HIZ bit must be set to 0 in non-TDM modes.

In I²S mode, the MSB of the audio word is latched on the second active BCLK edge after an LRCLK transition. In left-justified mode, the MSB of the audio word is latched on the first active BCLK edge after an LRCLK transition.

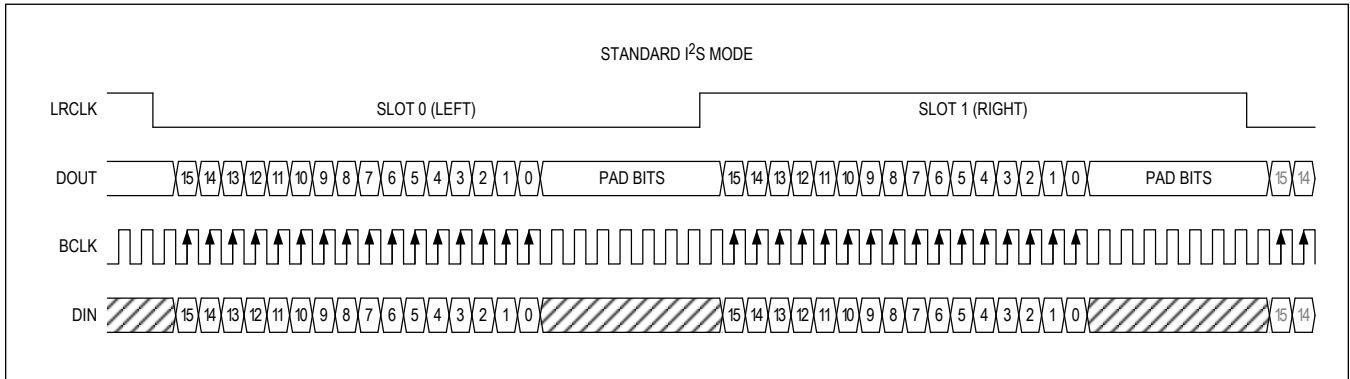


Figure 11. I²S Mode

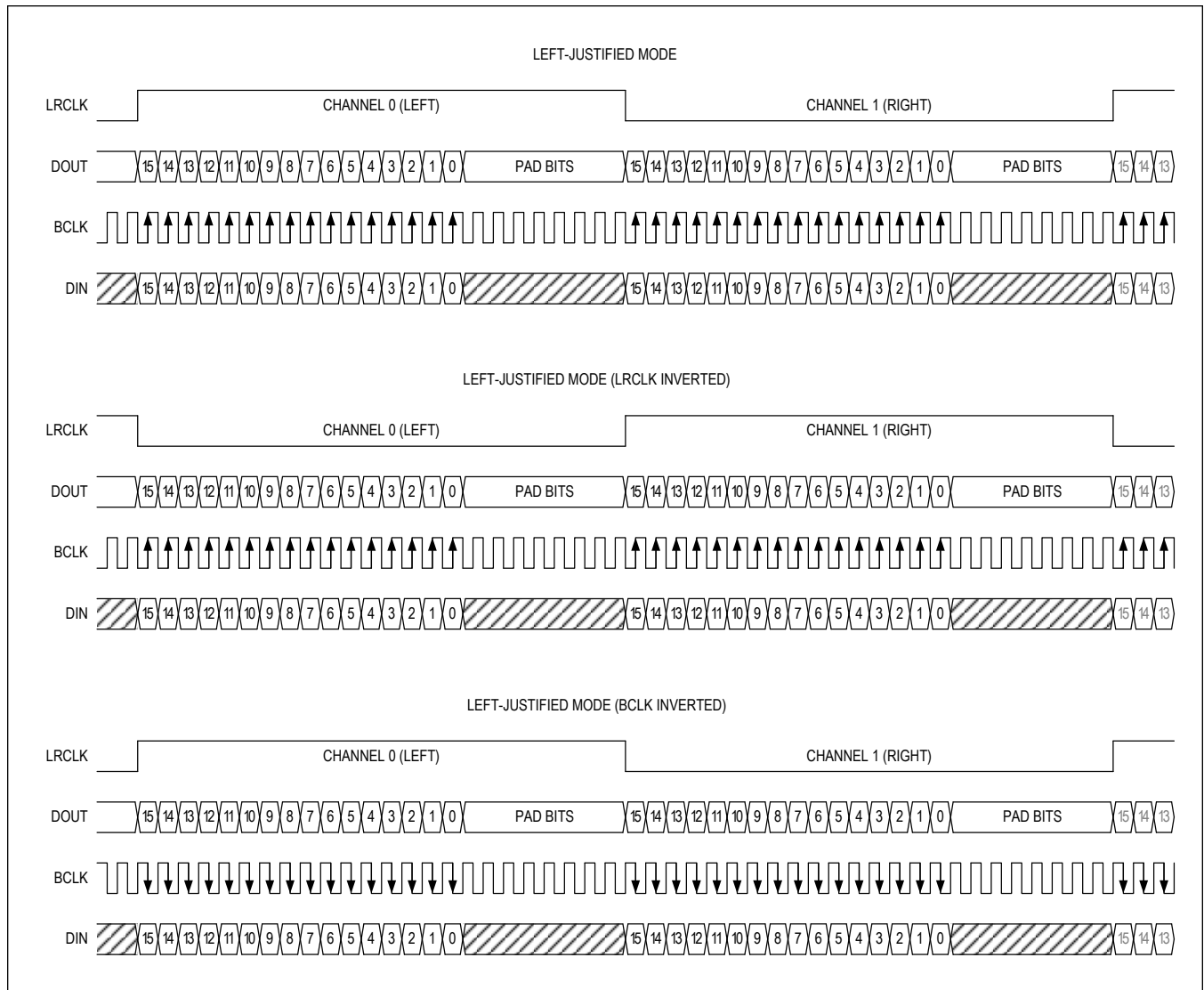


Figure 12. Left-Justified Modes

TDM Modes

TDM mode supports up to 16 audio channels of 16-, 24-, or 32-bits each. The number of TDM channels is determined by the number of BCLKs per LRCLK (set by PCM_BSEL or PCM_MSEL) divided by the channel length (set by PCM_CHANSZ). In TDM mode, the channel length and input data word size are always equal. Words are received contiguously, with no unused bits between words with the exception of the end of a frame where the frame length is not evenly divisible by the word length.

In slave mode, an active edge on LRCLK signifies the start of a frame. An inactive edge can occur at any time after the active edge is latched as long as there is a minimum of 1 BCLK period high and a minimum of 1 BCLK period low.

In master-TDM mode, LRCLK produces a pulse train with a pulse width of 1 BCLK period.

In TDM mode, the MSB of the first audio word can be latched on the first, second, or third active BCLK edge after the sync pulse and is programmed by the PCM_FORMAT bits (TDM mode 0, 1, and 2).

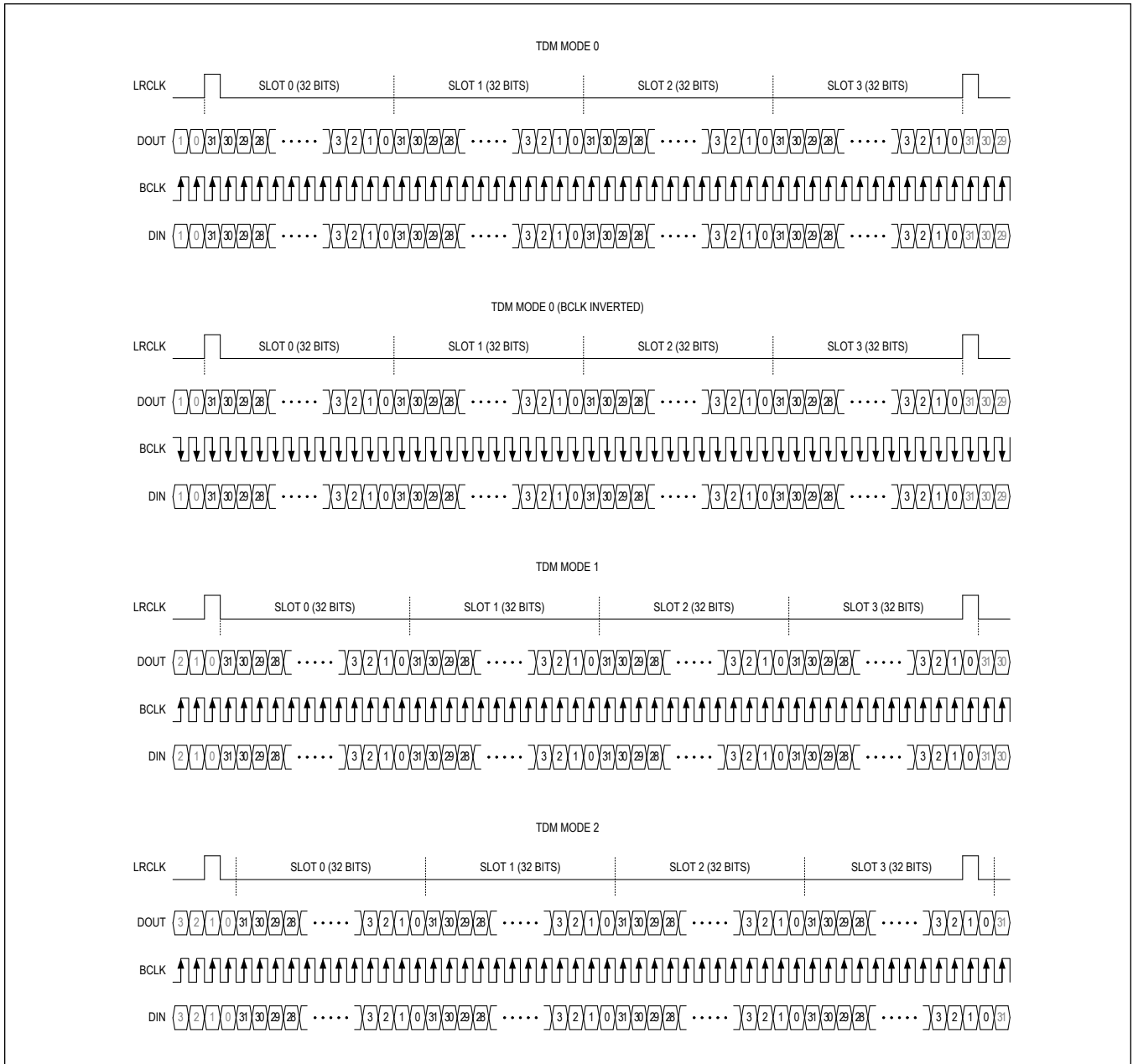


Figure 13. TDM Modes

Invalid TDM Configurations

Note that while in TDM mode with PCM_TX_EXTRA_HIZ set to 1, it is not valid to set the number of BCLKs per LRCLK (PCM_BSEL or PCM_MSEL) to be less than two times the audio data word size (PCM_CHANSZ). See [Table 10](#).

Table 10. Invalid TDM Configurations

| PCM_TX_EXTRA_HIZ | PCM_BSEL OR PCM_MSEL | PCM_CHANSZ |
|------------------|----------------------|--------------|
| 1 | 0010 (32 bits) | 10 (24 bits) |
| 1 | 0010 (32 bits) | 11 (32 bits) |
| 1 | 0011 (48 bits) | 11 (32 bits) |

PCM Data Path Configuration

The PCM interface data input accepts audio for the speaker path, while the data output accepts data from the speaker DSP monitor path.

PCM Data Input

The PCM interface data input (DIN) is enabled with the PCM_RX_CHm_EN bits. In I²S and left-justified modes, only channels 0 and 1 are available, while in TDM mode, up to 16 channels of data can be available.

The PCM_DAC_MAIN_SOURCE register is used to select the main audio source from the PCM_RX channels to be sent to the DSM path.

If stereo bass management is enabled (STEREO_BASS_EN = 1), then bass from the PCM_RX channel pointed to by PCM_DAC_BASS_SOURCE is added to the DSM path.

PCM Data Output

The PCM interface data output (DOUT) can drive output data onto any valid enabled output channel. In I²S and left-justified modes, only two output channels are available. In TDM mode, up to 16 output channels can be available.

Current and voltage sense data, as well as the output of the baseband processor, can be enabled as outputs with the IVADC_I_EN, IVADC_V_EN, and AMP_DSP_EN bits. The PCM_IVADC_I_DEST, PCM_IVADC_V_DEST, and PCM_AMP_DSP_DEST registers select the output channels. The PCM_TX_CHn_EN bits are the enable controls for the individual data output channels. If the I/V sense ADC path or DSP path is disabled and it is assigned to an active output channel, then the output data is a zero-code value.

If an output channel is enabled and no data source is assigned to it, then the output data is all zeros. The PCM data output is Hi-Z if the device is disabled (EN = 0), the PCM data output is disabled (PCM_TX_EN = 0), or all output channels are set to a Hi-Z output (all PCM_TX_CHn_HIZ = 1). A summary of the controls for the PCM data output (DOUT) is shown in [Table 11](#).

Table 11. Control Registers and the DOUT Pin

| EN | PCM_TX_CHm_EN | PCM_TX_CHm_HIZ | CHANNEL m CONTAINS DATA (*) | DOUT FOR CHANNEL m |
|----|---------------|----------------|-----------------------------|---------------------|
| 0 | — | — | — | Hi-Z (all channels) |
| 1 | 0 | 0 | — | 0 |
| 1 | 1 | 0 | No | 0 |
| 1 | 1 | 0 | Yes | Data |
| 1 | — | 1 | — | Hi-Z |

* A channel contains data if a path (I/V sense or amplifier DSP) is enabled and its DEST register points to the channel.

PCM Interface Timing

Figure 14, Figure 15, and Figure 16 show timing for BCLK, LRCLK, DIN, and DOUT. See the Electrical Characteristics table for more details.

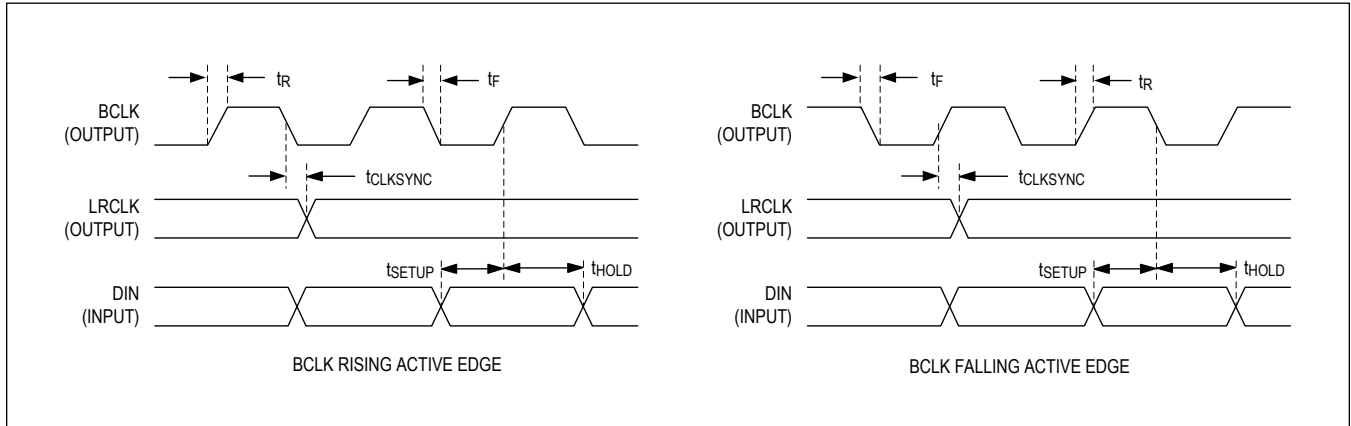


Figure 14. PCM Interface Timing/Master Mode—LRCLK, BCLK, DIN Timing Diagram

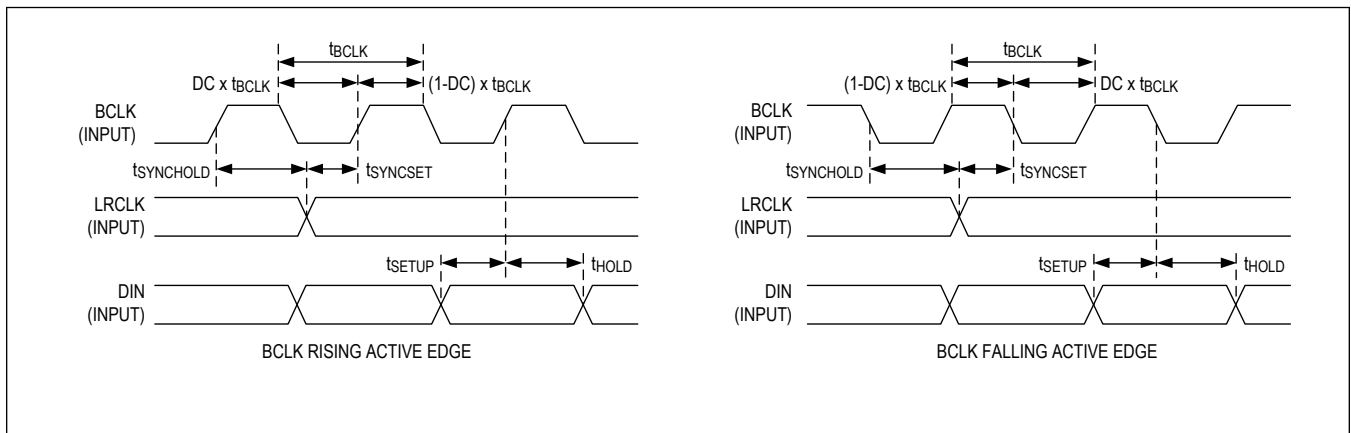


Figure 15. PCM Interface Timing/Slave Mode—LRCLK, BCLK, DIN Timing Diagram

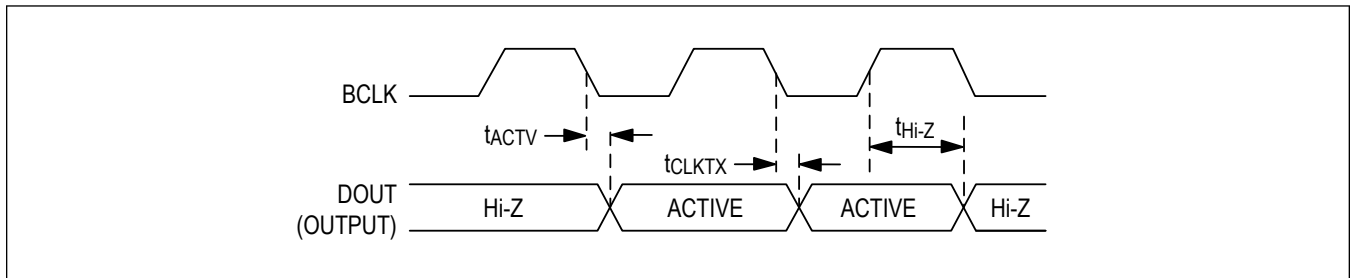


Figure 16. PCM Interface Timing/DOUT Timing Diagram

Logic Output Pin Drive Strength Control

The *_DRV bits set the drive strengths of the logic output pins. Different CMOS drive strengths can be selected (see the [Electrical Characteristics](#) tables). [Table 12](#) shows which pin is controlled by which register.

Table 12. Logic Output Pin Drive Strength Control

| REGISTER | EXTERNAL PIN CONTROLLED |
|-----------|-------------------------|
| DOUT_DRV | DOUT |
| BCLK_DRV | BCLK |
| LRCLK_DRV | LRCLK |
| ICC_DRV | ICC |

Tone Generator

The device includes a tone generator which can be used to generate sine wave tones or DC levels.

To enable the tone generator, select an output waveform with the TONE_CONFIG register and set SPK_SOURCE to 10b. A valid master or slave PCM clocking configuration (see the [PCM Clock Ratio Configuration](#) section for details) must be configured.

The frequency of the sine wave output is a division of the audio sample rate set by SPK_SR. The DC output does not vary with audio sample rate.

Note that when the tone generator is enabled (SPK_SOURCE = 10b), the input data monitor must be disabled (DMON_MAG_EN = 0 and DMON_STUCK_EN = 0).

Thermal Warning and Shutdown

The device features a thermal-protection circuit which can ensure that the die temperature does not exceed programmed limits. The device can warn the host if die temperature has reached a warning limit and shuts down the device if the die temperature has reached the shutdown limit. The circuit uses the measurement ADC temperature reading as an input.

Minimum Valid Setup

The temperature measurement rate is controlled as described in the [Measurement ADC](#) section. The minimum requirement for setup of the temperature input to the thermal-protection circuit is:

- MEAS_ADC_CH2_EN = 1
- MEAS_ADC_BASE_DIV ≤ 0x0100

If the conditions above are not satisfied when setting EN to 1, the device does not enable successfully. Instead, an interrupt is generated (PWRUP_FAIL_*). This check ensures that the device cannot be started without the ability to monitor and react to high die temperatures.

Note that when BST_BYP_MODE is set to 00b or 11b, the MEAS_ADC_BASE_DIV register setting is ignored and the measurement ADC base sample rate divider is internally forced to 0x0023.

Thermal Thresholds

The thermal-warning threshold is set using MEAS_ADC_WARN_THRESH. The thermal-shutdown threshold is set using MEAS_ADC_SHDN_THRESH. Measurement hysteresis for both thresholds is set using MEAS_ADC_HYST.

When the die temperature rises above the thermal-warning threshold, the device generates a THERMWARN_START_* interrupt. At this threshold, there is no further action taken by the device to reduce the temperature. When the die temperature falls below the thermal-warning threshold minus the hysteresis setting, the device generates another interrupt (THERMWARN_END_*).

When the die temperature rises above the thermal-shutdown threshold, the device generates a THERMSHDN_START_*

interrupt and the device disables the Class-D amplifier (SPK_EN is unchanged). When the die temperature falls below the thermal-shutdown threshold minus the hysteresis setting, the device generates a THERMSHND_END_* interrupt but the Class-D amplifier remains off. When the die temperature falls below the thermal-warning threshold minus the hysteresis setting, the device generates a THERMWARN_END_* interrupt, the Class-D amplifier remains off, and the device clears EN to 0.

Amplifier Path Controls

Figure 17 shows the audio signal path from the PCM Interface to the Class-D amplifier.

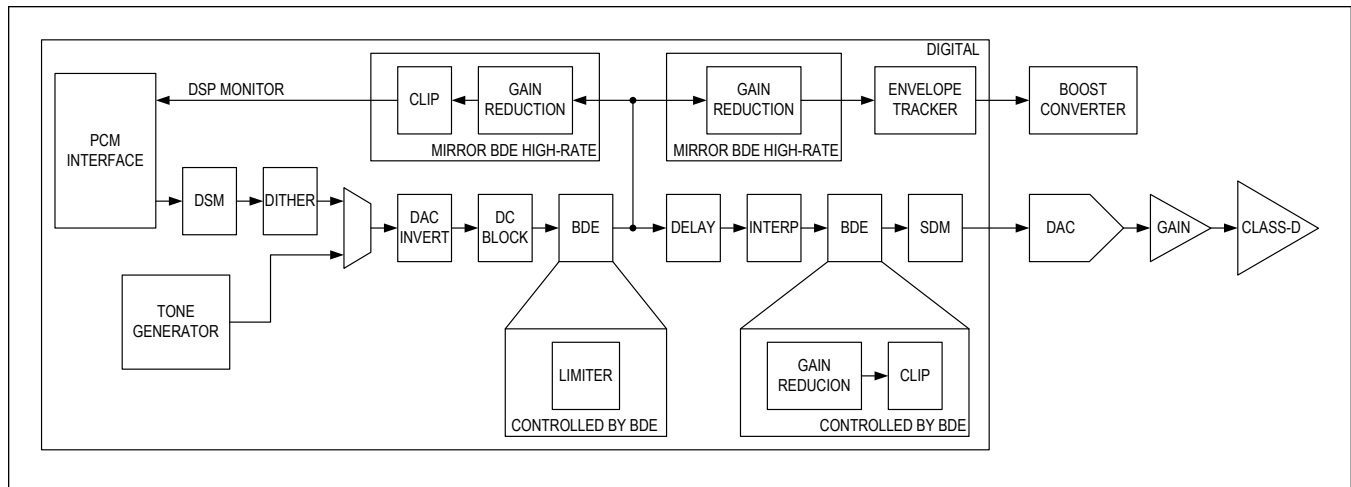


Figure 17. Amplifier Path

Path Routing Control

The data input source for the Class-D amplifier is controlled by the SPK_SOURCE register. This allows selection between the PCM interface (for I²S, left-justified, or TDM inputs), or the tone generator.

Note: Channel enables for all paths that are not used must be set to zero. For example:

- When SPK_SOURCE = 00 (PCM), ensure that TONE_CONFIG = 0000.
- When SPK_SOURCE = 10 (Tone), ensure that all PCM_RX_CHx_EN bits = 0.

Power Gating and Auto Muting

Power gating can be used to dynamically reduce power consumption when the input signal amplitude is below a threshold. Power reduction is achieved by disabling some signal processing. Power gating is enabled by setting POWER_GATING_EN to 1.

When the input-signal amplitude is lower than the level selected by the POWER_GATE_ENTRY_THRESH register for more than 1024 samples, audio amplitude is ramped down to zero over 5ms.

When the input-signal amplitude exceeds the level selected by the POWER_GATE_EXIT_THRESH register, audio amplitude is ramped back up over 100μs and signal processing is resumed.

Power gating cannot be entered if excursion protection is reducing peak-output amplitude or if the speaker temperature is above the threshold set in DSM_TPROT_PG_TEMP.

Auto muting behaves the same as power gating except that signal processing is not disabled and power consumption is not reduced.

Table 13. Power Gating and Auto Muting Enable Bits

| POWER_GATING_EN | AUTO_MUTING_EN | POWER GATING ENABLED | AUTO MUTING ENABLED |
|-----------------|----------------|----------------------|---------------------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 |

Note that if DSP_GLOBAL_EN is set to 0, THERMAL_PROT_EN must also be set to 0 for power gating to function.

When THERMAL_PROT_EN = 1, power gating and auto muting can produce a small pop or click noise when signal processing is resumed. For best pop-and-click performance, disable power gating when thermal protection is enabled.

PCM Dither

Dither (± 1 LSB peak-to-peak TPDF) is applied to the incoming PCM data when AMP_DITH_EN is set to 1.

DAC Inversion

The DAC output is inverted by setting DAC_INVERT to 1.

DC Blocking Filter

Setting AMP_DCBLK_EN to 1 enables the DC blocking filter in the amplifier path.

Digital Volume Control

The DSM_VOL_CTRL register sets the digital volume control. The range is -80dB to +12dB in 0.5dB steps.

To ensure pop-free transitions between steps, volume changes are ramped internally. This occurs during volume changes in normal operation and also as part of the internal start-up or shutdown procedures. The time for the ramp is controlled by the DSM_VOL_RAMP_TIME register. The ramp slope varies depending on the size of the volume change so that if DSM_VOL_RAMP_TIME is set to (for example) 4ms, the time needed for the ramp is 4ms whether DSM_VOL_CTRL is changed from -80dB to -79.5dB or changed from -80dB to +12dB.

To minimize pops after writing to DSM_VOL_CTRL, the host should wait enough time for the ramp to complete before writing a new volume setting to DSM_VOL_CTRL.

Internal volume ramping can be disabled by setting DSM_VOL_RAMP_UP_BYP and DSM_VOL_RAMP_DN_BYP to 1. This also reduces start-up and shutdown times.

If DSM is applying no filtering or compression and the BDE is not clipping, limiting, or changing the gain, the amplifier path gain can be calculated using the DAC output voltage of $2.16V_{PK}$ (3.68dBV) at full-scale, DSM_VOL_CTRL, and the fixed 15dB analog gain of the amplifier with the following equation:

$$\text{Output signal level (dBV)} = \text{input signal level (dBFS)} + 3.68\text{dB} + \text{DSM volume} + 15\text{dB}$$

where 0dBFS is referenced to 0dBV.

For example, if digital-input amplitude happens to be half of full-scale and DSM_VOL_CTRL is at -3dB, then output amplitude is:

$$-6\text{dBFS} + 3.68\text{dB} - 3\text{dB} + 15\text{dB} = 9.68\text{dBV}$$

Dynamic Range Extension (DRE)

The DRE block minimizes the output noise depending on the signal level. The internal analog volume automatically drops to a minimum if the signal level is low enough for greater than one second.

DSP Monitor

The output of the baseband processor (DSP Monitor) can be sent to the PCM interface by setting AMP_DSP_EN to 1. The gain of this path (with default configuration) is 0dB and the rate is the same as the base rate of the amplifier path.

The host can use this to monitor what data is being driven into the DAC after baseband processing (volume, BDE, etc.). It is invalid for AMP_DSP_EN to be 1 while SPK_EN is 0.

Class-D Amplifier

The Class-D amplifier is enabled or disabled by setting EN to 1 while SPK_EN = 1. Note that SPK_EN is a static bit and should only be changed while EN = 0.

Output Short-Circuit Detection

When a Class-D output short circuit occurs, the amplifier immediately shuts off. An interrupt is generated, the device waits for 110 μ s (50 μ s if SPK_SPEEDUP = 1), and then the amplifier automatically attempts to restart. Upon restart, if the short circuit is still present, the process repeats. This cycle continues as long as EN and SPK_EN are 1.

Spread-Spectrum Modulation

Spread-spectrum modulation is enabled or disabled using SSM_EN. The modulation index of the spread-spectrum modulation is controlled by SSM_MOD_INDEX. Higher percentage settings of modulation index results in the switching frequency of the amplifier being modulated by a wider range, spreading out-of-band energy across a wider bandwidth.

Output Sensing When Using Ferrite Beads

The device features two remote sensing pins, VSNSP and VSNSN. These are used as inputs to the speaker voltage measurement ADC, but they are also used as part of the feedback loop for the Class-D amplifier.

Remotely sensing the voltage at the load provides a THD+N advantage over sensing at the DUT output when ferrite beads are used. The remote sense lines connect the output signal at the load to the inverting terminal of the internal error amplifier of the Class-D. Ferrites are highly nonlinear, so sensing at the load versus at the output pins ensures that any signal degradation caused by the filtering components is appropriately compensated.

However, in many applications, there may not be a need to filter the output with a ferrite bead.

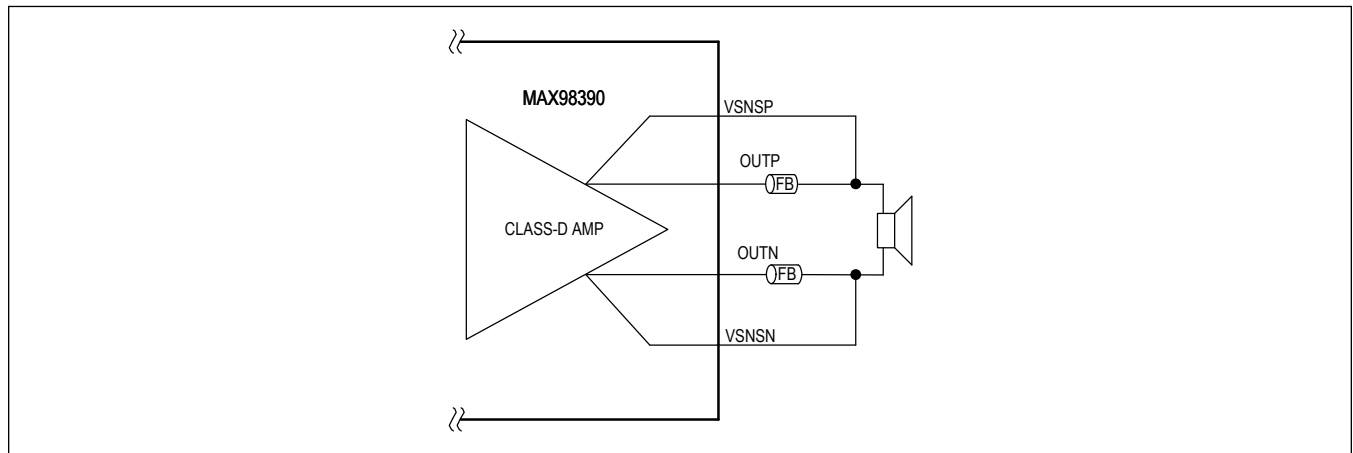


Figure 18. Output Sensing When Using Ferrite Beads

Ultra-Low EMI Filterless Output Stage

Traditional Class-D amplifiers require the use of external LC filters, or shielding, to meet electromagnetic-interference (EMI) regulation standards. The active emissions limiting edge-rate control circuitry reduces EMI emissions so that with 3 inches of speaker cable the device passes the EN55022B standard without the need for external filtering components. The SPK_EDGE_CTRL register further allows the device to reduce EMI by changing speaker edge rate.

Maxim's spread-spectrum modulation mode, enabled by setting SSM_EN to 1, flattens wideband spectral components while proprietary techniques ensure that the cycle-to-cycle variation of the switching period does not degrade efficiency.

The Class-D amplifier's spread-spectrum modulator randomly varies the switching frequency by as much as $\pm 71.28\text{kHz}$ around the center frequency according to the setting of `SSM_MOD_INDEX`. Above 10MHz, the wideband spectrum looks like noise for EMI purposes.

FET Scaling

The Class-D amplifier's output FETs are segmented so that they can be automatically scaled down to 1/4 size to save power.

To enable automatic Class-D FET scaling, set the `AMP_FET_SCALE_MODE` register to 00b. To force the Class-D FETs to their maximum size, set `AMP_FET_SCALE_MODE` to 01b. To force the Class-D FETs to 1/4 size, set `AMP_FET_SCALE_MODE` to 10b.

The input data to the DSP signal path is monitored by a peak-detect circuit. The threshold is controlled by the `AMP_FET_SCALE_THRESHOLD` register. The recommended maximum threshold setting varies depending on the minimum impedance of the amplifier load as shown in [Table 14](#).

Table 14. Maximum FET Scaling Threshold

| MINIMUM AMPLIFIER LOAD IMPEDANCE (Ω) | AMP_FET_SCALE_THRESHOLD (bin) | THRESHOLD (V_{PK}) |
|---|-------------------------------|------------------------|
| 4 | 00010 | 0.213 |
| 8 | 00110 | 0.327 |
| 16 | 01101 | 0.697 |

Once the threshold has been exceeded and the output FETs have scaled to their maximum size, they remain at their maximum size until the signal has dropped below the threshold minus the hysteresis (set by `AMP_FET_SCALE_HYST`) for at least the amount of time set by `AMP_FET_SCALE_HOLD_TIME`.

When `AMP_FET_SCALE_THRESHOLD` is set to 11111b (and automatic FET scaling is enabled by setting `AMP_FET_SCALE_MODE` = 00b), 1/4 size FETs are used when the boost is in bypass mode and full size FETs are used when the boost is on. `AMP_FET_SCALE_HYST` is ignored.

Current and Voltage Sense

Separate 16-bit ADCs are used to monitor amplifier voltage and current (IV sense).

For accurate voltage measurements, the `VSNSP` and `VSNSN` pins should be Kelvin connected to the load connected to `OUTP` and `OUTN`. If a filter exists between the amplifier output pins and the load, the sense lines should be connected after the filter. Current is measured internally and requires no external connections.

Voltage and current data can be sent to the host through the PCM interface. When using the PCM interface, ± 1 LSB peak-to-peak TPDF dither is applied to the output data.

First order highpass filtering for DC blocking in the current and voltage sense paths can be enabled by setting the `MEAS_I_DCBLK_EN` and `MEAS_V_DCBLK_EN` bits to 1. The [Electrical Characteristics](#) table lists cutoff frequencies for different settings of the `MEAS_I_DCBLK[1:0]` and `MEAS_V_DCBLK[1:0]` registers when the sample rate is 48kHz. If the sample rate is not 48kHz, the corner frequency scales down linearly. For example, when `MEAS_V_DCBLK` = 01 and the sample rate is 48kHz, the corner frequency is 0.118Hz. However, if the sample rate is 22.05kHz, the corner frequency is reduced to 0.054Hz (a factor of 22.05/48).

To ensure phase alignment, current and voltage sensing should be enabled by setting `IVADC_V_EN` and `IVADC_I_EN` to 1 while `EN` = 0.

I/V Sense Channel Sharing

Current and voltage measurement data can share a PCM interface channel. This is done by setting PCM_IVADC_I_DEST and PCM_IVADC_V_DEST to the same value (while PCM_TX_INTERLEAVE = 0). This is only supported for 32-bit channel widths (as set by PCM_CHANSZ). Each measurement consumes 16 of the 32 available bits, with the current using the least significant bits and the voltage using the most significant bits.

Measurement ADC

The measurement ADC measures V_{VBAT} , V_{PVDD} (boost converter output), and die temperature. Enabled channels are measured sequentially and continuously with a maximum sample rate of 1.024MHz. Each channel can run at an independent sub-multiple of this rate.

The measurement ADC's sample rate (f_S) is set by the following equations:

$$\text{Battery voltage } f_S = \text{MEAS_ADC_CLK} / [(\text{MEAS_ADC_CH0_DIV} + 1) \times (\text{MEAS_ADC_BASE_DIV} + 1)]$$

$$\text{Boost voltage } f_S = \text{MEAS_ADC_CLK} / [(\text{MEAS_ADC_CH1_DIV} + 1) \times (\text{MEAS_ADC_BASE_DIV} + 1)]$$

$$\text{Temperature } f_S = \text{MEAS_ADC_CLK} / [(\text{MEAS_ADC_CH2_DIV} + 1) \times (\text{MEAS_ADC_BASE_DIV} + 1)]$$

MEAS_ADC_CLK is derived from the MDLL output clock and can be one of three typical frequencies:

- 12.288MHz (48kHz-based sample rates)
- 11.2896MHz (44.1kHz-based sample rates)
- 12.000MHz (for master mode when MCLK = 12.0MHz or 6.0MHz)

The valid settings available for MEAS_ADC_BASE_DIV[15:0] varies according to the number of channels simultaneously enabled in the measurement ADC, according to [Table 15](#).

Table 15. Restriction on Base Division Setting with Channel Enables

| MEAS_ADC_CHn_EN SETTING | | | MINIMUM VALUE OF MEAS_ADC_BASE_DIV[15:0] | INVALID RANGE OF MEAS_ADC_BASE_DIV[15:0] |
|-------------------------|-----|-----|---|---|
| CH0 | CH1 | CH2 | | |
| 0 | 0 | 0 | N/A | N/A |
| 0 | 0 | 1 | 0x000B | 0x0000 to 0x000A |
| 0 | 1 | 0 | 0x000B | 0x0000 to 0x000A |
| 0 | 1 | 1 | 0x0017 | 0x0000 to 0x0016 |
| 1 | 0 | 0 | 0x000B | 0x0000 to 0x000A |
| 1 | 0 | 1 | 0x0017 | 0x0000 to 0x0016 |
| 1 | 1 | 0 | 0x0017 | 0x0000 to 0x0016 |
| 1 | 1 | 1 | 0x0023 | 0x0000 to 0x0022 |

For example, if MEAS_ADC_CH0_EN = 1, MEAS_ADC_CH1_EN = 0, MEAS_ADC_CH2_EN = 1, MEAS_ADC_CLK is set to 12.288MHz, MEAS_ADC_CH0_DIV = 0, MEAS_ADC_CH2_DIV = 1, and MEAS_ADC_BASE_DIV = 0x002F, then sample rate is 256kHz for the battery and 128kHz for the temperature and the boost is not sampled.

For example, if MEAS_ADC_CH0_EN = 0, MEAS_ADC_CH1_EN = 0, MEAS_ADC_CH2_EN = 1, MEAS_ADC_CLK is set to 12.288MHz, MEAS_ADC_CH2_DIV = 0, and MEAS_ADC_BASE_DIV = 0x000B, then sample rate is 1024kHz for the temperature and the battery and the boost is not sampled.

Each channel can independently (and optionally) have a simple moving-average filter applied to the result of the continuous conversion measurement, controlled by the relevant MEAS_ADC_CHn_FILT_EN bits. Each channel can be configured with a 2, 4, 8, or 16-point moving-average, controlled by the relevant MEAS_ADC_CHn_FILT_AVG bits. If filtering is selected, the result register won't be updated until a full set of averages is complete. After this initial delay, which may be up to 16 samples, the value in the register is updated at each sample.

The measurement ADC is enabled automatically when any one or more of the MEAS_ADC_CHn_EN bits is set to 1. The latest measured value of V_{VBAT} , V_{PVDD} , and die temperature can be read-back using the MEAS_ADC_CH0_DATA, MEAS_ADC_CH1_DATA, and MEAS_ADC_CH2_DATA registers respectively.

Brownout-Detection Engine (BDE)

The BDE allows the device to reduce its contribution to the overall system power consumption by enabling various power reduction methods when V_{VBAT} drops below a set of programmable thresholds. There are a total of four V_{VBAT} thresholds, individually configured using the relevant BDE_L1_VTHRESH to BDE_L4_VTHRESH bits.

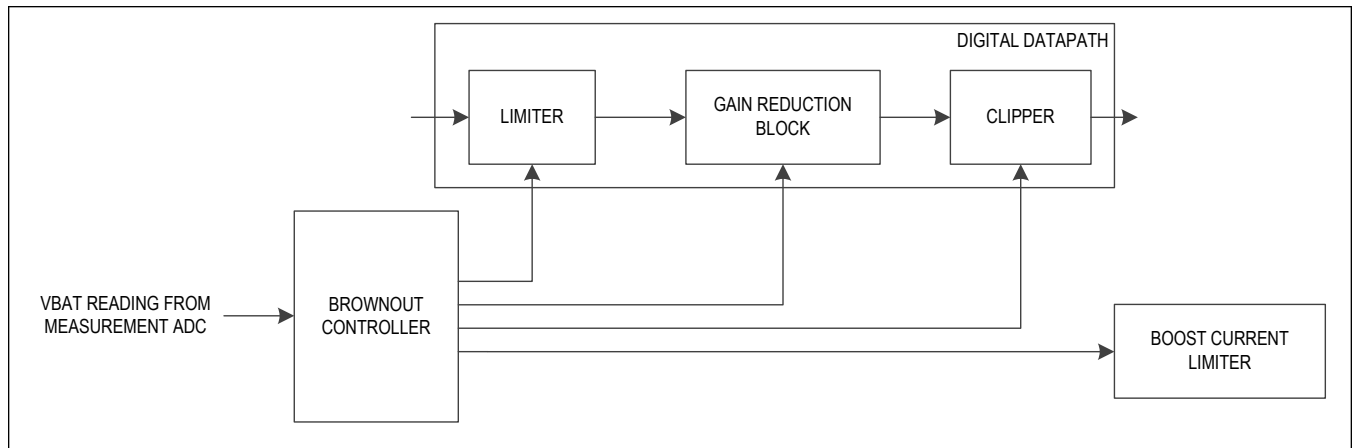


Figure 19. BDE Block Diagram

Table 16. Brownout-Detection Engine Levels

| THRESHOLD NAME | CONDITION |
|--------------------------|---|
| Normal operation | $V_{VBAT} > \text{Critical Battery Level 1} + \text{Hysteresis}$ |
| Critical Battery Level 1 | $\text{Critical Battery Level 1} \geq V_{VBAT} > \text{Critical Battery Level 2} + \text{Hysteresis}$ |
| Critical Battery Level 2 | $\text{Critical Battery Level 2} \geq V_{VBAT} > \text{Critical Battery Level 3} + \text{Hysteresis}$ |
| Critical Battery Level 3 | $\text{Critical Battery Level 3} \geq V_{VBAT} > \text{Critical Battery Level 4} + \text{Hysteresis}$ |
| Critical Battery Level 4 | $V_{VBAT} \leq \text{Critical Battery Level 4}$ |

The brownout engine supports hysteresis on the levels. This behaves as follows:

- When in level N, transition to level N + 1 when V_{VBAT} falls below level N threshold.
- When in level N, transition to level N - 1 when V_{VBAT} stays above (level N - 1 threshold) + (hysteresis) for the specified hold time.

The amount of hysteresis is defined by the BDE_VTHRESH_HYST register. The amount of hysteresis can be defined as larger than the distance between two levels. Regardless, movement is only one enabled level at a time.

Thresholds must be configured so that the level N threshold is greater than the sum of the level N + 1 threshold and the hysteresis. For example, if the level 3 threshold is set to 3.15V (BDE_L3_VTHRESH = 0x3C) and hysteresis is set to 25mV (BDE_VTHRESH_HYST = 0x02), then the level 2 threshold must be set to 3.1875V or higher (BDE_L2_VTHRESH \geq 0x3F).

For each threshold, the following settings can be adjusted by the brownout controller to reduce the overall current drawn by the device from the battery:

- Clipping level
- Gain reduction

- Limiter knee
- Boost converter input current limit

Each of these settings are independent from one another and are individually configurable for each threshold.

For each enabled BDE level, settings for level N must be equal or less than settings for level N - 1. For example, if the gain reduction at BDE level 2 is set to -6dB, the gain reduction at level 3 must be -6dB or more.

[Table 17](#) is provided as an illustrative example as opposed to a definitive use case.

Table 17. Example of BDE Settings

| THRESHOLD NAME | V _{BAT} THRESHOLD SETTING (V) | CLIPPING LEVEL (dBFS) | GAIN REDUCTION (dB) | LIMITER KNEE (dBFS) | BOOST INPUT CURRENT LIMIT (A) |
|--------------------------|--|-----------------------|---------------------|---------------------|--------------------------------|
| Normal Operation | N/A | 0 | 0 | 0 | As per Global Register Setting |
| Critical Battery Level 1 | 3.35 | -3 | 0 | 0 | 2.0 |
| Critical Battery Level 2 | 3.35 | -3 | 0 | 0 | 1.8 |
| Critical Battery Level 3 | 3.15 | -6 | -3 | -6 | 1.6 |
| Critical Battery Level 4 | 3.00 | N/A | Mute | N/A | 1.4 |

BDE Gain, Limit, and Clip Mirroring

Envelope tracking, boost bypass, and FET scaling thresholds can include gain adjustments and clipping that are applied by the BDE by setting BDE_MIRROR to 1. When this is enabled, threshold calculations include any gain adjustments and clipping from the BDE in their decisions to change the boost voltage, bypass the boost, and change the FET scaling. Note that BDE limiting is always included in threshold calculations.

BDE Enable Control

The master control for the BDE is BDE_EN. The BDE_AMP_EN setting controls whether the BDE acts on the boost only or on both the boost and amplifier signal path. [Table 18](#) shows the effect of these two bitfields on the device operations.

Table 18. BDE Enable Control

| BDE_EN | BDE_AMP_EN | FUNCTION |
|--------|------------|--|
| 0 | 0 | BDE disabled |
| 0 | 1 | Reserved |
| 1 | 0 | BDE enabled, boost input current-limit control only |
| 1 | 1 | BDE enabled, boost input current-limit control, audio path limiter, gain reduction, and clip control all available |

V_{BAT} Measurement

The input to the BDE comes from the V_{BAT} input (CH0) to the measurement ADC. See the [Measurement ADC](#) section for details on how to configure V_{BAT} measurement. The sample rate of the V_{BAT} measurement defines the speed at which the BDE updates.

Brownout Controller

The brownout controller monitors the measurement ADC VBAT output and makes state changes as shown in [Figure 20](#).

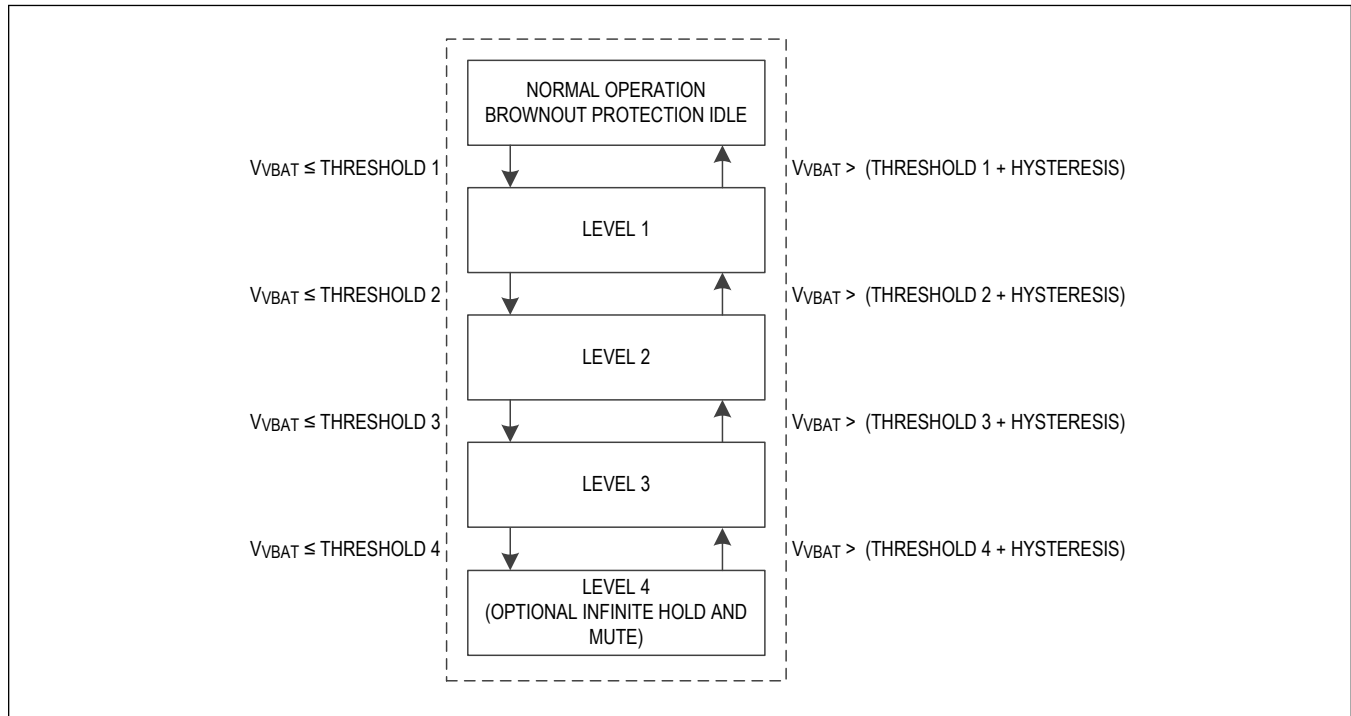


Figure 20. BDE Levels

Each level has a set of discrete registers that configure the attached blocks into various current-saving configurations. As the brownout controller progresses down the levels (from Level 2 to Level 3, Level 3 to Level 4 etc), transitions between states happen instantly. As the brownout controller progresses up the levels (from Level 4 to Level 3, Level 2 to Level 1 etc) transitions are subject to the hold time set by the BDE_HLD register.

Level 4 infinite hold can be enabled with the BDE_L4_INF_HLD bit. If infinite hold is enabled, once the level is entered, it is not be exited until a 1 is written to the BDE_L4_HLD_RLS bit or if I²C registers are reset.

The current level that the BDE is in can be read-back using the BDE_STATE register.

The BDE_LOWEST register contains the lowest BDE level that the controller has visited since the last time the BDE_LOWEST register was read.

Brownout Interrupts

The BDE can generate interrupts triggered by the following conditions:

- BDE controller enters level 4
- BDE controller changes from one level to another
- BDE controller leaves level 0
- BDE controller enters level 0

See the [Interrupts](#) section for more information.

Limiter

The limiter applies smooth digital gain changes to the signal path with programmable attack-and-release times. Input signals above the knee point are attenuated, while input signals below the knee point are not. The knee point is programmable between 0dB and -15dBFS in 1dB steps using the relevant BDE_Ln_AMP1_LIM bits. Attack-and-release times are programmable using AMP_LIM_ATK and AMP_LIM_RLS respectively. Attack-and-release times are common for all thresholds.

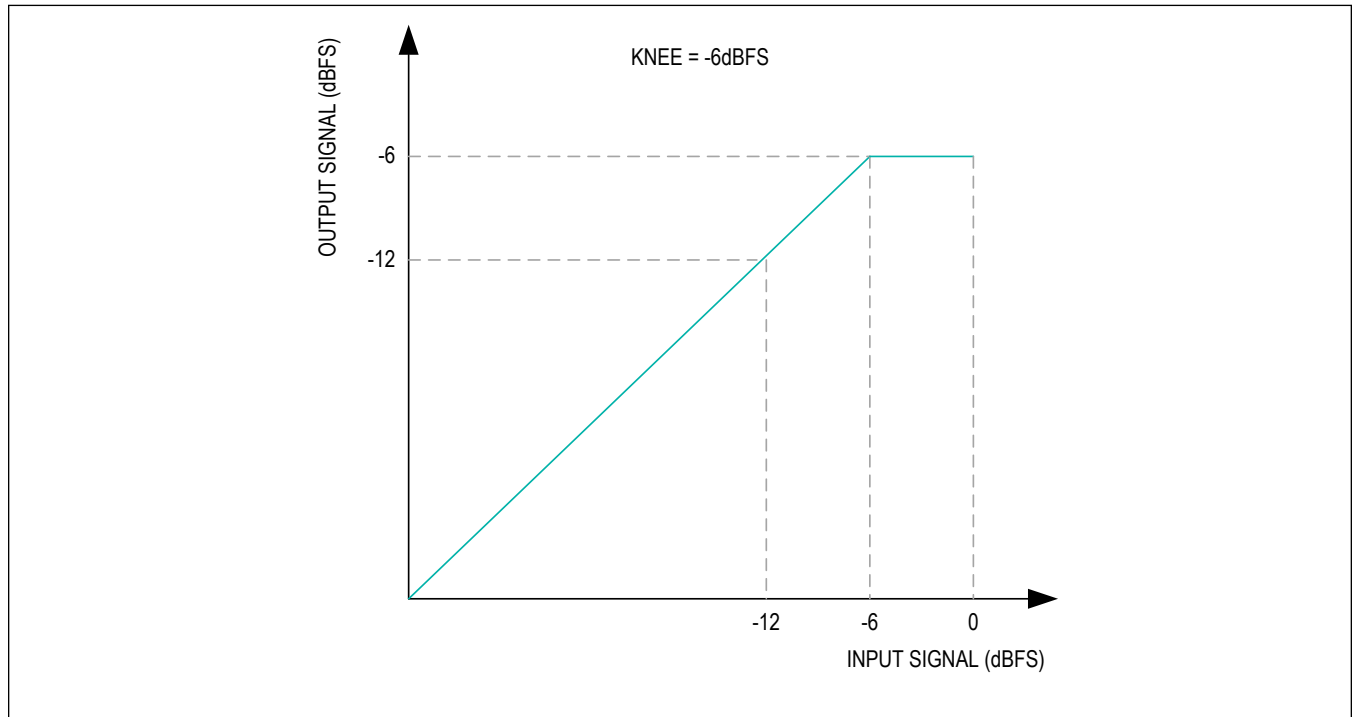


Figure 21. Limiter Profile Example with -6dBFS Knee Point

Gain Reduction

The gain-reduction block applies smooth digital gain changes to the signal path. Attenuation of 0 to 15dB is available in 0.25dB steps using the relevant BDE_Ln_AMP1_GAIN bits. Attack-and-release times are programmable using AMP_GAIN_ATK and AMP_GAIN_RLS respectively. Attack-and-release times are common for all thresholds.

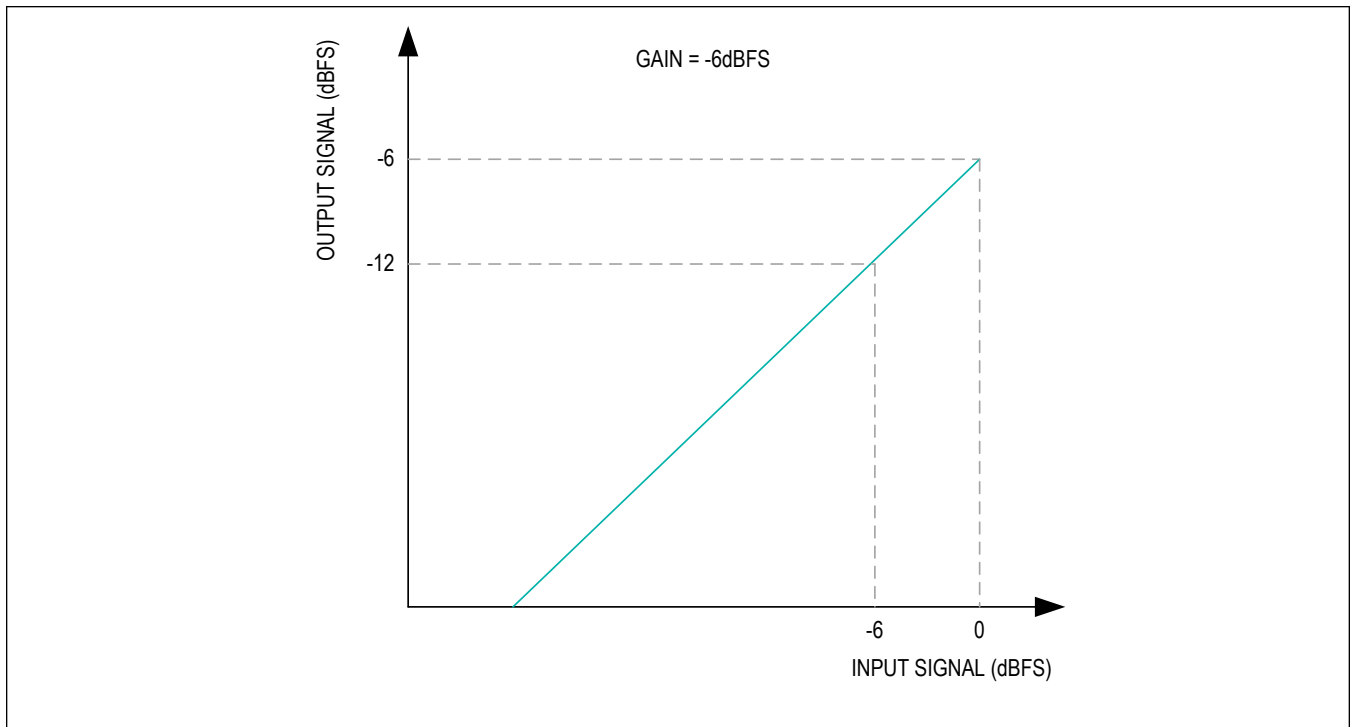


Figure 22. Gain Reduction Profile Example with -6dB Setting

Level 4 Mute

When the BDE is in level 4 and BDE_L4_AMP1_MUTE is set to 1, the BDE_L4_AMP1_GAIN setting is overridden and the signal path is muted.

Clipper

The digital-clipper block limits the maximum digital output codes to a programmable value. The clip level is programmable from 0dBFS to -15dBFS in 0.25dB steps using the relevant BDE_Ln_AMP1_CLIP bits.

Clip-attack (clip level is reduced) level changes are applied immediately. Clip-release (clip level is increased) level changes can be programmed to occur after a zero cross event or immediately with the AMP_CLIP_MODE bit.

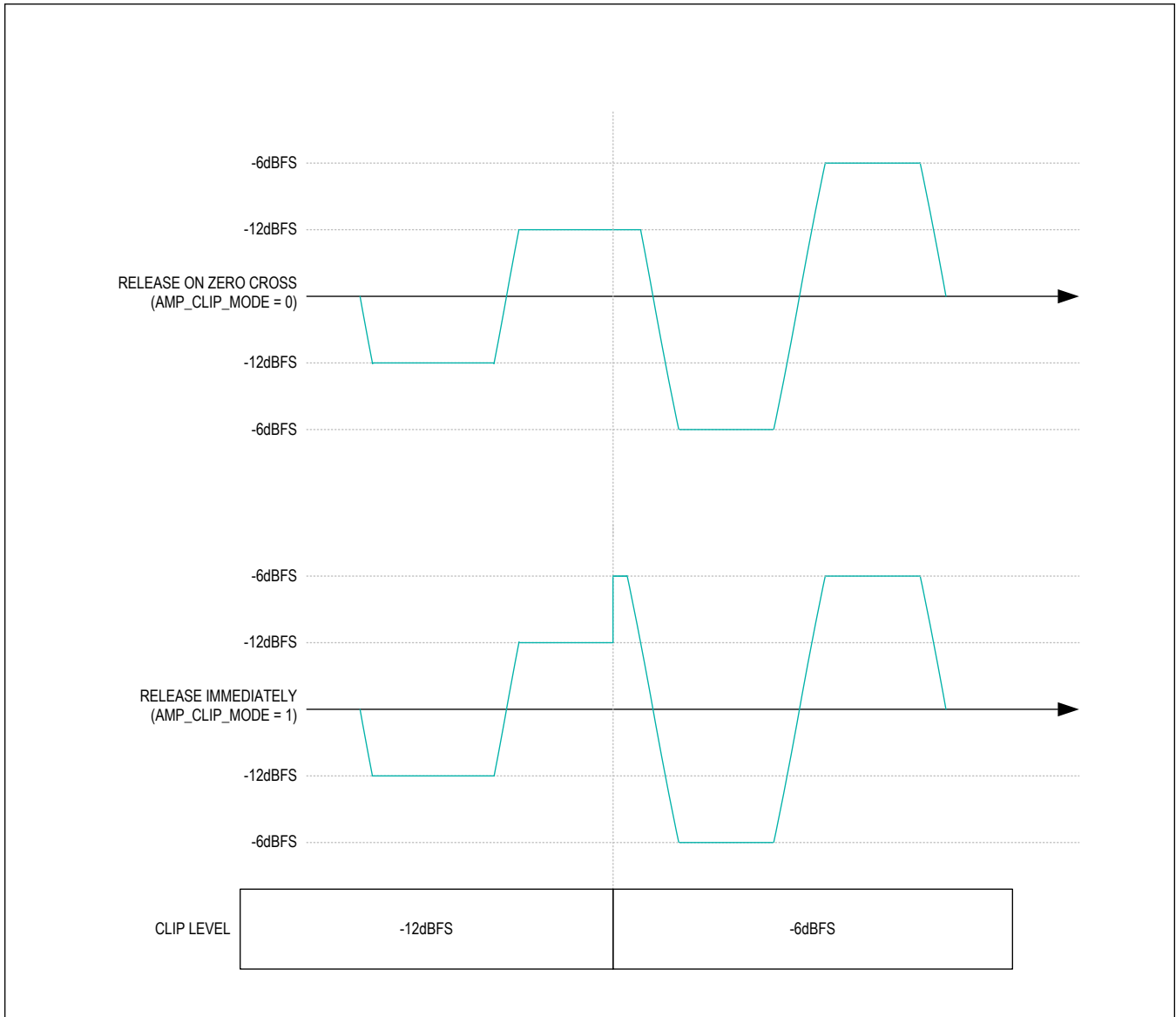


Figure 23. Clipper Examples with Level Change from -12dBFS to -6dBFS

Boost Input Current Limit

The boost regulator limits the input current limit. The limit is initially set by the BST_ILIM register but can be overridden by the brownout-detection engine using the BDE_Ln_ILIM bits. As output current increases, input current increases. If the input current limit is reached, V_{PVD} is reduced so that input current does not exceed the limit.

Using Brownout Boost Input Current Limit to Avoid System Brownouts

Note that whenever the boost turns on, it charges C_{PVDD} as fast as is allowed by the boost input current limit so that V_{PVDD} rises as quickly as possible to avoid clipping the output signal. This includes when the boost turns on after being turned off by automatic boost bypass.

This sudden large current demand may cause the battery voltage (V_{VBAT}) to sag until C_{PVDD} is charged and V_{PVDD} rises to its target output voltage. If the battery's voltage is well above the system brownout voltage and the battery's internal resistance is low, this does not present a problem as shown in [Figure 24](#).

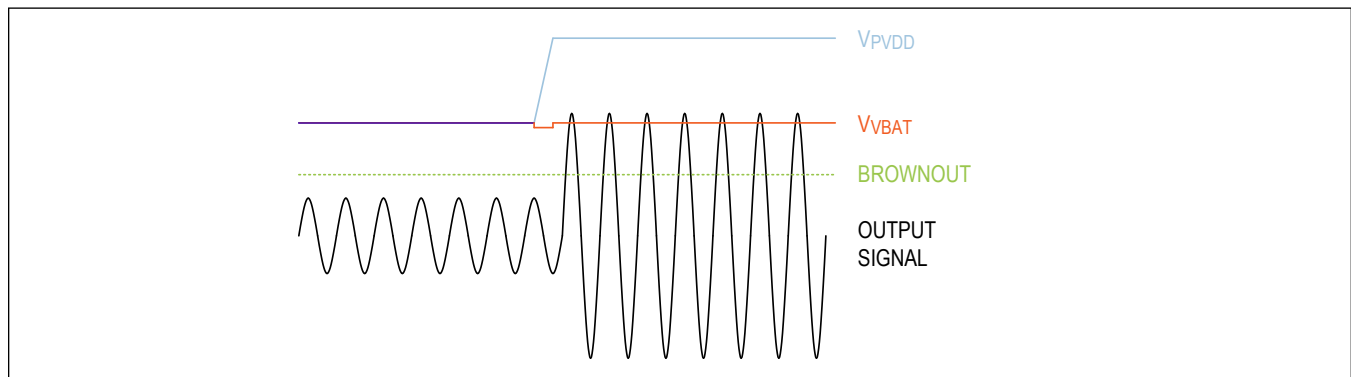


Figure 24. Acceptable V_{VBAT} Sag

However, if the battery's voltage is close to the system brownout voltage and/or the battery's internal resistance is high, V_{VBAT} may sag low enough to cause the system to shut down as shown in [Figure 25](#).

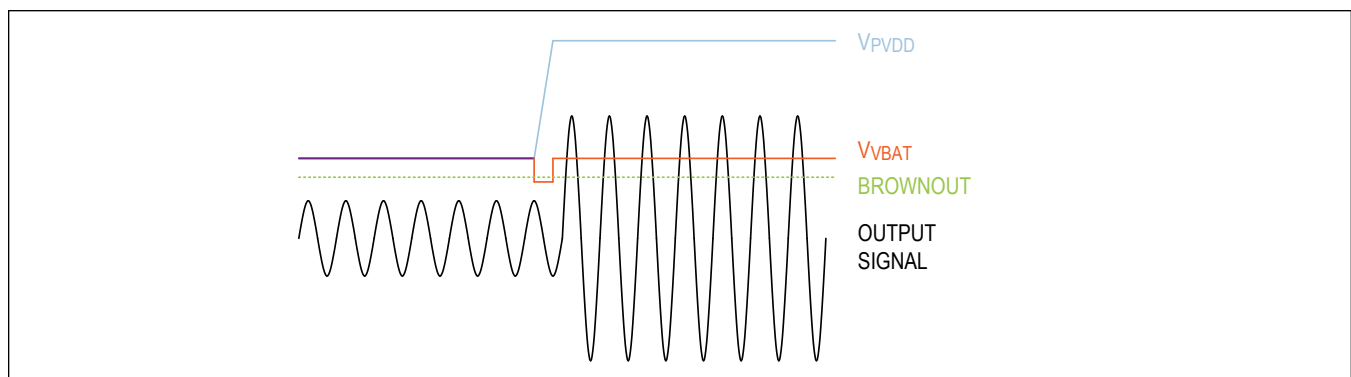


Figure 25. Unacceptable V_{VBAT} Sag

The BDE can be configured to automatically reduce the boost input current limit when V_{VBAT} is low as shown in [Figure 26](#). This decreases maximum output power and increases the amount of time needed for V_{PVDD} to reach its target voltage but V_{VBAT} sag is reduced. The BDE can be configured to automatically return the boost input current limit to its BST_ILIM programmed value after the battery is charged and V_{VBAT} rises.

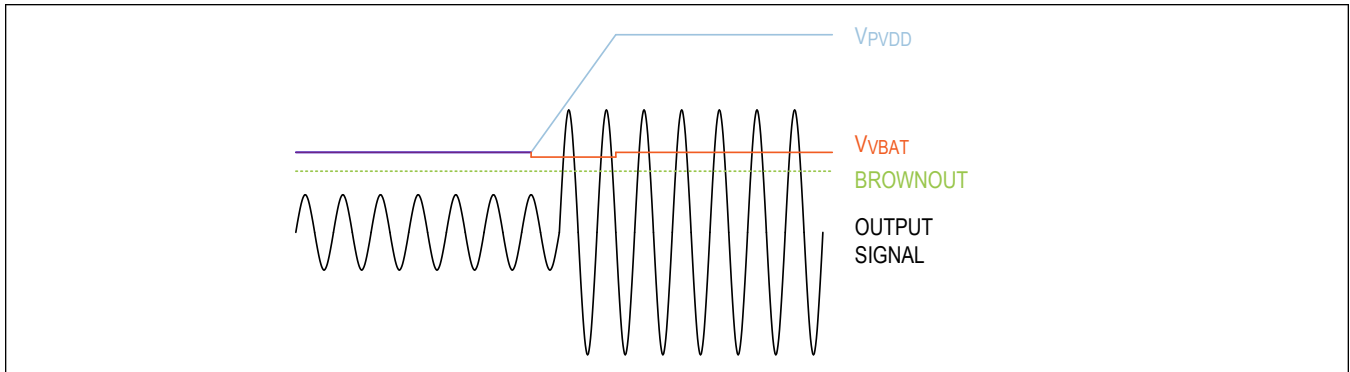


Figure 26. Reduced Boost ILIM for Reduced V_{VBAT} Sag

To reduce the chance of clipping while the input current limit is reduced, the BDEs gain reduction or limiter can also be configured to reduce the maximum output signal.

Interchip Communication

The device features an interchip communication (ICC) bus that facilitates synchronized gain adjustments between groups of amplifiers when using the BDE. ICC is supported when using the PCM interface only.

ICC Operation and Data Format

A bidirectional ICC pin is used to provide data to the applications processor and other similar devices. The data output from ICC shares the current BDE level. The data format used to frame the data carried on the ICC pin is the same as the data format of the input data on the DIN pin. The ICC pin only drives out during the channel assigned to the amplifier by ICC_TX_CHm_EN bit. At all other times, the ICC pin is an input (to allow other devices to drive the ICC signal).

The ICC pin can be configured to drive data, zeroes, or Hi-Z according to [Table 19](#).

Table 19. ICC Output Configuration

| ICC_TX_CHmEN | ICC_TX_HIZ_MANUAL | ICC_TX_CHm_HIZ | CHANNEL m RESULT |
|--------------|-------------------|----------------|------------------|
| 0 | 0 | X | Hi-Z |
| 1 | 0 | X | Drive Data |
| 0 | 1 | 0 | Drive 0 |
| 1 | 1 | 0 | Drive Data |
| X | 1 | 1 | Hi-Z |

Note that when ICC_LINK_EN = 1, the device's BDE limiter is disabled.

Note that when ICC_TX_HIZ_MANUAL is set to 1, any ICC receive channel enabled by the relevant ICC_RX_CHm_EN bit must also be manually set to Hi-Z by setting the relevant ICC_TX_CHm_HIZ to 1.

If the channel size is larger than 16-bits, the extra bits can be configured as zeros or Hi-Z with ICC_TX_EXTRA_HIZ.

BDE_INFO[3:0] contains the transmitter device's BDE level status.

[Figure 27](#) and [Figure 28](#) show examples of the ICC transmit protocol for 16-bit and 24-bit/32-bit operation. These figures show left-justified format for clarity, but the data structure is similar for I²S and TDM modes.

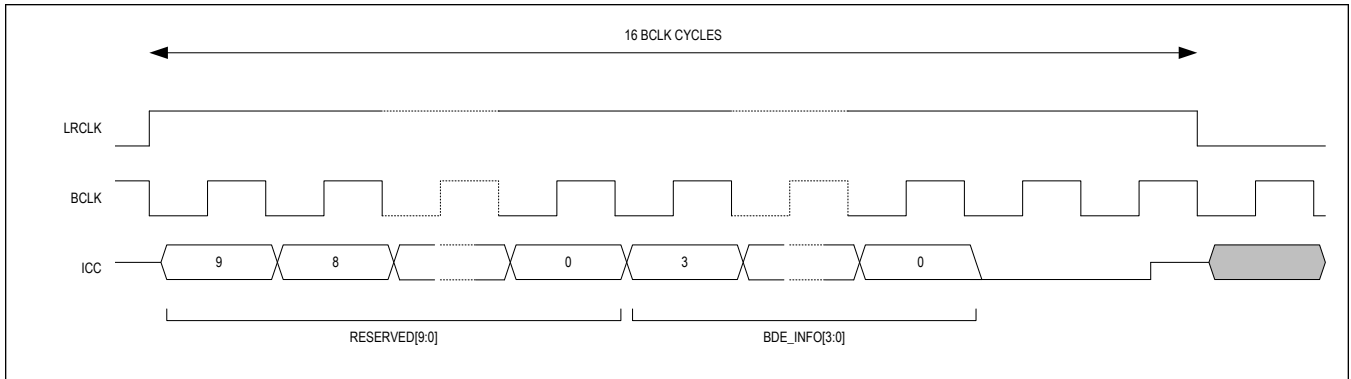


Figure 27. ICC Transmit Frame Structure (16-bit Left-Justified)

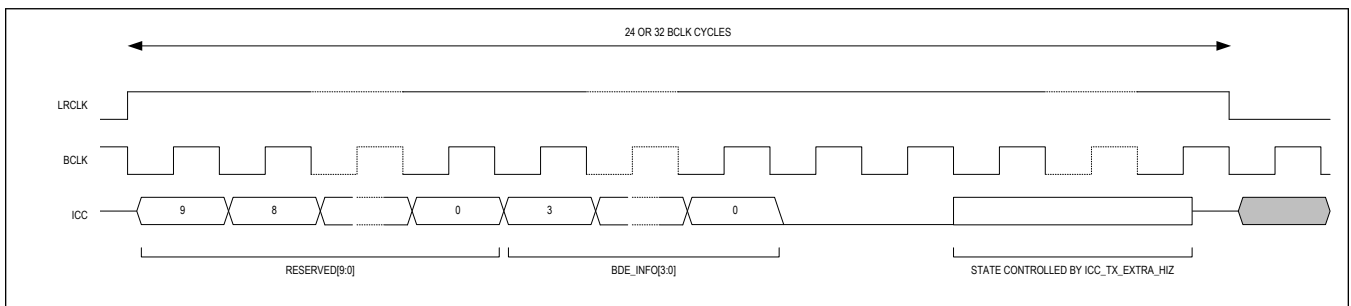


Figure 28. ICC Transmit Frame Structure (24-bit or 32-bit Left-Justified)

Figure 29 shows timing for BCLK and ICC. See the [Electrical Characteristics](#) table for more details.

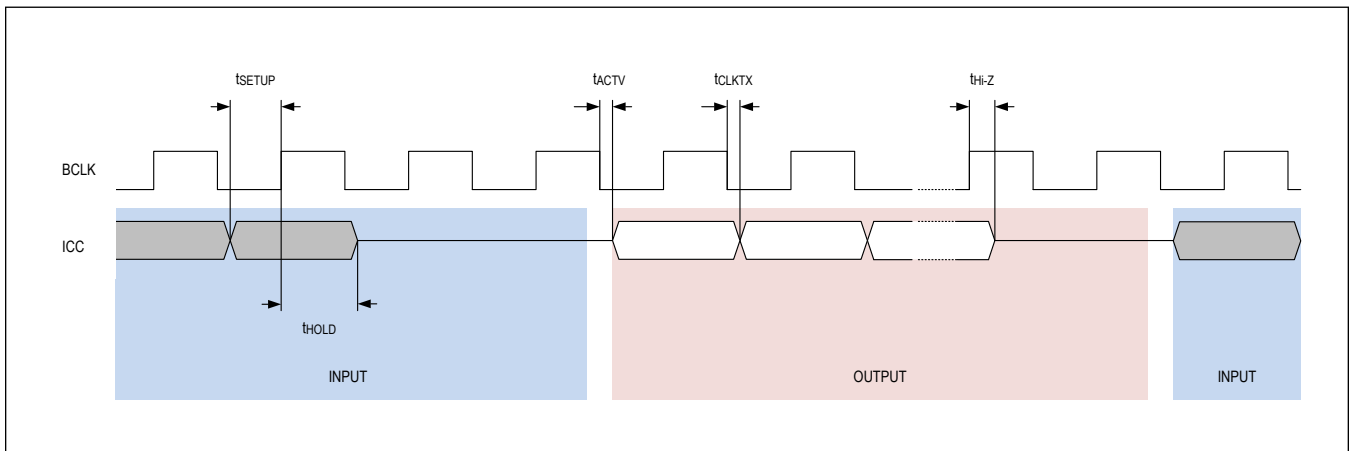


Figure 29. PCM Interface Timing/Interchip Communication—ICC Timing Diagram

Table 20. BDE_INFO

| VALUE | DECODE |
|-------|----------------|
| 0x0 | BDE not active |
| 0x2 | BDE Level 1 |

Table 20. BDE_INFO (continued)

| VALUE | DECODE |
|------------------------------------|-------------|
| 0x4 | BDE Level 2 |
| 0x6 | BDE Level 3 |
| 0x8 | BDE Level 4 |
| 0x1, 0x3, 0x5, 0x7, and 0x9 to 0xF | Reserved |

At the end of each LRCLK frame, the device adjusts its BDE level to the highest BDE level reported by all devices within the assigned group.

If ICC_LINK_EN = 0, the device ignores data presented on the ICC pin.

Multiamplifier Grouping

Multiple devices can be grouped so that any gain adjustments due to the BDE are synchronized.

To create a group, configure each amplifier to monitor the ICC pin during certain channels. The selected channels define the group to which each amplifier belongs. Each amplifier in a group must have the same settings for R_X enables. Each individual amplifier must also have only one ICC_TX_CH# enable set as well as the corresponding ICC_RX_CH# enable.

For example, if there are four amplifiers and two groups are needed, then one configuration can be that amplifiers 1 and 3 belong to one group and amplifiers 2 and 4 belong to another group. To configure the first group, assign amplifier 1 to broadcast on channel 0 with the ICC_TX_CH0_EN bit and assign amplifier 3 to broadcast on channel 2 with the ICC_TX_CH2_EN bit. Then configure both amplifiers to listen to both channels 0 and 2 by setting ICC_RX_CH0_EN and ICC_RX_CH2_EN to 1 on both amplifiers. To configure the second group, assign amplifier 2 to broadcast on channel 1 with the ICC_TX_CH1_EN bit and assign amplifier 4 to broadcast on channel 3 with the ICC_TX_CH3_EN bit. Then configure both amplifiers to listen to both channel 1 and 3 by setting ICC_RX_CH1_EN and ICC_RX_CH3_EN to 1 on both amplifiers.

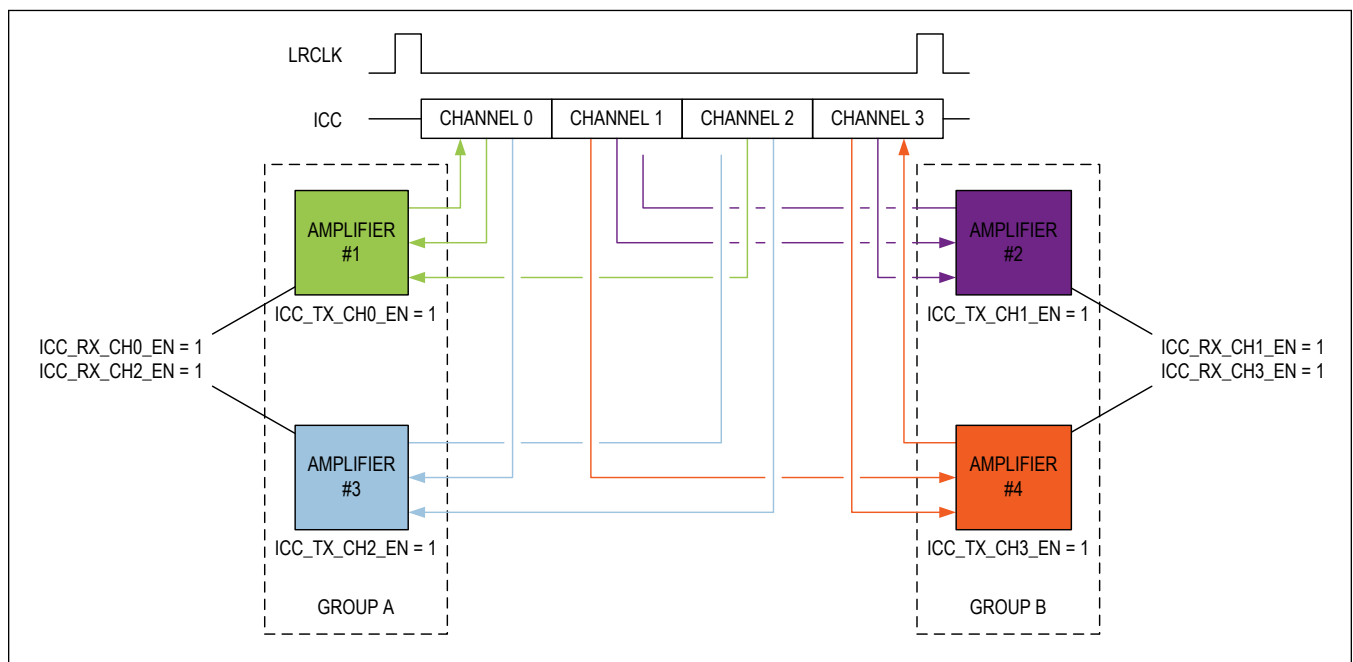


Figure 30. ICC Grouping Example

The minimum size of a group is two amplifiers, so the maximum number of groups that is supported is eight. A group can contain as many as 16 amplifiers, but then only one group is supported.

The host processor must ensure that the RX register bits are set to the same values across all amplifiers intended to be used in a group. Devices in the same group must also be configured with the same BDE gain reduction ballistics (AMP_GAIN_ATK and AMP_GAIN_RLS) to achieve a synchronized response across the group.

Shutdown Modes

Software Shutdown

When the EN bit is cleared to 0, the device is shut down.

When the $\overline{\text{RESET}}$ pin is high and EN = 0:

- All I²C register values are retained except for ENV_TRACKER_BST_VOUT_RD and BDE_STATE. Both of these registers are reset when EN = 0.
- PCM interface pins are Hi-Z.
- Internal LDO for digital circuitry remains enabled.
- I²C port remains available.

Note: If DSM_VOL_RMP_DN_BYP = 1 (ramp down disabled), after clearing EN to 0, the host must wait at least 400 μ s before resetting it to 1. If DSM_VOL_RMP_DN_BYP = 0 (ramp down enabled), after clearing EN to 0, the host must wait at least 6ms before resetting it to 1.

Software Reset

Writing a 1 to RST resets all I²C registers to their default values. Writing a 0 to RST has no effect. RST always reads back as 0.

Hardware Shutdown

When the $\overline{\text{RESET}}$ pin is low, the device is shut down and placed into a low-power state.

When $\overline{\text{RESET}}$ is low:

- Logic pins are Hi-Z.
- Internal LDOs for digital and analog circuitry are disabled.
- Current draw on DVDD is minimized.

When $\overline{\text{RESET}}$ goes high, the host must wait for at least $t_{\text{I}^2\text{C_READY}}$ before writing to the I²C port as shown in [Figure 31](#). See the [Electrical Characteristics](#) table for more details.

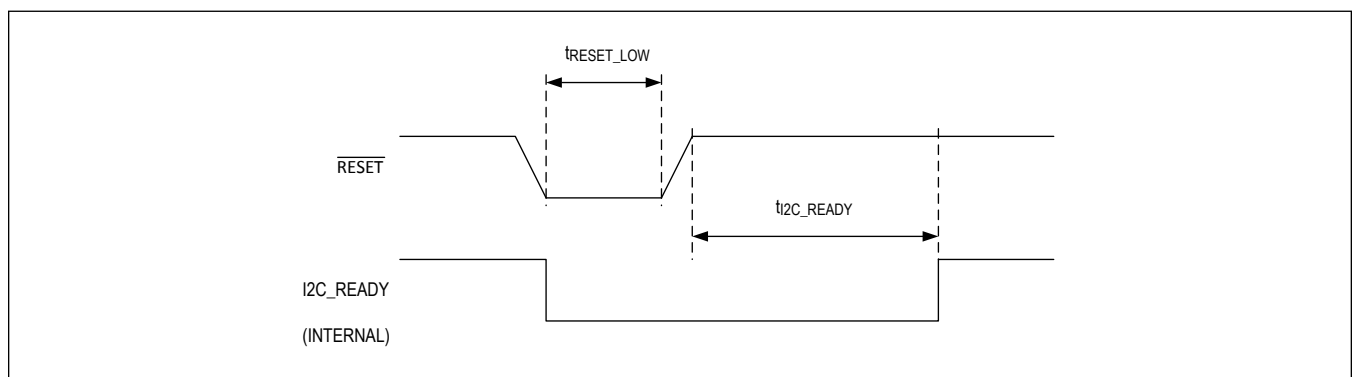


Figure 31. $\overline{\text{RESET}}$ Timing Diagram

I²C Serial Interface

Slave Address

The slave address is defined as the seven most significant bits (MSBs) followed by the read/write bit. The seven most significant bits are programmable through the ADDR1 and ADDR2 pins as shown in [Table 21](#). The device does not communicate if ADDR1 is unconnected. Setting the read/write bit to 1 configures the device for read mode. Setting the read/write bit to 0 configures the device for write mode. The address is the first byte of information sent to the device after the START condition.

Table 21. I²C Slave Address

| ADDR2 | ADDR1 | I ² C SLAVE ADDRESS (BINARY) | I ² C WRITE ADDRESS (BINARY) | I ² C READ ADDRESS (BINARY) |
|-------------------|-------------------|---|---|--|
| Connected to GND | Connected to GND | 0111000x | 01110000 | 01110001 |
| Connected to GND | Connected to DVDD | 0111001x | 01110010 | 01110011 |
| Connected to GND | Connected to SDA | 0111010x | 01110100 | 01110101 |
| Connected to GND | Connected to SCL | 0111011x | 01110110 | 01110111 |
| Connected to DVDD | Connected to GND | 0111100x | 01111000 | 01111001 |
| Connected to DVDD | Connected to DVDD | 0111101x | 01111010 | 01111011 |
| Connected to DVDD | Connected to SDA | 0111110x | 01111100 | 01111101 |
| Connected to DVDD | Connected to SCL | 0111111x | 01111110 | 01111111 |

The device features an I²C-compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the device and the master at clock rates up to 1MHz. [Figure 32](#) shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the device by transmitting the proper slave address followed by two register address bytes (most significant byte first) and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the device is 8-bits long and is followed by an acknowledge clock pulse. A master reading data from the device transmits the proper slave address followed by a series of nine SCL pulses. The device transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START (S) or REPEATED START (Sr) condition, a not acknowledge, and a STOP (P) condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on SDA. SCL operates only as an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the device from high voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

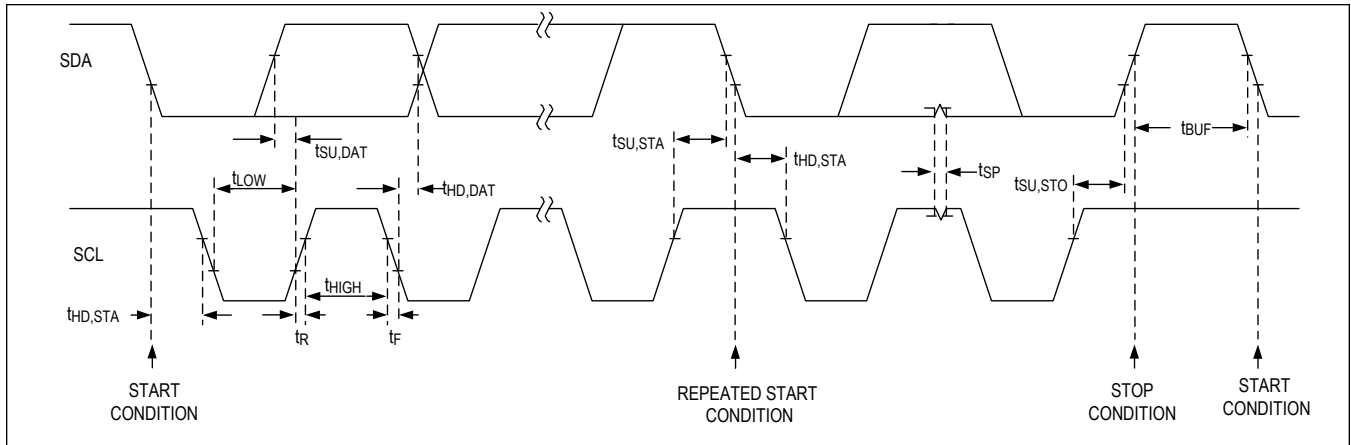


Figure 32. I²C Interface Timing Diagram

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the [START and STOP Conditions](#) section).

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high. A START condition from the master signals the beginning of a transmission to the device. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

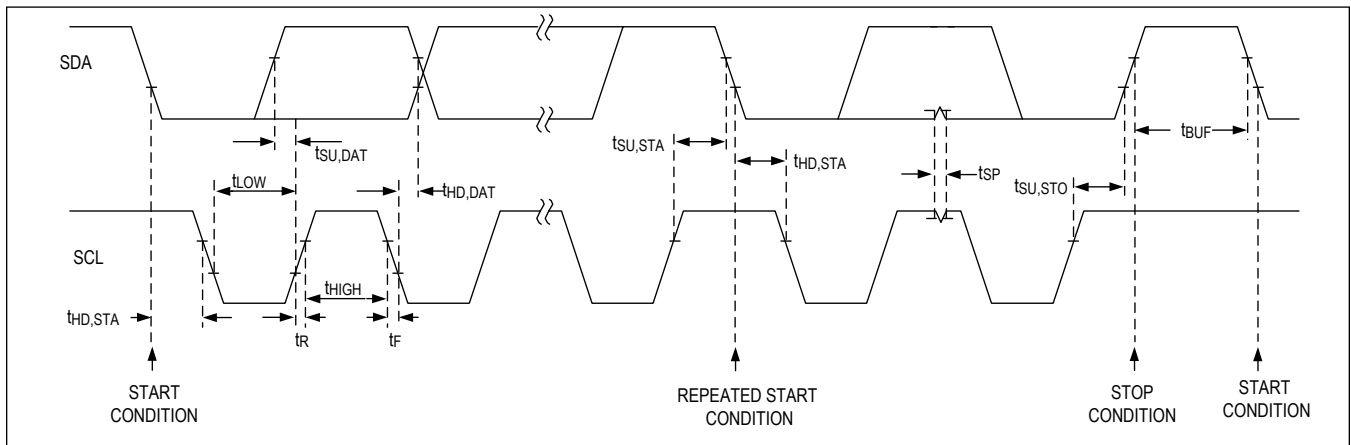


Figure 33. I²C START, STOP, and REPEATED START Conditions

Early STOP Conditions

The device recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the device uses to handshake receipt each byte of data when in write mode. The device pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master retries communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the device is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the device, followed by a STOP condition.

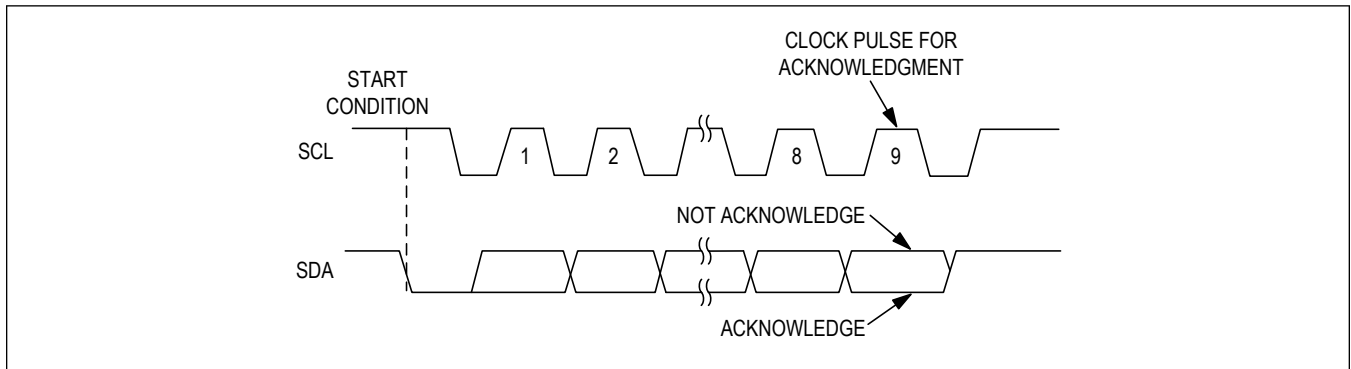


Figure 34. I²C Acknowledge

Write Data Format

A write to the device includes transmission of a START condition, the slave address with the R/W bit set to 0, two bytes of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition.

The slave address with the R/W bit set to 0 indicates that the master intends to write data to the device. The device acknowledges receipt of the address byte during the master-generated 9th SCL pulse.

The second and third bytes transmitted from the master configure the device's internal register address pointer. The pointer tells the device where to write the next byte of data. An acknowledge pulse is sent by the device upon receipt of the address pointer data.

The third byte sent to the device contains the data that is written to the chosen register. An acknowledge pulse from the device signals receipt of the data byte. The address pointer auto increments to the next register address after each received data byte. This auto-increment feature allows a master to write to sequential registers within one continuous frame. The master signals the end of transmission by issuing a STOP condition.

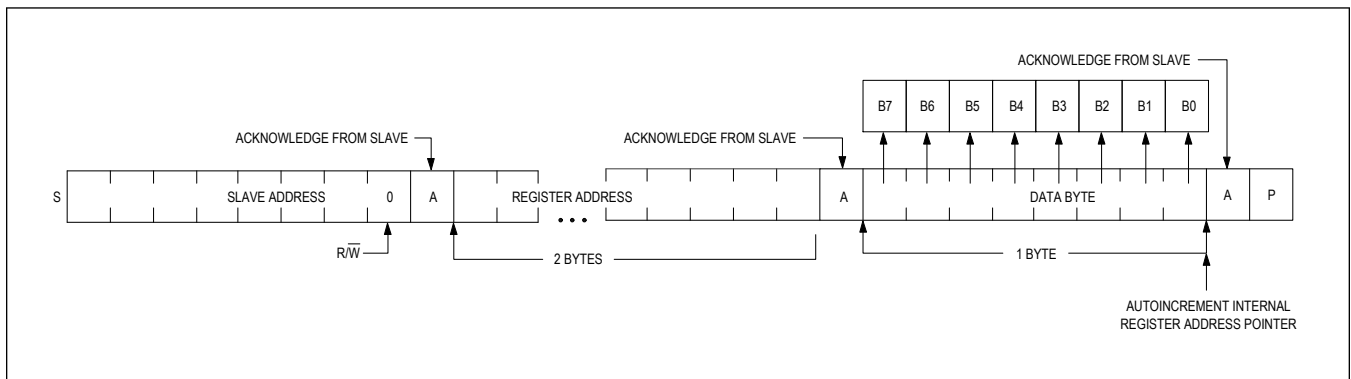


Figure 35. I²C Writing One Byte of Data to the Slave

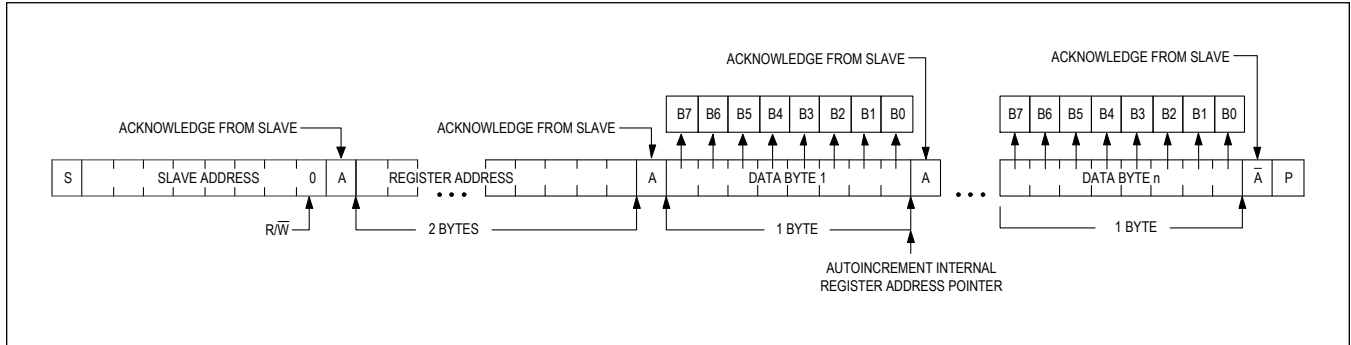


Figure 36. I²C Writing n-Bytes of Data to the Slave

Read Data Format

Sending the slave address with the R/W bit set to 1 to initiate a read operation. The device acknowledges receipt of its slave address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00.

The first byte transmitted from the device is the contents of register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer auto-increments after each read data byte. This auto-increment feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read is from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the device’s slave address with the R/W bit set to 0 followed by the two byte register address. A REPEATED START condition is then sent followed by the slave address with the R/W bit set to 1. The device then transmits the contents of the specified register. The address pointer auto-increments after transmitting the first byte.

The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition.

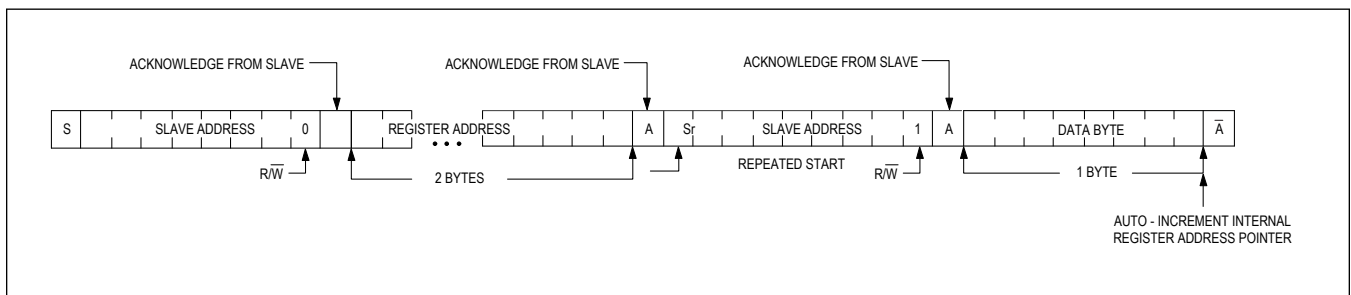


Figure 37. I²C Reading One Byte of Data from the Slave

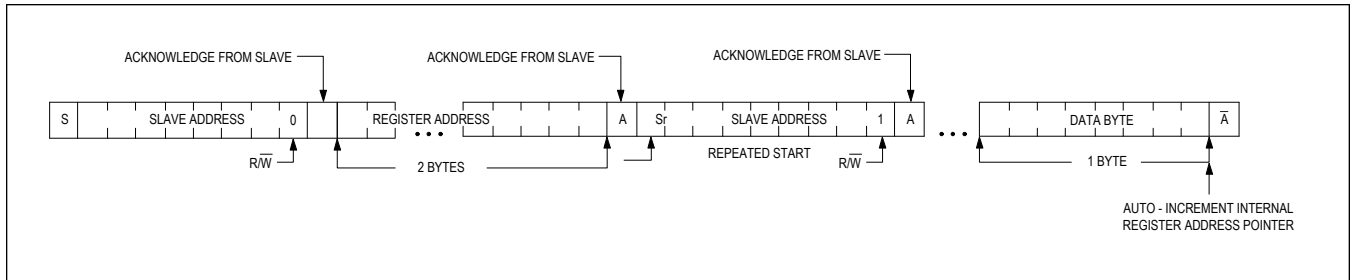


Figure 38. I²C Reading n-Bytes of Data from the Slave

I²C Register Map

Read-write registers can be both read and written by the host, the last written value is the value returned when the register is read. All registers are read-write unless specified otherwise.

Read-only registers indicate some internal device state and cannot be changed directly by the host. Writing to these registers has no effect.

Write only registers do not necessarily return the last written value when the register is read.

Undocumented registers must not be written to.

Control Bit Types and Write-Access Restrictions

The device control bits fall into one of three basic types: read, write, or read and write (denoted R, W, and RW respectively outside of some test bit exceptions). Furthermore, every write-enabled bit can have one of three access subtypes (read-only bits have no access restrictions). The first is dynamic (denoted as -D). Dynamic bits effectively have no access restrictions and can be changed (written) during any valid device state. The second bit-access subtype is static (denoted as -S). Static bits should only be changed (written) when the device is powered but placed in a software-shutdown state (device enable EN is not set). The third and final type of bit-access subtype is restricted (denoted with a -R). Unlike static bits, restricted bits can be written when the device is operating outside of a software-shutdown state, however, they require that certain related blocks be powered down individually before they are changed (written).

The general bit type and access subtype is provided individually for every register bit in the "TYPE" column of the corresponding detailed register description table. For all bits with restricted-access subtypes, the dependency setting is also denoted in the "RES" column.

Table 22 provides a detailed description of all device register types, access subtypes, and restriction dependencies used by this device. The write-access restrictions describe the specific device condition that should be met (and corresponding bit settings) before changing bits with that restriction type.

Table 22. Control Bit Types and Write-Access Restrictions

| REGISTER TYPE | WRITE ACCESS | "TYPE" SYMBOL | SUMMARY OF WRITE-ACCESS RESTRICTION CONDITIONS | "RES" SYMBOL |
|---------------|--------------|---------------|--|--------------|
| Read | Read Only | R | None | — |
| Write | Dynamic | W-D | None | — |
| | Static | RW-S | EN | EN |
| Read/Write | Dynamic | RW-D | None | — |
| | Restricted | RW-R | DSP_GLOBAL_EN | DSME |
| | | | SPK_EN | SE |
| | | | SSM_EN | SSE |
| | | | CMON_EN | CE |
| | | DMON_STUCK_EN | DSE | |

Table 22. Control Bit Types and Write-Access Restrictions (continued)

| | | | | |
|--|--|--|------------------------------|------|
| | | | DMON_MAG_EN | DME |
| | | | ICC_RX_CHn_EN, ICC_TX_CHn_EN | ICCE |
| | | | PCM_RX_CHn_EN, PCM_TX_CHn_EN | PCME |
| | | | IVADC_V_EN | VEN |
| | | | IVADC_I_EN | IEN |
| | | | AMP_DSP_EN | DE |
| | | | IRQ_EN | IE |
| | | | SPK_EN, AMP_DSP_EN | SEDE |
| | | | ENV_TRACKER_EN | ETE |
| | | | IVADC_V_EN, IVADC_I_EN | IVE |
| | | | MEAS_ADC_CH0_EN | A0E |
| | | | MEAS_ADC_CH1_EN | A1E |
| | | | MEAS_ADC_CH2_EN | A2E |
| | | | BDE_EN | BDE |
| | | | WDT_EN | WDE |

Register Map

Register Map

| ADDRESS | NAME | MSB | | | | | | | LSB |
|-----------------------|---|------------------------|----------------------|------------------------|----------------------|----------------------|------------------------|----------------------|----------------------|
| SOFTWARE RESET | | | | | | | | | |
| 0x2000 | SOFTWARE RESET[7:0] | - | - | - | - | - | - | - | RST |
| INTERRUPTS | | | | | | | | | |
| 0x2002 | INTERRUPT RAW 1[7:0] | THERM SHDN_START_RAW | THERM SHDN_END_RAW | THERM WARN_START_RAW | THERM WARN_END_RAW | BDE_L4_RAW | BDE_LEVEL_CHANGE_RAW | BDE_ACTIVE_BGN_RAW | BDE_ACTIVE_END_RAW |
| 0x2003 | INTERRUPT RAW 2[7:0] | BST_UV_LO_RAW | SPK_OVC_RAW | PWRUP_FAIL_RAW | PWRUP_DONE_RAW | PWRDN_DONE_RAW | BOOST_CURRLIM_RAW | WATCH_DOGFAIL_RAW | WATCH_DOGWARN_RAW |
| 0x2004 | INTERRUPT RAW 3[7:0] | - | DMON_ERR_RAW | FRAME_REC_RAW | FRAME_ERR_RAW | LRCLK_RATE_REC_RAW | LRCLK_RATE_ERR_RAW | BCLK_RATE_RC_RAW | BCLK_RATE_ERR_RAW |
| 0x2005 | INTERRUPT STATE 1[7:0] | THERM SHDN_START_STATE | THERM SHDN_END_STATE | THERM WARN_START_STATE | THERM WARN_END_STATE | BDE_L4_STATE | BDE_LEVEL_CHANGE_STATE | BDE_ACTIVE_BGN_STATE | BDE_ACTIVE_END_STATE |
| 0x2006 | INTERRUPT STATE 2[7:0] | BST_UV_LO_STATE | SPK_OVC_STATE | PWRUP_FAIL_STATE | PWRUP_DONE_STATE | PWRDN_DONE_STATE | BOOST_CURRLIM_STATE | WATCH_DOGFAIL_STATE | WATCH_DOGWARN_STATE |
| 0x2007 | INTERRUPT STATE 3[7:0] | - | DMON_ERR_STATE | FRAME_REC_STATE | FRAME_ERR_STATE | LRCLK_RATE_REC_STATE | LRCLK_RATE_ERR_STATE | BCLK_RATE_RC_STATE | BCLK_RATE_ERR_STATE |
| 0x2008 | INTERRUPT FLAG 1[7:0] | THERM SHDN_START_FLAG | THERM SHDN_END_FLAG | THERM WARN_START_FLAG | THERM WARN_END_FLAG | BDE_L4_FLAG | BDE_LEVEL_CHANGE_FLAG | BDE_ACTIVE_BGN_FLAG | BDE_ACTIVE_END_FLAG |
| 0x2009 | INTERRUPT FLAG 2[7:0] | BST_UV_LO_FLAG | SPK_OVC_FLAG | PWRUP_FAIL_FLAG | PWRUP_DONE_FLAG | PWRDN_DONE_FLAG | BOOST_CURRLIM_FLAG | WATCH_DOGFAIL_FLAG | WATCH_DOGWARN_FLAG |
| 0x200A | INTERRUPT FLAG 3[7:0] | - | DMON_ERR_FLAG | FRAME_REC_FLAG | FRAME_ERR_FLAG | LRCLK_RATE_REC_FLAG | LRCLK_RATE_ERR_FLAG | BCLK_RATE_RC_FLAG | BCLK_RATE_ERR_FLAG |
| 0x200B | INTERRUPT ENABLE 1[7:0] | THERM SHDN_START_EN | THERM SHDN_END_EN | THERM WARN_START_EN | THERM WARN_END_EN | BDE_L4_EN | BDE_LEVEL_CHANGE_EN | BDE_ACTIVE_BGN_EN | BDE_ACTIVE_END_EN |
| 0x200C | INTERRUPT ENABLE 2[7:0] | BST_UV_LO_EN | SPK_OVC_EN | PWRUP_FAIL_EN | PWRUP_DONE_EN | PWRDN_DONE_EN | BOOST_CURRLIM | WATCH_DOGFAIL | WATCH_DOGWARN |

| ADDRESS | NAME | MSB | | | | | | | LSB |
|-----------------------------------|---|---------------------------|--------------------|-----------------------|--------------------------|--------------------|----------------------|---------------------|--------------------|
| | | | | N | EN | EN | M_EN | L_EN | RN_EN |
| 0x200D | INTERRUPT ENABLE 3[7:0] | - | DMON_ERR_EN | FRAME_REC_EN | FRAME_ERR_EN | LRCLK_RATE_REC_EN | LRCLK_RATE_EN | BCLK_RATE_EN | BCLK_RATE_EN |
| 0x200E | INTERRUPT FLAG CLEAR 1[7:0] | THERM_SHDN_START_CLR | THERM_SHDN_END_CLR | THERM_WARN_START_CLR | THERM_WARN_END_CLR | BDE_L4_CLR | BDE_LEVEL_CHANGE_CLR | BDE_ACTIVE_BGN_CLR | BDE_ACTIVE_END_CLR |
| 0x200F | INTERRUPT FLAG CLEAR 2[7:0] | BST_UV_LO_CLR | SPK_OVC_CLR | PWRUP_FAIL_CLR | PWRUP_DONE_CLR | PWRDN_DONE_CLR | BOOST_CURRLIM_CLR | WATCHDOG_FAIL_CLR | WATCHDOG_WARN_CLR |
| 0x2010 | INTERRUPT FLAG CLEAR 3[7:0] | - | DMON_ERR_CLR | FRAME_REC_CLR | FRAME_ERR_CLR | LRCLK_RATE_REC_CLR | LRCLK_RATE_EN_CLR | BCLK_RATE_EN_CLR | BCLK_RATE_EN_CLR |
| 0x2011 | IRQ CONTROL[7:0] | - | - | - | - | - | IRQ_MODE | IRQ_POL | IRQ_EN |
| CLOCK MONITOR | | | | | | | | | |
| 0x2012 | CLOCK MONITOR CONTROL[7:0] | CMON_BSELTOL[2:0] | | | CMON_ERRTOL[2:0] | | | CMON_AUTORESTART_EN | CMON_EN |
| DATA MONITOR | | | | | | | | | |
| 0x2014 | DATA MONITOR CONTROL[7:0] | DMON_MAG_THRESH[1:0] | | DMON_STUCK_THRES[1:0] | | DMON_DURATION[1:0] | | DMON_MAG_EN | DMON_STUCK_EN |
| WATCHDOG | | | | | | | | | |
| 0x2015 | WATCHDOG CONTROL[7:0] | - | - | - | - | WDT_TO_SEL[1:0] | WDT_MODE | WDT_EN | |
| 0x2016 | WATCHDOG SW RESET[7:0] | WDT_SW_RST[7:0] | | | | | | | |
| MEASUREMENT ADC THRESHOLDS | | | | | | | | | |
| 0x2017 | MEAS ADC THERMAL WARNING THRESHHOLD[7:0] | MEAS_ADC_WARN_THRESH[7:0] | | | | | | | |
| 0x2018 | MEAS ADC THERMAL SHUTDOWN THRESHHOLD[7:0] | MEAS_ADC_SHDN_THRESH[7:0] | | | | | | | |
| 0x2019 | MEAS ADC THERMAL HYSTERESIS[7:0] | - | - | - | MEAS_ADC_THERM_HYST[4:0] | | | | |
| PIN CONFIGURATION | | | | | | | | | |
| 0x201A | PIN CONFIG[7:0] | ICC_DRV[1:0] | | LRCLK_DRV[1:0] | | BCLK_DRV[1:0] | | DOUT_DRV[1:0] | |
| PCM INTERFACE | | | | | | | | | |
| 0x201B | PCM RX ENABLES A[7:0] | PCM_RX_CH7_EN | PCM_RX_CH6_EN | PCM_RX_CH5_EN | PCM_RX_CH4_EN | PCM_RX_CH3_EN | PCM_RX_CH2_EN | PCM_RX_CH1_EN | PCM_RX_CH0_EN |
| 0x201C | PCM RX ENABLES B[7:0] | PCM_RX_CH15_EN | PCM_RX_CH14_EN | PCM_RX_CH13_EN | PCM_RX_CH12_EN | PCM_RX_CH11_EN | PCM_RX_CH10_EN | PCM_RX_CH9_EN | PCM_RX_CH8_EN |

| ADDRESS | NAME | MSB | | | | | | | LSB |
|------------|--|--------------------------|-----------------|--------------------|-----------------|--------------------------|--------------------|------------------|-------------------|
| 0x201D | PCM TX ENABLES A[7:0] | PCM_TX_CH7_EN | PCM_TX_CH6_EN | PCM_TX_CH5_EN | PCM_TX_CH4_EN | PCM_TX_CH3_EN | PCM_TX_CH2_EN | PCM_TX_CH1_EN | PCM_TX_CH0_EN |
| 0x201E | PCM TX ENABLES B[7:0] | PCM_TX_CH15_EN | PCM_TX_CH14_EN | PCM_TX_CH13_EN | PCM_TX_CH12_EN | PCM_TX_CH11_EN | PCM_TX_CH10_EN | PCM_TX_CH9_EN | PCM_TX_CH8_EN |
| 0x201F | PCM TX HIZ CONTROL A[7:0] | PCM_TX_CH7_HIZ | PCM_TX_CH6_HIZ | PCM_TX_CH5_HIZ | PCM_TX_CH4_HIZ | PCM_TX_CH3_HIZ | PCM_TX_CH2_HIZ | PCM_TX_CH1_HIZ | PCM_TX_CH0_HIZ |
| 0x2020 | PCM TX HIZ CONTROL B[7:0] | PCM_TX_CH15_HIZ | PCM_TX_CH14_HIZ | PCM_TX_CH13_HIZ | PCM_TX_CH12_HIZ | PCM_TX_CH11_HIZ | PCM_TX_CH10_HIZ | PCM_TX_CH9_HIZ | PCM_TX_CH8_HIZ |
| 0x2021 | PCM CHANNEL SOURCES 1[7:0] | PCM_DAC_BASS_SOURCE[3:0] | | | | PCM_DAC_MAIN_SOURCE[3:0] | | | |
| 0x2022 | PCM CHANNEL SOURCES 2[7:0] | PCM_IVADC_I_DEST[3:0] | | | | PCM_IVADC_V_DEST[3:0] | | | |
| 0x2023 | PCM CHANNEL SOURCES 3[7:0] | PCM_IVADC_INTERLEAVE | - | - | - | PCM_AMP_DSP_DEST[3:0] | | | |
| 0x2024 | PCM MODE CONFIG[7:0] | PCM_CHANSZ[1:0] | | PCM_FORMAT[2:0] | | PCM_BCLKEDGE | PCM_CHANSEL | PCM_TX_EXTRA_HIZ | |
| 0x2025 | PCM MASTER MODE[7:0] | - | PCM_CLK_SOURCE | PCM_MCLK_RATE[3:0] | | | PCM_MSTR_MODE[1:0] | | |
| 0x2026 | PCM CLOCK SETUP[7:0] | PCM_MSEL[3:0] | | | | PCM_BSEL[3:0] | | | |
| 0x2027 | PCM SAMPLE RATE SETUP 1[7:0] | - | - | - | - | SPK_SR[3:0] | | | |
| ICC | | | | | | | | | |
| 0x202C | ICC RX ENABLES A[7:0] | ICC_RX_CH7_EN | ICC_RX_CH6_EN | ICC_RX_CH5_EN | ICC_RX_CH4_EN | ICC_RX_CH3_EN | ICC_RX_CH2_EN | ICC_RX_CH1_EN | ICC_RX_CH0_EN |
| 0x202D | ICC RX ENABLES B[7:0] | ICC_RX_CH15_EN | ICC_RX_CH14_EN | ICC_RX_CH13_EN | ICC_RX_CH12_EN | ICC_RX_CH11_EN | ICC_RX_CH10_EN | ICC_RX_CH9_EN | ICC_RX_CH8_EN |
| 0x202E | ICC TX ENABLES A[7:0] | ICC_TX_CH7_EN | ICC_TX_CH6_EN | ICC_TX_CH5_EN | ICC_TX_CH4_EN | ICC_TX_CH3_EN | ICC_TX_CH2_EN | ICC_TX_CH1_EN | ICC_TX_CH0_EN |
| 0x202F | ICC TX ENABLES B[7:0] | ICC_TX_CH15_EN | ICC_TX_CH14_EN | ICC_TX_CH13_EN | ICC_TX_CH12_EN | ICC_TX_CH11_EN | ICC_TX_CH10_EN | ICC_TX_CH9_EN | ICC_TX_CH8_EN |
| 0x2030 | ICC HIZ MANUAL MODE[7:0] | - | - | - | - | - | - | ICC_TX_EXTRA_HIZ | ICC_TX_HIZ_MANUAL |
| 0x2031 | ICC TX HIZ ENABLES A[7:0] | ICC_TX_CH7_HIZ | ICC_TX_CH6_HIZ | ICC_TX_CH5_HIZ | ICC_TX_CH4_HIZ | ICC_TX_CH3_HIZ | ICC_TX_CH2_HIZ | ICC_TX_CH1_HIZ | ICC_TX_CH0_HIZ |
| 0x2032 | ICC TX HIZ ENABLES B[7:0] | ICC_TX_CH15_HIZ | ICC_TX_CH14_HIZ | ICC_TX_CH13_HIZ | ICC_TX_CH12_HIZ | ICC_TX_CH11_HIZ | ICC_TX_CH10_HIZ | ICC_TX_CH9_HIZ | ICC_TX_CH8_HIZ |

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| 0x2033 | ICC LINK ENABLES[7:0] | - | - | - | - | - | - | - | ICC_LINK_EN |
| AMP DSP | | | | | | | | | |
| 0x2039 | AMP DSP CONFIG[7:0] | - | DAC_IN VERT | STARTUP P_RAMP _BYPAS S | SHDN_R AMP_BY PASS | DAC_HA LF_REF _CURRE NT | DAC_DO UBLE_R FB | AMP_DI TH_EN | AMP_DC BLK_EN |
| AMP ENABLES | | | | | | | | | |
| 0x203A | AMP ENABLES[7:0] | ENABLE _DEM | - | - | - | - | - | - | SPK_EN |
| TONE GENERATOR | | | | | | | | | |
| 0x203B | TONE GENERATOR AND DC CONFIG[7:0] | - | - | - | - | TONE_CONFIG[3:0] | | | |
| SPEAKER | | | | | | | | | |
| 0x203C | SPEAKER SOURCE SELECT[7:0] | - | - | - | - | - | - | SPK_SOURCE[1:0] | |
| 0x203D | SPEAKER GAIN[7:0] | - | - | - | - | - | - | - | - |
| 0x203E | SSM CONFIGURATION[7:0] | SSM_EN | - | SPK_EDGE_CTRL[1:0] | | - | SSM_MOD_INDEX[2:0] | | |
| IV ADC | | | | | | | | | |
| 0x203F | MEASUREMENT ENABLES[7:0] | - | - | - | - | - | - | IVADC_I _EN | IVADC_V _EN |
| 0x2040 | MEASUREMENT DSP CONFIG[7:0] | MEAS_I_DCBLK[1:0] | | MEAS_V_DCBLK[1:0] | | - | MEAS_D ITH_EN | MEAS_I _DCBLK _EN | MEAS_V _DCBLK _EN |
| BOOST | | | | | | | | | |
| 0x2041 | BOOST CONTROL 0[7:0] | EXT_PV DD_EN | - | - | BST_VOUT[4:0] | | | | |
| 0x2042 | BOOST CONTROL 3[7:0] | - | - | BST_SL OWSTA RT | BST_PHASE[2:0] | | | BST_SKIPLOAD[1:0] | |
| 0x2043 | BOOST CONTROL 1[7:0] | BST_SKI P_CONT ROL | BST_ILIM[6:0] | | | | | | |
| MEASUREMENT ADC | | | | | | | | | |
| 0x2044 | MEAS ADC CONFIG[7:0] | - | - | - | - | - | MEAS_A DC_CH2 _EN | MEAS_A DC_CH1 _EN | MEAS_A DC_CH0 _EN |
| 0x2045 | MEAS ADC BASE DIVIDE MSBYTE[7:0] | MEAS_ADC_BASE_DIV[15:8] | | | | | | | |
| 0x2046 | MEAS ADC BASE DIVIDE LSBYTE[7:0] | MEAS_ADC_BASE_DIV[7:0] | | | | | | | |
| 0x2047 | MEAS ADC CHAN 0 DIVIDE[7:0] | MEAS_ADC_CH0_DIV[7:0] | | | | | | | |
| 0x2048 | MEAS ADC CHAN 1 DIVIDE[7:0] | MEAS_ADC_CH1_DIV[7:0] | | | | | | | |
| 0x2049 | MEAS ADC CHAN 2 | MEAS_ADC_CH2_DIV[7:0] | | | | | | | |

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| | DIVIDE[7:0] | | | | | | | | |
| 0x204A | MEAS ADC CHAN 0 FILT CONFIG[7:0] | - | - | - | - | MEAS_A DC_CH0 _FILT_E N | MEAS_ADC_CH0_FILT_AVG[2: 0] | | |
| 0x204B | MEAS ADC CHAN 1 FILT CONFIG[7:0] | - | - | - | - | MEAS_A DC_CH1 _FILT_E N | MEAS_ADC_CH1_FILT_AVG[2: 0] | | |
| 0x204C | MEAS ADC CHAN 2 FILT CONFIG[7:0] | - | - | - | - | MEAS_A DC_CH2 _FILT_E N | MEAS_ADC_CH2_FILT_AVG[2: 0] | | |
| 0x204D | MEAS ADC CHAN 0 READBACK[7:0] | MEAS_ADC_CH0_DATA[7:0] | | | | | | | |
| 0x204E | MEAS ADC CHAN 1 READBACK[7:0] | MEAS_ADC_CH1_DATA[7:0] | | | | | | | |
| 0x204F | MEAS ADC CHAN 2 READBACK[7:0] | MEAS_ADC_CH2_DATA[7:0] | | | | | | | |
| DSP POWER GATING | | | | | | | | | |
| 0x2050 | DSP POWER GATING CONTROL[7:0] | - | - | POWER _GATE_ EXIT_TH RESH | POWER_GATE_ENTRY_THRE SH[2:0] | | | AUTO_M UTING_ EN | POWER _GATIN G_EN |
| 0x2051 | DSP POWER GATING STATUS[7:0] | - | - | - | - | - | - | MUTE_A CTIVE | POWER _GATIN G_ACTI VE |
| VBAT AND PBDD STATUS | | | | | | | | | |
| 0x2052 | VBAT LOWEST STATUS[7:0] | VBAT_LOWEST[7:0] | | | | | | | |
| 0x2053 | PVDD LOWEST STATUS[7:0] | PVDD_LOWEST[7:0] | | | | | | | |
| BDE | | | | | | | | | |
| 0x2054 | BROWNOUT STATUS[7:0] | - | - | - | - | - | BDE_STATE[2:0] | | |
| 0x2055 | BROWNOUT ENABLES[7:0] | - | - | - | - | - | AMP_DS P_EN | BDE_AM P_EN | BDE_EN |
| 0x2056 | BROWNOUT LEVEL INFINITE HOLD[7:0] | - | - | - | - | - | - | BDE_L4 _INF_HL D | - |
| 0x2057 | BROWNOUT LEVEL INFINITE HOLD CLEAR[7:0] | - | - | - | - | - | - | BDE_L4 _HLD_R LS | - |
| 0x2058 | BROWNOUT LEVEL HOLD[7:0] | BDE_HLD[7:0] | | | | | | | |
| 0x2059 | BROWNOUT LEVEL 1 THRESHOLD[7:0] | BDE_L1_VTHRESH[7:0] | | | | | | | |
| 0x205A | BROWNOUT LEVEL 2 | BDE_L2_VTHRESH[7:0] | | | | | | | |

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| | THRESHOLD[7:0] | | | | | | | | |
| 0x205B | BROWNOUT LEVEL 3 THRESHOLD[7:0] | | | | | | | | BDE_L3_VTHRESH[7:0] |
| 0x205C | BROWNOUT LEVEL 4 THRESHOLD[7:0] | | | | | | | | BDE_L4_VTHRESH[7:0] |
| 0x205D | BROWNOUT THRESHOLD HYSTERESIS[7:0] | | | | | | | | BDE_VTHRESH_HYST[7:0] |
| 0x205E | BROWNOUT AMP LIMITER ATTACK RELEASE[7:0] | | | | | | | | AMP_LIM_ATK[3:0] AMP_LIM_RLS[3:0] |
| 0x205F | BROWNOUT AMP GAIN ATTACK RELEASE[7:0] | | | | | | | | AMP_GAIN_ATK[3:0] AMP_GAIN_RLS[3:0] |
| 0x2060 | BROWNOUT AMP1 CLIP MODE[7:0] | - | - | - | - | - | - | - | AMP_CLIP_MODE |
| 0x2061 | BROWNOUT LEVEL 1 CURRENT LIMIT[7:0] | - | | | | | | | BDE_L1_ILIM[6:0] |
| 0x2062 | BROWNOUT LEVEL 1 AMP 1 CONTROL 1[7:0] | - | - | - | - | | | | BDE_L1_AMP1_LIM[3:0] |
| 0x2063 | BROWNOUT LEVEL 1 AMP 1 CONTROL 2[7:0] | - | - | | | | | | BDE_L1_AMP1_CLIP[5:0] |
| 0x2064 | BROWNOUT LEVEL 1 AMP 1 CONTROL 3[7:0] | - | - | | | | | | BDE_L1_AMP1_GAIN[5:0] |
| 0x2065 | BROWNOUT LEVEL 2 CURRENT LIMIT[7:0] | - | | | | | | | BDE_L2_ILIM[6:0] |
| 0x2066 | BROWNOUT LEVEL 2 AMP 1 CONTROL 1[7:0] | - | - | - | - | | | | BDE_L2_AMP1_LIM[3:0] |
| 0x2067 | BROWNOUT LEVEL 2 AMP 1 CONTROL 2[7:0] | - | - | | | | | | BDE_L2_AMP1_CLIP[5:0] |
| 0x2068 | BROWNOUT LEVEL 2 AMP 1 CONTROL 3[7:0] | - | - | | | | | | BDE_L2_AMP1_GAIN[5:0] |
| 0x2069 | BROWNOUT LEVEL 3 CURRENT LIMIT[7:0] | - | | | | | | | BDE_L3_ILIM[6:0] |
| 0x206A | BROWNOUT LEVEL 3 AMP 1 CONTROL 1[7:0] | - | - | - | - | | | | BDE_L3_AMP1_LIM[3:0] |
| 0x206B | BROWNOUT LEVEL 3 AMP 1 CONTROL 2[7:0] | - | - | | | | | | BDE_L3_AMP1_CLIP[5:0] |
| 0x206C | BROWNOUT LEVEL 3 AMP 1 CONTROL 3[7:0] | - | - | | | | | | BDE_L3_AMP1_GAIN[5:0] |

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| 0x206D | BROWNOUT LEVEL 4 CURRENT LIMIT[7:0] | - | BDE_L4_ILIM[6:0] | | | | | |
| 0x206E | BROWNOUT LEVEL 4 AMP 1 CONTROL 1[7:0] | - | - | - | - | BDE_L4_AMP1_LIM[3:0] | | |
| 0x206F | BROWNOUT LEVEL 4 AMP 1 CONTROL 2[7:0] | BDE_L4_AMP1_MUTE | - | BDE_L4_AMP1_CLIP[5:0] | | | | |
| 0x2070 | BROWNOUT LEVEL 4 AMP 1 CONTROL 3[7:0] | - | - | BDE_L4_AMP1_GAIN[5:0] | | | | |
| 0x2071 | BROWNOUT LOWEST STATUS[7:0] | - | - | - | - | - | BDE_LOWEST[2:0] | |
| 0x2072 | BROWNOUT ILIM HOLD[7:0] | BDE_ILIM_HLD[7:0] | | | | | | |
| 0x2073 | BROWNOUT LIM HOLD[7:0] | BDE_LIM_HLD[7:0] | | | | | | |
| 0x2074 | BROWNOUT CLIP HOLD[7:0] | BDE_CLIP_HLD[7:0] | | | | | | |
| 0x2075 | BROWNOUT GAIN HOLD[7:0] | BDE_GAIN_HLD[7:0] | | | | | | |
| ENVELOPE TRACKER | | | | | | | | |
| 0x2076 | ENV TRACKER VOUT HEADROOM[7:0] | - | - | - | ENV_TRACKER_BST_VOUT_HEADROOM[4:0] | | | |
| 0x2077 | ENV TRACKER BOOST VOUT DELAY[7:0] | ENV_TRACKER_BDE_MODE | - | ENV_BYP_DELAY[5:0] | | | | |
| 0x2078 | ENV TRACKER RELEASE RATE[7:0] | - | - | ENV_TRACKER_RLS_RATE_SCALE[1:0] | - | ENV_TRACKER_RLS_RATE[2:0] | | |
| 0x2079 | ENV TRACKER HOLD RATE[7:0] | - | - | - | - | ENV_TRACKER_HOLD_RATE[2:0] | | |
| 0x207A | ENV TRACKER CONTROL[7:0] | - | - | - | - | - | - | ENV_TRACKER_EN |
| 0x207B | ENV TRACKER BOOST VOUT READBACK[7:0] | - | - | - | ENV_TRACKER_BST_VOUT_RD[4:0] | | | |
| BOOST BYPASS | | | | | | | | |
| 0x207C | BOOST BYPASS 1[7:0] | - | BST_CURRLIM_MASK_EN | - | - | BST_BYP_HEADROOM[3:0] | | |
| 0x207D | BOOST BYPASS 2[7:0] | - | BST_CURRLIM_MASK_TIMER[3:0] | | | - | BST_BYP_MODE[1:0] | |
| 0x207E | BOOST BYPASS 3[7:0] | - | - | - | - | BST_BYP_HOLD_TIME[3:0] | | |
| FET SCALING | | | | | | | | |

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| 0x207F | FET SCALING 1[7:0] | - | - | - | - | - | - | AMP_FET_SCALE_MODE[1:0] |
| 0x2080 | FET SCALING 2[7:0] | - | - | - | AMP_FET_SCALE_THRESHOLD[4:0] | | | |
| 0x2081 | FET SCALING 3[7:0] | - | - | - | - | AMP_FET_SCALE_HYST[3:0] | | |
| 0x2082 | FET SCALING 4[7:0] | - | - | - | - | AMP_FET_SCALE_HOLD_TIME[3:0] | | |
| ADVANCED SETTINGS | | | | | | | | |
| 0x2084 | ADVANCED SETTINGS[7:0] | - | - | - | - | - | - | SPK_SP EEDUP |
| DSM EQ BIQUAD 1 | | | | | | | | |
| 0x2129 | DSM_EQ_BQ1_B0_BY TE0[7:0] | DSM_EQ_BQ1_B0[7:0] | | | | | | |
| 0x212A | DSM_EQ_BQ1_B0_BY TE1[7:0] | DSM_EQ_BQ1_B0[15:8] | | | | | | |
| 0x212B | DSM_EQ_BQ1_B0_BY TE2[7:0] | DSM_EQ_BQ1_B0[23:16] | | | | | | |
| 0x212D | DSM_EQ_BQ1_B1_BY TE0[7:0] | DSM_EQ_BQ1_B1[7:0] | | | | | | |
| 0x212E | DSM_EQ_BQ1_B1_BY TE1[7:0] | DSM_EQ_BQ1_B1[15:8] | | | | | | |
| 0x212F | DSM_EQ_BQ1_B1_BY TE2[7:0] | DSM_EQ_BQ1_B1[23:16] | | | | | | |
| 0x2131 | DSM_EQ_BQ1_B2_BY TE0[7:0] | DSM_EQ_BQ1_B2[7:0] | | | | | | |
| 0x2132 | DSM_EQ_BQ1_B2_BY TE1[7:0] | DSM_EQ_BQ1_B2[15:8] | | | | | | |
| 0x2133 | DSM_EQ_BQ1_B2_BY TE2[7:0] | DSM_EQ_BQ1_B2[23:16] | | | | | | |
| 0x2135 | DSM_EQ_BQ1_A1_BY TE0[7:0] | DSM_EQ_BQ1_A1[7:0] | | | | | | |
| 0x2136 | DSM_EQ_BQ1_A1_BY TE1[7:0] | DSM_EQ_BQ1_A1[15:8] | | | | | | |
| 0x2137 | DSM_EQ_BQ1_A1_BY TE2[7:0] | DSM_EQ_BQ1_A1[23:16] | | | | | | |
| 0x2139 | DSM_EQ_BQ1_A2_BY TE0[7:0] | DSM_EQ_BQ1_A2[7:0] | | | | | | |
| 0x213A | DSM_EQ_BQ1_A2_BY TE1[7:0] | DSM_EQ_BQ1_A2[15:8] | | | | | | |
| 0x213B | DSM_EQ_BQ1_A2_BY TE2[7:0] | DSM_EQ_BQ1_A2[23:16] | | | | | | |
| DSM EQ BIQUAD 2 | | | | | | | | |
| 0x213D | DSM_EQ_BQ2_B0_BY TE0[7:0] | DSM_EQ_BQ2_B0[7:0] | | | | | | |
| 0x213E | DSM_EQ_BQ2_B0_BY TE1[7:0] | DSM_EQ_BQ2_B0[15:8] | | | | | | |
| 0x213F | DSM_EQ_BQ2_B0_BY TE2[7:0] | DSM_EQ_BQ2_B0[23:16] | | | | | | |

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| 0x2141 | DSM_EQ_BQ2_B1_BY TE0[7:0] | | | | | | | DSM_EQ_BQ2_B1[7:0] |
| 0x2142 | DSM_EQ_BQ2_B1_BY TE1[7:0] | | | | | | | DSM_EQ_BQ2_B1[15:8] |
| 0x2143 | DSM_EQ_BQ2_B1_BY TE2[7:0] | | | | | | | DSM_EQ_BQ2_B1[23:16] |
| 0x2145 | DSM_EQ_BQ2_B2_BY TE0[7:0] | | | | | | | DSM_EQ_BQ2_B2[7:0] |
| 0x2146 | DSM_EQ_BQ2_B2_BY TE1[7:0] | | | | | | | DSM_EQ_BQ2_B2[15:8] |
| 0x2147 | DSM_EQ_BQ2_B2_BY TE2[7:0] | | | | | | | DSM_EQ_BQ2_B2[23:16] |
| 0x2149 | DSM_EQ_BQ2_A1_BY TE0[7:0] | | | | | | | DSM_EQ_BQ2_A1[7:0] |
| 0x214A | DSM_EQ_BQ2_A1_BY TE1[7:0] | | | | | | | DSM_EQ_BQ2_A1[15:8] |
| 0x214B | DSM_EQ_BQ2_A1_BY TE2[7:0] | | | | | | | DSM_EQ_BQ2_A1[23:16] |
| 0x214D | DSM_EQ_BQ2_A2_BY TE0[7:0] | | | | | | | DSM_EQ_BQ2_A2[7:0] |
| 0x214E | DSM_EQ_BQ2_A2_BY TE1[7:0] | | | | | | | DSM_EQ_BQ2_A2[15:8] |
| 0x214F | DSM_EQ_BQ2_A2_BY TE2[7:0] | | | | | | | DSM_EQ_BQ2_A2[23:16] |
| DSM EQ BIQUAD 3 | | | | | | | | |
| 0x2151 | DSM_EQ_BQ3_B0_BY TE0[7:0] | | | | | | | DSM_EQ_BQ3_B0[7:0] |
| 0x2152 | DSM_EQ_BQ3_B0_BY TE1[7:0] | | | | | | | DSM_EQ_BQ3_B0[15:8] |
| 0x2153 | DSM_EQ_BQ3_B0_BY TE2[7:0] | | | | | | | DSM_EQ_BQ3_B0[23:16] |
| 0x2155 | DSM_EQ_BQ3_B1_BY TE0[7:0] | | | | | | | DSM_EQ_BQ3_B1[7:0] |
| 0x2156 | DSM_EQ_BQ3_B1_BY TE1[7:0] | | | | | | | DSM_EQ_BQ3_B1[15:8] |
| 0x2157 | DSM_EQ_BQ3_B1_BY TE2[7:0] | | | | | | | DSM_EQ_BQ3_B1[23:16] |
| 0x2159 | DSM_EQ_BQ3_B2_BY TE0[7:0] | | | | | | | DSM_EQ_BQ3_B2[7:0] |
| 0x215A | DSM_EQ_BQ3_B2_BY TE1[7:0] | | | | | | | DSM_EQ_BQ3_B2[15:8] |
| 0x215B | DSM_EQ_BQ3_B2_BY TE2[7:0] | | | | | | | DSM_EQ_BQ3_B2[23:16] |
| 0x215D | DSM_EQ_BQ3_A1_BY TE0[7:0] | | | | | | | DSM_EQ_BQ3_A1[7:0] |
| 0x215E | DSM_EQ_BQ3_A1_BY TE1[7:0] | | | | | | | DSM_EQ_BQ3_A1[15:8] |

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| 0x215F | DSM_EQ_BQ3_A1_BY TE2[7:0] | | | | | | | DSM_EQ_BQ3_A1[23:16] |
| 0x2161 | DSM_EQ_BQ3_A2_BY TE0[7:0] | | | | | | | DSM_EQ_BQ3_A2[7:0] |
| 0x2162 | DSM_EQ_BQ3_A2_BY TE1[7:0] | | | | | | | DSM_EQ_BQ3_A2[15:8] |
| 0x2163 | DSM_EQ_BQ3_A2_BY TE2[7:0] | | | | | | | DSM_EQ_BQ3_A2[23:16] |
| DSM EQ BIQUAD 4 | | | | | | | | |
| 0x2165 | DSM_EQ_BQ4_B0_BY TE0[7:0] | | | | | | | DSM_EQ_BQ4_B0[7:0] |
| 0x2166 | DSM_EQ_BQ4_B0_BY TE1[7:0] | | | | | | | DSM_EQ_BQ4_B0[15:8] |
| 0x2167 | DSM_EQ_BQ4_B0_BY TE2[7:0] | | | | | | | DSM_EQ_BQ4_B0[23:16] |
| 0x2169 | DSM_EQ_BQ4_B1_BY TE0[7:0] | | | | | | | DSM_EQ_BQ4_B1[7:0] |
| 0x216A | DSM_EQ_BQ4_B1_BY TE1[7:0] | | | | | | | DSM_EQ_BQ4_B1[15:8] |
| 0x216B | DSM_EQ_BQ4_B1_BY TE2[7:0] | | | | | | | DSM_EQ_BQ4_B1[23:16] |
| 0x216D | DSM_EQ_BQ4_B2_BY TE0[7:0] | | | | | | | DSM_EQ_BQ4_B2[7:0] |
| 0x216E | DSM_EQ_BQ4_B2_BY TE1[7:0] | | | | | | | DSM_EQ_BQ4_B2[15:8] |
| 0x216F | DSM_EQ_BQ4_B2_BY TE2[7:0] | | | | | | | DSM_EQ_BQ4_B2[23:16] |
| 0x2171 | DSM_EQ_BQ4_A1_BY TE0[7:0] | | | | | | | DSM_EQ_BQ4_A1[7:0] |
| 0x2172 | DSM_EQ_BQ4_A1_BY TE1[7:0] | | | | | | | DSM_EQ_BQ4_A1[15:8] |
| 0x2173 | DSM_EQ_BQ4_A1_BY TE2[7:0] | | | | | | | DSM_EQ_BQ4_A1[23:16] |
| 0x2175 | DSM_EQ_BQ4_A2_BY TE0[7:0] | | | | | | | DSM_EQ_BQ4_A2[7:0] |
| 0x2176 | DSM_EQ_BQ4_A2_BY TE1[7:0] | | | | | | | DSM_EQ_BQ4_A2[15:8] |
| 0x2177 | DSM_EQ_BQ4_A2_BY TE2[7:0] | | | | | | | DSM_EQ_BQ4_A2[23:16] |
| DSM EQ BIQUAD 5 | | | | | | | | |
| 0x2179 | DSM_EQ_BQ5_B0_BY TE0[7:0] | | | | | | | DSM_EQ_BQ5_B0[7:0] |
| 0x217A | DSM_EQ_BQ5_B0_BY TE1[7:0] | | | | | | | DSM_EQ_BQ5_B0[15:8] |
| 0x217B | DSM_EQ_BQ5_B0_BY TE2[7:0] | | | | | | | DSM_EQ_BQ5_B0[23:16] |
| 0x217D | DSM_EQ_BQ5_B1_BY | | | | | | | DSM_EQ_BQ5_B1[7:0] |

| ADDRESS | NAME | MSB | | | | | | LSB |
|------------------------|--|-----|--|--|--|--|--|----------------------|
| | TE0[7:0] | | | | | | | |
| 0x217E | DSM_EQ_BQ5_B1_BY TE1[7:0] | | | | | | | DSM_EQ_BQ5_B1[15:8] |
| 0x217F | DSM_EQ_BQ5_B1_BY TE2[7:0] | | | | | | | DSM_EQ_BQ5_B1[23:16] |
| 0x2181 | DSM_EQ_BQ5_B2_BY TE0[7:0] | | | | | | | DSM_EQ_BQ5_B2[7:0] |
| 0x2182 | DSM_EQ_BQ5_B2_BY TE1[7:0] | | | | | | | DSM_EQ_BQ5_B2[15:8] |
| 0x2183 | DSM_EQ_BQ5_B2_BY TE2[7:0] | | | | | | | DSM_EQ_BQ5_B2[23:16] |
| 0x2185 | DSM_EQ_BQ5_A1_BY TE0[7:0] | | | | | | | DSM_EQ_BQ5_A1[7:0] |
| 0x2186 | DSM_EQ_BQ5_A1_BY TE1[7:0] | | | | | | | DSM_EQ_BQ5_A1[15:8] |
| 0x2187 | DSM_EQ_BQ5_A1_BY TE2[7:0] | | | | | | | DSM_EQ_BQ5_A1[23:16] |
| 0x2189 | DSM_EQ_BQ5_A2_BY TE0[7:0] | | | | | | | DSM_EQ_BQ5_A2[7:0] |
| 0x218A | DSM_EQ_BQ5_A2_BY TE1[7:0] | | | | | | | DSM_EQ_BQ5_A2[15:8] |
| 0x218B | DSM_EQ_BQ5_A2_BY TE2[7:0] | | | | | | | DSM_EQ_BQ5_A2[23:16] |
| DSM EQ BIQUAD 6 | | | | | | | | |
| 0x218D | DSM_EQ_BQ6_B0_BY TE0[7:0] | | | | | | | DSM_EQ_BQ6_B0[7:0] |
| 0x218E | DSM_EQ_BQ6_B0_BY TE1[7:0] | | | | | | | DSM_EQ_BQ6_B0[15:8] |
| 0x218F | DSM_EQ_BQ6_B0_BY TE2[7:0] | | | | | | | DSM_EQ_BQ6_B0[23:16] |
| 0x2191 | DSM_EQ_BQ6_B1_BY TE0[7:0] | | | | | | | DSM_EQ_BQ6_B1[7:0] |
| 0x2192 | DSM_EQ_BQ6_B1_BY TE1[7:0] | | | | | | | DSM_EQ_BQ6_B1[15:8] |
| 0x2193 | DSM_EQ_BQ6_B1_BY TE2[7:0] | | | | | | | DSM_EQ_BQ6_B1[23:16] |
| 0x2195 | DSM_EQ_BQ6_B2_BY TE0[7:0] | | | | | | | DSM_EQ_BQ6_B2[7:0] |
| 0x2196 | DSM_EQ_BQ6_B2_BY TE1[7:0] | | | | | | | DSM_EQ_BQ6_B2[15:8] |
| 0x2197 | DSM_EQ_BQ6_B2_BY TE2[7:0] | | | | | | | DSM_EQ_BQ6_B2[23:16] |
| 0x2199 | DSM_EQ_BQ6_A1_BY TE0[7:0] | | | | | | | DSM_EQ_BQ6_A1[7:0] |
| 0x219A | DSM_EQ_BQ6_A1_BY TE1[7:0] | | | | | | | DSM_EQ_BQ6_A1[15:8] |
| 0x219B | DSM_EQ_BQ6_A1_BY TE2[7:0] | | | | | | | DSM_EQ_BQ6_A1[23:16] |

| ADDRESS | NAME | MSB | | | | | | LSB |
|------------------------|--|-----|--|--|--|--|--|----------------------|
| | TE2[7:0] | | | | | | | |
| 0x219D | DSM_EQ_BQ6_A2_BY TE0[7:0] | | | | | | | DSM_EQ_BQ6_A2[7:0] |
| 0x219E | DSM_EQ_BQ6_A2_BY TE1[7:0] | | | | | | | DSM_EQ_BQ6_A2[15:8] |
| 0x219F | DSM_EQ_BQ6_A2_BY TE2[7:0] | | | | | | | DSM_EQ_BQ6_A2[23:16] |
| DSM EQ BIQUAD 7 | | | | | | | | |
| 0x21A1 | DSM_EQ_BQ7_B0_BY TE0[7:0] | | | | | | | DSM_EQ_BQ7_B0[7:0] |
| 0x21A2 | DSM_EQ_BQ7_B0_BY TE1[7:0] | | | | | | | DSM_EQ_BQ7_B0[15:8] |
| 0x21A3 | DSM_EQ_BQ7_B0_BY TE2[7:0] | | | | | | | DSM_EQ_BQ7_B0[23:16] |
| 0x21A5 | DSM_EQ_BQ7_B1_BY TE0[7:0] | | | | | | | DSM_EQ_BQ7_B1[7:0] |
| 0x21A6 | DSM_EQ_BQ7_B1_BY TE1[7:0] | | | | | | | DSM_EQ_BQ7_B1[15:8] |
| 0x21A7 | DSM_EQ_BQ7_B1_BY TE2[7:0] | | | | | | | DSM_EQ_BQ7_B1[23:16] |
| 0x21A9 | DSM_EQ_BQ7_B2_BY TE0[7:0] | | | | | | | DSM_EQ_BQ7_B2[7:0] |
| 0x21AA | DSM_EQ_BQ7_B2_BY TE1[7:0] | | | | | | | DSM_EQ_BQ7_B2[15:8] |
| 0x21AB | DSM_EQ_BQ7_B2_BY TE2[7:0] | | | | | | | DSM_EQ_BQ7_B2[23:16] |
| 0x21AD | DSM_EQ_BQ7_A1_BY TE0[7:0] | | | | | | | DSM_EQ_BQ7_A1[7:0] |
| 0x21AE | DSM_EQ_BQ7_A1_BY TE1[7:0] | | | | | | | DSM_EQ_BQ7_A1[15:8] |
| 0x21AF | DSM_EQ_BQ7_A1_BY TE2[7:0] | | | | | | | DSM_EQ_BQ7_A1[23:16] |
| 0x21B1 | DSM_EQ_BQ7_A2_BY TE0[7:0] | | | | | | | DSM_EQ_BQ7_A2[7:0] |
| 0x21B2 | DSM_EQ_BQ7_A2_BY TE1[7:0] | | | | | | | DSM_EQ_BQ7_A2[15:8] |
| 0x21B3 | DSM_EQ_BQ7_A2_BY TE2[7:0] | | | | | | | DSM_EQ_BQ7_A2[23:16] |
| DSM EQ BIQUAD 8 | | | | | | | | |
| 0x21B5 | DSM_EQ_BQ8_B0_BY TE0[7:0] | | | | | | | DSM_EQ_BQ8_B0[7:0] |
| 0x21B6 | DSM_EQ_BQ8_B0_BY TE1[7:0] | | | | | | | DSM_EQ_BQ8_B0[15:8] |
| 0x21B7 | DSM_EQ_BQ8_B0_BY TE2[7:0] | | | | | | | DSM_EQ_BQ8_B0[23:16] |
| 0x21B9 | DSM_EQ_BQ8_B1_BY TE0[7:0] | | | | | | | DSM_EQ_BQ8_B1[7:0] |

| ADDRESS | NAME | MSB | | | | | | | LSB |
|-------------------------------|---|----------------------|---|----------------------|--------------------|---------------------|---|---|----------------|
| 0x21BA | DSM_EQ_BQ8_B1_BY TE1[7:0] | DSM_EQ_BQ8_B1[15:8] | | | | | | | |
| 0x21BB | DSM_EQ_BQ8_B1_BY TE2[7:0] | DSM_EQ_BQ8_B1[23:16] | | | | | | | |
| 0x21BD | DSM_EQ_BQ8_B2_BY TE0[7:0] | DSM_EQ_BQ8_B2[7:0] | | | | | | | |
| 0x21BE | DSM_EQ_BQ8_B2_BY TE1[7:0] | DSM_EQ_BQ8_B2[15:8] | | | | | | | |
| 0x21BF | DSM_EQ_BQ8_B2_BY TE2[7:0] | DSM_EQ_BQ8_B2[23:16] | | | | | | | |
| 0x21C1 | DSM_EQ_BQ8_A1_BY TE0[7:0] | DSM_EQ_BQ8_A1[7:0] | | | | | | | |
| 0x21C2 | DSM_EQ_BQ8_A1_BY TE1[7:0] | DSM_EQ_BQ8_A1[15:8] | | | | | | | |
| 0x21C3 | DSM_EQ_BQ8_A1_BY TE2[7:0] | DSM_EQ_BQ8_A1[23:16] | | | | | | | |
| 0x21C5 | DSM_EQ_BQ8_A2_BY TE0[7:0] | DSM_EQ_BQ8_A2[7:0] | | | | | | | |
| 0x21C6 | DSM_EQ_BQ8_A2_BY TE1[7:0] | DSM_EQ_BQ8_A2[15:8] | | | | | | | |
| 0x21C7 | DSM_EQ_BQ8_A2_BY TE2[7:0] | DSM_EQ_BQ8_A2[23:16] | | | | | | | |
| DSM DRC | | | | | | | | | |
| 0x2380 | DSMIG WB DRC RELEASE TIME 1[7:0] | DRC_RLS[15:8] | | | | | | | |
| 0x2381 | DSMIG WB DRC RELEASE TIME 2[7:0] | DRC_RLS[7:0] | | | | | | | |
| 0x2382 | DSMIG WB DRC ATTACK TIME 1[7:0] | DRC_ATK[15:8] | | | | | | | |
| 0x2383 | DSMIG WB DRC ATTACK TIME 2[7:0] | DRC_ATK[7:0] | | | | | | | |
| 0x2384 | DSMIG WB DRC COMPRESSION RATIO[7:0] | - | - | - | - | DRC_COMP_RATIO[3:0] | | | |
| 0x2385 | DSMIG WB DRC COMPRESSION THRESHOLD[7:0] | - | - | DRC_COMP_THRESH[5:0] | | | | | |
| 0x2386 | DSMIG WB DRC MAKEUPGAIN[7:0] | - | - | - | - | DRC_MAKEUPGAIN[3:0] | | | |
| 0x2387 | DSMIG WB DRC NOISE GATE THRESHOLD[7:0] | - | - | - | DRC_NG_THRESH[4:0] | | | | |
| 0x2388 | DSMIG WBDRC HPF ENABLE[7:0] | - | - | - | - | - | - | - | DRC_HP F_EN |
| DSM PPR | | | | | | | | | |
| 0x238B | DSMIG PPR THRESHOLD[7:0] | - | - | PPR_THRESH[5:0] | | | | | |
| DSM THERMAL PROTECTION | | | | | | | | | |

| ADDRESS | NAME | MSB | | | | | | LSB |
|---------------------------------|---|---------------------------------|----------------------------|---------------------------|---|---------------------------|--------------------------|-----|
| 0x238E | DSM TPROT THRESHOLD BYTE 0[7:0] | DSM_TPROT_TEMP_THRESH[7:0] | | | | | | |
| 0x238F | DSM TPROT THRESHOLD BYTE 1[7:0] | DSM_TPROT_TEMP_THRESH[15:8] | | | | | | |
| 0x2390 | DSM TPROT ROOM TEMPERATURE BYTE0[7:0] | DSM_TPROT_ROOM_TEMP[7:0] | | | | | | |
| 0x2391 | DSM TPROT ROOM TEMPERATURE BYTE 1[7:0] | DSM_TPROT_ROOM_TEMP[15:8] | | | | | | |
| 0x2392 | DSM TPROT RECIP RDC ROOM BYTE0[7:0] | DSM_TPROT_RECIP_RDC_ROOM[7:0] | | | | | | |
| 0x2393 | DSM TPROT RECIP RDC ROOM BYTE1[7:0] | DSM_TPROT_RECIP_RDC_ROOM[15:8] | | | | | | |
| 0x2394 | DSM TPROT RECIP RDC ROOM BYTE2[7:0] | DSM_TPROT_RECIP_RDC_ROOM[23:16] | | | | | | |
| 0x2395 | DSM TPROT RECIP TCONST BYTE0[7:0] | DSM_TPROT_RECIP_TCONST[7:0] | | | | | | |
| 0x2396 | DSM TPROT RECIP TCONST BYTE1[7:0] | DSM_TPROT_RECIP_TCONST[15:8] | | | | | | |
| 0x2397 | DSM TPROT RECIP TCONST BYTE2[7:0] | DSM_TPROT_RECIP_TCONST[23:16] | | | | | | |
| 0x2398 | DSM TPROT ATTENUATION SETTINGS[7:0] | - | - | - | - | DSM_TPROT_ATTEN_SKIP[1:0] | DSM_TPROT_MAX_ATTEN[1:0] | |
| 0x239A | DSM TPROT PG TEMP THRESH BYTE0[7:0] | DSM_TPROT_PG_TEMP_THRESH[7:0] | | | | | | |
| 0x239B | DSM TPROT PG TEMP THRESH BYTE1[7:0] | DSM_TPROT_PG_TEMP_THRESH[15:8] | | | | | | |
| 0x239C | THERMAL RESISTANCE RD BACK BYTE1[7:0] | - | - | THERMAL_RDC_RD_BACK[13:8] | | | | |
| 0x239D | THERMAL RESISTANCE RD BACK BYTE0[7:0] | THERMAL_RDC_RD_BACK[7:0] | | | | | | |
| DSM EXCURSION PROTECTION | | | | | | | | |
| 0x23A4 | DSMIG EXCURSION PROTECTION RELEASE TIME BYTE 0[7:0] | EXCURSION_PROT_RLS[7:0] | | | | | | |
| 0x23A5 | DSMIG EXCURSION PROTECTION RELEASE TIME BYTE 1[7:0] | EXCURSION_PROT_RLS[15:8] | | | | | | |
| 0x23A6 | DSMIG EXCURSION | - | EXCURSION_PROT_THRESH[6:0] | | | | | |

| ADDRESS | NAME | MSB | | | | | | | LSB |
|---------------------------|--|----------------------------------|----------|-----------------|-------------|-------------------|----------------------|----------------------|-----------------|
| | PROTECTION THRESHOLD[7:0] | | | | | | | | |
| 0x23A7 | DSMIG EXCURSION PROTECTION DELAY BUFFER[7:0] | EXCURSION_PROT_DELAY_BUFFER[7:0] | | | | | | | |
| DSM DEBUZZER | | | | | | | | | |
| 0x23B5 | DSMIG DEBUZZER THRESHOLD[7:0] | - | - | DBZ_THRESH[5:0] | | | | | |
| DSM VOLUME CONTROL | | | | | | | | | |
| 0x23B9 | DSM VOL ENA[7:0] | DSM_VOL_RAMP_TIME[2:0] | | - | - | - | DSM_VOL_RAM_P_DN_BYP | DSM_VOL_RAM_P_UP_BYP | |
| 0x23BA | DSM_VOL_CTRL[7:0] | DSM_VOL_CTRL[7:0] | | | | | | | |
| DSM ENABLES | | | | | | | | | |
| 0x23E0 | DSMIG ENABLES[7:0] | STEREO_BASS_EN | WBDRC_EN | EQ8_EN | BASS_EXT_EN | EXCURSION_PROT_EN | PPR_EN | DEBUZZER_EN | THERMAL_PROT_EN |
| 0x23E1 | DSP GLOBAL ENABLE[7:0] | - | - | - | - | - | - | - | DSP_GLOBAL_EN |
| DSM GAIN RESULTS | | | | | | | | | |
| 0x23F0 | DSM_THERMAL_GAIN[7:0] | DSM_THERMAL_GAIN[7:0] | | | | | | | |
| 0x23F1 | DSM_PPR_GAIN[7:0] | DSM_PPR_GAIN[7:0] | | | | | | | |
| 0x23F2 | DSM_DBZ_GAIN[7:0] | DSM_DBZ_GAIN[7:0] | | | | | | | |
| 0x23F3 | DSM_WBDRC_GAIN[7:0] | DSM_WBDRC_GAIN[7:0] | | | | | | | |
| GLOBAL ENABLE | | | | | | | | | |
| 0x23FF | GLOBAL_ENABLE[7:0] | - | - | - | - | - | - | - | EN |
| ID READBACK | | | | | | | | | |
| 0x24FF | REV_ID[7:0] | REV_ID[7:0] | | | | | | | |

Register Details

SOFTWARE RESET (0x2000)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|---|---|------------|
| Field | - | - | - | - | - | - | - | RST |
| Reset | - | - | - | - | - | - | - | 0b0 |
| Access Type | - | - | - | - | - | - | - | Write Only |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--|
| RST | 0 | Triggers a momentary power-on reset to the device. After software reset, no further action is required to release the reset. This is a write-only register field. It is immediately | 0: No action 1: Resets register map to POR (default) values |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--------|
| | | cleared to zero after writing. Writing a 1 to RST resets all I ² C registers to their default values. Writing a 0 to RST has no effect. RST always reads back 0. | |

INTERRUPT RAW 1 (0x2002)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|----------------------|--------------------|----------------------|--------------------|------------|----------------------|--------------------|--------------------|
| Field | THERMSH DN_START_RAW | THERMSH DN_END_RAW | THERMWAR N_START_RAW | THERMWAR N_END_RAW | BDE_L4_RAW | BDE_LEVEL_CHANGE_RAW | BDE_ACTIVE_BGN_RAW | BDE_ACTIVE_END_RAW |
| Reset | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------------|------|---|--|
| THERMSHD N_START_RAW | 7 | Raw value of thermal-shutdown begin indicator. | 0: Die temperature below thermal-shutdown limit 1: Die temperature above thermal-shutdown limit |
| THERMSHD N_END_RAW | 6 | Raw value of thermal-shutdown end indicator. | 0: Die temperature above thermal-shutdown limit 1: Die temperature below thermal-shutdown limit |
| THERMWAR N_START_RAW | 5 | Raw value of thermal-warning begin indicator. | 0: Die temperature below thermal-warning limit 1: Die temperature above thermal-warning limit |
| THERMWAR N_END_RAW | 4 | Raw value of thermal-warning end indicator. | 0: Die temperature above thermal-warning limit 1: Die temperature below thermal-warning limit |
| BDE_L4_RAW | 3 | High when the BDE controller has entered level 4. | 0: Brownout controller not in level 4 1: Brownout controller in level 4 |
| BDE_LEVEL_CHANGE_RAW | 2 | Pulses high when BDE moves from one level to another. | 0: BDE level is static 1: BDE level is changing |
| BDE_ACTIVE_BGN_RAW | 1 | High when the BDE is active and is no longer in the normal state. | 0: Brownout-detection engine inactive BDE_STATE = 0 1: Brownout-detection engine active BDE_STATE > 0 |
| BDE_ACTIVE_END_RAW | 0 | High when the BDE is not active and is in the normal state. | 0: Brownout detection engine active BDE_STATE > 0 1: Brownout detection engine inactive BDE_STATE = 0 |

INTERRUPT RAW 2 (0x2003)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|--------------|-------------|----------------|----------------|----------------|------------------|-------------------|-------------------|
| Field | BST_UVLO_RAW | SPK_OVC_RAW | PWRUP_FAIL_RAW | PWRUP_DONE_RAW | PWRDN_DONE_RAW | BOOSTCURRLIM_RAW | WATCHDOG_FAIL_RAW | WATCHDOG_WARN_RAW |
| Reset | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------------|------|--|---|
| BST_UVLO_RAW | 7 | Raw value of boost undervoltage lockout. | 0: Boost voltage above UVLO threshold 1: Boost voltage below UVLO threshold |
| SPK_OVC_RAW | 6 | Raw value of speaker overcurrent limit. | 0: Speaker overcurrent limit inactive 1: Speaker overcurrent limit active |
| PWRUP_FAIL_RAW | 5 | Raw value of power-up fail. | 0: No power-up failure 1: Device has failed to completed power-up routine after setting EN = 1. Check measurement ADC temperature setup. |
| PWRUP_DONE_RAW | 4 | Raw value of power-up done. | 0: Device is not powered-up 1: Device has completed power-up routine after setting EN = 1 |
| PWRDN_DONE_RAW | 3 | Raw value of power-down done. | 0: Device is not powered-down 1: Device has completed power-down sequence after setting EN = 0 |
| BOOSTCURRENT_LIMIT_RAW | 2 | Raw value of boost current limit. | 0: Boost current limit inactive 1: Boost current limit active |
| WATCHDOG_FAIL_RAW | 1 | Raw value of watchdog timer expiry. | 0: Watchdog timer has not passed timeout threshold since last reset 1: Watchdog timer has passed timeout threshold since last reset |
| WATCHDOG_WARN_RAW | 0 | Raw value of watchdog timer warning. | 0: Watchdog timer has not passed threshold since last reset 1: Watchdog timer has passed threshold since last reset |

INTERRUPT RAW 3 (0x2004)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|----------------|-------------------|-----------------|------------------------|----------------------|-----------------------|---------------------|
| Field | – | DMON_ERROR_RAW | FRAME_RECOVER_RAW | FRAME_ERROR_RAW | LRCLK_RATE_RECOVER_RAW | LRCLK_RATE_ERROR_RAW | BCLK_RATE_RECOVER_RAW | BCLK_RATE_ERROR_RAW |
| Reset | – | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | – | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------------|------|-----------------------------------|--|
| DMON_ERR_RAW | 6 | Raw value of data monitor error. | 0: No Dmon error since last reset 1: Dmon error since last reset |
| FRAME_RECOVER_RAW | 5 | Raw value of PCM frame recovered. | 0: PCM frame has not recovered since last reset 1: PCM frame has recovered since last reset |
| FRAME_ERROR_RAW | 4 | Raw value of PCM frame error. | 0: PCM frame has not failed since last reset 1: PCM frame has failed since last reset |
| LRCLK_RATE_RECOVER_RAW | 3 | Raw value of LRCLK recovered. | 0: LRCLK rate has not recovered since last reset 1: LRCLK rate has recovered since last reset |
| LRCLK_RATE_ERROR_RAW | 2 | Raw value of LRCLK error. | 0: LRCLK rate has not failed since last reset 1: LRCLK rate has failed since last reset |
| BCLK_RATE_RECOVER_RAW | 1 | Raw value of BCLK recovered. | 0: BCLK rate has not recovered since last reset 1: BCLK rate has recovered since last reset |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------------|------|--------------------------|--|
| BCLK_RATE_ERR_RAW | 0 | Raw value of BCLK error. | 0: BCLK rate has not failed since last reset 1: BCLK rate has failed since last reset |

INTERRUPT STATE 1 (0x2005)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------------|---------------------|------------------------|----------------------|--------------|------------------------|----------------------|----------------------|
| Field | THERMSHDN_START_STATE | THERMSHDN_END_STATE | THERMWARNS_START_STATE | THERMWARNS_END_STATE | BDE_L4_STATE | BDE_LEVEL_CHANGE_STATE | BDE_ACTIVE_BGN_STATE | BDE_ACTIVE_END_STATE |
| Reset | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------------|------|--|---|
| THERMSHDN_START_STATE | 7 | Thermal shutdown begin unmaskable interrupt state. Cleared by THERMSHDN_START_CLR. | 0: No rising edge of THERMSHDN_START_RAW since last THERMSHDN_START_CLR 1: Rising edge of THERMSHDN_START_RAW since last THERMSHDN_START_CLR |
| THERMSHDN_END_STATE | 6 | Thermal shutdown end unmaskable interrupt state. Cleared by THERMSHDN_END_CLR. | 0: No rising edge of THERMSHDN_END_RAW since last THERMSHDN_END_CLR 1: Rising edge of THERMSHDN_END_RAW since last THERMSHDN_END_CLR |
| THERMWARNS_START_STATE | 5 | Thermal warning begin unmaskable interrupt state. Cleared by THERMWARNS_START_CLR. | 0: No rising edge of THERMWARNS_START_RAW since last THERMWARNS_START_CLR 1: Rising edge of THERMWARNS_START_RAW since last THERMWARNS_START_CLR |
| THERMWARNS_END_STATE | 4 | Thermal warning end unmaskable interrupt state. Cleared by THERMWARNS_END_CLR. | 0: No rising edge of THERMWARNS_END_RAW since last THERMWARNS_END_CLR 1: Rising edge of THERMWARNS_END_RAW since last THERMWARNS_END_CLR |
| BDE_L4_STATE | 3 | Brownout-detection engine level 4 entered unmaskable interrupt state. Cleared by BDE_L4_CLR. | 0: No rising edge of BDE_L4_RAW since last BDE_L4_CLR 1: Rising edge of BDE_L4_RAW since last BDE_L4_CLR |
| BDE_LEVEL_CHANGE_STATE | 2 | Brownout-detection engine level change unmaskable interrupt state. Cleared by BDE_LEVEL_CLR. | 0: No rising edge of BDE_LEVEL_RAW since last BDE_LEVEL_CLR 1: Rising edge of BDE_LEVEL_RAW since last BDE_LEVEL_CLR |
| BDE_ACTIVE_BGN_STATE | 1 | Brownout-detection engine active begin state. Cleared by BDE_ACTIVE_BGN_CLR. | 0: No rising edge of BDE_ACTIVE_BGN_RAW since last BDE_ACTIVE_BGN_CLR 1: Rising edge of BDE_ACTIVE_BGN_RAW since last BDE_ACTIVE_BGN_CLR |
| BDE_ACTIVE_END_STATE | 0 | Brownout-detection engine active end state. Cleared by BDE_ACTIVE_END_CLR. | 0: No rising edge of BDE_ACTIVE_RAW since last BDE_ACTIVE_END_CLR 1: Rising edge of BDE_ACTIVE_END_RAW since last BDE_ACTIVE_END_CLR |

INTERRUPT STATE 2 (0x2006)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------|---------------|------------------|------------------|------------------|--------------------|---------------------|---------------------|
| Field | BST_UVLO_STATE | SPK_OVC_STATE | PWRUP_FAIL_STATE | PWRUP_DONE_STATE | PWRDN_DONE_STATE | BOOSTCURRLIM_STATE | WATCHDOG_FAIL_STATE | WATCHDOG_WARN_STATE |
| Reset | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------------|------|---|---|
| BST_UVLO_STATE | 7 | Boost undervoltage lockout unmaskable interrupt state. Cleared by BST_UVLO_CLR. | 0: No rising edge of BST_UVLO_RAW since last BST_UVLO_CLR 1: Rising edge of BST_UVLO_RAW since last BST_UVLO_CLR |
| SPK_OVC_STATE | 6 | Speaker overcurrent limit unmaskable interrupt state. Cleared by SPK_OVC_CLR. | 0: No rising edge of SPK_OVC_RAW since last SPK_OVC_CLR 1: Rising edge of SPK_OVC_RAW since last SPK_OVC_CLR |
| PWRUP_FAIL_STATE | 5 | Power-up fail unmaskable interrupt state. Cleared by PWRUP_FAIL_CLR. | 0: No rising edge of PWRUP_FAIL_RAW since last PWRUP_FAIL_CLR 1: Rising edge of PWRUP_FAIL_RAW since last PWRUP_FAIL_CLR |
| PWRUP_DONE_STATE | 4 | Power-up done unmaskable interrupt state. Cleared by PWRUP_DONE_CLR. | 0: No rising edge of PWRUP_DONE_RAW since last PWRUP_DONE_CLR 1: Rising edge of PWRUP_DONE_RAW since last PWRUP_DONE_CLR |
| PWRDN_DONE_STATE | 3 | Power-down done unmaskable interrupt state. Cleared by PWRDN_DONE_CLR. | 0: No rising edge of PWRDN_DONE_RAW since last PWRDN_DONE_CLR 1: Rising edge of PWRDN_DONE_RAW since last PWRDN_DONE_CLR |
| BOOSTCURRLIM_STATE | 2 | Boost current limit unmaskable interrupt state. Cleared by BSTILIM_CLR. | 0: No rising edge of BSTILIM_RAW since last BSTILIM_CLR 1: Rising edge of BSTILIM_RAW since last BSTILIM_CLR |
| WATCHDOG_FAIL_STATE | 1 | Watchdog timer expiry unmaskable interrupt state. Cleared by WATCHFAIL_CLR. | 0: No rising edge of WATCHFAIL_RAW since last WATCHFAIL_CLR 1: Rising edge of WATCHFAIL_RAW since last WATCHFAIL_CLR |
| WATCHDOG_WARN_STATE | 0 | Watchdog timer warning unmaskable interrupt state. Cleared by WATCHWARN_CLR. | 0: No rising edge of WATCHWARN_RAW since last WATCHWARN_CLR 1: Rising edge of WATCHWARN_RAW since last WATCHWARN_CLR |

INTERRUPT STATE 3 (0x2007)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|----------------|-----------------|-----------------|----------------------|----------------------|---------------------|---------------------|
| Field | – | DMON_ERR_STATE | FRAME_REC_STATE | FRAME_ERR_STATE | LRCLK_RATE_REC_STATE | LRCLK_RATE_ERR_STATE | BCLK_RATE_REC_STATE | BCLK_RATE_ERR_STATE |
| Reset | – | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | – | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------------|------|--|---|
| DMON_ERR_STATE | 6 | DMON error unmaskable interrupt state. Cleared by DMON_ERR_CLR. | 0: No rising edge of DMON_ERR_RAW since last DMON_ERR_CLR 1: Rising edge of DMON_ERR_RAW since last DMON_ERR_CLR |
| FRAME_REC_STATE | 5 | PCM frame recovered unmaskable interrupt state. Cleared by FRAME_REC_CLR. | 0: No rising edge of FRAME_REC_RAW since last FRAME_REC_CLR 1: Rising edge of FRAME_REC_RAW since last FRAME_REC_CLR |
| FRAME_ERR_STATE | 4 | PCM frame error unmaskable interrupt state. Cleared by FRAME_ERR_CLR. | 0: No rising edge of FRAME_ERR_RAW since last FRAME_ERR_CLR 1: Rising edge of FRAME_ERR_RAW since last FRAME_ERR_CLR |
| LRCLK_RATE_REC_STATE | 3 | LRCLK frequency recovered unmaskable interrupt state. Cleared by LRCLK_RATE_REC_CLR. | 0: No rising edge of LRCLK_RATE_REC_RAW since last LRCLK_RATE_REC_CLR 1: Rising edge of LRCLK_RATE_REC_RAW since last LRCLK_RATE_REC_CLR |
| LRCLK_RATE_ERR_STATE | 2 | LRCLK frequency error unmaskable interrupt state. Cleared by LRCLK_RATE_ERR_CLR. | 0: No rising edge of LRCLK_RATE_ERR_RAW since last LRCLK_RATE_ERR_CLR 1: Rising edge of LRCLK_RATE_ERR_RAW since last LRCLK_RATE_ERR_CLR |
| BCLK_RATE_REC_STATE | 1 | BCLK frequency recovered unmaskable interrupt state. Cleared by BCLK_RATE_REC_CLR. | 0: No rising edge of BCLK_RATE_REC_RAW since last BCLK_RATE_REC_CLR 1: Rising edge of BCLK_RATE_REC_RAW since last BCLK_RATE_REC_CLR |
| BCLK_RATE_ERR_STATE | 0 | BCLK frequency error unmaskable interrupt state. Cleared by BCLK_RATE_ERR_CLR. | 0: No rising edge of BCLK_RATE_ERR_RAW since last BCLK_RATE_ERR_CLR 1: Rising edge of BCLK_RATE_ERR_RAW since last BCLK_RATE_ERR_CLR |

INTERRUPT FLAG 1 (0x2008)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|--------------------|----------------------|--------------------|-------------|-----------------------|---------------------|---------------------|
| Field | THERMSHDN_START_FLAG | THERMSHDN_END_FLAG | THERMWARN_START_FLAG | THERMWARN_END_FLAG | BDE_L4_FLAG | BDE_LEVEL_CHANGE_FLAG | BDE_ACTIVE_BGN_FLAG | BDE_ACTIVE_END_FLAG |
| Reset | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------------|------|--|--|
| THERMSHDN_START_FLAG | 7 | Thermal shutdown begin maskable interrupt flag. Masked by THERMSHDN_START_EN and cleared by THERMSHDN_START_CLR. | 0: No rising edge of THERMSHDN_START_RAW since last THERMSHDN_START_CLR or THERMSHDN_START_EN is low 1: THERMSHDN_START_EN high and rising edge of THERMSHDN_START_RAW since last THERMSHDN_START_CLR |
| THERMSHDN_END_FLAG | 6 | Thermal shutdown end maskable interrupt flag. Masked by THERMSHDN_END_EN and cleared by THERMSHDN_END_CLR. | 0: No rising edge of THERMSHDN_END_RAW since last THERMSHDN_END_CLR or THERMSHDN_END_EN is low 1: THERMSHDN_END_EN high and rising edge of THERMSHDN_END_RAW since last THERMSHDN_END_CLR |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------------------------|------|--|--|
| THERMWAR N_START_F LAG | 5 | Thermal warning begin maskable interrupt flag. Masked by THERMWARN_START_EN and cleared by THERMWARN_START_CLR. | 0: No rising edge of THERMWARN_START_RAW since last THERMWARN_START_CLR or THERMWARN_START_EN is low 1: THERMWARN_BGN_EN high and rising edge of THERMWARN_START_RAW since last THERMWARN_START_CLR |
| THERMWAR N_END_FLA G | 4 | Thermal warning end maskable interrupt flag. Masked by THERMWARN_END_EN and cleared by THERMWARN_END_CLR. | 0: No rising edge of THERMWARN_END_RAW since last THERMWARN_END_CLR or THERMWARN_END_EN is low 1: THERMWARN_END_EN high and rising edge of THERMWARN_END_RAW since last THERMWARN_END_CLR |
| BDE_L4_FL AG | 3 | Brownout-detection engine level 4 entered maskable interrupt flag. Masked by BDE_L4_EN and cleared by BDE_L4_CLR. | 0: No rising edge of BDE_L4_RAW since last BDE_L4_CLR or BDE_L4_EN is low 1: BDE_L4_EN high and rising edge of BDE_L4_RAW since last BDE_L4_CLR |
| BDE_LEVEL _CHANGE_F LAG | 2 | Brownout-detection engine level change maskable interrupt flag. Masked by BDE_LEVEL_EN and cleared by BDE_LEVEL_CLR. | 0: No rising edge of BDE_LEVEL_RAW since last BDE_LEVEL_CLR or BDE_LEVEL_EN is low 1: BDE_LEVEL_EN high and rising edge of BDE_LEVEL_RAW since last BDE_LEVEL_CLR |
| BDE_ACTIV E_BGN_FLA G | 1 | Brownout-detection engine active begin maskable interrupt flag. Masked by BDE_ACTIVE_BGN_EN and cleared by BDE_ACTIVE_BGN_CLR. | 0: No rising edge of BDE_ACTIVE_BGN_RAW since last BDE_ACTIVE_BGN_CLR or BDEACTIVE_BGN_EN is low 1: BDE_ACTIVE_BGN_EN high and rising edge of BDE_ACTIVE_BGN_RAW since last BDE_ACTIVE_BGN_CLR |
| BDE_ACTIV E_END_FLA G | 0 | Brownout-detection engine active end maskable interrupt flag. Masked by BDE_ACTIVE_END_EN and cleared by BDE_ACTIVE_END_CLR. | 0: No rising edge of BDE_ACTIVE_END_RAW since last BDE_ACTIVE_END_CLR or BDE_ACTIVE_END_EN is low 1: BDE_ACTIVE_END_EN high and rising edge of BDE_ACTIVE_END_RAW since last BDE_ACTIVE_END_CLR |

INTERRUPT FLAG 2 (0x2009)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|---------------|--------------|-----------------|-----------------|-----------------|----------------------|--------------------|--------------------|
| Field | BST_UVLO_FLAG | SPK_OVC_FLAG | PWRUP_FAIL_FLAG | PWRUP_DOWN_FLAG | PWRDN_DOWN_FLAG | BOOSTCURRENTRIM_FLAG | WATCHDOG_FAIL_FLAG | WATCHDOG_WARN_FLAG |
| Reset | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------|------|--|--|
| BST_UVLO_FLAG | 7 | Boost undervoltage lockout maskable interrupt flag. Masked by BST_UVLO_EN and cleared by BST_UVLO_CLR. | 0: No rising edge of BST_UVLO_RAW since last BST_UVLO_CLR or BST_UVLO_EN is low 1: BST_UVLO_EN high and rising edge of BST_UVLO_RAW since last BST_UVLO_CLR |
| SPK_OVC_FLAG | 6 | Speaker overcurrent limit maskable interrupt flag. Masked by SPK_OVC_EN and cleared by SPK_OVC_CLR. | 0: No rising edge of SPK_OVC_RAW since last SPK_OVC_CLR or SPK_OVC_EN is low 1: SPK_OVC_EN high and rising edge of SPK_OVC_RAW since last SPK_OVC_CLR |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------------|------|--|--|
| PWRUP_FAIL_FLAG | 5 | Power-up fail maskable interrupt flag. Masked by PWRUP_FAIL_EN and cleared by PWRUP_FAIL_CLR. | 0: No rising edge of PWRUP_FAIL_RAW since last PWRUP_FAIL_CLR or PWRUP_FAIL_EN is low 1: PWRUP_FAIL_EN high and rising edge of PWRUP_FAIL_RAW since last PWRUP_FAIL_CLR |
| PWRUP_DONE_FLAG | 4 | Power-up done maskable interrupt flag. Masked by PWRUP_DONE_EN and cleared by PWRUP_DONE_CLR. | 0: No rising edge of PWRUP_DONE_RAW since last PWRUP_DONE_CLR or PWRUP_DONE_EN is low 1: PWRUP_DONE_EN high and rising edge of PWRUP_DONE_RAW since last PWRUP_DONE_CLR |
| PWRDN_DONE_FLAG | 3 | Power-down done maskable interrupt flag. Masked by PWRDN_DONE_EN and cleared by PWRDN_DONE_CLR. | 0: No rising edge of PWRDN_DONE_RAW since last PWRDN_DONE_CLR or PWRDN_DONE_EN is low 1: PWRDN_DONE_EN high and rising edge of PWRDN_DONE_RAW since last PWRDN_DONE_CLR |
| BOOSTCURLIM_FLAG | 2 | Boost current limit maskable interrupt flag. Masked by BSTILIM_EN and cleared by BSTILIM_CLR. | 0: No rising edge of BSTILIM_RAW since last BSTILIM_CLR or BSTILIM_EN is low 1: BSTILIM_EN high and rising edge of BSTILIM_RAW since last BSTILIM_CLR |
| WATCHDOG_FAIL_FLAG | 1 | Watchdog timer expiry maskable interrupt flag. Masked by WATCHFAIL_EN and cleared by WATCHFAIL_CLR. | 0: No rising edge of WATCHFAIL_RAW since last WATCHFAIL_CLR or WATCHFAIL_EN is low 1: WATCHFAIL_EN high and rising edge of WATCHFAIL_RAW since last WATCHFAIL_CLR |
| WATCHDOG_WARN_FLAG | 0 | Watchdog timer warning maskable interrupt flag. Masked by WATCHWARN_EN and cleared by WATCHWARN_CLR. | 0: No rising edge of WATCHWARN_RAW since last WATCHWARN_CLR or WATCHWARN_EN is low 1: WATCHWARN_EN high and rising edge of WATCHWARN_RAW since last WATCHWARN_CLR |

INTERRUPT FLAG 3 (0x200A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---------------|----------------|----------------|---------------------|---------------------|--------------------|--------------------|
| Field | – | DMON_ERR_FLAG | FRAME_REC_FLAG | FRAME_ERR_FLAG | LRCLK_RATE_REC_FLAG | LRCLK_RATE_ERR_FLAG | BCLK_RATE_REC_FLAG | BCLK_RATE_ERR_FLAG |
| Reset | – | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | – | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------|------|---|--|
| DMON_ERR_FLAG | 6 | Data monitor error maskable interrupt flag. Masked by DMON_ERR_EN and cleared by DMON_ERR_CLR. | 0: No rising edge of DMON_ERR_RAW since last DMON_ERR_CLR or DMON_ERR_EN is low 1: DMON_ERR_EN high and rising edge of DMON_ERR_RAW since last DMON_ERR_CLR |
| FRAME_REC_FLAG | 5 | PCM frame recovered maskable interrupt flag. Masked by FRAME_ERR_EN and cleared by FRAME_ERR_CLR. | 0: No rising edge of FRAME_REC_RAW since last FRAME_REC_CLR or FRAME_REC_EN is low 1: FRAME_REC_EN high and rising edge of FRAME_REC_RAW since last FRAME_REC_CLR |
| FRAME_ERR | 4 | PCM frame error maskable interrupt flag. | 0: No rising edge of FRAME_ERR_RAW since last |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------------|------|---|--|
| R_FLAG | | Masked by FRAME_ERR_EN and cleared by FRAME_ERR_CLR. | FRAME_ERR_CLR or FRAME_ERR_EN is low 1: FRAME_ERR_EN high and rising edge of FRAME_ERR_RAW since last FRAME_ERR_CLR |
| LRCLK_RATE_REC_FLAG | 3 | LRCLK frequency recovered maskable interrupt flag. Masked by LRCLK_RATE_REC_EN and cleared by LRCLK_RATE_REC_CLR. | 0: No rising edge of LRCLK_RATE_REC_RAW since last LRCLK_RATE_REC_CLR or LRCLK_RATE_REC_EN is low 1: LRCLK_RATE_REC_EN high and rising edge of LRCLK_RATE_REC_RAW since last LRCLK_RATE_REC_CLR |
| LRCLK_RATE_ERR_FLAG | 2 | LRCLK frequency error maskable interrupt flag. Masked by LRCLK_RATE_ERR_EN and cleared by LRCLK_RATE_ERR_CLR. | 0: No rising edge of LRCLK_RATE_ERR_RAW since last LRCLK_RATE_ERR_CLR or LRCLK_RATE_ERR_EN is low 1: LRCLK_RATE_ERR_EN high and rising edge of LRCLK_RATE_ERR_RAW since last LRCLK_RATE_ERR_CLR |
| BCLK_RATE_REC_FLAG | 1 | BCLK frequency recovered maskable interrupt flag. Masked by BCLK_RATE_REC_EN and cleared by BCLK_RATE_REC_CLR. | 0: No rising edge of BCLK_RATE_REC_RAW since last BCLK_RATE_REC_CLR or BCLK_RATE_REC_EN is low 1: BCLK_RATE_REC_EN high and rising edge of BCLK_RATE_REC_RAW since last BCLK_RATE_REC_CLR |
| BCLK_RATE_ERR_FLAG | 0 | BCLK frequency error maskable interrupt flag. Masked by BCLK_RATE_ERR_EN and cleared by BCLK_RATE_ERR_CLR. | 0: No rising edge of BCLK_RATE_ERR_RAW since last BCLK_RATE_ERR_CLR or BCLK_RATE_ERR_EN is low 1: BCLK_RATE_ERR_EN high and rising edge of BCLK_RATE_ERR_RAW since last BCLK_RATE_ERR_CLR |

INTERRUPT ENABLE 1 (0x200B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|--------------------|------------------|---------------------|-------------------|-------------|---------------------|-------------------|-------------------|
| Field | THERMSHDN_START_EN | THERMSHDN_END_EN | THERMWARNS_START_EN | THERMWARNS_END_EN | BDE_L4_EN | BDE_LEVEL_CHANGE_EN | BDE_ACTIVE_BGN_EN | BDE_ACTIVE_END_EN |
| Reset | 0b1 | 0b1 | 0b1 | 0b1 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------------|------|--|--|
| THERMSHDN_START_EN | 7 | Enable (unmask) thermal shutdown begin flag. | 0: THERMSHDN_START_FLAG cannot go high 1: THERMSHDN_START_FLAG goes high if there is a rising edge on THERMSHDN_START_RAW since last THERMSHDN_START_CLR. |
| THERMSHDN_END_EN | 6 | Enable (unmask) thermal shutdown end flag. | 0: THERMSHDN_END_FLAG cannot go high 1: THERMSHDN_END_FLAG goes high if there is a rising edge on THERMSHDN_END_RAW since last THERMSHDN_END_CLR. |
| THERMWARNS_START_EN | 5 | Enable (unmask) thermal warning begin flag. | 0: THERMWARNS_START_FLAG cannot go high 1: THERMWARNS_START_FLAG goes high if there is a rising edge on THERMWARNS_START_RAW since last THERMWARNS_START_CLR. |
| THERMWARNS_END_EN | 4 | Enable (unmask) thermal warning end flag. | 0: THERMWARNS_END_FLAG cannot go high |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------------|------|---|--|
| N_END_EN | | | 1: THERMWARN_END_FLAG goes high if there is a rising edge on THERMWARN_END_RAW since last THERMWARN_END_CLR. |
| BDE_L4_EN | 3 | Enable (unmask) brownout-detection engine level 4 entered flag. | 0: BDE_L4_FLAG cannot go high 1: BDE_L4_FLAG goes high if there is a rising edge on BDE_L4_RAW since last BDE_L4_CLR. |
| BDE_LEVEL_CHANGE_EN | 2 | Enable (unmask) brownout-detection engine level change flag. | 0: BDE_LEVEL_FLAG cannot go high 1: BDE_LEVEL_FLAG goes high if there is a rising edge on BDE_LEVEL_RAW since last BDE_LEVEL_CLR. |
| BDE_ACTIVE_BGN_EN | 1 | Enable (unmask) brownout-detection engine active begin flag. | 0: BDE_ACTIVE_BGN_FLAG cannot go high 1: BDE_ACTIVE_BGN_FLAG goes high if there is a rising edge on BDE_ACTIVE_BGN_RAW since last BDE_ACTIVE_BGN_CLR. |
| BDE_ACTIVE_END_EN | 0 | Enable (unmask) brownout-detection engine active end flag. | 0: BDE_ACTIVE_END_FLAG cannot go high 1: BDE_ACTIVE_END_FLAG goes high if there is a rising edge on BDE_ACTIVE_END_RAW since last BDE_ACTIVE_END_CLR. |

INTERRUPT ENABLE 2 (0x200C)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|---------------|---------------|---------------|------------------|------------------|------------------|
| Field | BST_UVLO_EN | SPK_OVC_EN | PWRUP_FAIL_EN | PWRUP_DONE_EN | PWRDN_DONE_EN | BOOSTCURRELIM_EN | WATCHDOG_FAIL_EN | WATCHDOG_WARN_EN |
| Reset | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------|------|--|--|
| BST_UVLO_EN | 7 | Enable (unmask) boost undervoltage lockout flag. | 0: BST_UVLO_FLAG cannot go high 1: BST_UVLO_FLAG goes high if there is a rising edge on BST_UVLO_RAW since last BST_UVLO_CLR. |
| SPK_OVC_EN | 6 | Enable (unmask) speaker overcurrent limit flag. | 0: SPK_OVC_FLAG cannot go high 1: SPK_OVC_FLAG goes high if there is a rising edge on SPK_OVC_RAW since last SPK_OVC_CLR. |
| PWRUP_FAIL_EN | 5 | Enable (unmask) Power-up fail flag. | 0: PWRUP_FAIL_FLAG cannot go high 1: PWRUP_FAIL_FLAG goes high if there is a rising edge on PWRUP_FAIL_RAW since last PWRUP_FAIL_CLR. |
| PWRUP_DONE_EN | 4 | Enable (unmask) Power-up done flag. | 0: PWRUP_DONE_FLAG cannot go high 1: PWRUP_DONE_FLAG goes high if there is a rising edge on PWRUP_DONE_RAW since last PWRUP_DONE_CLR. |
| PWRDN_DONE_EN | 3 | Enable (unmask) Power-down done flag. | 0: PWRDN_DONE_FLAG cannot go high 1: PWRDN_DONE_FLAG goes high if there is a rising edge on PWRDN_DONE_RAW since last PWRDN_DONE_CLR. |
| BOOSTCURRELIM_EN | 2 | Enable (unmask) boost current limit flag. | 0: BSTILIM_FLAG cannot go high 1: BSTILIM_FLAG goes high if there is a rising |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------|------|--|--|
| | | | edge on BSTILIM_RAW since last BSTILIM_CLR. |
| WATCHDOG_FAIL_EN | 1 | Enable (unmask) watchdog timer expiry flag. | 0: WATCHFAIL_FLAG cannot go high 1: WATCHFAIL_FLAG goes high if there is a rising edge on WATCHFAIL_RAW since last WATCHFAIL_CLR. |
| WATCHDOG_WARN_EN | 0 | Enable (unmask) watchdog timer warning flag. | 0: WATCHWARN_FLAG cannot go high 1: WATCHWARN_FLAG goes high if there is a rising edge on WATCHWARN_RAW since last WATCHWARN_CLR. |

INTERRUPT ENABLE 3 (0x200D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|-------------|--------------|--------------|-------------------|-------------------|------------------|------------------|
| Field | – | DMON_ERR_EN | FRAME_REC_EN | FRAME_ERR_EN | LRCLK_RATE_REC_EN | LRCLK_RATE_ERR_EN | BCLK_RATE_REC_EN | BCLK_RATE_ERR_EN |
| Reset | – | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | – | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------------|------|---|--|
| DMON_ERR_EN | 6 | Enable (unmask) data monitor error flag. | 0: DMON_ERR_FLAG cannot go high 1: DMON_ERR_FLAG goes high if there is a rising edge on DMON_ERR_RAW since last DMON_ERR_CLR. |
| FRAME_REC_EN | 5 | Enable (unmask) PCM frame recovered flag. | 0: FRAME_REC_FLAG cannot go high 1: FRAME_REC_FLAG goes high if there is a rising edge on FRAME_REC_RAW since last FRAME_REC_CLR. |
| FRAME_ERR_EN | 4 | Enable (unmask) PCM frame error flag. | 0: FRAME_ERR_FLAG cannot go high 1: FRAME_ERR_FLAG goes high if there is a rising edge on FRAME_ERR_RAW since last FRAME_ERR_CLR. |
| LRCLK_RATE_REC_EN | 3 | Enable (unmask) LRCLK frequency recovered flag. | 0: LRCLK_RATE_REC_FLAG cannot go high 1: LRCLK_RATE_REC_FLAG goes high if there is a rising edge on LRCLK_RATE_REC_RAW since last LRCLK_RATE_REC_CLR. |
| LRCLK_RATE_ERR_EN | 2 | Enable (unmask) LRCLK frequency error flag. | 0: LRCLK_RATE_ERR_FLAG cannot go high 1: LRCLK_RATE_ERR_FLAG goes high if there is a rising edge on LRCLK_RATE_ERR_RAW since last LRCLK_RATE_ERR_CLR. |
| BCLK_RATE_REC_EN | 1 | Enable (unmask) BCLK frequency recovered flag. | 0: BCLK_RATE_REC_FLAG cannot go high 1: BCLK_RATE_REC_FLAG goes high if there is a rising edge on BCLK_RATE_REC_RAW since last BCLK_RATE_REC_CLR. |
| BCLK_RATE_ERR_EN | 0 | Enable (unmask) BCLK frequency error flag. | 0: BCLK_RATE_ERR_FLAG cannot go high 1: BCLK_RATE_ERR_FLAG goes high if there is a rising edge on BCLK_RATE_ERR_RAW since last BCLK_RATE_ERR_CLR. |

INTERRUPT FLAG CLEAR 1 (0x200E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|-------------------|---------------------|-------------------|------------|----------------------|--------------------|--------------------|
| Field | THERMSHDN_START_CLR | THERMSHDN_END_CLR | THERMWARN_START_CLR | THERMWARN_END_CLR | BDE_L4_CLR | BDE_LEVEL_CHANGE_CLR | BDE_ACTIVE_BGN_CLR | BDE_ACTIVE_END_CLR |
| Reset | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Write Only | Write Only | Write Only | Write Only | Write Only | Write Only | Write Only | Write Only |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------------|------|---|---|
| THERMSHDN_START_CLR | 7 | Thermal shutdown begin flag clear. | 0: Writing zero has no effect 1: Writing one clears THERMSHDN_START_STATE and THERMSHDN_START_FLAG to zero |
| THERMSHDN_END_CLR | 6 | Thermal shutdown end flag clear. | 0: Writing zero has no effect 1: Writing one clears THERMSHDN_END_STATE and THERMSHDN_END_FLAG to zero |
| THERMWARN_START_CLR | 5 | Thermal warning begin flag clear. | 0: Writing zero has no effect 1: Writing one clears THERMWARN_START_STATE and THERMWARN_START_FLAG to zero |
| THERMWARN_END_CLR | 4 | Thermal warning end flag clear. | 0: Writing zero has no effect 1: Writing one clears THERMWARN_END_STATE and THERMWARN_END_FLAG to zero |
| BDE_L4_CLR | 3 | Brownout-detection engine level 4 entered flag clear. | 0: Writing zero has no effect 1: Writing one clears BDE_L4_STATE and BDE_L4_FLAG to zero |
| BDE_LEVEL_CHANGE_CLR | 2 | Brownout-detection engine level change flag clear. | 0: Writing zero has no effect 1: Writing one clears BDE_LEVEL_STATE and BDE_LEVEL_FLAG to zero |
| BDE_ACTIVE_BGN_CLR | 1 | Brownout-detection engine active begin flag clear. | 0: Writing zero has no effect 1: Writing one clears BDE_ACTIVE_BGN_STATE and BDE_ACTIVE_BGN_FLAG to zero |
| BDE_ACTIVE_END_CLR | 0 | Brownout-detection engine active end flag clear. | 0: Writing zero has no effect 1: Writing one clears BDE_ACTIVE_END_STATE and BDE_ACTIVE_END_FLAG to zero |

INTERRUPT FLAG CLEAR 2 (0x200F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|-------------|----------------|----------------|----------------|------------------|-------------------|-------------------|
| Field | BST_UVLO_CLR | SPK_OVC_CLR | PWRUP_FAIL_CLR | PWRUP_DOWN_CLR | PWRDN_DOWN_CLR | BOOSTCURRLIM_CLR | WATCHDOG_FAIL_CLR | WATCHDOG_WARN_CLR |
| Reset | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Write Only | Write Only | Write Only | Write Only | Write Only | Write Only | Write Only | Write Only |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------|------|--|---|
| BST_UVLO_CLR | 7 | Boost undervoltage lockout flag clear. | 0: Writing zero has no effect 1: Writing one clears BST_UVLO_STATE and BST_UVLO_FLAG to zero |
| SPK_OVC_CLR | 6 | Speaker overcurrent limit flag clear. | 0: Writing zero has no effect |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------------|------|------------------------------------|---|
| LR | | | 1: Writing one clears SPK_OVC_STATE and SPK_OVC_FLAG to zero |
| PWRUP_FAIL_CLR | 5 | Power-up fail flag clear. | 0: Writing zero has no effect 1: Writing one clears PWRUP_FAIL_STATE and PWRUP_FAIL_FLAG to zero |
| PWRUP_DONE_CLR | 4 | Power-up done flag clear. | 0: Writing zero has no effect 1: Writing one clears PWRUP_DONE_STATE and PWRUP_DONE_FLAG to zero |
| PWRDN_DONE_CLR | 3 | Power-down done flag clear. | 0: Writing zero has no effect 1: Writing one clears PWRDN_DONE_STATE and PWRDN_DONE_FLAG to zero |
| BOOSTCURRENTLIMIT_CLR | 2 | Boost current limit flag clear. | 0: Writing zero has no effect 1: Writing one clears BSTILIM_STATE and BSTILIM_FLAG to zero |
| WATCHDOG_FAIL_CLR | 1 | Watchdog timer expiry flag clear. | 0: Writing zero has no effect 1: Writing one clears WATCHFAIL_STATE and WATCHFAIL_FLAG to zero |
| WATCHDOG_WARN_CLR | 0 | Watchdog timer warning flag clear. | 0: Writing zero has no effect 1: Writing one clears WATCHWARN_STATE and WATCHWARN_FLAG to zero |

INTERRUPT FLAG CLEAR 3 (0x2010)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|--------------|---------------|---------------|--------------------|--------------------|-------------------|-------------------|
| Field | – | DMON_ERR_CLR | FRAME_REC_CLR | FRAME_ERR_CLR | LRCLK_RATE_REC_CLR | LRCLK_RATE_ERR_CLR | BCLK_RATE_REC_CLR | BCLK_RATE_ERR_CLR |
| Reset | – | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | – | Write Only | Write Only | Write Only | Write Only | Write Only | Write Only | Write Only |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------------|------|---------------------------------------|---|
| DMON_ERR_CLR | 6 | Data monitor error flag clear. | 0: Writing zero has no effect 1: Writing one clears DMON_ERR_STATE and DMON_ERR_FLAG to zero |
| FRAME_REC_CLR | 5 | PCM frame recovered flag clear. | 0: Writing zero has no effect 1: Writing one clears FRAME_REC_STATE and FRAME_REC_FLAG to zero |
| FRAME_ERR_CLR | 4 | PCM frame error flag clear. | 0: Writing zero has no effect 1: Writing one clears FRAME_ERR_STATE and FRAME_ERR_FLAG to zero |
| LRCLK_RATE_REC_CLR | 3 | LRCLK frequency recovered flag clear. | 0: Writing zero has no effect 1: Writing one clears LRCLK_RATE_REC_STATE and LRCLK_RATE_REC_FLAG to zero |
| LRCLK_RATE_ERR_CLR | 2 | LRCLK frequency error flag clear. | 0: Writing zero has no effect 1: Writing one clears LRCLK_RATE_ERR_STATE and LRCLK_RATE_ERR_FLAG to zero |
| BCLK_RATE_REC_CLR | 1 | BCLK frequency recovered flag clear. | 0: Writing zero has no effect 1: Writing one clears BCLK_RATE_REC_STATE and BCLK_RATE_REC_FLAG to zero |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------------|------|----------------------------------|---|
| BCLK_RATE_ERR_CLR | 0 | BCLK frequency error flag clear. | 0: Writing zero has no effect 1: Writing one clears BCLK_RATE_ERR_STATE and BCLK_RATE_ERR_FLAG to zero |

IRQ CONTROL (0x2011)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|-------------|-------------|-------------|
| Field | – | – | – | – | – | IRQ_MODE | IRQ_POL | IRQ_EN |
| Reset | – | – | – | – | – | 0b0 | 0b0 | 0b1 |
| Access Type | – | – | – | – | – | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---------------------------------|--|
| IRQ_MODE | 2 | Controls the drive mode of IRQ. | 0: Open-drain. An external pullup resistor is necessary. 1: CMOS |
| IRQ_POL | 1 | Controls IRQ polarity. | 0: Low when any interrupt FLAG bits are high (i.e., active-low) 1: High when any interrupt FLAG bits are high (i.e., active-high) |
| IRQ_EN | 0 | Enables IRQ pin. | 0: Pin is disabled and high-impedance 1: Pin is enabled and is controlled by the interrupt controller |

CLOCK MONITOR CONTROL (0x2012)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|---|---|------------------|---|---|-----------------------------|-------------|
| Field | CMON_BSELTOL[2:0] | | | CMON_ERRTOL[2:0] | | | CMON_AU TORESTAR T_EN | CMON_EN |
| Reset | 0x3 | | | 0x3 | | | 0b0 | 0b1 |
| Access Type | Write, Read | | | Write, Read | | | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------|------|---|--|
| CMON_BSELTOL | 7:5 | The number of LRCLK frames of incorrect or correct BCLKs per LRCLK needed to trigger or recover from a clock monitor framing error. | 0x0: Trigger after 1 incorrect LRCLK frame, recover after 1 correct LRCLK frame 0x1: Trigger after 2 incorrect LRCLK frames, recover after 16 correct LRCLK frames 0x2: Trigger after 3 incorrect LRCLK frames, recover after 24 correct LRCLK frame 0x3: Trigger after 4 incorrect LRCLK frames, recover after 32 correct LRCLK frames 0x4: Trigger after 5 incorrect LRCLK frames, recover after 40 correct LRCLK frames 0x5: Trigger after 6 incorrect LRCLK frames, recover after 48 correct LRCLK frames 0x6: Trigger after 7 incorrect LRCLK frames, recover after 56 correct LRCLK frames 0x7: Trigger after 8 incorrect LRCLK frames, recover after 64 correct LRCLK frames |
| CMON_ERR | 4:2 | The number of of incorrect or correct LRCLK | 0x0: Trigger after 1 incorrect LRCLK frame, |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------------|------|---|--|
| TOL | | periods of incorrect clock rate needed to trigger or recover from a Clock Monitor rate error. | recover after 1 correct LRCLK frame 0x1: Trigger after 2 incorrect LRCLK frames, recover after 16 correct LRCLK frames 0x2: Trigger after 3 incorrect LRCLK frames, recover after 24 correct LRCLK frame 0x3: Trigger after 4 incorrect LRCLK frames, recover after 32 correct LRCLK frames 0x4: Trigger after 5 incorrect LRCLK frames, recover after 40 correct LRCLK frames 0x5: Trigger after 6 incorrect LRCLK frames, recover after 48 correct LRCLK frames 0x6: Trigger after 7 incorrect LRCLK frames, recover after 56 correct LRCLK frames 0x7: Trigger after 8 incorrect LRCLK frames, recover after 64 correct LRCLK frames |
| CMON_AUTORESTART_EN | 1 | Controls whether or not the device automatically resumes playback when the clock returns after stopping. | 0: Device does not automatically restart following a valid clock being reapplied. 1: Device automatically restarts following a valid clock being reapplied. |
| CMON_EN | 0 | Enables the clock monitor. Note that it is not valid to enable the clock monitor (CMON_EN = 1) while the PCM interface is in master mode (PCM_MSTR_MODE = 11). The clock monitor should only be used while in slave mode. | 0: Clock monitor disabled 1: Clock monitor enabled |

DATA MONITOR CONTROL (0x2014)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|-----------------------|---|--------------------|---|-------------|---------------|
| Field | DMON_MAG_THRES[1:0] | | DMON_STUCK_THRES[1:0] | | DMON_DURATION[1:0] | | DMON_MAG_EN | DMON_STUCK_EN |
| Reset | 0x0 | | 0x0 | | 0x0 | | 0x1 | 0x1 |
| Access Type | Write, Read | | Write, Read | | Write, Read | | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------|------|---|---|
| DMON_MAG_THRES | 7:6 | Sets an amplitude threshold which the input PCM amplitude level is compared against. If the input signal is above this threshold for longer than the DMON_DURATION, DMON_ERR is asserted. | 0x0: -30.1030dB (5 bits) 0x1: -24.0824dB (4 bits) 0x2: -18.0618dB (3 bits) 0x3: -12.0412dB (2 bits) |
| DMON_STUCK_THRES | 5:4 | Sets an amplitude threshold which the input PCM amplitude level is compared against. If the input signal is stuck at the same value above this threshold for longer than the DMON_DURATION, DMON_ERR is asserted. | 0x0: -90.3090dB (15 bits) 0x1: -78.2678dB (13 bits) 0x2: -66.2266dB (11 bits) 0x3: -54.1854dB (9 bits) |
| DMON_DURATION | 3:2 | Sets the time duration over which the data monitor must consecutively detect erroneous input PCM data before asserting DMON_ERR. | 0x0: 64ms 0x1: 256ms 0x2: 1024ms 0x3: 4096ms |
| DMON_MAG_EN | 1 | Enables the data monitor circuit to monitor PCM input data for large magnitude (DC) | 0x0: Data magnitude check disabled |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------|------|---|---|
| | | audio | 0x1: Data magnitude check enabled |
| DMON_STUCK_EN | 0 | Enables the data monitor circuit to monitor PCM input for stuck data. | 0: Data stuck-at monitor disabled 1: Data stuck-at monitor enabled |

WATCHDOG CONTROL (0x2015)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|-----------------|---|-------------|-------------|
| Field | – | – | – | – | WDT_TO_SEL[1:0] | | WDT_MODE | WDT_EN |
| Reset | – | – | – | – | 0b00 | | 0b0 | 0b0 |
| Access Type | – | – | – | – | Write, Read | | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------|------|---|---|
| WDT_TO_SEL | 3:2 | Sets the time allowed to pass between watchdog timer resets. If the duration is exceeded, the watchdog timer times out. | 00: 100ms software mode, 5ms hardware mode 01: 500ms software mode, 10ms hardware mode 10: 1000ms software mode, 35ms hardware mode 11: 2000ms software mode, 50ms hardware mode |
| WDT_MODE | 1 | Selects the operating mode for the watchdog timer. | 0: Software mode (monitor WDT_SW_RESET register) 1: Hardware mode (monitor WDT pin) |
| WDT_EN | 0 | Enables the watchdog timer. | 0: Watchdog timer disabled 1: Watchdog timer enabled |

WATCHDOG SW RESET (0x2016)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|---|---|---|---|---|---|---|
| Field | WDT_SW_RST[7:0] | | | | | | | |
| Reset | 0b00000000 | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------|------|-----------------------|---|
| WDT_SW_RST | 7:0 | Watchdog timer reset. | 0xE9 (1110_1001b): Resets watchdog timer All other values: Triggers watchdog timeout |

MEAS ADC THERMAL WARNING THRESHOLD (0x2017)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------------|---|---|---|---|---|---|---|
| Field | MEAS_ADC_WARN_THRESH[7:0] | | | | | | | |
| Reset | 0b01110101 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------------------|------|---|--|
| MEAS_ADC_WARN_THRESHOLD | 7:0 | Sets the thermal-warning threshold using the following formula: MEAS_ADC_WARN_THRESH[7:0] = [required temperature (in °C) + 29]/1.28 | 0000_0000: -29.0°C 0000_0001: -27.7°C 0000_0010: -26.4°C ...: in 1.28°C steps 1000_1010: 147.6°C 1000_1011: 148.9°C |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-------------|---|
| | | | 1000_1100: 150°C 1000_1101 to 1111_1111: 150°C |

MEAS_ADC_THERMAL_SHUTDOWN_THRESHOLD (0x2018)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------------|---|---|---|---|---|---|---|
| Field | MEAS_ADC_SHDN_THRESH[7:0] | | | | | | | |
| Reset | 0b10001100 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------------------|------|--|---|
| MEAS_ADC_SHDN_THRESHOLD | 7:0 | Sets the thermal-shutdown threshold using the following formula: MEAS_ADC_SHDN_THRESH[7:0] = [required temperature (in °C) + 29]/1.28 | 0000_0000: -29.0°C 0000_0001: -27.7°C 0000_0010: -26.4°C ...: in 1.28°C steps 1000_1010: 147.6°C 1000_1011: 148.9°C 1000_1100: 150°C 1000_1101 to 1111_1111: 150°C |

MEAS_ADC_THERMAL_HYSTERESIS (0x2019)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|--------------------------|---|---|---|---|
| Field | – | – | – | MEAS_ADC_THERM_HYST[4:0] | | | | |
| Reset | – | – | – | 0b01000 | | | | |
| Access Type | – | – | – | Write, Read | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------------|------|---|--|
| MEAS_ADC_THERM_HYST | 4:0 | Controls the amount hysteresis applied to the thermal threshold measurements. | 00000: Reserved 00001: Reserved 00010: Reserved 00011: Reserved 00100: 5.12°C 00101: 6.4°C 00110: 7.68°C 00111: 8.96°C ...: 1.28°C steps 11101: 37.12°C 11110: 38.40°C 11111: 39.68°C |

PIN_CONFIG (0x201A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|----------------|---|---------------|---|---------------|---|
| Field | ICC_DRV[1:0] | | LRCLK_DRV[1:0] | | BCLK_DRV[1:0] | | DOUT_DRV[1:0] | |
| Reset | 0b01 | | 0b01 | | 0b01 | | 0b01 | |
| Access Type | Write, Read | | Write, Read | | Write, Read | | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------|------|--|--|
| ICC_DRV | 7:6 | Configures the drive strength of the output pin. | 00: Reduced drive mode 01: Normal drive mode 10: High drive mode 11: Highest drive mode |
| LRCLK_DRV | 5:4 | Configures the drive strength of the output pin. | 00: Reduced drive mode 01: Normal drive mode 10: High drive mode 11: Highest drive mode |
| BCLK_DRV | 3:2 | Configures the drive strength of the output pin. | 00: Reduced drive mode 01: Normal drive mode 10: High drive mode 11: Highest drive mode |
| DOUT_DRV | 1:0 | Configures the drive strength of the output pin. | 00: Reduced drive mode 01: Normal drive mode 10: High drive mode 11: Highest drive mode |

PCM RX ENABLES A (0x201B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| Field | PCM_RX_C H7_EN | PCM_RX_C H6_EN | PCM_RX_C H5_EN | PCM_RX_C H4_EN | PCM_RX_C H3_EN | PCM_RX_C H2_EN | PCM_RX_C H1_EN | PCM_RX_C H0_EN |
| Reset | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------------|------|--|---|
| PCM_RX_C H7_EN | 7 | Enables the relevant channel on the PCM receive interface. | 0: PCM receive channel disabled 1: PCM receive channel enabled |
| PCM_RX_C H6_EN | 6 | Enables the relevant channel on the PCM receive interface. | 0: PCM receive channel disabled 1: PCM receive channel enabled |
| PCM_RX_C H5_EN | 5 | Enables the relevant channel on the PCM receive interface. | 0: PCM receive channel disabled 1: PCM receive channel enabled |
| PCM_RX_C H4_EN | 4 | Enables the relevant channel on the PCM receive interface. | 0: PCM receive channel disabled 1: PCM receive channel enabled |
| PCM_RX_C H3_EN | 3 | Enables the relevant channel on the PCM receive interface. | 0: PCM receive channel disabled 1: PCM receive channel enabled |
| PCM_RX_C H2_EN | 2 | Enables the relevant channel on the PCM receive interface. | 0: PCM receive channel disabled 1: PCM receive channel enabled |
| PCM_RX_C H1_EN | 1 | Enables the relevant channel on the PCM receive interface. | 0: PCM receive channel disabled 1: PCM receive channel enabled |
| PCM_RX_C H0_EN | 0 | Enables the relevant channel on the PCM receive interface. | 0: PCM receive channel disabled 1: PCM receive channel enabled |

PCM RX ENABLES B (0x201C)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|
| Field | PCM_RX_C H15_EN | PCM_RX_C H14_EN | PCM_RX_C H13_EN | PCM_RX_C H12_EN | PCM_RX_C H11_EN | PCM_RX_C H10_EN | PCM_RX_C H9_EN | PCM_RX_C H8_EN |
| Reset | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------|------|--|---|
| PCM_RX_C H15_EN | 7 | Enables the relevant channel on the PCM receive interface. | 0: PCM receive channel disabled 1: PCM receive channel enabled |
| PCM_RX_C H14_EN | 6 | Enables the relevant channel on the PCM receive interface. | 0: PCM receive channel disabled 1: PCM receive channel enabled |
| PCM_RX_C H13_EN | 5 | Enables the relevant channel on the PCM receive interface. | 0: PCM receive channel disabled 1: PCM receive channel enabled |
| PCM_RX_C H12_EN | 4 | Enables the relevant channel on the PCM receive interface. | 0: PCM receive channel disabled 1: PCM receive channel enabled |
| PCM_RX_C H11_EN | 3 | Enables the relevant channel on the PCM receive interface. | 0: PCM receive channel disabled 1: PCM receive channel enabled |
| PCM_RX_C H10_EN | 2 | Enables the relevant channel on the PCM receive interface. | 0: PCM receive channel disabled 1: PCM receive channel enabled |
| PCM_RX_C H9_EN | 1 | Enables the relevant channel on the PCM receive interface. | 0: PCM receive channel disabled 1: PCM receive channel enabled |
| PCM_RX_C H8_EN | 0 | Enables the relevant channel on the PCM receive interface. | 0: PCM receive channel disabled 1: PCM receive channel enabled |

PCM TX ENABLES A (0x201D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Field | PCM_TX_C H7_EN | PCM_TX_C H6_EN | PCM_TX_C H5_EN | PCM_TX_C H4_EN | PCM_TX_C H3_EN | PCM_TX_C H2_EN | PCM_TX_C H1_EN | PCM_TX_C H0_EN |
| Reset | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------|------|---|---|
| PCM_TX_CH 7_EN | 7 | Enables the relevant channel on the PCM transmit interface. | 0: PCM transmit channel disabled 1: PCM transmit channel enabled |
| PCM_TX_CH 6_EN | 6 | Enables the relevant channel on the PCM transmit interface. | 0: PCM transmit channel disabled 1: PCM transmit channel enabled |
| PCM_TX_CH 5_EN | 5 | Enables the relevant channel on the PCM transmit interface. | 0: PCM transmit channel disabled 1: PCM transmit channel enabled |
| PCM_TX_CH 4_EN | 4 | Enables the relevant channel on the PCM transmit interface. | 0: PCM transmit channel disabled 1: PCM transmit channel enabled |
| PCM_TX_CH 3_EN | 3 | Enables the relevant channel on the PCM transmit interface. | 0: PCM transmit channel disabled 1: PCM transmit channel enabled |
| PCM_TX_CH 2_EN | 2 | Enables the relevant channel on the PCM transmit interface. | 0: PCM transmit channel disabled 1: PCM transmit channel enabled |
| PCM_TX_CH 1_EN | 1 | Enables the relevant channel on the PCM transmit interface. | 0: PCM transmit channel disabled 1: PCM transmit channel enabled |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------|------|---|---|
| PCM_TX_CH0_EN | 0 | Enables the relevant channel on the PCM transmit interface. | 0: PCM transmit channel disabled 1: PCM transmit channel enabled |

PCM TX ENABLES B (0x201E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|
| Field | PCM_TX_C H15_EN | PCM_TX_C H14_EN | PCM_TX_C H13_EN | PCM_TX_C H12_EN | PCM_TX_C H11_EN | PCM_TX_C H10_EN | PCM_TX_C H9_EN | PCM_TX_C H8_EN |
| Reset | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------|------|---|---|
| PCM_TX_CH15_EN | 7 | Enables the relevant channel on the PCM transmit interface. | 0: PCM transmit channel disabled 1: PCM transmit channel enabled |
| PCM_TX_CH14_EN | 6 | Enables the relevant channel on the PCM transmit interface. | 0: PCM transmit channel disabled 1: PCM transmit channel enabled |
| PCM_TX_CH13_EN | 5 | Enables the relevant channel on the PCM transmit interface. | 0: PCM transmit channel disabled 1: PCM transmit channel enabled |
| PCM_TX_CH12_EN | 4 | Enables the relevant channel on the PCM transmit interface. | 0: PCM transmit channel disabled 1: PCM transmit channel enabled |
| PCM_TX_CH11_EN | 3 | Enables the relevant channel on the PCM transmit interface. | 0: PCM transmit channel disabled 1: PCM transmit channel enabled |
| PCM_TX_CH10_EN | 2 | Enables the relevant channel on the PCM transmit interface. | 0: PCM transmit channel disabled 1: PCM transmit channel enabled |
| PCM_TX_CH9_EN | 1 | Enables the relevant channel on the PCM transmit interface. | 0: PCM transmit channel disabled 1: PCM transmit channel enabled |
| PCM_TX_CH8_EN | 0 | Enables the relevant channel on the PCM transmit interface. | 0: PCM transmit channel disabled 1: PCM transmit channel enabled |

PCM TX HIZ CONTROL A (0x201F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Field | PCM_TX_C H7_HIZ | PCM_TX_C H6_HIZ | PCM_TX_C H5_HIZ | PCM_TX_C H4_HIZ | PCM_TX_C H3_HIZ | PCM_TX_C H2_HIZ | PCM_TX_C H1_HIZ | PCM_TX_C H0_HIZ |
| Reset | 0b1 | 0b1 | 0b1 | 0b1 | 0b1 | 0b1 | 0b1 | 0b1 |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------|------|---|--|
| PCM_TX_CH7_HIZ | 7 | Configures whether unused output bits are zero or Hi-Z. | 0: If the relevant PCM transmit channel is disabled or unused, output zero on channel. If the relevant PCM transmit channel is enabled, output data on channel. 1: In non-TDM mode, unused or disabled channels are Hi-Z. In TDM mode, unused bytes and disabled channels are Hi-Z. |
| PCM_TX_CH6_HIZ | 6 | Configures whether unused output bits are zero or Hi-Z. | 0: If the relevant PCM transmit channel is disabled or unused, output zero on channel. If the relevant PCM transmit channel is enabled, output data on channel. |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------------|------|---|--|
| | | | 1: In non-TDM mode, unused or disabled channels are Hi-Z. In TDM mode, unused bytes and disabled channels are Hi-Z. |
| PCM_TX_CH 5_HIZ | 5 | Configures whether unused output bits are zero or Hi-Z. | 0: If the relevant PCM transmit channel is disabled or unused, output zero on channel. If the relevant PCM transmit channel is enabled, output data on channel. 1: In non-TDM mode, unused or disabled channels are Hi-Z. In TDM mode, unused bytes and disabled channels are Hi-Z. |
| PCM_TX_CH 4_HIZ | 4 | Configures whether unused output bits are zero or Hi-Z. | 0: If the relevant PCM transmit channel is disabled or unused, output zero on channel. If the relevant PCM transmit channel is enabled, output data on channel. 1: In non-TDM mode, unused or disabled channels are Hi-Z. In TDM mode, unused bytes and disabled channels are Hi-Z. |
| PCM_TX_CH 3_HIZ | 3 | Configures whether unused output bits are zero or Hi-Z. | 0: If the relevant PCM transmit channel is disabled or unused, output zero on channel. If the relevant PCM transmit channel is enabled, output data on channel. 1: In non-TDM mode, unused or disabled channels are Hi-Z. In TDM mode, unused bytes and disabled channels are Hi-Z. |
| PCM_TX_CH 2_HIZ | 2 | Configures whether unused output bits are zero or Hi-Z. | 0: If the relevant PCM transmit channel is disabled or unused, output zero on channel. If the relevant PCM transmit channel is enabled, output data on channel. 1: In non-TDM mode, unused or disabled channels are Hi-Z. In TDM mode, unused bytes and disabled channels are Hi-Z. |
| PCM_TX_CH 1_HIZ | 1 | Configures whether unused output bits are zero or Hi-Z. | 0: If the relevant PCM transmit channel is disabled or unused, output zero on channel. If the relevant PCM transmit channel is enabled, output data on channel. 1: In non-TDM mode, unused or disabled channels are Hi-Z. In TDM mode, unused bytes and disabled channels are Hi-Z. |
| PCM_TX_CH 0_HIZ | 0 | Configures whether unused output bits are zero or Hi-Z. | 0: If the relevant PCM transmit channel is disabled or unused, output zero on channel. If the relevant PCM transmit channel is enabled, output data on channel. 1: In non-TDM mode, unused or disabled channels are Hi-Z. In TDM mode, unused bytes and disabled channels are Hi-Z. |

PCM TX HIZ CONTROL B (0x2020)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|--------------------|--------------------|
| Field | PCM_TX_C H15_HIZ | PCM_TX_C H14_HIZ | PCM_TX_C H13_HIZ | PCM_TX_C H12_HIZ | PCM_TX_C H11_HIZ | PCM_TX_C H10_HIZ | PCM_TX_C H9_HIZ | PCM_TX_C H8_HIZ |
| Reset | 0b1 | 0b1 | 0b1 | 0b1 | 0b1 | 0b1 | 0b1 | 0b1 |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------------|------|---|--|
| PCM_TX_CH 15_HIZ | 7 | Configures whether unused output bits are zero or Hi-Z. | 0: If the relevant PCM transmit channel is disabled or unused, output zero on channel. If the relevant PCM transmit channel is enabled, output data on channel. 1: In non-TDM mode, unused or disabled channels are Hi-Z. In TDM mode, unused bytes and disabled channels are Hi-Z. |
| PCM_TX_CH 14_HIZ | 6 | Configures whether unused output bits are zero or Hi-Z. | 0: If the relevant PCM transmit channel is disabled or unused, output zero on channel. If the relevant PCM transmit channel is enabled, output data on channel. 1: In non-TDM mode, unused or disabled channels are Hi-Z. In TDM mode, unused bytes and disabled channels are Hi-Z. |
| PCM_TX_CH 13_HIZ | 5 | Configures whether unused output bits are zero or Hi-Z. | 0: If the relevant PCM transmit channel is disabled or unused, output zero on channel. If the relevant PCM transmit channel is enabled, output data on channel. 1: In non-TDM mode, unused or disabled channels are Hi-Z. In TDM mode, unused bytes and disabled channels are Hi-Z. |
| PCM_TX_CH 12_HIZ | 4 | Configures whether unused output bits are zero or Hi-Z. | 0: If the relevant PCM transmit channel is disabled or unused, output zero on channel. If the relevant PCM transmit channel is enabled, output data on channel. 1: In non-TDM mode, unused or disabled channels are Hi-Z. In TDM mode, unused bytes and disabled channels are Hi-Z. |
| PCM_TX_CH 11_HIZ | 3 | Configures whether unused output bits are zero or Hi-Z. | 0: If the relevant PCM transmit channel is disabled or unused, output zero on channel. If the relevant PCM transmit channel is enabled, output data on channel. 1: In non-TDM mode, unused or disabled channels are Hi-Z. In TDM mode, unused bytes and disabled channels are Hi-Z. |
| PCM_TX_CH 10_HIZ | 2 | Configures whether unused output bits are zero or Hi-Z. | 0: If the relevant PCM transmit channel is disabled or unused, output zero on channel. If the relevant PCM transmit channel is enabled, output data on channel. 1: In non-TDM mode, unused or disabled channels are Hi-Z. In TDM mode, unused bytes and disabled channels are Hi-Z. |
| PCM_TX_CH 9_HIZ | 1 | Configures whether unused output bits are zero or Hi-Z. | 0: If the relevant PCM transmit channel is disabled or unused, output zero on channel. If the relevant PCM transmit channel is enabled, output data on |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------|------|---|--|
| | | | channel. 1: In non-TDM mode, unused or disabled channels are Hi-Z. In TDM mode, unused bytes and disabled channels are Hi-Z. |
| PCM_TX_CH8_HIZ | 0 | Configures whether unused output bits are zero or Hi-Z. | 0: If the relevant PCM transmit channel is disabled or unused, output zero on channel. If the relevant PCM transmit channel is enabled, output data on channel. 1: In non-TDM mode, unused or disabled channels are Hi-Z. In TDM mode, unused bytes and disabled channels are Hi-Z. |

PCM CHANNEL SOURCES 1 (0x2021)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------------|---|---|---|--------------------------|---|---|---|
| Field | PCM_DAC_BASS_SOURCE[3:0] | | | | PCM_DAC_MAIN_SOURCE[3:0] | | | |
| Reset | 0x0 | | | | 0x0 | | | |
| Access Type | Write, Read | | | | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------------|------|--|--|
| PCM_DAC_BASS_SOURCE | 7:4 | PCM channel selection for bass channel playback data. Only used when stereo bass is enabled. | 0000: PCM channel 0 0001: PCM channel 1 ...: ... 1110: PCM channel 14 1111: PCM channel 15 |
| PCM_DAC_MAIN_SOURCE | 3:0 | PCM channel selection for main channel playback data. | 0000: PCM channel 0 0001: PCM channel 1 ...: ... 1110: PCM channel 14 1111: PCM channel 15 |

PCM CHANNEL SOURCES 2 (0x2022)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------------|---|---|---|-----------------------|---|---|---|
| Field | PCM_IVADC_I_DEST[3:0] | | | | PCM_IVADC_V_DEST[3:0] | | | |
| Reset | 0x0 | | | | 0x0 | | | |
| Access Type | Write, Read | | | | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------|------|---|--|
| PCM_IVADC_I_DEST | 7:4 | PCM channel selection for measurement I path. | 0000: PCM channel 0 0001: PCM channel 1 ...: ... 1110: PCM channel 14 1111: PCM channel 15 |
| PCM_IVADC_V_DEST | 3:0 | PCM channel selection for measurement V path. | 0000: PCM channel 0 0001: PCM channel 1 ...: ... 1110: PCM channel 14 1111: PCM channel 15 |

PCM CHANNEL SOURCES 3 (0x2023)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|-----------------------|---|---|---|
| Field | PCM_IVADC_INTERLEAVE | - | - | - | PCM_AMP_DSP_DEST[3:0] | | | |
| Reset | 0x0 | - | - | - | 0x0 | | | |
| Access Type | Write, Read | - | - | - | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------------|------|---|---|
| PCM_IVADC_INTERLEAVE | 7 | Enables interleave mode for the V/I data output on the PCM interface. | 0: I/V data is not interleaved 1: I/V data is interleaved |
| PCM_AMP_DSP_DEST | 3:0 | PCM channel selection for amplifier to DAI feedback path. | 0000: PCM channel 0 0001: PCM channel 1 ... 1110: PCM channel 14 1111: PCM channel 15 |

PCM MODE CONFIG (0x2024)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|---|-----------------|---|---|---------------|-------------|------------------|
| Field | PCM_CHANSZ[1:0] | | PCM_FORMAT[2:0] | | | PCM_BCLK_EDGE | PCM_CHANSEL | PCM_TX_EXTRA_HIZ |
| Reset | 0b11 | | 0b000 | | | 0b0 | 0b0 | 0b0 |
| Access Type | Write, Read | | Write, Read | | | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------|------|--|--|
| PCM_CHANSZ | 7:6 | Configures the word length of a channel. | 00: Reserved 01: 16 10: 24 11: 32 |
| PCM_FORMAT | 5:3 | Selects the PCM format. | 000: I ² S mode 001: Left-justified 010: Reserved 011: TDM mode 0 (0 BCLK delay from LRCLK) 100: TDM mode 1 (1 BCLK delay from LRCLK) 101: TDM mode 2 (2 BCLK delay from LRCLK) 110 to 111: Reserved |
| PCM_BCLK_EDGE | 2 | Selects the active BCLK edge. | 0: Data captured and valid on rising edge of BCLK 1: Data captured and valid on falling edge of BCLK |
| PCM_CHANSEL | 1 | Selects which edge of LRCLK indicates the start of channels (channel 0). | 0: In I ² S and left-justified modes: Falling LRCLK indicates the start of channel 0 In TDM modes: Rising LRCLK indicates the start of channel 0 1: In I ² S and left-justified modes: Rising LRCLK indicates the start of channel 0 In TDM modes: Falling LRCLK indicates the start of channel 0 |
| PCM_TX_EXTRA_HIZ | 0 | Selects whether DOUT is driven to zero or Hi-Z during extra BCLK cycles. | 0: Extra BCLK cycles drive DOUT to zero 1: Extra BCLK cycles drive DOUT to Hi-Z |

PCM MASTER MODE (0x2025)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|----------------|--------------------|---|---|--------------------|---|---|
| Field | – | PCM_CLK_SOURCE | PCM_MCLK_RATE[3:0] | | | PCM_MSTR_MODE[1:0] | | |
| Reset | – | 0b0 | 0b0111 | | | 0b00 | | |
| Access Type | – | Write, Read | Write, Read | | | Write, Read | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------|------|---|---|
| PCM_CLK_SOURCE | 6 | Determines the MDLL reference clock in slave mode. | 0: BCLK used as clock source (MCLK input not required) 1: MCLK used as clock source |
| PCM_MCLK_RATE | 5:2 | Used to set MCLK rate when MCLK is selected as MDLL input using PCM_CLK_SOURCE. | 0000 to 0100: Reserved 0101: 11.2896MHz 0110: 12.000MHz 0111: 12.288MHz 1000 to 1111: Reserved |
| PCM_MSTR_MODE | 1:0 | Selects PCM interface master mode. | 00: Slave mode (BCLK input LRCLK input) 01: Reserved 10: Reserved 11: Master mode (BCLK output LRCLK output) |

PCM CLOCK SETUP (0x2026)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------|---|---|---|---------------|---|---|---|
| Field | PCM_MSEL[3:0] | | | | PCM_BSEL[3:0] | | | |
| Reset | 0b0100 | | | | 0b0100 | | | |
| Access Type | Write, Read | | | | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--|---|
| PCM_MSEL | 7:4 | Selects the number of BCLKs per LRCLK in master mode. Selects the number of BCLKs per LRCLK in slave mode when PCM_CLK_SOURCE is 1 (i.e., MCLK input is used). | 0000: Reserved 0001: Reserved 0010: 32 0011: 48 0100: 64 0101: 96 0110: 128 0111: 192 1000: 256 1001: Reserved 1010: 384 1011: 512 1100 to 1111: Reserved |
| PCM_BSEL | 3:0 | Selects the number of BCLKs per LRCLK. This needs to be set in slave mode and is only active when PCM_CLK_SOURCE is 0 (i.e., MCLK input is not used). | 0000: Reserved 0001: Reserved 0010: 32 0011: 48 0100: 64 0101: 96 0110: 128 0111: 192 1000: 256 |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-------------|---|
| | | | 1001: 320 1010: 384 1011: 512 1100 to 1111: Reserved |

PCM SAMPLE RATE SETUP 1 (0x2027)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|-------------|---|---|---|
| Field | – | – | – | – | SPK_SR[3:0] | | | |
| Reset | – | – | – | – | 0b1000 | | | |
| Access Type | – | – | – | – | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--|
| SPK_SR | 3:0 | Sets the sample-rate of the PCM interface. This corresponds to the LRCLK frequency. | 0000: 8000Hz 0001: 11025Hz 0010: 12000Hz 0011: 16000Hz 0100: 22050Hz 0101: 24000Hz 0110: 32000Hz 0111: 44100Hz 1000: 48000Hz 1001 to 1111: Reserved |

ICC RX ENABLES A (0x202C)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| Field | ICC_RX_C H7_EN | ICC_RX_C H6_EN | ICC_RX_C H5_EN | ICC_RX_C H4_EN | ICC_RX_C H3_EN | ICC_RX_C H2_EN | ICC_RX_C H1_EN | ICC_RX_C H0_EN |
| Reset | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------------|------|---|---|
| ICC_RX_CH 7_EN | 7 | Each amplifier is configured by a register setting to monitor the ICC during certain slots. The slots selected define to which group each amplifier belongs. Therefore, each amplifier in a group must have the same settings for R _x enables. | 0: ICC receive channel is disabled 1: ICC receive channel is enabled |
| ICC_RX_CH 6_EN | 6 | Each amplifier is configured by a register setting to monitor the ICC during certain slots. The slots selected define to which group each amplifier belongs. Therefore, each amplifier in a group must have the same settings for R _x enables. | 0: ICC receive channel is disabled 1: ICC receive channel is enabled |
| ICC_RX_CH 5_EN | 5 | Each amplifier is configured by a register setting to monitor the ICC during certain slots. The slots selected define to which group each amplifier belongs. Therefore, each amplifier in a group must have the same settings for R _x enables. | 0: ICC receive channel is disabled 1: ICC receive channel is enabled |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------------|------|---|---|
| ICC_RX_CH 4_EN | 4 | Each amplifier is configured by a register setting to monitor the ICC during certain slots. The slots selected define to which group each amplifier belongs. Therefore, each amplifier in a group must have the same settings for R _X enables. | 0: ICC receive channel is disabled 1: ICC receive channel is enabled |
| ICC_RX_CH 3_EN | 3 | Each amplifier is configured by a register setting to monitor the ICC during certain slots. The slots selected define to which group each amplifier belongs. Therefore, each amplifier in a group must have the same settings for R _X enables. | 0: ICC receive channel is disabled 1: ICC receive channel is enabled |
| ICC_RX_CH 2_EN | 2 | Each amplifier is configured by a register setting to monitor the ICC during certain slots. The slots selected define to which group each amplifier belongs. Therefore, each amplifier in a group must have the same settings for R _X enables. | 0: ICC receive channel is disabled 1: ICC receive channel is enabled |
| ICC_RX_CH 1_EN | 1 | Each amplifier is configured by a register setting to monitor the ICC during certain slots. The slots selected define to which group each amplifier belongs. Therefore, each amplifier in a group must have the same settings for R _X enables. | 0: ICC receive channel is disabled 1: ICC receive channel is enabled |
| ICC_RX_CH 0_EN | 0 | Each amplifier is configured by a register setting to monitor the ICC during certain slots. The slots selected define to which group each amplifier belongs. Therefore, each amplifier in a group must have the same settings for R _X enables. | 0: ICC receive channel is disabled 1: ICC receive channel is enabled |

ICC RX ENABLES B (0x202D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|-------------------|-------------------|
| Field | ICC_RX_C H15_EN | ICC_RX_C H14_EN | ICC_RX_C H13_EN | ICC_RX_C H12_EN | ICC_RX_C H11_EN | ICC_RX_C H10_EN | ICC_RX_C H9_EN | ICC_RX_C H8_EN |
| Reset | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------------|------|---|---|
| ICC_RX_CH 15_EN | 7 | Each amplifier is configured by a register setting to monitor the ICC during certain slots. The slots selected define to which group each amplifier belongs. Therefore, each amplifier in a group must have the same settings for R _X enables. | 0: ICC receive channel is disabled 1: ICC receive channel is enabled |
| ICC_RX_CH 14_EN | 6 | Each amplifier is configured by a register setting to monitor the ICC during certain slots. The slots selected define to which group each amplifier belongs. Therefore, each amplifier in a group must have the same settings for R _X enables. | 0: ICC receive channel is disabled 1: ICC receive channel is enabled |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------------|------|---|---|
| ICC_RX_CH 13_EN | 5 | Each amplifier is configured by a register setting to monitor the ICC during certain slots. The slots selected define to which group each amplifier belongs. Therefore, each amplifier in a group must have the same settings for R _X enables. | 0: ICC receive channel is disabled 1: ICC receive channel is enabled |
| ICC_RX_CH 12_EN | 4 | Each amplifier is configured by a register setting to monitor the ICC during certain slots. The slots selected define to which group each amplifier belongs. Therefore, each amplifier in a group must have the same settings for R _X enables. | 0: ICC receive channel is disabled 1: ICC receive channel is enabled |
| ICC_RX_CH 11_EN | 3 | Each amplifier is configured by a register setting to monitor the ICC during certain slots. The slots selected define to which group each amplifier belongs. Therefore, each amplifier in a group must have the same settings for R _X enables. | 0: ICC receive channel is disabled 1: ICC receive channel is enabled |
| ICC_RX_CH 10_EN | 2 | Each amplifier is configured by a register setting to monitor the ICC during certain slots. The slots selected define to which group each amplifier belongs. Therefore, each amplifier in a group must have the same settings for R _X enables. | 0: ICC receive channel is disabled 1: ICC receive channel is enabled |
| ICC_RX_CH 9_EN | 1 | Each amplifier is configured by a register setting to monitor the ICC during certain slots. The slots selected define to which group each amplifier belongs. Therefore, each amplifier in a group must have the same settings for R _X enables. | 0: ICC receive channel is disabled 1: ICC receive channel is enabled |
| ICC_RX_CH 8_EN | 0 | Each amplifier is configured by a register setting to monitor the ICC during certain slots. The slots selected define to which group each amplifier belongs. Therefore, each amplifier in a group must have the same settings for R _X enables. | 0: ICC receive channel is disabled 1: ICC receive channel is enabled |

ICC TX ENABLES A (0x202E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| Field | ICC_TX_C H7_EN | ICC_TX_C H6_EN | ICC_TX_C H5_EN | ICC_TX_C H4_EN | ICC_TX_C H3_EN | ICC_TX_C H2_EN | ICC_TX_C H1_EN | ICC_TX_C H0_EN |
| Reset | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------------|------|--|---|
| ICC_TX_CH 7_EN | 7 | The ICC pin only drives out during the slot assigned to the amplifier by TX_CH _n _EN bit. Only one TX_CH _n _EN bit should be set per amplifier. Note: n is valid between 0 to 15. | 0: Transmit channel n is disabled (default) 1: Transmit channel n is enabled |
| ICC_TX_CH 6_EN | 6 | The ICC pin only drives out during the slot assigned to the amplifier by TX_CH _n _EN bit. | 0: Transmit channel n is disabled (default) 1: Transmit channel n is enabled |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------|------|--|---|
| | | Only one TX_CHn_EN bit should be set per amplifier. Note: n is valid between 0 to 15. | |
| ICC_TX_CH 5_EN | 5 | The ICC pin only drives out during the slot assigned to the amplifier by TX_CHn_EN bit. Only one TX_CHn_EN bit should be set per amplifier. Note: n is valid between 0 to 15. | 0: Transmit channel n is disabled (default) 1: Transmit channel n is enabled |
| ICC_TX_CH 4_EN | 4 | The ICC pin only drives out during the slot assigned to the amplifier by TX_CHn_EN bit. Only one TX_CHn_EN bit should be set per amplifier. Note: n is valid between 0 to 15. | 0: Transmit channel n is disabled (default) 1: Transmit channel n is enabled |
| ICC_TX_CH 3_EN | 3 | The ICC pin only drives out during the slot assigned to the amplifier by TX_CHn_EN bit. Only one TX_CHn_EN bit should be set per amplifier. Note: n is valid between 0 to 15. | 0: Transmit channel n is disabled (default) 1: Transmit channel n is enabled |
| ICC_TX_CH 2_EN | 2 | The ICC pin only drives out during the slot assigned to the amplifier by TX_CHn_EN bit. Only one TX_CHn_EN bit should be set per amplifier. Note: n is valid between 0 to 15. | 0: Transmit channel n is disabled (default) 1: Transmit channel n is enabled |
| ICC_TX_CH 1_EN | 1 | The ICC pin only drives out during the slot assigned to the amplifier by TX_CHn_EN bit. Only one TX_CHn_EN bit should be set per amplifier. Note: n is valid between 0 to 15. | 0: Transmit channel n is disabled (default) 1: Transmit channel n is enabled |
| ICC_TX_CH 0_EN | 0 | The ICC pin only drives out during the slot assigned to the amplifier by TX_CHn_EN bit. Only one TX_CHn_EN bit should be set per amplifier. Note: n is valid between 0 to 15. | 0: Transmit channel n is disabled (default) 1: Transmit channel n is enabled |

ICC TX ENABLES B (0x202F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|
| Field | ICC_TX_C H15_EN | ICC_TX_C H14_EN | ICC_TX_C H13_EN | ICC_TX_C H12_EN | ICC_TX_C H11_EN | ICC_TX_C H10_EN | ICC_TX_C H9_EN | ICC_TX_C H8_EN |
| Reset | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------|------|--|---|
| ICC_TX_CH 15_EN | 7 | The ICC pin only drives out during the slot assigned to the amplifier by TX_CHn_EN bit. Only one TX_CHn_EN bit should be set per amplifier. Note: n is valid between 0 to 15. | 0: Transmit channel n is disabled (default) 1: Transmit channel n is enabled |
| ICC_TX_CH 14_EN | 6 | The ICC pin only drives out during the slot assigned to the amplifier by TX_CHn_EN bit. Only one TX_CHn_EN bit should be set per amplifier. Note: n is valid between 0 to 15. | 0: Transmit channel n is disabled (default) 1: Transmit channel n is enabled |
| ICC_TX_CH 13_EN | 5 | The ICC pin only drives out during the slot assigned to the amplifier by TX_CHn_EN bit. Only one TX_CHn_EN bit should be set per amplifier. Note: n is valid between 0 to 15. | 0: Transmit channel n is disabled (default) 1: Transmit channel n is enabled |
| ICC_TX_CH 12_EN | 4 | The ICC pin only drives out during the slot assigned to the amplifier by TX_CHn_EN bit. Only one TX_CHn_EN bit should be set per | 0: Transmit channel n is disabled (default) 1: Transmit channel n is enabled |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------------|------|--|---|
| | | amplifier. Note: n is valid between 0 to 15. | |
| ICC_TX_CH 11_EN | 3 | The ICC pin only drives out during the slot assigned to the amplifier by TX_CHn_EN bit. Only one TX_CHn_EN bit should be set per amplifier. Note: n is valid between 0 to 15. | 0: Transmit channel n is disabled (default) 1: Transmit channel n is enabled |
| ICC_TX_CH 10_EN | 2 | The ICC pin only drives out during the slot assigned to the amplifier by TX_CHn_EN bit. Only one TX_CHn_EN bit should be set per amplifier. Note: n is valid between 0 to 15. | 0: Transmit channel n is disabled (default) 1: Transmit channel n is enabled |
| ICC_TX_CH 9_EN | 1 | The ICC pin only drives out during the slot assigned to the amplifier by TX_CHn_EN bit. Only one TX_CHn_EN bit should be set per amplifier. Note: n is valid between 0 to 15. | 0: Transmit channel n is disabled (default) 1: Transmit channel n is enabled |
| ICC_TX_CH 8_EN | 0 | The ICC pin only drives out during the slot assigned to the amplifier by TX_CHn_EN bit. Only one TX_CHn_EN bit should be set per amplifier. Note: n is valid between 0 to 15. | 0: Transmit channel n is disabled (default) 1: Transmit channel n is enabled |

ICC HIZ MANUAL MODE (0x2030)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|---|---|---|---|---|---|----------------------|-----------------------|
| Field | – | – | – | – | – | – | ICC_TX_EX TRA_HIZ | ICC_TX_HI Z_MANUAL |
| Reset | – | – | – | – | – | – | 0b0 | 0b0 |
| Access Type | – | – | – | – | – | – | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------------|------|---|---|
| ICC_TX_EXT RA_HIZ | 1 | Selects whether ICC is driven to zero or Hi-Z during extra BCLK cycles. | 0: Extra BCLK cycles drive ICC to zero 1: Extra BCLK cycles drive ICC to Hi-Z |
| ICC_TX_HIZ _MANUAL | 0 | Forces the ICC pin to Hi-Z. | 0: ICC pin state is controlled on a slot by slot basis 1: ICC pin is Hi-Z at all times |

ICC TX HIZ ENABLES A (0x2031)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| Field | ICC_TX_C H7_HI \bar{Z} | ICC_TX_C H6_HI \bar{Z} | ICC_TX_C H5_HI \bar{Z} | ICC_TX_C H4_HI \bar{Z} | ICC_TX_C H3_HI \bar{Z} | ICC_TX_C H2_HI \bar{Z} | ICC_TX_C H1_HI \bar{Z} | ICC_TX_C H0_HI \bar{Z} |
| Reset | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------------------|------|--|--|
| ICC_TX_CH 7_HI \bar{Z} | 7 | Each ICC transmit channel can be configured to be Hi-Z regardless of whether or not it is enabled. | 0: If the relevant ICC transmit channel is disabled, output zero on channel. If the relevant ICC transmit channel is enabled, output data on channel. 1: Set Hi-Z on channel regardless of whether or not the relevant ICC transmit channel is enabled or disabled. |
| ICC_TX_CH 6_HI \bar{Z} | 6 | Each ICC transmit channel can be configured to be Hi-Z regardless of whether or not it is | 0: If the relevant ICC transmit channel is disabled, output zero on channel. If the relevant ICC transmit |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------|------|--|--|
| | | enabled. | channel is enabled, output data on channel. 1: Set Hi-Z on channel regardless of whether or not the relevant ICC transmit channel is enabled or disabled. |
| ICC_TX_CH 5_HIZ | 5 | Each ICC transmit channel can be configured to be Hi-Z regardless of whether or not it is enabled. | 0: If the relevant ICC transmit channel is disabled, output zero on channel. If the relevant ICC Transmit channel is enabled, output data on channel. 1: Set Hi-Z on channel regardless of whether or not the relevant ICC transmit channel is enabled or disabled. |
| ICC_TX_CH 4_HIZ | 4 | Each ICC transmit channel can be configured to be Hi-Z regardless of whether or not it is enabled. | 0: If the relevant ICC transmit channel is disabled, output zero on channel. If the relevant ICC transmit channel is enabled, output data on channel. 1: Set Hi-Z on channel regardless of whether or not the relevant ICC transmit channel is enabled or disabled. |
| ICC_TX_CH 3_HIZ | 3 | Each ICC transmit channel can be configured to be Hi-Z regardless of whether or not it is enabled. | 0: If the relevant ICC transmit channel is disabled, output zero on channel. If the relevant ICC transmit channel is enabled, output data on channel. 1: Set Hi-Z on channel regardless of whether or not the relevant ICC transmit channel is enabled or disabled. |
| ICC_TX_CH 2_HIZ | 2 | Each ICC transmit channel can be configured to be Hi-Z regardless of whether or not it is enabled. | 0: If the relevant ICC transmit channel is disabled, output zero on channel. If the relevant ICC transmit channel is enabled, output data on channel. 1: Set Hi-Z on channel regardless of whether or not the relevant ICC transmit channel is enabled or disabled. |
| ICC_TX_CH 1_HIZ | 1 | Each ICC transmit channel can be configured to be Hi-Z regardless of whether or not it is enabled. | 0: If the relevant ICC transmit channel is disabled, output zero on channel. If the relevant ICC transmit channel is enabled, output data on channel. 1: Set Hi-Z on channel regardless of whether or not the relevant ICC transmit channel is enabled or disabled. |
| ICC_TX_CH 0_HIZ | 0 | Each ICC transmit channel can be configured to be Hi-Z regardless of whether or not it is enabled. | 0: If the relevant ICC transmit channel is disabled, output zero on channel. If the relevant ICC transmit channel is enabled, output data on channel. 1: Set Hi-Z on channel regardless of whether or not the relevant ICC transmit channel is enabled or disabled. |

ICC TX HIZ ENABLES B (0x2032)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|------------------|------------------|------------------|------------------|------------------|------------------|-----------------|-----------------|
| Field | ICC_TX_C H15_HIZ | ICC_TX_C H14_HIZ | ICC_TX_C H13_HIZ | ICC_TX_C H12_HIZ | ICC_TX_C H11_HIZ | ICC_TX_C H10_HIZ | ICC_TX_C H9_HIZ | ICC_TX_C H8_HIZ |
| Reset | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------|------|---|--|
| ICC_TX_CH | 7 | Each ICC transmit channel can be configured | 0: If the relevant ICC transmit channel is disabled, |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------------|------|--|--|
| 15_HIZ | | to be Hi-Z regardless of whether or not it is enabled. | output zero on channel. If the relevant ICC transmit channel is enabled, output data on channel. 1: Set Hi-Z on channel regardless of whether or not the relevant ICC transmit channel is enabled or disabled. |
| ICC_TX_CH 14_HIZ | 6 | Each ICC transmit channel can be configured to be Hi-Z regardless of whether or not it is enabled. | 0: If the relevant ICC transmit channel is disabled, output zero on channel. If the relevant ICC transmit channel is enabled, output data on channel. 1: Set Hi-Z on channel regardless of whether or not the relevant ICC transmit channel is enabled or disabled. |
| ICC_TX_CH 13_HIZ | 5 | Each ICC transmit channel can be configured to be Hi-Z regardless of whether or not it is enabled. | 0: If the relevant ICC transmit channel is disabled, output zero on channel. If the relevant ICC transmit channel is enabled, output data on channel. 1: Set Hi-Z on channel regardless of whether or not the relevant ICC transmit channel is enabled or disabled. |
| ICC_TX_CH 12_HIZ | 4 | Each ICC transmit channel can be configured to be Hi-Z regardless of whether or not it is enabled. | 0: If the relevant ICC transmit channel is disabled, output zero on channel. If the relevant ICC transmit channel is enabled, output data on channel. 1: Set Hi-Z on channel regardless of whether or not the relevant ICC transmit channel is enabled or disabled. |
| ICC_TX_CH 11_HIZ | 3 | Each ICC transmit channel can be configured to be Hi-Z regardless of whether or not it is enabled. | 0: If the relevant ICC transmit channel is disabled, output zero on channel. If the relevant ICC transmit channel is enabled, output data on channel. 1: Set Hi-Z on channel regardless of whether or not the relevant ICC transmit channel is enabled or disabled. |
| ICC_TX_CH 10_HIZ | 2 | Each ICC transmit channel can be configured to be Hi-Z regardless of whether or not it is enabled. | 0: If the relevant ICC transmit channel is disabled, output zero on channel. If the relevant ICC transmit channel is enabled, output data on channel. 1: Set Hi-Z on channel regardless of whether or not the relevant ICC transmit channel is enabled or disabled. |
| ICC_TX_CH 9_HIZ | 1 | Each ICC transmit channel can be configured to be Hi-Z regardless of whether or not it is enabled. | 0: If the relevant ICC transmit channel is disabled, output zero on channel. If the relevant ICC transmit channel is enabled, output data on channel. 1: Set Hi-Z on channel regardless of whether or not the relevant ICC transmit channel is enabled or disabled. |
| ICC_TX_CH 8_HIZ | 0 | Each ICC transmit channel can be configured to be Hi-Z regardless of whether or not it is enabled. | 0: If the relevant ICC transmit channel is disabled, output zero on channel. If the relevant ICC transmit channel is enabled, output data on channel. 1: Set Hi-Z on channel regardless of whether or not the relevant ICC transmit channel is enabled or disabled. |

ICC LINK ENABLES (0x2033)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|---|-------------|---|
| Field | – | – | – | – | – | – | ICC_LINK_EN | – |
| Reset | – | – | – | – | – | – | 0b0 | – |
| Access Type | – | – | – | – | – | – | Write, Read | – |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------|------|---------------------------------------|-----------------------------------|
| ICC_LINK_EN | 1 | Enables the ICC link between devices. | 0: ICC disabled 1: ICC enabled |

AMP DSP CONFIG (0x2039)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|-------------|---------------------|------------------|----------------------|----------------|-------------|--------------|
| Field | – | DAC_INVERT | STARTUP_RAMP_BYPASS | SHDN_RAMP_BYPASS | DAC_HALF_REF_CURRENT | DAC_DOUBLE_RFB | AMP_DITH_EN | AMP_DCBLK_EN |
| Reset | – | 0b0 | 0b0 | 0b0 | 0b1 | 0b1 | 0b1 | 0b1 |
| Access Type | – | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------------|------|---|--|
| DAC_INVERT | 6 | Inverts DAC data. | 0: Normal DAC data 1: Invert DAC data |
| STARTUP_RAMP_BYPASS | 5 | Controls volume ramping during startup. | 0: Startup volume ramp enabled. Volume ramps smoothly from mute to active level at startup. 1: Startup volume ramp disabled. Signal immediately goes to the active level with no ramping. |
| SHDN_RAMP_BYPASS | 4 | Controls volume ramping during shutdown. | 0: Shutdown volume ramp enabled. During normal shutdown (initiated by setting EN to 0 while SPK_EN = 1) the volume ramps down smoothly before the amplifier is turned off. Note that the shutdown ramp waits for a pilot tone zero crossing before beginning. 1: Shutdown ramp bypassed. During normal shutdown (initiated by setting EN to 0 while SPK_EN = 1) the signal immediately goes to zero with no ramping before the amplifier is turned off. |
| DAC_HALF_REF_CURRENT | 3 | Reduces signal swing of DAC by -6dB. | 0: DAC output normal 1: Cut DAC output by 6dB |
| DAC_DOUBLE_RFB | 2 | Doubles the output swing of the DAC. Usually only used with DAC_HALF_REF_CURRENT for low power operation. | 0: Disabled 1: Enabled |
| AMP_DITH_EN | 1 | Selects whether or not the PCM input data is dithered at the LSB. | 0: Dither disabled 1: Dither enabled |
| AMP_DCBLK_EN | 0 | Enables the DC blocking filter. | 0: DC blocking filter disabled 1: DC blocking filter enabled |

AMP ENABLES (0x203A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|-------------|
| Field | ENABLE_DEM | – | – | – | – | – | – | SPK_EN |
| Reset | 0b1 | – | – | – | – | – | – | 0b1 |
| Access Type | Write, Read | – | – | – | – | – | – | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------|------|--|---|
| ENABLE_DEM | 7 | Always enable DEM. | 0: Reserved 1: Default value. DEM is enabled. DEM_OFF_TRIM should be 0 when this bit is high. |
| SPK_EN | 0 | Enable output amplifier path. Note that the amplifier is powered up if this bit is set AND the global enable bit (EN) is set. Note that SPK_EN is a static bit and should not be changed while EN = 1. | 0: Amplifier disabled 1: Amplifier enabled |

TONE GENERATOR AND DC CONFIG (0x203B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|------------------|---|---|---|
| Field | – | – | – | – | TONE_CONFIG[3:0] | | | |
| Reset | – | – | – | – | 0b0000 | | | |
| Access Type | – | – | – | – | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------|------|--|---|
| TONE_CONFIG | 3:0 | Configures the output frequency of the tone generator as a division of the sample rate (fs). Note that the maximum speaker sample rate is 48kHz when using the tone generator. | 0000: Disabled 0001: fs/4 (At 48kHz = 12kHz) 0010: fs/6 (At 48kHz = 8kHz) 0011: fs/8 (At 48kHz = 6kHz) 0100: fs/16 (At 48kHz = 3kHz) 0101: fs/32 (At 48kHz = 1.5kHz) 0110: fs/64 (At 48kHz = 750Hz) 0111: fs/128 (At 48kHz = 375Hz) 1000: DC = 0x0000 = 0 1001: DC = 0x4000 = +FullScale/2 1010: DC = 0xC000 = -FullScale/2 1011 to 1111: Reserved |

SPEAKER SOURCE SELECT (0x203C)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|---|-----------------|---|
| Field | – | – | – | – | – | – | SPK_SOURCE[1:0] | |
| Reset | – | – | – | – | – | – | 0b00 | |
| Access Type | – | – | – | – | – | – | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------|------|---|--|
| SPK_SOURCE | 1:0 | Controls the input source to the speaker amplifier. | 00: PCM interface (for I ² S/TDM) 01: Reserved 10: Tone generator 11: Reserved |

SSM CONFIGURATION (0x203E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|--------------------|---|---|--------------------|---|---|
| Field | SSM_EN | – | SPK_EDGE_CTRL[1:0] | | – | SSM_MOD_INDEX[2:0] | | |
| Reset | 0b1 | – | 0b00 | | – | 0b101 | | |
| Access Type | Write, Read | – | Write, Read | | – | Write, Read | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------|------|--|---|
| SSM_EN | 7 | Enables spread-spectrum clocking. | 0: Spread-spectrum clocking is disabled 1: Spread-spectrum clocking is enabled |
| SPK_EDGE_CTRL | 5:4 | Controls the speaker output edge rate. | 00: Speaker driver bias default 01: Speaker driver bias decreased by 30% 10: Speaker driver bias decreased by 60% 11: Speaker driver bias increased by 30% |
| SSM_MOD_INDEX | 2:0 | Determines the modulation index of the Class-D amplifier spread-spectrum clocks. The maximum modulation index (MMI) is 10.8%. The modulation index can be varied as follows. | 000: MMI 001: MMI x 5/6 010: MMI x 4/6 011: MMI x 3/6 100: MMI x 2/6 101: MMI x 1/6 (Recommended) 110 to 111: Reserved |

MEASUREMENT ENABLES (0x203F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|---|-------------|-------------|
| Field | – | – | – | – | – | – | IVADC_I_EN | IVADC_V_EN |
| Reset | – | – | – | – | – | – | 0b1 | 0b1 |
| Access Type | – | – | – | – | – | – | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------|------|---|---|
| IVADC_I_EN | 1 | IVADC_I_EN enables the speaker current measurement path. Note that the measurement path is enabled only if this bit is set AND the EN bit is set. | 0: Speaker current measurement path disabled 1: Speaker current measurement path enabled |
| IVADC_V_EN | 0 | IVADC_V_EN enables the speaker voltage measurement path. Note that the measurement path is enabled only if this bit is set AND the EN bit is set. | 0: Speaker voltage measurement path disabled 1: Speaker voltage measurement path enabled |

MEASUREMENT DSP CONFIG (0x2040)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|---|-------------------|---|---|--------------|-----------------|------------------|
| Field | MEAS_I_DCBLK[1:0] | | MEAS_V_DCBLK[1:0] | | – | MEAS_DITH_EN | MEAS_ID_CBLK_EN | MEAS_V_D_CBLK_EN |
| Reset | 0b11 | | 0b11 | | – | 0b1 | 0b1 | 0b1 |
| Access Type | Write, Read | | Write, Read | | – | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------|------|--|------------|
| MEAS_I_DC | 7:6 | Sets the corner frequency of the DC blocking | 00: 0.06Hz |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------------|------|--|---|
| BLK | | filter on the current measurement path. Values below valid at 48kHz sample rate and scale across other sample rates. | 01: 0.118Hz 10: 0.235Hz 11: 3.7Hz |
| MEAS_V_DC BLK | 5:4 | Sets the corner frequency of the DC blocking filter on the voltage measurement path. Values below valid at 48kHz sample rate and scale across other sample rates. | 00: 0.06Hz 01: 0.118Hz 10: 0.235Hz 11: 3.7Hz |
| MEAS_DITH _EN | 2 | Selects whether dither is applied to the measurement ADC data read out through I ² C. | 0: Dither disabled 1: Dither enabled |
| MEAS_I_DC BLK_EN | 1 | Enable the DC blocker in the current sense path. | 0: DC blocker disabled 1: DC blocker enabled |
| MEAS_V_DC BLK_EN | 0 | Enable the DC blocker in the voltage sense path. | |

BOOST CONTROL 0 (0x2041)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|-----------------|---|---|---------------|---|---|---|---|
| Field | EXT_PVDD _EN | – | – | BST_VOUT[4:0] | | | | |
| Reset | 0b0 | – | – | 0b11100 | | | | |
| Access Type | Write, Read | – | – | Write, Read | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------|------|--|---|
| EXT_PVDD_ EN | 7 | Disables boost and bypasses boost influence on speaker state machine. | 0: Normal boost operation 1: Boost is disabled |
| BST_VOUT | 4:0 | Controls the nominal output from the boost converter which supplies the speaker amplifier. | Value: Decode 00000: 6.500V 00001: 6.625V 00010: 6.750V 00011: 6.875V 00100: 7.000V 00101: 7.125V 00110: 7.250V 00111: 7.375V 01000: 7.500V 01001: 7.625V 01010: 7.750V 01011: 7.875V 01100: 8.000V 01101: 8.125V 01110: 8.250V 01111: 8.375V 10000: 8.500V 10001: 8.625V 10010: 8.750V 10011: 8.875V 10100: 9.000V 10101: 9.125V 10110: 9.250V 10111: 9.375V 11000: 9.500V |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-------------|--|
| | | | 11001: 9.625V 11010: 9.750V 11011: 9.875V 11100: 10.000V 11101: Reserved 11110: Reserved 11111: Reserved |

BOOST CONTROL 3 (0x2042)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|----------------|----------------|---|---|-------------------|---|
| Field | – | – | BST_SLOW START | BST_PHASE[2:0] | | | BST_SKIPLOAD[1:0] | |
| Reset | – | – | 0b0 | 0b000 | | | 0b01 | |
| Access Type | – | – | Write, Read | Write, Read | | | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------|------|---|--|
| BST_SLOW START | 5 | Increase start-up time of the boost converter which is necessary if very large capacitance is present on the boost converter output (PVDD). | 0: Quick startup (1ms - use for $C_{PVDD} \leq 100\mu\text{F}$ 1: Slow startup (12ms - use for $C_{PVDD} > 100\mu\text{F}$) |
| BST_PHASE | 4:2 | Selects the phase alignment of the boost control clocks with respect to LRCLK. | 000 to 011: See the <i>Electrical Characteristics</i> for settings 1XX: disabled |
| BST_SKIPLOAD | 1:0 | Selects the skip mode of the boost converter. | 00: FPWM mode (no skip mode) 01: Skip mode 1: Natural skip 10: Skip mode 2: $f > 30\text{kHz}$ 11: Skip mode 3: $f > 340\text{kHz}$ |

BOOST CONTROL 1 (0x2043)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|---------------|---|---|---|---|---|---|
| Field | BST_SKIP_CONTROL | BST_ILIM[6:0] | | | | | | |
| Reset | 0b0 | 0b1000000 | | | | | | |
| Access Type | Write, Read | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------|------|---|---|
| BST_SKIP_CONTROL | 7 | If BST_BYP_MODE = 10b (boost bypass disabled), set BST_SKIP_CONTROL to 1. Otherwise, set BST_SKIP_CONTROL to 0. | 0: Normal mode 1: Force skip on |
| BST_ILIM | 6:0 | Sets the peak input current limit for the boost converter. | 0000000: 0.00A 0000001: 0.50A 0000010: 1.00A 0000011: 1.05A 0000100: 1.10A: in 0.05A steps 0111110: 4.00A 0111111: 4.05A 1000000: 4.10A 1000001 to 1111111: Reserved |

MEAS_ADC_CONFIG (0x2044)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|-----------------|-----------------|-----------------|
| Field | – | – | – | – | – | MEAS_ADC_CH2_EN | MEAS_ADC_CH1_EN | MEAS_ADC_CH0_EN |
| Reset | – | – | – | – | – | 0b1 | 0b1 | 0b1 |
| Access Type | – | – | – | – | – | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------|------|--|---|
| MEAS_ADC_CH2_EN | 2 | Enables the measurement input for CH0 (VBAT), CH1 (PVDD), or CH2 (temperature) when the Measurement ADC is in automatic mode. Any combination of inputs can be selected. The measurement ADC is disabled when no measurements are enabled. | 0: Channel disabled 1: Channel enabled |
| MEAS_ADC_CH1_EN | 1 | Enables the measurement input for CH0 (VBAT), CH1 (PVDD), or CH2 (temperature) when the measurement ADC is in automatic mode. Any combination of inputs can be selected. The measurement ADC is disabled when no measurements are enabled. | 0: Channel disabled 1: Channel enabled |
| MEAS_ADC_CH0_EN | 0 | Enables the measurement input for CH0 (VBAT), CH1 (PVDD), or CH2 (temperature) when the measurement ADC is in automatic mode. Any combination of inputs can be selected. The measurement ADC is disabled when no measurements are enabled. | 0: Channel disabled 1: Channel enabled |

MEAS_ADC_BASE_DIVIDE_MSBYTE (0x2045)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------------|---|---|---|---|---|---|---|
| Field | MEAS_ADC_BASE_DIV[15:8] | | | | | | | |
| Reset | 0x00 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|-------------------|------|---|
| MEAS_ADC_BASE_DIV | 7:0 | <p>MEAS_ADC_BASE_DIV[15:0] Division to set the base sampling rate for the measurement ADC.</p> <p>Base sample rate = $MEAS_ADC_CLK / (MEAS_ADC_BASE_DIV[15:0] + 1)$</p> <p>MEAS_ADC_CLK is derived from the MDLL output clock and can be one of three typical frequencies:</p> <ul style="list-style-type: none"> • 12.288MHz (48kHz-based sample rates) • 11.2896MHz (44.1kHz-based sample rates) • 12.000MHz (for master mode when MCLK = 12.0MHz or 6.0MHz) <p>For example if 48kHz sampling rate in the measurement ADC is required when using a 48kHz-based sample rate:</p> <p>$MEAS_ADC_BASE_DIV[15:0] = (12.288MHz / 48kHz) - 1 = 255$</p> |

MEAS ADC BASE DIVIDE LSBYTE (0x2046)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------------|---|---|---|---|---|---|---|
| Field | MEAS_ADC_BASE_DIV[7:0] | | | | | | | |
| Reset | 0x23 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|-------------------|------|---|
| MEAS_ADC_BASE_DIV | 7:0 | <p>MEAS_ADC_BASE_DIV[15:0] Division to set the base sampling rate for the measurement ADC.</p> <p>Base sample rate = MEAS_ADC_CLK/(MEAS_ADC_BASE_DIV[15:0] + 1)</p> <p>MEAS_ADC_CLK is derived from the MDLL output clock and can be one of three typical frequencies:</p> <ul style="list-style-type: none"> • 12.288MHz (48kHz-based sample rates) • 11.2896MHz (44.1kHz-based sample rates) • 12.000MHz (for master mode when MCLK = 12.0MHz or 6.0MHz) <p>For example if 48kHz sampling rate in the measurement ADC is required when using a 48kHz-based sample rate:</p> <p>MEAS_ADC_BASE_DIV[15:0] = (12.288MHz/48kHz) - 1 = 255</p> |

MEAS ADC CHAN 0 DIVIDE (0x2047)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------------|---|---|---|---|---|---|---|
| Field | MEAS_ADC_CH0_DIV[7:0] | | | | | | | |
| Reset | 0b00000000 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------|------|---|--|
| MEAS_ADC_CH0_DIV | 7:0 | <p>Controls the sample rate of the given channel in the measurement ADC as a function of the measurement ADC base sample rate:</p> <p>Note: The set value for MEAS_ADC_CHn_DIV[7:0] is (integer divisor - 1)</p> <p>For example, if the base sample rate is 48kHz, a 4kHz sample rate (48kHz/12) is set by programming MEAS_ADC_CHn_DIV[7:0] = 11.</p> | <p>0: Divide by 1 1: Divide by 2 2: Divide by 3 ... 253: Divide by 254 254: Divide by 255 255: Divide by 256</p> |

MEAS ADC CHAN 1 DIVIDE (0x2048)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------------|---|---|---|---|---|---|---|
| Field | MEAS_ADC_CH1_DIV[7:0] | | | | | | | |
| Reset | 0b00000000 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------|------|---|--|
| MEAS_ADC_CH1_DIV | 7:0 | <p>Controls the sample rate of the given channel in the measurement ADC as a function of the measurement ADC base sample rate:</p> <p>Note: The set value for MEAS_ADC_CHn_DIV[7:0] is (integer divisor - 1)</p> <p>For example, if the base sample rate is 48kHz, a 4kHz sample rate (48kHz/12) is set by programming MEAS_ADC_CHn_DIV[7:0] = 11.</p> | <p>0: Divide by 1 1: Divide by 2 2: Divide by 3 ... 253: Divide by 254 254: Divide by 255 255: Divide by 256</p> |

MEAS ADC CHAN 2 DIVIDE (0x2049)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----------------------|---|---|---|---|---|---|---|
| Field | MEAS_ADC_CH2_DIV[7:0] | | | | | | | |
| Reset | 0b00000000 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------|------|---|--|
| MEAS_ADC_CH2_DIV | 7:0 | <p>Controls the sample rate of the given channel in the measurement ADC as a function of the measurement ADC Base Sample Rate:</p> <p>Note: The set value for MEAS_ADC_CHn_DIV[7:0] is (integer divisor - 1)</p> <p>For example, if the base sample rate is 48kHz, a 4kHz sample rate (48kHz/12) is set by programming MEAS_ADC_CHn_DIV[7:0] = 11.</p> | <p>0: Divide by 1 1: Divide by 2 2: Divide by 3 ... 253: Divide by 254 254: Divide by 255 255: Divide by 256</p> |

MEAS ADC CHAN 0 FILT CONFIG (0x204A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|---|---|---|---|----------------------|----------------------------|---|---|
| Field | - | - | - | - | MEAS_ADC_CH0_FILT_EN | MEAS_ADC_CH0_FILT_AVG[2:0] | | |
| Reset | - | - | - | - | 0b0 | 0b000 | | |
| Access Type | - | - | - | - | Write, Read | Write, Read | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------------|------|--|--|
| MEAS_ADC_CH0_FILT_EN | 3 | Controls whether filtering is applied to the measurement ADC channel output. | <p>0: Filter disabled 1: Filtering applied as per measurement ADC channel filter</p> |
| MEAS_ADC_CH0_FILT_AVG | 2:0 | MEAS_ADC_CHn_FILT_AVG[2:0] A moving-average filter is available on each channel of the measurement ADC. This field controls the depth of the filter. | <p>000: No filtering (1-point) 001: 2 points 010: 4 points 011: 8 points</p> |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-------------|--|
| | | | 100: 16 points 101 to 111: Reserved |

MEAS ADC CHAN 1 FILT CONFIG (0x204B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|----------------------|----------------------------|---|---|
| Field | – | – | – | – | MEAS_ADC_CH1_FILT_EN | MEAS_ADC_CH1_FILT_AVG[2:0] | | |
| Reset | – | – | – | – | 0b0 | 0b000 | | |
| Access Type | – | – | – | – | Write, Read | Write, Read | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------------|------|--|--|
| MEAS_ADC_CH1_FILT_EN | 3 | Controls whether filtering is applied to the measurement ADC channel output. | 0: Filter disabled 1: Filtering applied as per measurement ADC channel filter |
| MEAS_ADC_CH1_FILT_AVG | 2:0 | MEAS_ADC_CHn_FILT_AVG[2:0] A moving-average filter is available on each channel of the measurement ADC. This field controls the depth of the filter. | 000: No filtering (1-point) 001: 2 points 010: 4 points 011: 8 points 100: 16 points 101 to 111: Reserved |

MEAS ADC CHAN 2 FILT CONFIG (0x204C)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|----------------------|----------------------------|---|---|
| Field | – | – | – | – | MEAS_ADC_CH2_FILT_EN | MEAS_ADC_CH2_FILT_AVG[2:0] | | |
| Reset | – | – | – | – | 0b0 | 0b000 | | |
| Access Type | – | – | – | – | Write, Read | Write, Read | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------------|------|--|--|
| MEAS_ADC_CH2_FILT_EN | 3 | Controls whether filtering is applied to the measurement ADC channel output. | 0: Filter disabled 1: Filtering applied as per measurement ADC channel filter |
| MEAS_ADC_CH2_FILT_AVG | 2:0 | MEAS_ADC_CHn_FILT_AVG[2:0] A moving-average filter is available on each channel of the measurement ADC. This field controls the depth of the filter. | 000: No filtering (1-point) 001: 2 points 010: 4 points 011: 8 points 100: 16 points 101 to 111: Reserved |

MEAS ADC CHAN 0 READBACK (0x204D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------------|---|---|---|---|---|---|---|
| Field | MEAS_ADC_CH0_DATA[7:0] | | | | | | | |
| Reset | 0b00000000 | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|------------------------|------|---|
| MEAS_ADC_CH0_DATA A | 7:0 | MEAS_ADC_CH0_DATA[7:0] Provides the latest measured V_{VBAT} value. To convert the 8-bit code into a real voltage, use the following: Measured $V_{VBAT} = 2.4V + (CH0DAT[7:0] \times 12.5mV)$. This register reads-back 0x00 when EN = 0. |

MEAS ADC CHAN 1 READBACK (0x204E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------------|---|---|---|---|---|---|---|
| Field | MEAS_ADC_CH1_DATA[7:0] | | | | | | | |
| Reset | 0b00000000 | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|------------------------|------|---|
| MEAS_ADC_CH1_DATA A | 7:0 | MEAS_ADC_CH1_DATA[7:0] Provides the latest measured V_{PVDD} value. To convert the 8-bit code into a real voltage, use the following: Measured $V_{PVDD} = 4.8V + (CH1DAT[7:0] \times 25mV)$. This register reads-back 0x00 when EN = 0. |

MEAS ADC CHAN 2 READBACK (0x204F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------------|---|---|---|---|---|---|---|
| Field | MEAS_ADC_CH2_DATA[7:0] | | | | | | | |
| Reset | 0b00000000 | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|------------------------|------|---|
| MEAS_ADC_CH2_DATA A | 7:0 | MEAS_ADC_CH2_DATA[7:0] Provides the latest measured temperature value. To convert the 8-bit code into a real temperature, use the following: Measured Temperature ($^{\circ}C$) = $(CH2DAT[7:0] \times 1.28) - 29$. This register reads-back 0x00 when EN = 0. |

DSP POWER GATING CONTROL (0x2050)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|------------------------|------------------------------|---|---|----------------|-----------------|
| Field | – | – | POWER_GATE_EXIT_THRESH | POWER_GATE_ENTRY_THRESH[2:0] | | | AUTO_MUTING_EN | POWER_GATING_EN |
| Reset | – | – | 0x1 | 0x3 | | | 0x0 | 0x0 |
| Access Type | – | – | Write, Read | Write, Read | | | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------------|------|--|---|
| POWER_GATE_EXIT_TH | 5 | Sets the peak signal level above which the power gating is removed. The setting is | 0x0: Entry threshold + 6dB 0x1: Entry threshold + 12dB |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------------------|------|--|--|
| RESH | | relative to that of POWER_GATE_ENTRY_THRESH. | |
| POWER_GATE_ENTRY_THRESH | 4:2 | Sets the peak signal level below which the power gating triggers. | 0x0: ~-91dBFS 0x1: ~-91dBFS 0x2: ~-85dBFS 0x3: ~-81dBFS 0x4: ~-78dBFS 0x5: ~-76dBFS 0x6: Reserved 0x7: Reserved |
| AUTO_MUTING_EN | 1 | Enables the automatic muting of the DSP output when low signal level is present. When POWER_GATING_EN = 1, automatic muting is enabled regardless of the AUTO_MUTING_EN setting. | 0x0: Auto-mute disabled 0x1: Auto-mute enabled |
| POWER_GATING_EN | 0 | Enables the automatic power gating of the DSP core and DSMIG when low signal level is present. When POWER_GATING_EN = 1, automatic muting is enabled regardless of the AUTO_MUTING_EN setting. | 0x0: Power gating disabled 0x1: Power gating and auto-mute enabled |

DSP POWER GATING STATUS (0x2051)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|---|-------------|---------------------|
| Field | – | – | – | – | – | – | MUTE_ACTIVE | POWER_GATING_ACTIVE |
| Reset | – | – | – | – | – | – | 0x0 | 0x0 |
| Access Type | – | – | – | – | – | – | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------------|------|--|--|
| MUTE_ACTIVE | 1 | Readback of whether the power automatic muting has been triggered and is active. | 0x0: Auto-mute not active 0x1: Auto-mute active |
| POWER_GATING_ACTIVE | 0 | Readback of whether the power automatic power gating has been triggered and is active. | 0x0: Power gating not active 0x1: Power gating active |

VBAT LOWEST STATUS (0x2052)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|---|---|---|---|---|---|---|
| Field | VBAT_LOWEST[7:0] | | | | | | | |
| Reset | 0b11111111 | | | | | | | |
| Access Type | Read, Ext | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|-------------|------|---|
| VBAT_LOWEST | 7:0 | VBAT_LOWEST[7:0] Reports the lowest VBAT value since the last read. |

PVDD LOWEST STATUS (0x2053)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|---|---|---|---|---|---|---|
| Field | PVDD_LOWEST[7:0] | | | | | | | |
| Reset | 0b11111111 | | | | | | | |
| Access Type | Read, Ext | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|-------------|------|---|
| PVDD_LOWEST | 7:0 | PVDD_LOWEST[7:0] Reports the lowest PVDD value since the last read. |

BROWNOUT STATUS (0x2054)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|----------------|---|---|
| Field | - | - | - | - | - | BDE_STATE[2:0] | | |
| Reset | - | - | - | - | - | 0b000 | | |
| Access Type | - | - | - | - | - | Read, Ext | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------|------|---|---|
| BDE_STATE | 2:0 | Current level of brownout controller. This reads-back 0000 when EN = 0. | 000: Brownout idle - normal operation 001: Level 1 010: Level 2 011: Level 3 100: Level 4 101 to 111: Reserved |

BROWNOUT ENABLES (0x2055)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|-------------|-------------|-------------|
| Field | - | - | - | - | - | AMP_DSP_EN | BDE_AMP_EN | BDE_EN |
| Reset | - | - | - | - | - | 0b0 | 0b0 | 0b0 |
| Access Type | - | - | - | - | - | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------|------|--|---|
| AMP_DSP_EN | 2 | Enables the output path from the end of the amplifier baseband programming to the host through a PCM interface. | 0: Amplifier DSP monitor output path disabled 1: Amplifier DSP monitor output path enabled |
| BDE_AMP_EN | 1 | Enables BDE to be active on the amplifier path when brownout enable is set. When this bit is 0, the BDE only functions on the input current limit for the boost converter. | 0: Disabled 1: Enabled |
| BDE_EN | 0 | Enables the brownout controller. Note that BDE_EN can be set to 1 at any time. However, BDE_EN can only be cleared to 0 when EN = 0 or when the brownout controller is in normal operation (brownout-protection idle). | 0: Brownout disabled 1: Brownout enabled |

BROWNOUT LEVEL INFINITE HOLD (0x2056)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|---|----------------|---|
| Field | – | – | – | – | – | – | BDE_L4_INF_HLD | – |
| Reset | – | – | – | – | – | – | 0b0 | – |
| Access Type | – | – | – | – | – | – | Write, Read | – |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------|------|---|---|
| BDE_L4_INF_HLD | 1 | Controls an infinite hold feature while in level 4. | 0: Transition from level 4 automatically based on VBAT measurement 1: Transition from level 4 only after writing to BDE_L4_HLD_RLS |

BROWNOUT LEVEL INFINITE HOLD CLEAR (0x2057)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|---|----------------|---|
| Field | – | – | – | – | – | – | BDE_L4_HLD_RLS | – |
| Reset | – | – | – | – | – | – | 0b0 | – |
| Access Type | – | – | – | – | – | – | Write Only | – |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------|------|---|---|
| BDE_L4_HLD_RLS | 1 | Manually releases the BDE controller from level 4 when used with BDE infinite hold. | 0: Writing zero has no effect 1: Releases brownout controller to level 3 |

BROWNOUT LEVEL HOLD (0x2058)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field | BDE_HLD[7:0] | | | | | | | |
| Reset | 0b00000000 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--|
| BDE_HLD | 7:0 | Sets the hold time for each ascending state in the brownout controller. | 0x00: 0ms 0x01: 0.1ms 0x02: 1ms ...: 1ms steps 0xFD: 252ms 0xFE: 253ms 0xFF: 254ms |

BROWNOUT LEVEL 1 THRESHOLD (0x2059)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | BDE_L1_VTHRESH[7:0] | | | | | | | |
| Reset | 0b00000000 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------------|------|---|
| BDE_L1_VTHRESH | 7:0 | BDE_Ln_VTHRESH[7:0] Sets the trigger level for each threshold in the brownout controller. Refer to the measurement ADC CH0 (VBAT) result register to set these levels. A value of 0000 0000 (all zeros) means that state is not used and is entirely bypassed (no hold times). |

BROWNOUT LEVEL 2 THRESHOLD (0x205A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | BDE_L2_VTHRESH[7:0] | | | | | | | |
| Reset | 0b00000000 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------------|------|---|
| BDE_L2_VTHRESH | 7:0 | BDE_Ln_VTHRESH[7:0] Sets the trigger level for each threshold in the brownout controller. Refer to the measurement ADC CH0 (VBAT) result register to set these levels. A value of 0000 0000 (all zeros) means that state is not used and is entirely bypassed (no hold times). |

BROWNOUT LEVEL 3 THRESHOLD (0x205B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | BDE_L3_VTHRESH[7:0] | | | | | | | |
| Reset | 0b00000000 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------------|------|---|
| BDE_L3_VTHRESH | 7:0 | BDE_Ln_VTHRESH[7:0] Sets the trigger level for each threshold in the brownout controller. Refer to the measurement ADC CH0 (VBAT) result register to set these levels. A value of 0000 0000 (all zeros) means that state is not used and is entirely bypassed (no hold times). |

BROWNOUT LEVEL 4 THRESHOLD (0x205C)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | BDE_L4_VTHRESH[7:0] | | | | | | | |
| Reset | 0b00000000 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------------|------|---|
| BDE_L4_VTHRESH | 7:0 | BDE_Ln_VTHRESH[7:0] Sets the trigger level for each threshold in the brownout controller. Refer to the measurement ADC CH0 (VBAT) result register to set these |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|---|
| | | levels. A value of 0000 0000 (all zeros) means that state is not used and is entirely bypassed (no hold times). |

BROWNOUT THRESHOLD HYSTERYISIS (0x205D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------------|---|---|---|---|---|---|---|
| Field | BDE_VTHRESH_HYST[7:0] | | | | | | | |
| Reset | 0b00000000 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------|------|---|--|
| BDE_VTHRESH_HYST | 7:0 | BDE_VTHRESH_HYST[7:0] Sets a hysteresis value for the threshold levels. Refer to the measurement ADC CH0 (VBAT) result register for details of the LSB size. | 00000000: No hysteresis 00000001: 1 LSB of hysteresis 00000010: 2 LSBs of hysteresis ...: 1 LSB steps 11111101: 253 LSBs of hysteresis 11111110: 254 LSBs of hysteresis 11111111: 255 LSBs of hysteresis |

BROWNOUT AMP LIMITER ATTACK RELEASE (0x205E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|---|---|---|------------------|---|---|---|
| Field | AMP_LIM_ATK[3:0] | | | | AMP_LIM_RLS[3:0] | | | |
| Reset | 0b0000 | | | | 0b0000 | | | |
| Access Type | Write, Read | | | | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------|------|---|---|
| AMP_LIM_ATK | 7:4 | Selects the attack rate for the gain change. | 0000: 10µs/dB 0001: 20µs/dB 0010: 40µs/dB 0011: 80µs/dB 0100: 160µs/dB 0101: 320µs/dB 0110: 640µs/dB 0111: 1.28ms/dB 1000: 2.56ms/dB 1001: 5.12ms/dB 1010: 10.24ms/dB 1011: 20.48ms/dB 1100: 40.96ms/dB 1101: 81.92ms/dB 1110: 163.84ms/dB 1111: 327.68ms/dB |
| AMP_LIM_RLS | 3:0 | Selects the release rate for the gain change. | 0000: 40µs/dB 0001: 80µs/dB 0010: 160µs/dB 0011: 320µs/dB 0100: 640µs/dB 0101: 1.28ms/dB 0110: 2.56ms/dB 0111: 5.12ms/dB |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-------------|---|
| | | | 1000: 10.24ms/dB 1001: 20.48ms/dB 1010: 40.96ms/dB 1011: 81.92ms/dB 1100: 163.84ms/dB 1101: 327.68ms/dB 1110: 655.36ms/dB 1111: 1310.72ms/dB |

BROWNOUT AMP GAIN ATTACK RELEASE (0x205F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|---|---|---|-------------------|---|---|---|
| Field | AMP_GAIN_ATK[3:0] | | | | AMP_GAIN_RLS[3:0] | | | |
| Reset | 0b0001 | | | | 0b1111 | | | |
| Access Type | Write, Read | | | | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------|------|---|--|
| AMP_GAIN_ATK | 7:4 | Selects the attack rate for the gain change. | 0000: Instantaneous (step change, no ramp) 0001: 10µs/dB 0010: 20µs/dB 0011: 40µs/dB 0100: 80µs/dB 0101: 160µs/dB 0110: 320µs/dB 0111: 640µs/dB 1000: 1.28ms/dB 1001: 2.56ms/dB 1010: 5.12ms/dB 1011: 10.24ms/dB 1100: 20.48ms/dB 1101: 40.96ms/dB 1110: 81.92ms/dB 1111: 163.84ms/dB |
| AMP_GAIN_RLS | 3:0 | Selects the release rate for the gain change. | 0000: 40µs/dB 0001: 80µs/dB 0010: 160µs/dB 0011: 320µs/dB 0100: 640µs/dB 0101: 1.28ms/dB 0110: 2.56ms/dB 0111: 5.12ms/dB 1000: 10.24ms/dB 1001: 20.48ms/dB 1010: 40.96ms/dB 1011: 81.92ms/dB 1100: 163.84ms/dB 1101: 327.68ms/dB 1110: 655.36ms/dB 1111: 1310.72ms/dB |

BROWNOUT AMP1 CLIP MODE (0x2060)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|---|---|---------------|
| Field | – | – | – | – | – | – | – | AMP_CLIP_MODE |
| Reset | – | – | – | – | – | – | – | 0b0 |
| Access Type | – | – | – | – | – | – | – | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------|------|--|---|
| AMP_CLIP_MODE | 0 | Controls how clip level changes are applied. | 0: Clip release level changes occur on zero crossing event 1: Clip release level changes occur as soon as possible |

BROWNOUT LEVEL 1 CURRENT LIMIT (0x2061)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|------------------|---|---|---|---|---|---|
| Field | – | BDE_L1_ILIM[6:0] | | | | | | |
| Reset | – | 0b000000 | | | | | | |
| Access Type | – | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------|------|---|---|
| BDE_L1_ILIM | 6:0 | Sets the override for the boost converter input current limit for each threshold level. | 0000000: 0.00A 0000001: 0.50A 0000010: 1.00A 0000011: 1.05A ...: in 0.05A steps 0111111: 4.05A 1000000: 4.10A 1000001 to 1111111: Reserved |

BROWNOUT LEVEL 1 AMP 1 CONTROL 1 (0x2062)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|----------------------|---|---|---|
| Field | – | – | – | – | BDE_L1_AMP1_LIM[3:0] | | | |
| Reset | – | – | – | – | 0b0000 | | | |
| Access Type | – | – | – | – | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------|------|--|--|
| BDE_L1_AMP1_LIM | 3:0 | Sets the limiter threshold for critical battery level n. | 0: 0dBFS 1: -1dBFS 2: -2dBFS: in -1dBFS steps 14: -14dBFS 15: -15dBFS |

BROWNOUT LEVEL 1 AMP 1 CONTROL 2 (0x2063)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-----------------------|---|---|---|---|---|
| Field | – | – | BDE_L1_AMP1_CLIP[5:0] | | | | | |
| Reset | – | – | 0b000000 | | | | | |
| Access Type | – | – | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------|------|--|--|
| BDE_L1_AMP1_CLIP | 5:0 | Sets the threshold at which clipping occurs in the digital signal processing for critical battery level n. | 000000: 0dB 000001: -0.25dB 000010: -0.50dB 000011: -0.75dB 000100: -1.00dB 000101: -1.25dB: in -0.25dB steps 111010: -14.50dB 111011: -14.75dB 111100: -15.00dB 111101 to 111111: Reserved |

BROWNOUT LEVEL 1 AMP 1 CONTROL 3 (0x2064)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-----------------------|---|---|---|---|---|
| Field | – | – | BDE_L1_AMP1_GAIN[5:0] | | | | | |
| Reset | – | – | 0b000000 | | | | | |
| Access Type | – | – | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------|------|---|--|
| BDE_L1_AMP1_GAIN | 5:0 | Sets the gain reduction for critical battery level n. | 000000: 0dB 000001: -0.25dB 000010: -0.50dB 000011: -0.75dB 000100: -1.00dB 000101: -1.25dB: in -0.25dB steps 111010: -14.50dB 111011: -14.75dB 111100: -15.00dB 111101 to 111111: Reserved |

BROWNOUT LEVEL 2 CURRENT LIMIT (0x2065)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|------------------|---|---|---|---|---|---|
| Field | – | BDE_L2_ILIM[6:0] | | | | | | |
| Reset | – | 0b000000 | | | | | | |
| Access Type | – | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------|------|---|--|
| BDE_L2_ILIM | 6:0 | Sets the override for the boost converter input current limit for each threshold level. | 0000000: 0.00A 0000001: 0.50A 0000010: 1.00A |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-------------|--|
| | | | 000011: 1.05A ...: in 0.05A steps 0111111: 4.05A 1000000: 4.10A 1000001 to 1111111: Reserved |

BROWNOUT LEVEL 2 AMP 1 CONTROL 1 (0x2066)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|----------------------|---|---|---|
| Field | – | – | – | – | BDE_L2_AMP1_LIM[3:0] | | | |
| Reset | – | – | – | – | 0b0000 | | | |
| Access Type | – | – | – | – | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------|------|--|--|
| BDE_L2_AMP1_LIM | 3:0 | Sets the limiter threshold for critical battery level n. | 0: 0dBFS 1: -1dBFS 2: -2dBFS: in -1dBFS steps 14: -14dBFS 15: -15dBFS |

BROWNOUT LEVEL 2 AMP 1 CONTROL 2 (0x2067)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-----------------------|---|---|---|---|---|
| Field | – | – | BDE_L2_AMP1_CLIP[5:0] | | | | | |
| Reset | – | – | 0b000000 | | | | | |
| Access Type | – | – | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------|------|--|---|
| BDE_L2_AMP1_CLIP | 5:0 | Sets the threshold at which clipping occurs in the digital signal processing for critical battery level n. | 000000: 0dB 000001: -0.25dB 000010: -0.50dB 000011: -0.75dB 000100: -1.00dB 000101: -1.25dB: in -0.25dB steps 111010: -14.50dB 111011: -14.75dB 111100: -15.00dB 111101 to 111111: Reserved |

BROWNOUT LEVEL 2 AMP 1 CONTROL 3 (0x2068)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-----------------------|---|---|---|---|---|
| Field | – | – | BDE_L2_AMP1_GAIN[5:0] | | | | | |
| Reset | – | – | 0b000000 | | | | | |
| Access Type | – | – | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------------|------|---|---|
| BDE_L2_AM P1_GAIN | 5:0 | Sets the gain reduction for critical battery level n. | 000000: 0dB 000001: -0.25dB 000010: -0.50dB 000011: -0.75dB 000100: -1.00dB 000101: -1.25dB: in -0.25dB steps 111010: -14.50dB 111011: -14.75dB 111100: -15.00dB 111101 to 111111: Reserved |

BROWNOUT LEVEL 3 CURRENT LIMIT (0x2069)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|------------------|---|---|---|---|---|---|
| Field | – | BDE_L3_ILIM[6:0] | | | | | | |
| Reset | – | 0b000000 | | | | | | |
| Access Type | – | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------|------|---|---|
| BDE_L3_ILIM | 6:0 | Sets the override for the boost converter input current limit for each threshold level. | 0000000: 0.00A 0000001: 0.50A 0000010: 1.00A 0000011: 1.05A ...: in 0.05A steps 0111111: 4.05A 1000000: 4.10A 1000001 to 1111111: Reserved |

BROWNOUT LEVEL 3 AMP 1 CONTROL 1 (0x206A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|----------------------|---|---|---|
| Field | – | – | – | – | BDE_L3_AMP1_LIM[3:0] | | | |
| Reset | – | – | – | – | 0b0000 | | | |
| Access Type | – | – | – | – | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------|------|--|--|
| BDE_L3_AMP1_LIM | 3:0 | Sets the limiter threshold for critical battery level n. | 0: 0dBFS 1: -1dBFS 2: -2dBFS: in -1dBFS steps 14: -14dBFS 15: -15dBFS |

BROWNOUT LEVEL 3 AMP 1 CONTROL 2 (0x206B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-----------------------|---|---|---|---|---|
| Field | – | – | BDE_L3_AMP1_CLIP[5:0] | | | | | |
| Reset | – | – | 0b000000 | | | | | |
| Access Type | – | – | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------------|------|--|---|
| BDE_L3_AM P1_CLIP | 5:0 | Sets the threshold at which clipping occurs in the digital signal processing for critical battery level n. | 000000: 0dB 000001: -0.25dB 000010: -0.50dB 000011: -0.75dB 000100: -1.00dB 000101: -1.25dB: in -0.25dB steps 111010: -14.50dB 111011: -14.75dB 111100: -15.00dB 111101 to 111111: Reserved |

BROWNOUT LEVEL 3 AMP 1 CONTROL 3 (0x206C)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-----------------------|---|---|---|---|---|
| Field | – | – | BDE_L3_AMP1_GAIN[5:0] | | | | | |
| Reset | – | – | 0b000000 | | | | | |
| Access Type | – | – | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------------|------|---|---|
| BDE_L3_AM P1_GAIN | 5:0 | Sets the gain reduction for critical battery level n. | 000000: 0dB 000001: -0.25dB 000010: -0.50dB 000011: -0.75dB 000100: -1.00dB 000101: -1.25dB: in -0.25dB steps 111010: -14.50dB 111011: -14.75dB 111100: -15.00dB 111101 to 111111: Reserved |

BROWNOUT LEVEL 4 CURRENT LIMIT (0x206D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|------------------|---|---|---|---|---|---|
| Field | – | BDE_L4_ILIM[6:0] | | | | | | |
| Reset | – | 0b000000 | | | | | | |
| Access Type | – | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------|------|---|---|
| BDE_L4_ILI M | 6:0 | Sets the override for the boost converter input current limit for each threshold level. | 0000000: 0.00A 0000001: 0.50A 0000010: 1.00A 0000011: 1.05A ...: in 0.05A steps 0111111: 4.05A 1000000: 4.10A 1000001 to 1111111: Reserved |

BROWNOUT LEVEL 4 AMP 1 CONTROL 1 (0x206E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|----------------------|---|---|---|
| Field | – | – | – | – | BDE_L4_AMP1_LIM[3:0] | | | |
| Reset | – | – | – | – | 0b0000 | | | |
| Access Type | – | – | – | – | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------|------|--|--|
| BDE_L4_AMP1_LIM | 3:0 | Sets the limiter threshold for critical battery level n. | 0: 0dBFS 1: -1dBFS 2: -2dBFS: in -1dBFS steps 14: -14dBFS 15: -15dBFS |

BROWNOUT LEVEL 4 AMP 1 CONTROL 2 (0x206F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|---|-----------------------|---|---|---|---|---|
| Field | BDE_L4_AMP1_MUTE | – | BDE_L4_AMP1_CLIP[5:0] | | | | | |
| Reset | 0b0 | – | 0b000000 | | | | | |
| Access Type | Write, Read | – | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------|------|--|---|
| BDE_L4_AMP1_MUTE | 7 | Brownout level 4 mute. Mutes the audio stream when the battery reaches critical level 4. | 0: Not muted at critical level 4. 1: Mute active at critical level 4. |
| BDE_L4_AMP1_CLIP | 5:0 | Sets the threshold at which clipping occurs in the digital signal processing for critical battery level n. | 000000: 0dB 000001: -0.25dB 000010: -0.50dB 000011: -0.75dB 000100: -1.00dB 000101: -1.25dB: in -0.25dB steps 111010: -14.50dB 111011: -14.75dB 111100: -15.00dB 111101 to 111111: Reserved |

BROWNOUT LEVEL 4 AMP 1 CONTROL 3 (0x2070)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-----------------------|---|---|---|---|---|
| Field | – | – | BDE_L4_AMP1_GAIN[5:0] | | | | | |
| Reset | – | – | 0b000000 | | | | | |
| Access Type | – | – | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------|------|---|--|
| BDE_L4_AMP1_GAIN | 5:0 | Sets the gain reduction for critical battery level n. | 000000: 0dB 000001: -0.25dB 000010: -0.50dB 000011: -0.75dB |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-------------|---|
| | | | 000100: -1.00dB 000101: -1.25dB: in -0.25dB steps 111010: -14.50dB 111011: -14.75dB 111100: -15.00dB 111101 to 111111: Reserved |

BROWNOUT LOWEST STATUS (0x2071)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|-----------------|---|---|
| Field | – | – | – | – | – | BDE_LOWEST[2:0] | | |
| Reset | – | – | – | – | – | 0b000 | | |
| Access Type | – | – | – | – | – | Read, Ext | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------|------|--|---|
| BDE_LOWEST | 2:0 | Reports the lowest BDE level (highest level number) since the last read. | 000: Brownout idle - normal operation 001: Level 1 010: Level 2 011: Level 3 100: Level 4 101 to 111: Reserved |

BROWNOUT ILIM HOLD (0x2072)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|---|---|---|---|---|---|---|
| Field | BDE_ILIM_HLD[7:0] | | | | | | | |
| Reset | 0b00000000 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------|------|------------------------------------|--|
| BDE_ILIM_HLD | 7:0 | Sets the hold time for boost ILIM. | 0x00: 0ms 0x01: 0.1ms 0x02: 1ms: 1ms steps 0xFD: 252ms 0xFE: 253ms 0xFF: 254ms |

BROWNOUT LIM HOLD (0x2073)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|---|---|---|---|---|---|---|
| Field | BDE_LIM_HLD[7:0] | | | | | | | |
| Reset | 0b00000000 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------|------|---------------------------------|--------------------------|
| BDE_LIM_HLD | 7:0 | Sets the hold time for limiter. | 0x00: 0ms 0x01: 0.1ms |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-------------|--|
| | | | 0x02: 1ms ...: 1ms steps 0xFD: 252ms 0xFE: 253ms 0xFF: 254ms |

BROWNOUT CLIP HOLD (0x2074)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-------------------|---|---|---|---|---|---|---|
| Field | BDE_CLIP_HLD[7:0] | | | | | | | |
| Reset | 0b00000000 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------|------|--|--|
| BDE_CLIP_HLD | 7:0 | Sets the hold time for clipper function. | 0x00: 0ms 0x01: 0.1ms 0x02: 1ms ...: 1ms steps 0xFD: 252ms 0xFE: 253ms 0xFF: 254ms |

BROWNOUT GAIN HOLD (0x2075)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-------------------|---|---|---|---|---|---|---|
| Field | BDE_GAIN_HLD[7:0] | | | | | | | |
| Reset | 0b00000000 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------|------|---------------------------------------|--|
| BDE_GAIN_HLD | 7:0 | Sets the hold time for gain function. | 0x00: 0ms 0x01: 0.1ms 0x02: 1ms ...: 1ms steps 0xFD: 252ms 0xFE: 253ms 0xFF: 254ms |

ENV TRACKER VOUT HEADROOM (0x2076)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|---|---|---|------------------------------------|---|---|---|---|
| Field | – | – | – | ENV_TRACKER_BST_VOUT_HEADROOM[4:0] | | | | |
| Reset | – | – | – | 0b01111 | | | | |
| Access Type | – | – | – | Write, Read | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------------------|------|---|---|
| ENV_TRACKER_BST_VOUT_HEADR | 4:0 | Boost voltage output headroom for envelope tracker. | 00000: 0.000V 00001: 0.125V 00010: 0.250V |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-------------|--|
| OOM | | | 00011: 0.375V 00100: 0.500V 00101: 0.625V 00110: 0.750V 00111: 0.875V 01000: 1.000V 01001: 1.125V 01010: 1.250V 01011: 1.375V 01100: 1.500V 01101: 1.625V 01110: 1.750V 01111: 1.875V 10000: 2.000V 10001: 2.125V 10010: 2.250V 10011: 2.375V 10100: 2.500V 10101: 2.625V 10110: 2.750V 10111: 2.875V 11000: 3.000V 11001: 3.125V 11010: 3.250V 11011: 3.375V 11100: 3.500V 11101 to 11111: Reserved |

ENV TRACKER BOOST VOUT DELAY (0x2077)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|----------------------|---|--------------------|---|---|---|---|---|
| Field | ENV_TRACKER_BDE_MODE | – | ENV_BYP_DELAY[5:0] | | | | | |
| Reset | 0b1 | – | 0b000000 | | | | | |
| Access Type | Write, Read | – | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------------|------|---|---|
| ENV_TRACKER_BDE_MODE | 7 | Mirror BDE gain adjustments and clipping at the front end of the envelope tracker boost bypass and FET scaling threshold detectors. | 0: Do not mirror BDE gain adjustments and clipping at the front end of the envelope tracker boost bypass and FET scaling threshold detectors. 1: Mirror BDE gain adjustments and clipping at the front end of the envelope tracker boost bypass and FET scaling threshold detectors. |
| ENV_BYP_DELAY | 5:0 | Delay time for the Envelope Tracker and Automatic Boost Bypass. Delays the audio output by N base rate samples. (N x FS) | 000000: No delay 000001: Delay 1 base rate sample 000010: Delay 2 base rate samples ... 011111: Delay 31 base rate samples 100000: Delay 32 base rate samples 100001 to 111111: Reserved |

ENV TRACKER RELEASE RATE (0x2078)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---------------------------------|---|---|---------------------------|---|---|
| Field | – | – | ENV_TRACKER_RLS_RATE_SCALE[1:0] | | – | ENV_TRACKER_RLS_RATE[2:0] | | |
| Reset | – | – | 0b00 | | – | 0b111 | | |
| Access Type | – | – | Write, Read | | – | Write, Read | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------------------|------|---|--|
| ENV_TRACKER_RLS_RATE_SCALE | 5:4 | Scaling factor for envelope tracker release rate as controlled by ENV_TRACKER_RLS_RATE. | 00: No scaling 01: 2x faster 10: 2x slower 11: 4x slower |
| ENV_TRACKER_RLS_RATE | 2:0 | Boost gain reduction rate. This setting should be used together with ENV_TRACKER_RLS_RATE_SCALE. The decode shown assumes no scaling. | 000: 10ms/V 001: 50ms/V 010: 100ms/V 011: 250ms/V 100: 500ms/V 101: 750ms/V 110: 1000ms/V 111: 1500ms/V |

ENV TRACKER HOLD RATE (0x2079)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|----------------------------|---|---|
| Field | – | – | – | – | – | ENV_TRACKER_HOLD_RATE[2:0] | | |
| Reset | – | – | – | – | – | 0b111 | | |
| Access Type | – | – | – | – | – | Write, Read | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------------|------|--|--|
| ENV_TRACKER_HOLD_RATE | 2:0 | Sets the hold time before the envelope tracker starts boost output voltage decrease. | 000: 10ms 001: 50ms 010: 100ms 011: 250ms 100: 500ms 101: 750ms 110: 1000ms 111: 1500ms |

ENV TRACKER CONTROL (0x207A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|---|---|----------------|
| Field | – | – | – | – | – | – | – | ENV_TRACKER_EN |
| Reset | – | – | – | – | – | – | – | 0b1 |
| Access Type | – | – | – | – | – | – | – | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------|------|---|---|
| ENV_TRACKER_EN | 0 | Enable the boost output envelope tracker. | 0: Disable boost envelope tracker 1: Enable boost envelope tracker |

ENV TRACKER BOOST VOUT READBACK (0x207B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|------------------------------|---|---|---|---|
| Field | – | – | – | ENV_TRACKER_BST_VOUT_RD[4:0] | | | | |
| Reset | – | – | – | 0b00000 | | | | |
| Access Type | – | – | – | Read Only | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------------------|------|--|---|
| ENV_TRACKER_BST_VOUT_RD | 4:0 | <p>ENV_TRACKER_BST_VOUT_RD Boost output voltage readback:</p> <ul style="list-style-type: none"> When EN = 0, this register reads-back 00000 as all circuit blocks are in reset. When EN = 1, and the envelope tracker is disabled, this register reads-back the programmed boost output value set by BST_VOUT. When EN = 1, and the envelope tracker is enabled, this register reads-back the boost output value as set by the envelope tracker circuit. | <p>00000: 6.500V 00001: 6.625V 00010: 6.750V 00011: 6.875V 00100: 7.000V 00101: 7.125V 00110: 7.250V 00111: 7.375V 01000: 7.500V 01001: 7.625V 01010: 7.750V 01011: 7.875V 01100: 8.000V 01101: 8.125V 01110: 8.250V 01111: 8.375V 10000: 8.500V 10001: 8.625V 10010: 8.750V 10011: 8.875V 10100: 9.000V 10101: 9.125V 10110: 9.250V 10111: 9.375V 11000: 9.500V 11001: 9.625V 11010: 9.750V 11011: 9.875V 11100: 10.000V 11101 to 11111: Reserved</p> |

BOOST BYPASS 1 (0x207C)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---------------------|---|---|-----------------------|---|---|---|
| Field | – | BST_CURRLIM_MASK_EN | – | – | BST_BYP_HEADROOM[3:0] | | | |
| Reset | – | 0b1 | – | – | 0b1001 | | | |
| Access Type | – | Write, Read | – | – | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------------|------|--|--|
| BST_CURRLIM_MASK_EN | 6 | Enables the boost current limit interrupt masking timer. | <p>0: Disable boost current limit interrupt masking timer 1: Enable boost current limit interrupt masking timer</p> |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------------|------|--|--|
| BST_BYP_H EADROOM | 3:0 | Sets the amount of headroom between V_{VBAT} and the boost bypass threshold. | 0000: 0.0mV 0001: 125mV 0010: 250mV 0011: 375mV ...: ... 1101: 1625mV 1110: 1750mV 1111: 1875mV |

BOOST BYPASS 2 (0x207D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|-----------------------------|---|---|---|---|-------------------|---|
| Field | – | BST_CURRLIM_MASK_TIMER[3:0] | | | | – | BST_BYP_MODE[1:0] | |
| Reset | – | 0b0101 | | | | – | 0b11 | |
| Access Type | – | Write, Read | | | | – | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------------|------|--|--|
| BST_CURRLIM_MASK_TIMER | 6:3 | Sets the amount of time that the interrupt needs to be masked every time the boost bypass exits. | 0000: 20µs 0001: 40µs 0010: 80µs 0011: 160µs 0100: 320µs 0101: 640µs 0110: 1.28ms 0111: 2.56ms 1000: 5.12ms 1001: 10.24ms 1010: 20.48ms 1011 to 1111: Reserved |
| BST_BYP_MODE | 1:0 | Sets the boost bypass mode. | 00: Automatic boost bypass—Boost is automatically turned on and off depending on V_{VBAT} and the audio signal amplitude. The measurement ADC is automatically configured to monitor V_{VBAT} . When EN is changed from 0 to 1, the boost is forced to turn on. Automatic boost bypass can then turn off the boost after it determines whether the boost is needed. 01: Boost bypass on—Boost does not switch. 10: Boost bypass off—Boost is on. 11: Automatic boost bypass—Boost is automatically turned on and off depending on V_{VBAT} and the audio signal amplitude. The measurement ADC is automatically configured to monitor V_{VBAT} . When EN is changed from 0 to 1, the boost stays off until automatic boost bypass determines whether the boost is needed. |

BOOST BYPASS 3 (0x207E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|------------------------|---|---|---|
| Field | – | – | – | – | BST_BYP_HOLD_TIME[3:0] | | | |
| Reset | – | – | – | – | 0b1000 | | | |
| Access Type | – | – | – | – | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------------|------|---|--|
| BST_BYP_HOLD_TIME | 3:0 | Sets the amount of time that the audio signal needs to be below the boost bypass threshold before the boost is allowed to stop switching and go into bypass mode. | 0000: 10ms 0001: 20ms 0010: 60ms 0011: 110ms 0100: 260ms 0101: 510ms 0110: 760ms 0111: 1.0s 1000: 1.5s 1001: 2.0s 1010: 2.5s 1011: 3.0s 1100: 3.5s 1101: 4.0s 1110: 4.5s 1111: 5.0s |

FET SCALING 1 (0x207F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|---|--------------------------|---|
| Field | – | – | – | – | – | – | AMP_FET_SCALE_MODE [1:0] | |
| Reset | – | – | – | – | – | – | 0b00 | |
| Access Type | – | – | – | – | – | – | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------------|------|--------------------------------------|---|
| AMP_FET_SCALE_MODE | 1:0 | Sets the amplifier FET scaling mode. | 00: Automatic amplifier FET scaling 01: Amplifier FETs are forced to maximum size 10: Amplifier FETs are forced to 1/4 size 11: Reserved |

FET SCALING 2 (0x2080)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|------------------------------|---|---|---|---|
| Field | – | – | – | AMP_FET_SCALE_THRESHOLD[4:0] | | | | |
| Reset | – | – | – | 0b00011 | | | | |
| Access Type | – | – | – | Write, Read | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------------------|------|---|---|
| AMP_FET_SCALE_THRESHOLD | 4:0 | Sets the signal threshold amplitude above which the FETs are scaled to their maximum size. When AMP_FET_SCALE_THRESHOLD is set to | 00000: -15.3271dBV _{PK} , 0.171V _{PK} 00001: -14.3896dBV _{PK} , 0.191V _{PK} 00010: -13.4521dBV _{PK} , 0.213V _{PK} |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|---|
| | | 11111b (and AMP_FET_SCALE_MODE is 00b), 1/4 size FETs are used when the boost is in bypass mode and full size FETs are used when the boost is on. | 11100: 10.9229dBV _{PK} , 3.517V _{PK} 11101: 11.8604dBV _{PK} , 3.918V _{PK} 11110: 12.7979dBV _{PK} , 4.364V _{PK} 11111: Controlled by boost bypass |

FET SCALING 3 (0x2081)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|-------------------------|---|---|---|
| Field | – | – | – | – | AMP_FET_SCALE_HYST[3:0] | | | |
| Reset | – | – | – | – | 0b0000 | | | |
| Access Type | – | – | – | – | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------------|------|--|---|
| AMP_FET_SCALE_HYST | 3:0 | Sets the amplifier FET scaling hysteresis. | 0000: 0.00000 0001: 0.46875 0010: 0.93750 0011: 1.40625 0100: 1.8750 0101: 2.34375 0110: 2.81250 0111: 3.28125 1000 to 1111: Reserved |

FET SCALING 4 (0x2082)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|------------------------------|---|---|---|
| Field | – | – | – | – | AMP_FET_SCALE_HOLD_TIME[3:0] | | | |
| Reset | – | – | – | – | 0b0111 | | | |
| Access Type | – | – | – | – | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------------------|------|---|--|
| AMP_FET_SCALE_HOLD_TIME | 3:0 | Sets the amount of time that the audio signal needs to be below the amplifier FET scaling threshold minus the amplifier FET scaling hysteresis before the FET scale is allowed to reduce to 1/4 size. | 0000: 10ms 0001: 20ms 0010: 60ms 0011: 110ms 0100: 260ms 0101: 510ms 0110: 760ms 0111: 1.0s 1000: 1.5s 1001: 2.0s 1010: 2.5s 1011: 3.0s 1100: 3.5s 1101: 4.0s 1110: 4.5s 1111: 5.0s |

ADVANCED SETTINGS (0x2084)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|---|---|---|---|---|---|---|-----------------|
| Field | – | – | – | – | – | – | – | SPK_SPEE DUP |
| Reset | – | – | – | – | – | – | – | 0b1 |
| Access Type | – | – | – | – | – | – | – | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------|------|--|---|
| SPK_SPEED UP | 0 | Speaker state machine speed up option. | 0: Normal speaker PLAY signal startup time 1: Speedup speaker PLAY signal startup time |

DSM_EQ_BQ1_B0_BYTE0 (0x2129)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ1_B0[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ1_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ1_B0_BYTE1 (0x212A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ1_B0[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ1_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ1_B0_BYTE2 (0x212B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ1_B0[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ1_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ1_B1_BYTE0 (0x212D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ1_B1[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ1_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ1_B1_BYTE1 (0x212E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ1_B1[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ1_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ1_B1_BYTE2 (0x212F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ1_B1[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ1_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ1_B2_BYTE0 (0x2131)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ1_B2[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ1_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ1_B2_BYTE1 (0x2132)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ1_B2[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ1_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ1_B2_BYTE2 (0x2133)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ1_B2[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ1_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ1_A1_BYTE0 (0x2135)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ1_A1[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ1_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ1_A1_BYTE1 (0x2136)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ1_A1[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ1_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ1_A1_BYTE2 (0x2137)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ1_A1[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ1_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ1_A2_BYTE0 (0x2139)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ1_A2[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ1_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ1_A2_BYTE1 (0x213A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ1_A2[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ1_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ1_A2_BYTE2 (0x213B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ1_A2[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ1_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ2_B0_BYTE0 (0x213D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ2_B0[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ2_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ2_B0_BYTE1 (0x213E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ2_B0[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ2_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ2_B0_BYTE2 (0x213F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ2_B0[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ2_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ2_B1_BYTE0 (0x2141)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ2_B1[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ2_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ2_B1_BYTE1 (0x2142)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ2_B1[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ2_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ2_B1_BYTE2 (0x2143)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ2_B1[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ2_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ2_B2_BYTE0 (0x2145)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ2_B2[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ2_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ2_B2_BYTE1 (0x2146)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ2_B2[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ2_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ2_B2_BYTE2 (0x2147)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ2_B2[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ2_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ2_A1_BYTE0 (0x2149)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ2_A1[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ2_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ2_A1_BYTE1 (0x214A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ2_A1[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ2_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ2_A1_BYTE2 (0x214B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ2_A1[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ2_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ2_A2_BYTE0 (0x214D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ2_A2[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ2_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ2_A2_BYTE1 (0x214E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ2_A2[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ2_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ2_A2_BYTE2 (0x214F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ2_A2[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ2_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ3_B0_BYTE0 (0x2151)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ3_B0[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ3_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ3_B0_BYTE1 (0x2152)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ3_B0[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ3_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ3_B0_BYTE2 (0x2153)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ3_B0[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ3_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ3_B1_BYTE0 (0x2155)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ3_B1[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ3_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ3_B1_BYTE1 (0x2156)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ3_B1[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ3_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ3_B1_BYTE2 (0x2157)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ3_B1[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ3_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ3_B2_BYTE0 (0x2159)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ3_B2[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ3_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ3_B2_BYTE1 (0x215A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ3_B2[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ3_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ3_B2_BYTE2 (0x215B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ3_B2[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ3_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ3_A1_BYTE0 (0x215D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ3_A1[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ3_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ3_A1_BYTE1 (0x215E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ3_A1[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ3_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ3_A1_BYTE2 (0x215F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ3_A1[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ3_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ3_A2_BYTE0 (0x2161)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ3_A2[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ3_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ3_A2_BYTE1 (0x2162)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ3_A2[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ3_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ3_A2_BYTE2 (0x2163)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ3_A2[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ3_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ4_B0_BYTE0 (0x2165)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ4_B0[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ4_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ4_B0_BYTE1 (0x2166)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ4_B0[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ4_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ4_B0_BYTE2 (0x2167)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ4_B0[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ4_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ4_B1_BYTE0 (0x2169)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ4_B1[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ4_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ4_B1_BYTE1 (0x216A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ4_B1[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ4_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ4_B1_BYTE2 (0x216B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ4_B1[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ4_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ4_B2_BYTE0 (0x216D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ4_B2[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ4_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ4_B2_BYTE1 (0x216E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ4_B2[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ4_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ4_B2_BYTE2 (0x216F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ4_B2[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ4_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ4_A1_BYTE0 (0x2171)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ4_A1[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ4_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ4_A1_BYTE1 (0x2172)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ4_A1[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ4_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ4_A1_BYTE2 (0x2173)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ4_A1[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ4_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ4_A2_BYTE0 (0x2175)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ4_A2[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ4_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ4_A2_BYTE1 (0x2176)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ4_A2[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ4_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ4_A2_BYTE2 (0x2177)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ4_A2[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ4_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ5_B0_BYTE0 (0x2179)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ5_B0[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ5_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ5_B0_BYTE1 (0x217A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ5_B0[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ5_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ5_B0_BYTE2 (0x217B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ5_B0[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ5_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ5_B1_BYTE0 (0x217D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ5_B1[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ5_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ5_B1_BYTE1 (0x217E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ5_B1[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ5_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ5_B1_BYTE2 (0x217F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ5_B1[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ5_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ5_B2_BYTE0 (0x2181)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ5_B2[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ5_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ5_B2_BYTE1 (0x2182)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ5_B2[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ5_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ5_B2_BYTE2 (0x2183)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ5_B2[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ5_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ5_A1_BYTE0 (0x2185)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ5_A1[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ5_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ5_A1_BYTE1 (0x2186)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ5_A1[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ5_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ5_A1_BYTE2 (0x2187)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ5_A1[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ5_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ5_A2_BYTE0 (0x2189)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ5_A2[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ5_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ5_A2_BYTE1 (0x218A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ5_A2[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ5_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ5_A2_BYTE2 (0x218B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ5_A2[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ5_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ6_B0_BYTE0 (0x218D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ6_B0[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ6_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ6_B0_BYTE1 (0x218E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ6_B0[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ6_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ6_B0_BYTE2 (0x218F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ6_B0[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ6_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ6_B1_BYTE0 (0x2191)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ6_B1[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ6_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ6_B1_BYTE1 (0x2192)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ6_B1[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ6_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ6_B1_BYTE2 (0x2193)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ6_B1[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ6_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ6_B2_BYTE0 (0x2195)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ6_B2[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ6_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ6_B2_BYTE1 (0x2196)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ6_B2[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ6_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ6_B2_BYTE2 (0x2197)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ6_B2[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ6_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ6_A1_BYTE0 (0x2199)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ6_A1[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ6_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ6_A1_BYTE1 (0x219A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ6_A1[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ6_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ6_A1_BYTE2 (0x219B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ6_A1[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ6_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ6_A2_BYTE0 (0x219D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ6_A2[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ6_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ6_A2_BYTE1 (0x219E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ6_A2[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ6_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ6_A2_BYTE2 (0x219F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ6_A2[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ6_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ7_B0_BYTE0 (0x21A1)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ7_B0[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ7_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ7_B0_BYTE1 (0x21A2)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ7_B0[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ7_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ7_B0_BYTE2 (0x21A3)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ7_B0[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ7_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ7_B1_BYTE0 (0x21A5)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ7_B1[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ7_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ7_B1_BYTE1 (0x21A6)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ7_B1[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ7_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ7_B1_BYTE2 (0x21A7)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ7_B1[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ7_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ7_B2_BYTE0 (0x21A9)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ7_B2[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ7_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ7_B2_BYTE1 (0x21AA)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ7_B2[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ7_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ7_B2_BYTE2 (0x21AB)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ7_B2[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ7_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ7_A1_BYTE0 (0x21AD)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ7_A1[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ7_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ7_A1_BYTE1 (0x21AE)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ7_A1[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ7_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ7_A1_BYTE2 (0x21AF)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ7_A1[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ7_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ7_A2_BYTE0 (0x21B1)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ7_A2[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ7_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ7_A2_BYTE1 (0x21B2)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ7_A2[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ7_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ7_A2_BYTE2 (0x21B3)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ7_A2[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ7_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ8_B0_BYTE0 (0x21B5)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ8_B0[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ8_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ8_B0_BYTE1 (0x21B6)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ8_B0[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ8_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ8_B0_BYTE2 (0x21B7)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ8_B0[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ8_B0 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ8_B1_BYTE0 (0x21B9)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ8_B1[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ8_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ8_B1_BYTE1 (0x21BA)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ8_B1[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ8_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ8_B1_BYTE2 (0x21BB)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ8_B1[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ8_B1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ8_B2_BYTE0 (0x21BD)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ8_B2[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ8_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ8_B2_BYTE1 (0x21BE)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ8_B2[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ8_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ8_B2_BYTE2 (0x21BF)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ8_B2[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ8_B2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ8_A1_BYTE0 (0x21C1)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ8_A1[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ8_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ8_A1_BYTE1 (0x21C2)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ8_A1[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ8_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ8_A1_BYTE2 (0x21C3)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ8_A1[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ8_A1 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ8_A2_BYTE0 (0x21C5)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ8_A2[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ8_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ8_A2_BYTE1 (0x21C6)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ8_A2[15:8] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ8_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSM_EQ_BQ8_A2_BYTE2 (0x21C7)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field | DSM_EQ_BQ8_A2[23:16] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|---------------------------------------|
| DSM_EQ_BQ8_A2 | 7:0 | 24-bit fixed point coefficient <4.20> |

DSMIG WB DRC RELEASE TIME 1 (0x2380)

| | | | | | | | | |
|--------------------|---------------|----------|----------|----------|----------|----------|----------|----------|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | DRC_RLS[15:8] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------|-------------|---|--|
| DRC_RLS | 7:0 | Coefficient[15:0] fixed point <0,16> Real coefficient value = $2^6 / (F_s \times \text{Release_time} + 1)$ Fs: audio sample rate in Hz, Release_time: in seconds Decode shows examples at 48kHz sample rate. | 0x0000: Reserved 0x0001: 87400ms 0x0057: 1000ms 0x036A: 100ms 0x06D3: 50ms 0x2210: 10ms 0xFFFF: 1.3ms |

DSMIG WB DRC RELEASE TIME 2 (0x2381)

| | | | | | | | | |
|--------------------|--------------|----------|----------|----------|----------|----------|----------|----------|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | DRC_RLS[7:0] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------|-------------|---|--|
| DRC_RLS | 7:0 | Coefficient[15:0] fixed point <0,16> Real coefficient value = $2^6 / (F_s \times \text{Release_time} + 1)$ Fs: audio sample rate in Hz, Release_time: in seconds Decode shows examples at 48kHz sample rate. | 0x0000: Reserved 0x0001: 87400ms 0x0057: 1000ms 0x036A: 100ms 0x06D3: 50ms 0x2210: 10ms 0xFFFF: 1.3ms |

DSMIG WB DRC ATTACK TIME 1 (0x2382)

| | | | | | | | | |
|--------------------|---------------|----------|----------|----------|----------|----------|----------|----------|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | DRC_ATK[15:8] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|---|
| DRC_ATK | 7:0 | Coefficient[15:0] fixed point <0,16> Real coefficient value = $2^6 / (F_s \times \text{Attack_time} + 1)$ Fs: audio sample rate in Hz, Attack_time: in seconds Decode shows examples at 48kHz sample rate. | 0x0000: Reserved 0x0001: 87400ms 0x0057: 1000ms 0x036A: 100ms 0x06D3: 50ms 0x2210: 10ms 0xFFFF: 1.3ms |

DSMIG WB DRC ATTACK TIME 2 (0x2383)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field | DRC_ATK[7:0] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|---|
| DRC_ATK | 7:0 | Coefficient[15:0] fixed point <0,16> Real coefficient value = $2^6 / (F_s \times \text{Attack_time} + 1)$ Fs: audio sample rate in Hz, Attack_time: in seconds Decode shows examples at 48kHz sample rate. | 0x0000: Reserved 0x0001: 87400ms 0x0057: 1000ms 0x036A: 100ms 0x06D3: 50ms 0x2210: 10ms 0xFFFF: 1.3ms |

DSMIG WB DRC COMPRESSION RATIO (0x2384)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---------------------|---|---|---|
| Field | - | - | - | - | DRC_COMP_RATIO[3:0] | | | |
| Reset | - | - | - | - | 0x0 | | | |
| Access Type | - | - | - | - | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------|------|-------------------|--|
| DRC_COMP_RATIO | 3:0 | Compression ratio | 0x0: 1:1 0x1: 2:1 0x2: 3:1 0x3: 4:1 0x4: 5:1 0x5: 6:1 0x6: 7:1 0x7: 8:1 |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-------------|---|
| | | | 0x8: 9:1 0x9: 10:1 0xA: 11:1 0xB: 12:1 0xC: 13:1 0xD: 14:1 0xE: 15:1 0xF: 16:1 |

DSMIG WB DRC COMPRESSION THRESHOLD (0x2385)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|----------------------|---|---|---|---|---|
| Field | - | - | DRC_COMP_THRESH[5:0] | | | | | |
| Reset | - | - | 0x0 | | | | | |
| Access Type | - | - | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------|------|----------------------------------|---|
| DRC_COMP_THRESH | 5:0 | Compression threshold (1dB step) | 0x0: Reserved 0x1: 0dB 0x2: -1dB 0x3: -2dB 0x4: -3dB ...: 0x31: -48dB 0x32: -49dB 0x33: -50dB 0x34 to 0x3F: Reserved |

DSMIG WB DRC MAKEUPGAIN (0x2386)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---------------------|---|---|---|
| Field | - | - | - | - | DRC_MAKEUPGAIN[3:0] | | | |
| Reset | - | - | - | - | 0x0 | | | |
| Access Type | - | - | - | - | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------|------|-------------------------|--|
| DRC_MAKEUPGAIN | 3:0 | Make-up gain (1dB step) | 0x0: 0dB 0x1: 1dB 0x2: 2dB 0x3: 3dB 0x4: 4dB 0x5: 5dB 0x6: 6dB 0x7: 7dB 0x8: 8dB 0x9: 9dB 0xA: 10dB 0xB: 11dB 0xC: 12dB 0xD: 13dB 0xE: 14dB 0xF: 15dB |

DSMIG WB DRC NOISE GATE THRESHOLD (0x2387)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|--------------------|---|---|---|---|
| Field | - | - | - | DRC_NG_THRESH[4:0] | | | | |
| Reset | - | - | - | 0x0 | | | | |
| Access Type | - | - | - | Write, Read | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------|------|---|---|
| DRC_NG_THRESHOLD | 4:0 | Noise gate threshold (3dB steps, min -90dB) | 0x0: -29dB 0x1: -32dB 0x2: -35dB 0x3: -38dB 0x4: -41dB ... 0x13: -86dB 0x14: -89dB ... 0x1D: -89dB 0x1E: -89dB 0x1F: -89dB |

DSMIG WBDRC HPF ENABLE (0x2388)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|---|---|-------------|
| Field | - | - | - | - | - | - | - | DRC_HPF_EN |
| Reset | - | - | - | - | - | - | - | 0x0 |
| Access Type | - | - | - | - | - | - | - | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------|------|---|-------------------------|
| DRC_HPF_EN | 0 | If enabled, the WBDRC compresses the audio based on the evaluation of the highpass filtered data, otherwise it is based on the raw input data (unfiltered). | 0: Disable 1: Enable |

DSMIG PPR THRESHOLD (0x238B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-----------------|---|---|---|---|---|
| Field | - | - | PPR_THRESH[5:0] | | | | | |
| Reset | - | - | 0x0 | | | | | |
| Access Type | - | - | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------|------|-------------------------------------|---|
| PPR_THRESHOLD | 5:0 | PPR Threshold (1dB step, min -60dB) | 0x0: -20dB 0x1: -21dB 0x2: -22dB 0x3: -23dB 0x4: -24dB ... 0x28: -60dB ... |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-------------|-------------|
| | | | 0x3F: -60dB |

DSM TPROT THRESHOLD BYTE 0 (0x238E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|----------------------------|---|---|---|---|---|---|---|
| Field | DSM_TPROT_TEMP_THRESH[7:0] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------------|------|---|--|
| DSM_TPROT_TEMP_THRESH | 7:0 | Speaker coil temperature threshold. Above this threshold, the gain is reduced by the algorithm. 16-bit fixed point format <4,12>. Temperature threshold fixed point real = (temperature threshold °C)/100 Max temp 799.98°C, min temp -800°C, resolution 0.0244°C. | 0x0000: 0°C 0x0001: 0.0244°C ... 0x0400: 25.0°C ... 0x0CCD: 80.0°C ... 0x1000: 100.0°C ... 0x1333: 120.0°C ... 0x7FFF: 799.9°C 0x8000: -800.0°C ... 0xFFFFE: -0.0488°C 0xFFFFF: -0.0244°C |

DSM TPROT THRESHOLD BYTE 1 (0x238F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----------------------------|---|---|---|---|---|---|---|
| Field | DSM_TPROT_TEMP_THRESH[15:8] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------------|------|---|--|
| DSM_TPROT_TEMP_THRESH | 7:0 | Speaker coil temperature threshold. Above this threshold, the gain is reduced by the algorithm. 16-bit fixed point format <4,12>. Temperature threshold fixed point real = (temperature threshold °C)/100 Max temp 799.98°C, min temp -800°C, resolution 0.0244°C. | 0x0000: 0°C 0x0001: 0.0244°C ... 0x0400: 25.0°C ... 0x0CCD: 80.0°C ... 0x1000: 100.0°C ... 0x1333: 120.0°C ... 0x7FFF: 799.9°C 0x8000: -800.0°C ... 0xFFFFE: -0.0488°C |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-------------|-------------------|
| | | | 0xFFFF: -0.0244°C |

DSM TPROT ROOM TEMPERATURE BYTE0 (0x2390)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------------|---|---|---|---|---|---|---|
| Field | DSM_TPROT_ROOM_TEMP[7:0] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------------|------|---|---|
| DSM_TPROT_ROOM_TEMP | 7:0 | Temperature corresponding to room temperature for the thermal protection algorithm. 16-bit fixed point format <4,12>. Room temperature fixed point real = (room temperature °C)/100 Max temp 799.98°C, min temp -800°C, resolution 0.0244°C. | 0x0000: 0°C 0x0001: 0.0244°C ... 0x0400: 25.0°C ... 0x0CCD: 80.0°C ... 0x1000: 100.0°C ... 0x1333: 120.0°C ... 0x7FFF: 799.9°C 0x8000: -800.0°C ... 0xFFFFE: -0.0488°C 0xFFFF: -0.0244°C |

DSM TPROT ROOM TEMPERATURE BYTE 1 (0x2391)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------------|---|---|---|---|---|---|---|
| Field | DSM_TPROT_ROOM_TEMP[15:8] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------------|------|---|---|
| DSM_TPROT_ROOM_TEMP | 7:0 | Temperature corresponding to room temperature for the thermal protection algorithm. 16-bit fixed point format <4,12>. Room temperature fixed point real = (room temperature °C)/100 Max temp 799.98°C, min temp -800°C, resolution 0.0244°C. | 0x0000: 0°C 0x0001: 0.0244°C ... 0x0400: 25.0°C ... 0x0CCD: 80.0°C ... 0x1000: 100.0°C ... 0x1333: 120.0°C ... 0x7FFF: 799.9°C 0x8000: -800.0°C |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-------------|--|
| | | | 0xFFFFE: -0.0488°C 0xFFFFF: -0.0244°C |

DSM TPROT RECIP RDC ROOM BYTE0 (0x2392)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-------------------------------|---|---|---|---|---|---|---|
| Field | DSM_TPROT_RECIP_RDC_ROOM[7:0] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------------------|------|--|--|
| DSM_TPROT_RECIP_RDC_ROOM | 7:0 | Reciprocal of Rdc (admittance) at room temperature. Register = $1/(Rdc(\Omega) \times 3/11)$ (fullscale voltage 11V, fullscale current 3A) Fixed point <4,20> Max value = 2.1818S (siemens) Min value = 260nS (siemens) Resolution = 260nS | 0x000000: Reserved 0x000001: 260nS 0x075555: 0.125S 0x09C71C: 0.167S 0x0EAAAB: 0.250S 0x7FFFFFFF: 2.18S 0x800000: Reserved 0xFFFFFFFF: Reserved |

DSM TPROT RECIP RDC ROOM BYTE1 (0x2393)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|--------------------------------|---|---|---|---|---|---|---|
| Field | DSM_TPROT_RECIP_RDC_ROOM[15:8] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------------------|------|--|--|
| DSM_TPROT_RECIP_RDC_ROOM | 7:0 | Reciprocal of Rdc (admittance) at room temperature. Register = $1/(Rdc(\Omega) \times 3/11)$ (fullscale voltage 11V, fullscale current 3A) Fixed point <4,20> Max value = 2.1818S (siemens) Min value = 260nS (siemens) Resolution = 260nS | 0x000000: Reserved 0x000001: 260nS 0x075555: 0.125S 0x09C71C: 0.167S 0x0EAAAB: 0.250S 0x7FFFFFFF: 2.18S 0x800000: Reserved 0xFFFFFFFF: Reserved |

DSM TPROT RECIP RDC ROOM BYTE2 (0x2394)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|---------------------------------|---|---|---|---|---|---|---|
| Field | DSM_TPROT_RECIP_RDC_ROOM[23:16] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------------------|------|--|--|
| DSM_TPROT_RECIP_RDC_ROOM | 7:0 | Reciprocal of Rdc (admittance) at room temperature. Register = $1/(Rdc(\Omega) \times 3/11)$ (fullscale voltage 11V, fullscale current 3A) Fixed point <4,20> Max value = 2.1818S (siemens) Min value = 260nS (siemens) Resolution = 260nS | 0x000000: Reserved 0x000001: 260nS 0x075555: 0.125S 0x09C71C: 0.167S 0x0EAAAB: 0.250S 0x7FFFFFF: 2.18S 0x800000: Reserved 0xFFFFFFFF: Reserved |

DSM TPROT RECIP TCONST BYTE0 (0x2395)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-----------------------------|---|---|---|---|---|---|---|
| Field | DSM_TPROT_RECIP_TCONST[7:0] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------------|------|--|---|
| DSM_TPROT_RECIP_TCONST | 7:0 | Reciprocal of copper temperature constant. Register = $1/(100 \times \text{copper constant})$ Fixed point <4,20> Max value = 7.9999999 Min value = -8.0 Resolution = 954e-9 | 0x000000: 0 0x000001: 954e-9 0x28B664: 2.544 0x09C71C: 0.167S 0x0EAAAB: 0.250S 0x7FFFFFF: 2.18S 0x800000: Reserved 0xFFFFFFFF: Reserved |

DSM TPROT RECIP TCONST BYTE1 (0x2396)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|------------------------------|---|---|---|---|---|---|---|
| Field | DSM_TPROT_RECIP_TCONST[15:8] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------------|------|--|--|
| DSM_TPROT_RECIP_TCONST | 7:0 | Reciprocal of copper temperature constant. Register = 1/(100 x copper constant) Fixed point <4,20> Max value = 7.9999999 Min value = -8.0 Resolution = 954e-9 | 0x000000: 0 0x000001: 954e-9 0x28B664: 2.544 0x7FFFFFF: 8.000 0x800000: Reserved 0xFFFFFFFF: Reserved |

DSM TPROT RECIP TCONST BYTE2 (0x2397)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------------------|---|---|---|---|---|---|---|
| Field | DSM_TPROT_RECIP_TCONST[23:16] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------------|------|--|--|
| DSM_TPROT_RECIP_TCONST | 7:0 | Reciprocal of copper temperature constant. Register = 1/(100 x copper constant) Fixed point <4,20> Max value = 7.9999999 Min value = -8.0 Resolution = 954e-9 | 0x000000: 0 0x000001: 954e-9 0x28B664: 2.544 0x7FFFFFF: 8.000 0x800000: Reserved 0xFFFFFFFF: Reserved |

DSM TPROT ATTENUATION SETTINGS (0x2398)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|----------------------------|---|--------------------------|---|
| Field | - | - | - | - | DSM_TPROT_ATTEN_SKI P[1:0] | | DSM_TPROT_MAX_ATT N[1:0] | |
| Reset | - | - | - | - | 0x2 | | 0x0 | |
| Access Type | - | - | - | - | Write, Read | | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------------|------|---|---|
| DSM_TPROT_ATTEN_SKI P | 3:2 | Sets the number of attenuation calculations skipped at the startup of thermal protection to allow for settling. | 0x0: Skip no gain calculations 0x1: Skip first 2 gain calculations 0x2: Skip first 4 gain calculations 0x3: Skip first 8 gain calculations |
| DSM_TPROT_MAX_ATT N | 1:0 | Maximum attenuation which can be provided by the thermal protection algorithm | |

DSM TPROT PG TEMP THRESH BYTE0 (0x239A)

| | | | | | | | | |
|--------------------|-------------------------------|----------|----------|----------|----------|----------|----------|----------|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | DSM_TPROT_PG_TEMP_THRESH[7:0] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------------------|-------------|---|--|
| DSM_TPROT_PG_TEMP_THRESH | 7:0 | Speaker coil power gating temperature threshold. Above this threshold, the system is not allowed to enter power gating, if enabled. 16-bit fixed point format <4,12>. Temperature PG threshold fixed point real = (temperature PG threshold °C)/100 Max temp 799.98°C, min temp -800°C, resolution 0.0244°C. | 0x0000: 0°C 0x0001: 0.0244°C ... 0x0400: 25.0°C ... 0x0CCD: 80.0°C ... 0x1000: 100.0°C ... 0x1333: 120.0°C ... 0x7FFF: 799.9°C 0x8000: -800.0°C ... 0xFFFFE: -0.0488°C 0xFFFFF: -0.0244°C |

DSM TPROT PG TEMP THRESH BYTE1 (0x239B)

| | | | | | | | | |
|--------------------|--------------------------------|----------|----------|----------|----------|----------|----------|----------|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | DSM_TPROT_PG_TEMP_THRESH[15:8] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------------------|-------------|---|--|
| DSM_TPROT_PG_TEMP_THRESH | 7:0 | Speaker coil power gating temperature threshold. Above this threshold, the system is not allowed to enter power gating, if enabled. 16-bit fixed point format <4,12>. Temperature PG threshold fixed point real = (temperature PG threshold °C)/100 Max temp 799.98°C, min temp -800°C, resolution 0.0244°C. | 0x0000: 0°C 0x0001: 0.0244°C ... 0x0400: 25.0°C ... 0x0CCD: 80.0°C ... 0x1000: 100.0°C ... 0x1333: 120.0°C ... 0x7FFF: 799.9°C 0x8000: -800.0°C ... 0xFFFFE: -0.0488°C 0xFFFFF: -0.0244°C |

THERMAL RESISTANCE RD BACK BYTE1 (0x239C)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------------|---|---|---|---|---|---|---|
| Field | THERMAL_RDC_RD_BACK[13:8] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------------|------|---|---|
| THERMAL_RDC_RD_BACK | 5:0 | Rdc value to read for calibration. $Rdc (\Omega) = Rdc (\text{code}) \times 11/3$ (Fullscale voltage 11V, fullscale current 3A) 14-bit fixed point <6,8> Max value = 117.32Ω Min value = 14.3mΩ Resolution = 14.3mΩ | 0x0000: 0Ω 0x0001: 0.0039Ω 0x0017: 4.00Ω 0x01A3: 6.00Ω 0x022F: 8.01Ω 0x1FFF: 32.00Ω 0x2000: Reserved 0x3FFF: Reserved |

THERMAL RESISTANCE RD BACK BYTE0 (0x239D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------------|---|---|---|---|---|---|---|
| Field | THERMAL_RDC_RD_BACK[7:0] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------------|------|---|---|
| THERMAL_RDC_RD_BACK | 7:0 | Rdc value to read for calibration. $Rdc (\Omega) = Rdc (\text{code}) \times 11/3$ (Fullscale voltage 11V, fullscale current 3A) 14-bit fixed point <6,8> Max value = 117.32Ω Min value = 14.3mΩ Resolution = 14.3mΩ | 0x0000: 0Ω 0x0001: 0.0039Ω 0x0017: 4.00Ω 0x01A3: 6.00Ω 0x022F: 8.01Ω 0x1FFF: 32.00Ω 0x2000: Reserved 0x3FFF: Reserved |

DSMIG EXCURSION PROTECTION RELEASE TIME BYTE 0 (0x23A4)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------------|---|---|---|---|---|---|---|
| Field | EXCURSION_PROT_RLS[7:0] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------------|------|---|--|
| EXCURSION_PROT_RLS | 7:0 | Coefficient[15:0] fixed point <0,16> Real coefficient value = $2^6 / (F_s \times \text{Release_time} + 1)$ Fs: audio sample rate in Hz, Release_time (to get to 63% of steady-state value): in seconds Decode shows examples at 48kHz sample rate. | 0x0000: Reserved 0x0001: 87400ms ... 0x0057: 1000ms ... 0x036A: 100ms ... 0x06D3: 50ms ... 0x2210: 10ms ... 0xFFFF: 1.3ms |

DSMIG EXCURSION PROTECTION RELEASE TIME BYTE 1 (0x23A5)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------------|---|---|---|---|---|---|---|
| Field | EXCURSION_PROT_RLS[15:8] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------------|------|---|--|
| EXCURSION_PROT_RLS | 7:0 | Coefficient[15:0] fixed point <0,16> Real coefficient value = $2^6 / (F_s \times \text{Release_time} + 1)$ Fs: audio sample rate in Hz, Release_time (to get to 63% of steady-state value): in seconds Decode shows examples at 48kHz sample rate. | 0x0000: Reserved 0x0001: 87400ms ... 0x0057: 1000ms ... 0x036A: 100ms ... 0x06D3: 50ms ... 0x2210: 10ms ... 0xFFFF: 1.3ms |

DSMIG EXCURSION PROTECTION THRESHOLD (0x23A6)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|----------------------------|---|---|---|---|---|---|
| Field | – | EXCURSION_PROT_THRESH[6:0] | | | | | | |
| Reset | – | 0x0 | | | | | | |
| Access Type | – | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------------------|------|--|--|
| EXCURSION_PROT_THRESHOLD | 6:0 | Excursion protection threshold expressed in % of full-scale (1% step). | 0x0: 0% of FullScale 0x1: 1% of FullScale 0x2: 2% of FullScale 0x3: 3% of FullScale ... 0x63: 99% of FullScale 0x64: 100% of FullScale |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-------------|-------------------------------------|
| | | | ...: ... 0x7F: 100% of FullScale |

DSMIG EXCURSION PROTECTION DEL BUFFER (0x23A7)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------------------|---|---|---|---|---|---|---|
| Field | EXCURSION_PROT_DELAY_BUFFER[7:0] | | | | | | | |
| Reset | 0d120 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------------------|------|---|--|
| EXCURSION_PROT_DELAY_BUFFER | 7:0 | Samples of delay on the audio path (from 2 to 157 samples). | 0x0: 2 samples 0x1: 3 samples 0x2: 4 samples ...:: ... 0x9A: 156 samples 0x9B: 157 samples 0x9C: Reserved ...: ... 0xFF: Reserved |

DSMIG DEBUZZER THRESHOLD (0x23B5)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-----------------|---|---|---|---|---|
| Field | - | - | DBZ_THRESH[5:0] | | | | | |
| Reset | - | - | 0x0 | | | | | |
| Access Type | - | - | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------|------|---|--|
| DBZ_THRESHOLD | 5:0 | Debuzzer threshold (1dB step, min -60dB). | 0x0: -0dB 0x1: -1dB 0x2: -2dB 0x3: -3dB 0x4: -4dB ...: ... 0x3D: -60dB 0x3E: -60dB 0x3F: -60dB |

DSM VOL ENA (0x23B9)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------------|---|---|---|---|---|---------------------|---------------------|
| Field | DSM_VOL_RAMP_TIME[2:0] | | | - | - | - | DSM_VOL_RAMP_DN_BYP | DSM_VOL_RAMP_UP_BYP |
| Reset | 0x1 | | | - | - | - | 0x0 | 0x0 |
| Access Type | Write, Read | | | - | - | - | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------------|------|--|---|
| DSM_VOL_RAMP_TIME | 7:5 | Set the duration of the volume smooth ramping (S-Curve profile). | 0x0: 8ms ramp-up/down time 0x1: 4ms ramp-up/down time 0x2: 2ms ramp-up/down time 0x3: 1ms ramp-up/down time 0x4: 0.5ms ramp-up/down time 0x5: 0.25ms ramp-up/down time 0x6: Reserved 0x7: Reserved |
| DSM_VOL_RAMP_DN_BY_P | 1 | DSM ramp-down bypass | 0x0: Ramp-down enabled 0x1: Ramp-down disabled |
| DSM_VOL_RAMP_UP_BY_P | 0 | DSM ramp-up bypass | 0x0: Ramp-up enabled 0x1: Ramp-up disabled |

DSM_VOL_CTRL (0x23BA)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|---|---|---|---|---|---|---|
| Field | DSM_VOL_CTRL[7:0] | | | | | | | |
| Reset | 0xA0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------|------|--|--|
| DSM_VOL_CTRL | 7:0 | Sets the digital volume level of the DSM. Digital volume = -80dB + DSMIG_VOL_CTRL/2 | 0x00: -80.00dB 0x01: -79.5dB 0x02: -79.00dB 0x03: -78.5dB 0x04: -78.00dB ... 0x9F: -0.50dB 0xA0: 0.00dB 0xA1: 0.50dB 0xA2: 1.00dB 0xA3: 1.50dB ... 0xB4: 10.00 0xB5: 10.50 0xB6: 11.00 0xB7: 11.50 0xB8: 12.00 0xB9 to 0xFF: Reserved |

DSMIG_ENABLES (0x23E0)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------|-------------|-------------|-------------|-------------------|-------------|-------------|-----------------|
| Field | STEREO_BASS_EN | WBDRC_EN | EQ8_EN | BASS_EXT_EN | EXCURSION_PROT_EN | PPR_EN | DEBUZZER_EN | THERMAL_PROT_EN |
| Reset | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 | 0b0 |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------------|------|---|-------------------------|
| STEREO_BASS_EN | 7 | Enables Stereo Bass Management. Note that when DSP_GLOBAL_EN = 0 and EN = 1, STEREO_BASS_EN must not be set to 1. | 0: Disable 1: Enable |
| WBDRM_EN | 6 | Enables Dynamic Range Compression | 0: Disable 1: Enable |
| EQ8_EN | 5 | Enables the Equalizer | 0: Disable 1: Enable |
| BASS_EXT_EN | 4 | Enables Low Frequency Extension | 0: Disable 1: Enable |
| EXCURSION_PROT_EN | 3 | Enables Excursion Protection | 0: Disable 1: Enable |
| PPR_EN | 2 | Enables PPR | 0: Disable 1: Enable |
| DEBUZZER_EN | 1 | Enables the Debuzzer | 0: Disable 1: Enable |
| THERMAL_PROT_EN | 0 | Enables Thermal Protection | 0: Disable 1: Enable |

DSP GLOBAL ENABLE (0x23E1)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|---|---|---------------|
| Field | – | – | – | – | – | – | – | DSP_GLOBAL_EN |
| Reset | – | – | – | – | – | – | – | 0b0 |
| Access Type | – | – | – | – | – | – | – | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------|------|--|-------------------------|
| DSP_GLOBAL_EN | 0 | Global enable for DSP functions including stereo bass management, dynamic range compression, EQ, low frequency extension, excursion protection, PPR, debuzzer, and thermal protection. | 0: Disable 1: Enable |

DSM_THERMAL_GAIN (0x23F0)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------------|---|---|---|---|---|---|---|
| Field | DSM_THERMAL_GAIN[7:0] | | | | | | | |
| Reset | 0x00 | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------------|------|---|--|
| DSM_THERMAL_GAIN | 7:0 | Internal gain value for thermal protection. <2,6> | 00000000: Reserved 00000001: -36.12dB 00000010: -30.10dB 00000011: -26.58dB 00000100: -24.08dB ...: ... 11111100: 11.90dB 11111101: 11.94dB |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-------------|--|
| | | | 11111110: 11.97dB 11111111: 12.01dB |

DSM_PPR_GAIN (0x23F1)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|---|---|---|---|---|---|---|
| Field | DSM_PPR_GAIN[7:0] | | | | | | | |
| Reset | 0x00 | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------|------|------------------------------------|--|
| DSM_PPR_GAIN | 7:0 | Internal gain value for PPR. <2,6> | 00000000: Reserved 00000001: -36.12dB 00000010: -30.10dB 00000011: -26.58dB 00000100: -24.08dB ...: ... 11111100: 11.90dB 11111101: 11.94dB 11111110: 11.97dB 11111111: 12.01dB |

DSM_DBZ_GAIN (0x23F2)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|---|---|---|---|---|---|---|
| Field | DSM_DBZ_GAIN[7:0] | | | | | | | |
| Reset | 0x00 | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------|------|---|--|
| DSM_DBZ_GAIN | 7:0 | Internal gain value for debuzzer. <2,6> | 00000000: Reserved 00000001: -36.12dB 00000010: -30.10dB 00000011: -26.58dB 00000100: -24.08dB ...: ... 11111100: 11.90dB 11111101: 11.94dB 11111110: 11.97dB 11111111: 12.01dB |

DSM_WBDRG_GAIN (0x23F3)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Field | DSM_WBDRG_GAIN[7:0] | | | | | | | |
| Reset | 0x00 | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------------|------|-------------------------------------|--|
| DSM_WBDR C_GAIN | 7:0 | Internal gain value for WBDR. <4,4> | 00000000: Reserved 00000001: -24.08dB 00000010: -18.06dB 00000011: -14.54dB 00000100: -12.04dB ...: ... 11111100: 23.95dB 11111101: 23.98dB 11111110: 24.01dB 11111111: 24.05dB |

GLOBAL ENABLE (0x23FF)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|---|---|------------------|
| Field | - | - | - | - | - | - | - | EN |
| Reset | - | - | - | - | - | - | - | 0b0 |
| Access Type | - | - | - | - | - | - | - | Write, Read, Ext |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|---|
| EN | 0 | Disable or enable all blocks and reset all logic except the I ² C interface and control registers. | 0: Device is powered-down 1: Device is enabled |

REV ID (0x24FF)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field | REV_ID[7:0] | | | | | | | |
| Reset | 0b01000001 | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--------------|---|
| REV_ID | 7:0 | Revision ID. | [7:0]: Read back the revision ID of the device. |

Applications Information

Boost Converter Component Selection

Battery Input Capacitor Selection

The decoupling capacitors at the VBAT pin reduce the current peaks drawn from the battery or input power source and reduce switching noise due to the boost converter. The impedance of the input capacitors at the boost switching frequency should be kept as low as possible to reduce ripple on the VBAT supply. Ceramic capacitors are highly recommended due to their small size and low ESR. Ceramic capacitors with X5R or X7R temperature characteristics generally perform well.

The decoupling capacitors at the boost inductor input reduce the current peaks drawn from the battery or input power source and ensure that the boost remains stable under all loading conditions. The impedance of the input capacitors at the boost switching frequency should be kept as low as possible to reduce ripple on the VBAT supply. Ceramic capacitors are highly recommended due to their small size and low ESR. Ceramic capacitors with X5R or X7R temperature characteristics generally perform well.

Bypass the battery supply with $2 \times 10\mu\text{F} + 1 \times 0.1\mu\text{F}$ capacitors at the VBAT pin. Place the capacitors as close to the IC as possible as seen in the Typical Application Circuit. Use components that retain greater than 30% of their nominal value at 4.3VDC.

Boost Inductor Selection (L1)

The recommended minimum inductance for the boost inductor is $1.0\mu\text{H}$. Use a boost inductor with a peak saturation current rating above the set limit to maximize the available output power. Nominal inductance decreases as the inductor current increases.

If the decrease from nominal inductance is severe, the boost converter can become unstable or shut down at lower output power levels than expected. Ensure the minimum inductance at the peak inductor current is $0.7\mu\text{H}$.

Power Amplifier Supply Bypass Capacitors (CPVDD)

Capacitors at the PVDD pin (power amplifier supply and boost converter output) are required to keep the output voltage ripple small and to ensure the stability of the boost. These capacitors must have low impedance at the switching frequency. Ceramic capacitors are highly recommended due to their small size and low ESR. Ceramic capacitors with X5R or X7R temperature characteristics generally perform well.

Bypass PVDD with $2 \times 10\mu\text{F} + 1 \times 0.1\mu\text{F}$ capacitors. Capacitor tolerance, temperature, and DC voltage can reduce the effective capacitance of the network. Select components that result in a total effective capacitance of at least $4\mu\text{F}$.

Boost Converter Settings

The following boost converter settings were used to gather data for the Typical Operating Characteristics:

- Boost envelope tracker voltage output headroom = 1.75V (ENV_TRACKER_BST_VOUT_HEADROOM = 01110b)
- Boost envelope tracker hold rate = 10ms/V (ENV_TRACKER_HOLD_RATE = 000b)
- Boost envelope tracker release rate = 10ms/V (ENV_TRACKER_RLS_RATE = 000b and ENV_TRACKER_RLS_RATE_SCALE = 00b)
- Boost envelope tracker and boost bypass delay = 0 samples (ENV_BYP_DELAY = 000000b)
- Boost bypass headroom = 0.75V (BST_BYP_HEADROOM = 0110b)

Startup Sequence

1. Apply the nominal voltage to the VBAT and DVDD pins. Hold $\overline{\text{RESET}}$ low until DVDD is within its operation range.
2. Apply logic-high to the $\overline{\text{RESET}}$ pin and wait at least $500\mu\text{s}$ for I²C communication to become available.

3. Program the IC to the desired mode of operation.
 - Enable the measurement ADC and program thermal thresholds
 - Program the PCM interface inputs and outputs
 - Program the boost converter
 - Program the speaker output amplifier
 - Program the I/V ADCs
 - Program the BDE
 - Set global enable high

Note: Be mindful of the restricted bits when programming the IC. Consult the [Control Bit Types and Write-Access Restrictions](#) section for more details.
4. Digital audio data can be applied to the IC before or after the global enable is set high.
5. After enabling the IC, look for a "Power-Up Done" state bit in the register 0x0005.
6. If a "Power-Up Fail" state is readback in register 0x0006, then double check that the ICs temperature ADC is enabled and that the thermal-warning and thermal-shutdown threshold are programmed correctly.
7. When applying an audio signal to an active IC, the signal should be ramped.
8. For a quicker turn-on time, configure and enable all blocks except the speaker, then enable the speaker 3ms in advance of when audio is desired.

Shutdown Sequence

1. Set global enable (EN) low.
2. Remove digital audio clocks.
3. Apply logic-low signal to $\overline{\text{RESET}}$ pin.
4. Remove power from VBAT and DVDD pins.

Recommended External Components

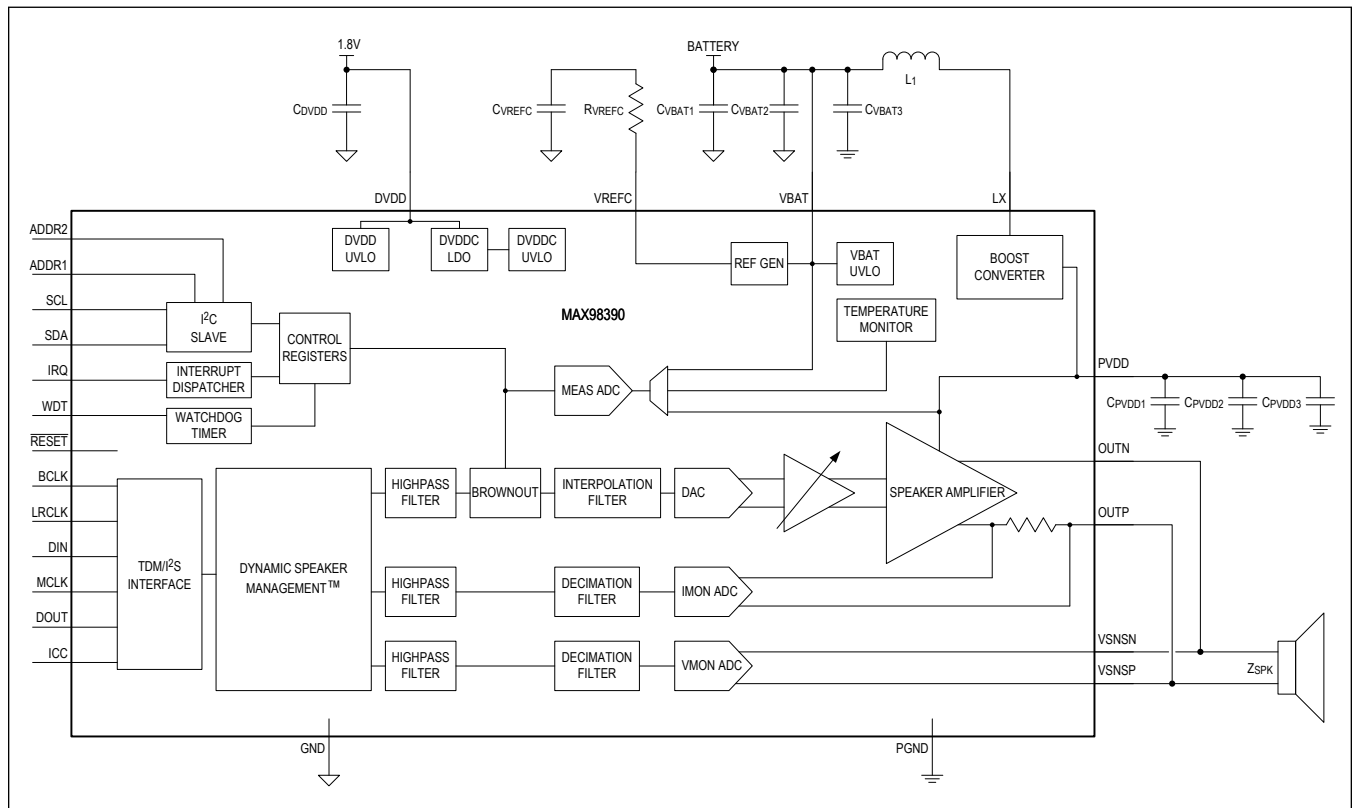
[Table 23](#) shows the recommended external components. See [Boost Converter Component Selection](#) and [Typical Application Circuits](#) for more details.

Table 23. Component List

| REFERENCE DESIGNATOR | DESCRIPTION |
|----------------------|--|
| CDVDD | 0.1 μ F \pm 10%, 6.3V X5R ceramic capacitor (0201) |
| CVREFC | 1 μ F \pm 20%, 6.3V X5R ceramic capacitor (0201) |
| RVREFC | 30 Ω \pm 1%, 0.05W resistor (0201) |
| CVBAT1 | 0.1 μ F \pm 10%, 10V X5R ceramic capacitor (0201) |
| CVBAT2, CVBAT3 | 10 μ F \pm 20%, 10V X5R ceramic capacitor (0402) |
| CPVDD1 | 0.1 μ F \pm 20%, 16V X5R ceramic capacitor (0201) |
| CPVDD2, CPVDD3 | 10 μ F \pm 20%, 25V X5R ceramic capacitor (0603) |
| L1 | 1.0 μ H, 4.7A inductor (3.2mm x 2.5mm x 1.2mm) |

Typical Application Circuit

MAX98390



Ordering Information

| PART NUMBER | PIN-PACKAGE |
|---------------|-------------|
| MAX98390EWX+T | 36 WLP |

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|-----------------|---------------|
| 0 | 4/19 | Initial release | — |

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at <https://www.maximintegrated.com/en/storefront/storefront.html>.

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