GreenPAK Advanced Development Platform
User Guide

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Contents

1 Introduction

Thank you for choosing Silego Technology products. The GreenPAK Advanced Development Platform allows you to develop your custom design using GreenPAK mixed signal ICs. You can design your own projects starting from a blank project or by altering the sample projects provided at Silego website.

1.1 GreenPAK Designer

GreenPAK Designer is an easy-to-use full-featured integrated development environment (IDE) that allows you to specify exactly how you want the device to be configured. This provides you a direct access to all GreenPAK device features and complete control over the routing and configuration of a PAK project with just one tool.

With GreenPAK Designer, you can:

- Design the configuration which corresponds to your project needs
- Verify the project using software interface to GreenPAK Advanced Development Platform hardware
- With simple-to-use and intuitive software and hardware tools you can reduce your project development time and get to market faster

To start working with GreenPAK Designer please take the following steps:

- Download and install GreenPAK Designer software
- Configure modules that you will need for your project
- Interconnect and configure modules
- Specify the pin out
- Test your design with the GreenPAK Advanced Development Board

1.2 Support

Free support for GreenPAK Advanced Development Platform is available online at http://www.silego.com/.

At facebook : Silego-Technology

GreenPAK Designer will automatically notify you when a new version of software is available. For manual updates please go to http://www.silego.com/softdoc/software.html.

These resources are also available under the **Help** menu of GreenPAK Designer.

2 Getting Started

2.1 Introduction

This chapter describes how to install and configure the GreenPAK Advanced Development Platform. *Chapter 3* provides the details of hardware operation. *Chapter 4* provides instructions on how to create a simple project example.

2.2 Install Hardware

No hardware installation is required for this platform.

2.3 Install Software

GreenPAK Designer software is available free of charge from the Silego website at http://www.silego.com/softdoc/software.html page.

2.4 Uninstall Software

The software can be uninstalled in the way typical for your operating system. Please refer to your operating system support documentation if you need the specific instructions or visit Support section of this document for additional support from Silego.

3 Hardware

3.1 Overview

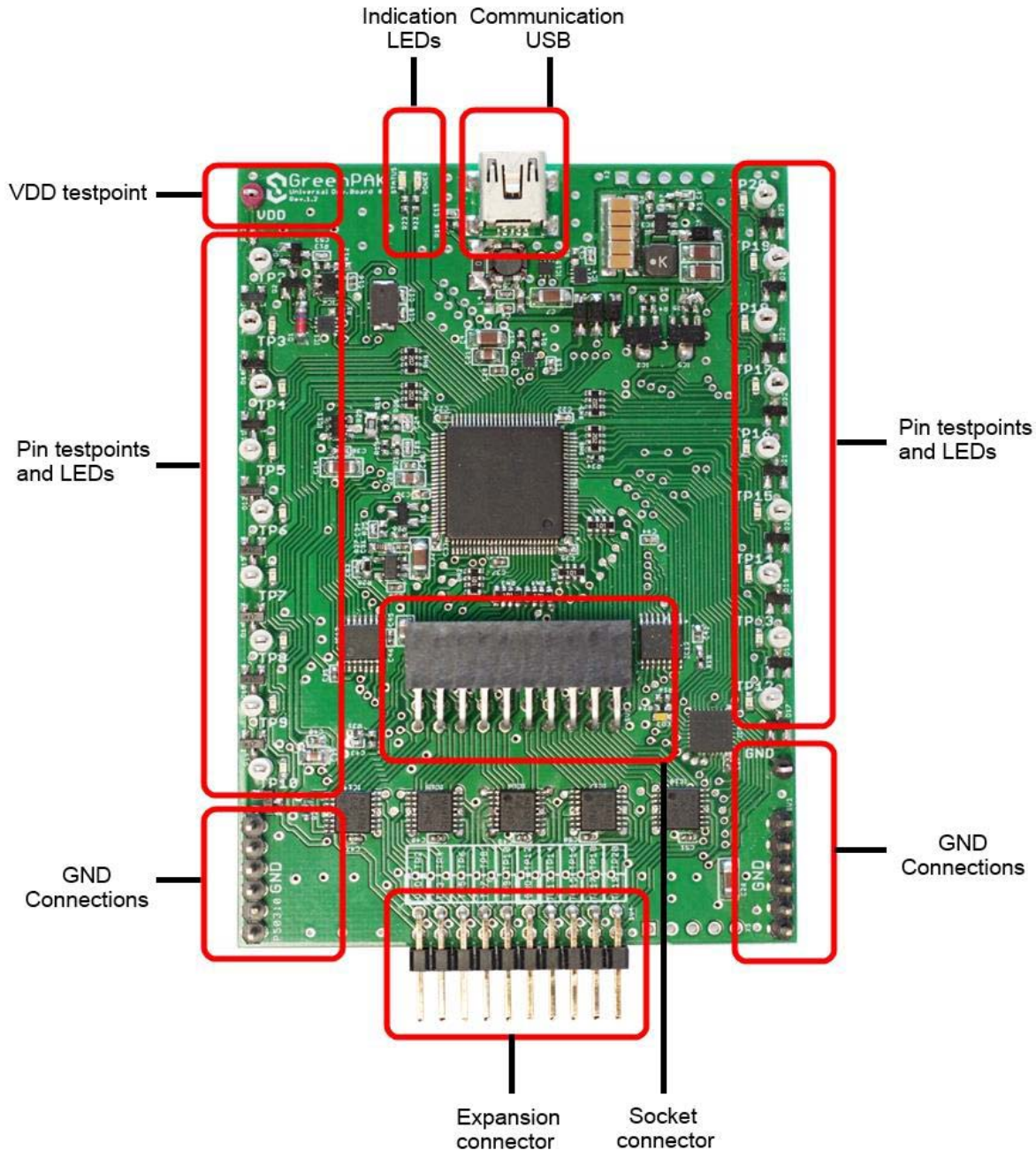


Figure 1. GreenPAK Advanced Development Board, Top View

Note: All test points were designed only for observation of signals on the pins. Please do not try to connect external power/signal source to test points, this will affect GreenPAK Advanced Development Board functionality and may even damage it.

3.2 Functional Description

3.2.1 Power Supply

The main power source of the GreenPAK Advanced Development Board is the USB power line. The Development Board can deliver power from 0 to 5.5 V. To provide this power range, the Development Board is equipped with a boost converter. A Signal generator with a buffered output controls the GreenPAK chip power rail. For more information about GreenPAK electrical specification, please refer to the datasheet.

3.2.2 USB Communication

The board has the USB communications interface that uses the USB mini-B connector, as shown in *Figure 2.* This interface provides communication with the software control tool and supplies power to the board, as discussed in Power Supply chapter.

Figure 2. USB Interface

3.2.3 GND Connections

There are 6 GND pins on the left side, 6 pins and 1 header on the right side. These can be used for test equipment (oscilloscope, multimeter etc.) ground reference connection or to connect external test circuitry ground.

3.2.4 Pin Test Points

Each GreenPAK chip pin including VDD has its own observation test point. These test points were designed only for observation. To connect an external signal source use a software-controlled expansion connector.

3.2.5 LEDs

All the pins except Pin2 can be connected to buffered LEDs. This option allows visualization of digital levels on chip pins. There are 2 selection modes:

- Buffered LED (with high impedance input)
- Inverted Buffered LED (with high impedance input)

This option can be enabled in GreenPAK Designer.

3.2.6 Socket Connector

The GreenPAK Advanced Development Board should be used with a detachable socket board. Its main purpose is to connect the GreenPAK chip to the Development Board. It‘s easy to use the programmed chip in external circuits, or to measure current consumption of the project.

3.2.7 Expansion Connector

This port was designed to connect the GreenPAK Advanced Development Board to external circuits and apply external power, signal sources and loads. It can be used to apply the GreenPAK chip into your custom design with minimal additional tools. For schematic diagram refer to *Figure 3.*

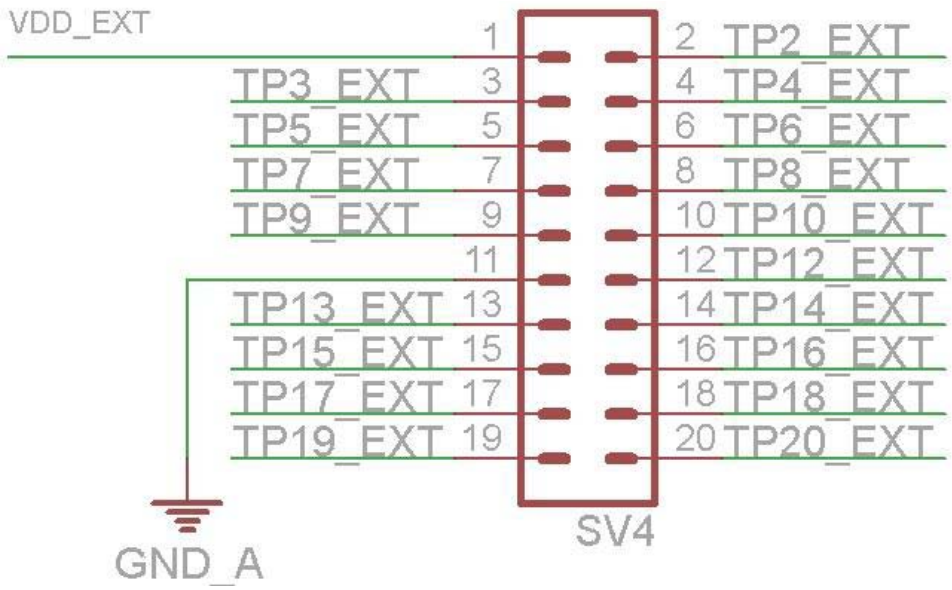


Figure 3. GreenPAK Expansion Connector Schematic

Each pin except PIN11 (GND) is controlled through an individual analog switch. Expansion connector is a standard 0.1” double row connector. GreenPAK Designer can enable or disable external pins, as it is shown in the *Figure 4. The* main purpose of the Expansion connector is to connect an external signal/power source safely to the GreenPAK Advanced Development Board.

Figure 4. Expansion Connector Control in GreenPAK Designer

Figure 5 demonstrates the schematic diagram of the expansion connector control.

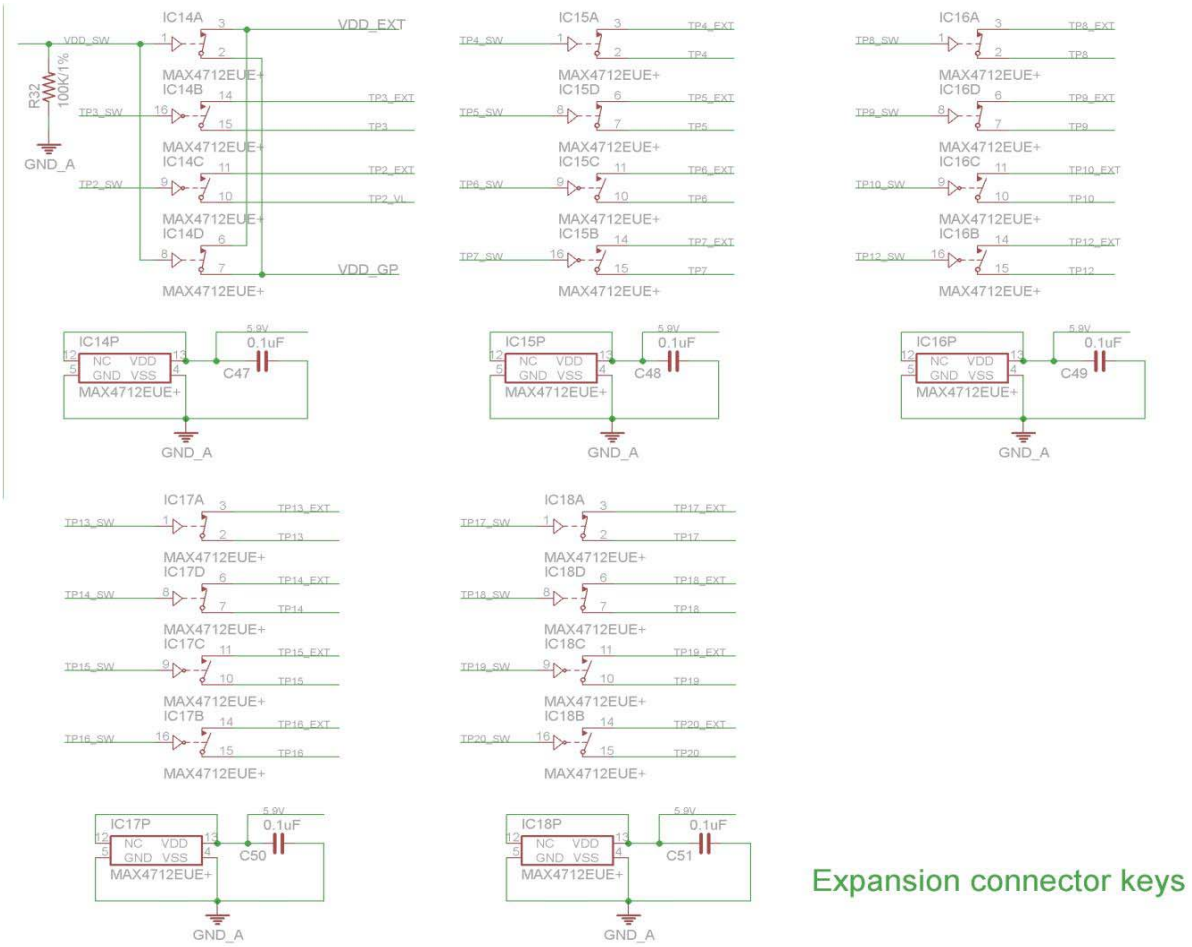


Figure 5. Socket and Expansion Connector Schematic

Expansion connector is enabled only in Emulation mode or Test mode. To enter either of these two modes the GreenPAK chip must be in the socket. When the Test mode button is pressed the software will first read the chip to verify if it was inserted and then configure the GreenPAK Advanced Development Board as set in Emulation Tool window. When the Test mode button is gray then the Development Board is in Default state and all expansion port switches are open (disconnected). After Emulation button is pressed, the software will automatically perform the following steps:

- check chip presence
- open all expansion port switches (external signals/loads can be left connected to expansion port)
- use internal power and load configuration to the chip
- only for case #3: adjust internal power source to external power level ⟶ close external power switch ⟶ open internal power switch
- configure Development Board as set in Emulation Tool window

Parasitic effects should be also considered while using the GreenPAK Advanced Development Board in-circuit with analog signals. The entire Development Board circuitry along with the wiring have a significant amount of mutual capacitance and inductance. The detachable socket can also be used for the in-circuit development with programmed chips (the Development Board and socket connectors have the same pinout).

The GreenPAK Advanced Development Board provides three possible ways of using expansion connector:

1) Internal power is used to run the chip, no external power output is needed, external signal sources and loads can be connected between pins and GND.
The configuration steps:
- close internal and open external power switch
- close all used expansion port switches in the software
- hit Emulation/Test mode button

This is the common way of using an Expansion connector.

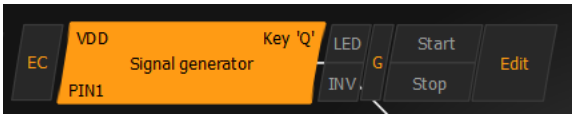


Figure 6. Internal Power Source

2) Internal power is used to run the chip and external circuit (internal power source/sink current is limited to 50 mA).
The configuration steps:
- close internal power switch
- close external power switch
- close all used expansion port switches in the software
- hit Emulation/Test mode button

Figure 7. Internal Power Source for GreenPAK Chip and External Development Board

3) External power is used to run the chip and external circuit (internal source output is in Hi-Z state).
The configuration steps:
- open internal power switch
- close external power switch
- close all used expansion port switches in the software
- hit Emulation/Test mode button (External power should be applied before this step)

Note that the GreenPAK chip has internal OTP memory which is normally loaded into RAM registers at initialization time.“Emulation mode” will bypass this load, and write the updated version of the project directly into the RAM register inside the GreenPAK chip many times, but after power loss all internal data will be lost. When the GreenPAK chip is already programmed the user can use Emulation mode to load another project and test it on the emulation tool in Emulation mode, in that case emulation data will be cleared. The “Emulation” mode is not necessary for checking programmed parts: in this case the “Test mode” is used.

Expansion connector can be divided by types of connections:
1. VDD
2. GND
3. Data connections

The VDD connection enables the user to connect/disconnect external and internal power source. This connection meets next requirements:
- External power range: 1.8 - 5.5 V
- High resistance voltage dividers are not recommended

The GND connection is connected directly to the Development Board, and cannot be controlled by GreenPAK Designer.

Data connections are the easiest way to connect external lines to the GreenPAK chip. They are software controlled switches. Every line is connected with a 100 Ω resistor.

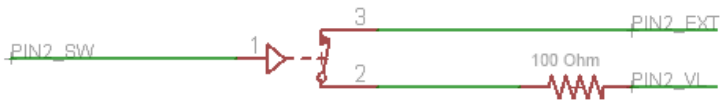


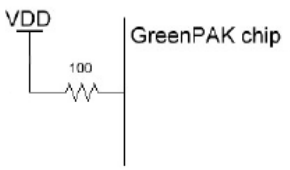
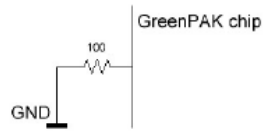
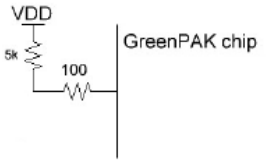
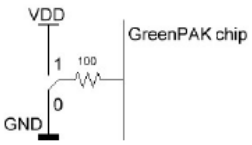
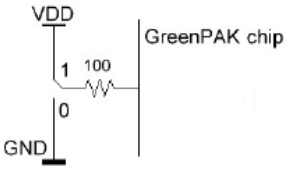
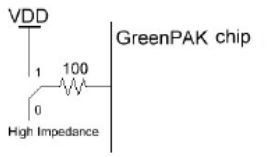
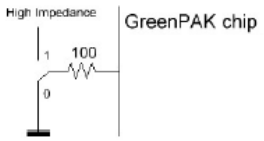
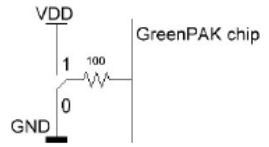
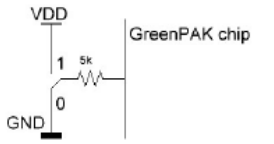
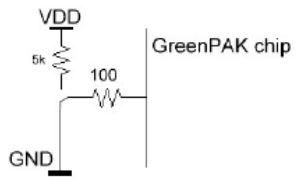
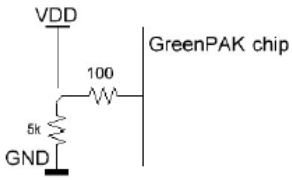
Figure 8. Expansion Connector. Pin with Protection Resistor

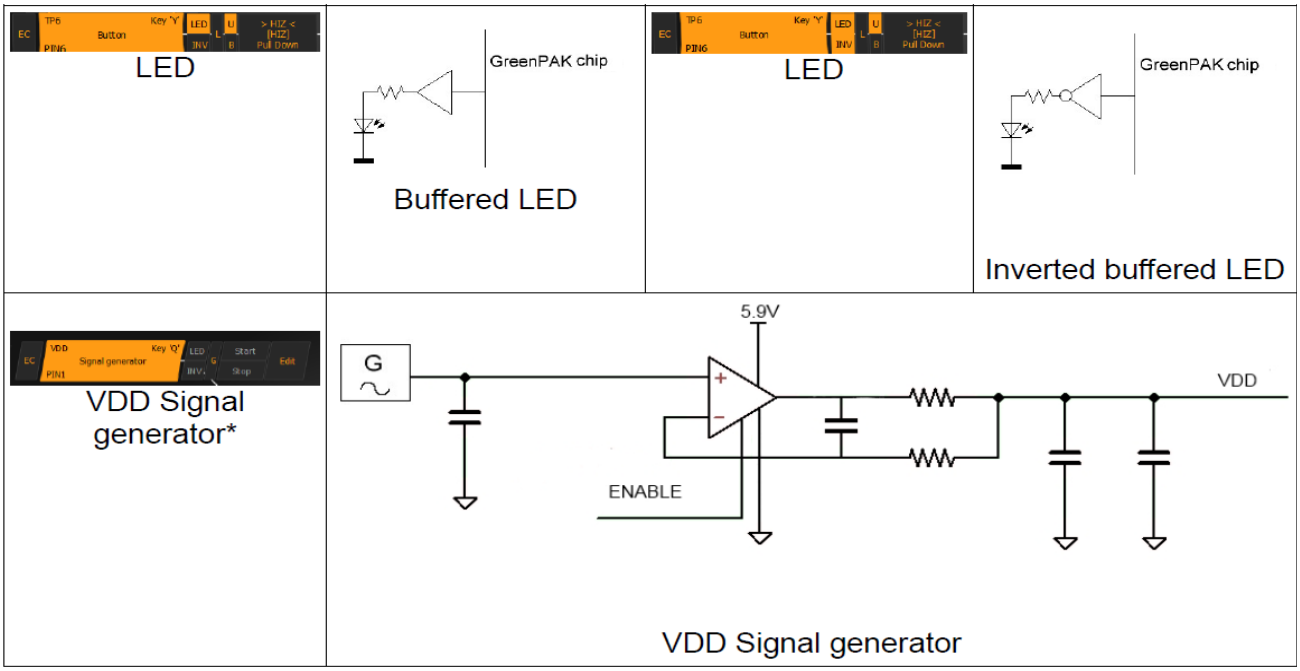
3.2.8 Pins Connectivity

The GreenPAK Advanced Development Board supports connecting eight types of loads and signal sources. Each source has its own special purpose. The List of available connections for each test point is presented in the table below.

Pin	Set to VDD	Set to GND	Pull up	Pull down	Set Confi-gurable Button	LED	Signal Generator	Logic Generator
#	1	2	3	4	5	6	7	8
VDD	-	-	-	-	-	-	+	-
TP2	+	+	+	+	+	-	-	+
TP3	+	+	+	+	+	+	-	+
TP4	+	+	+	+	+	+	-	+
TP5	+	+	+	+	+	+	-	+
TP6	+	+	+	+	+	+	+	+
TP7	+	+	+	+	+	+	+	+
TP8	+	+	+	+	+	+	+	+
TP9	+	+	+	+	+	+	-	+
TP10	+	+	+	+	+	+	+	+
TP12	+	+	+	+	+	+	+	+
TP13	+	+	+	+	+	+	+	+
TP14	+	+	+	+	+	+	+	+
TP15	+	+	+	+	+	+	-	+
TP16	+	+	+	+	+	+	-	+
TP17	+	+	+	+	+	+	-	+
TP18	+	+	+	+	+	+	-	+
TP19	+	+	+	+	+	+	-	+
TP20	+	+	+	+	+	+	-	+

Pin signal sources/loading schematics:

 Set to VDD	 Set to VDD	 Set to GND	 Set to GND
 Pull up	 Pull up	 Pull down	 Pull down
 Button pressed	 Button pressed	 Button released	 Button released
 Button with different configurations	 Button VDD – HI-Z	 Button HI-Z - GND	 Button VDD - GND
	 Button Pull up - Pull down	 Button Pull up - GND	 Button VDD – Pull down



Note: VDD Signal generator works similar to other Signal generators but has wider output voltage range. It can provide maximum supply level of 5.5 V.*

4 Example Projects using SLG46721

4.1 Project: Counter with Clock Enable

Blocks required:

- 2 digital inputs
- 1 digital output
- 1 Look-Up table with two inputs
- 1 Counter

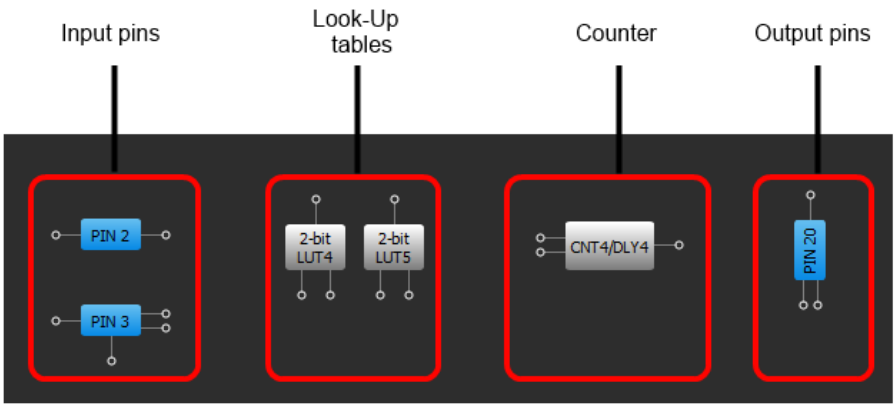


Figure 9. GreenPAK Designer

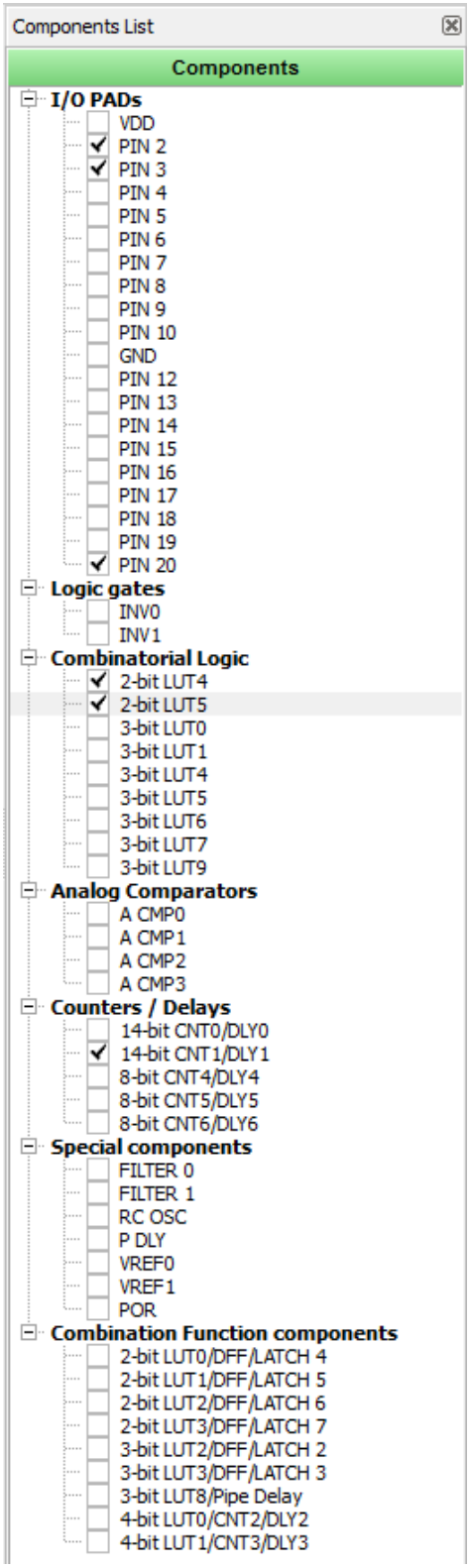


Figure 10. GreenPAK Components List

All these components can be found in components list. If there are no components on the work area - make sure this component is enabled.

Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
2	Clock	Digital input	Digital input
3	Enable	Digital Input	Digital Input
11	GND	GND	Ground
20	Counter Output	Push pull output	Digital input

All components used in the project are shown in *Figure 9*, next step is to configure selected blocks. Double click on PIN20 to open “Properties” panel. Select “1x push pull” from the drop-down menu in Pin20 properties and hit “Apply” button.

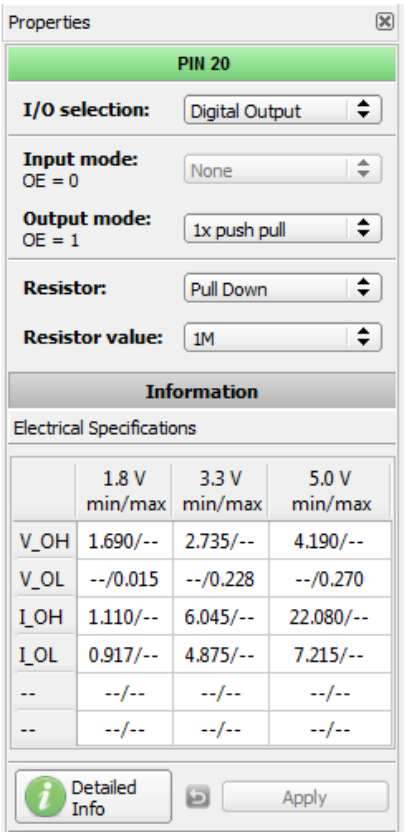


Figure 11. Pin 20 Mode

The next component in this design is the Look-Up table. First Look-Up Table (LUT4) is used to generate logic “1” only when there are high logic levels on both inputs (AND gate). Select AND gate from “Standard gates” drop-down menu or set table manually. Second Look-Up Table (LUT5) is configured as NOR gate. It is used to generate reset signal for counter on PIN3 falling edge.

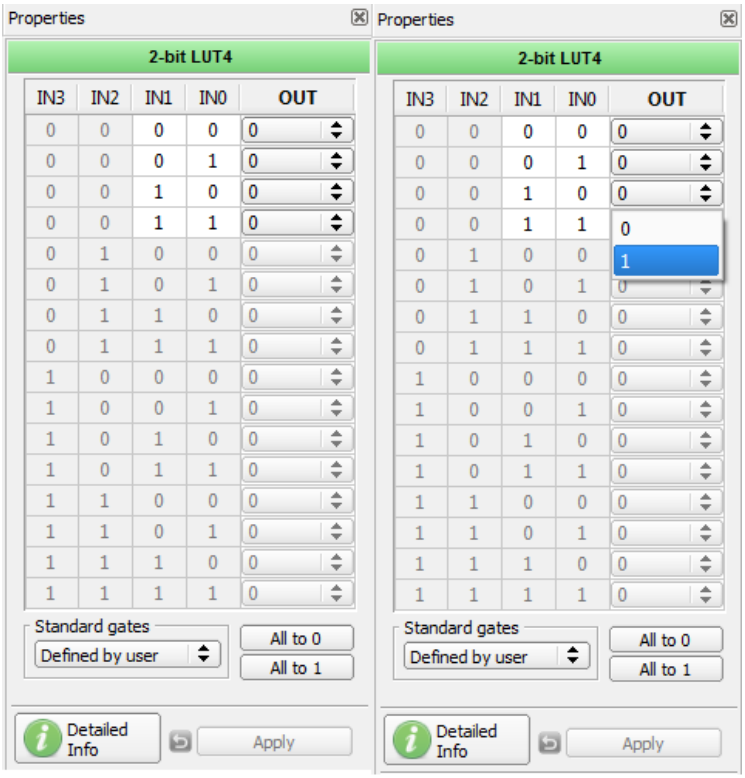


Figure 12. Look-Up Table Properties Configured as AND Gate

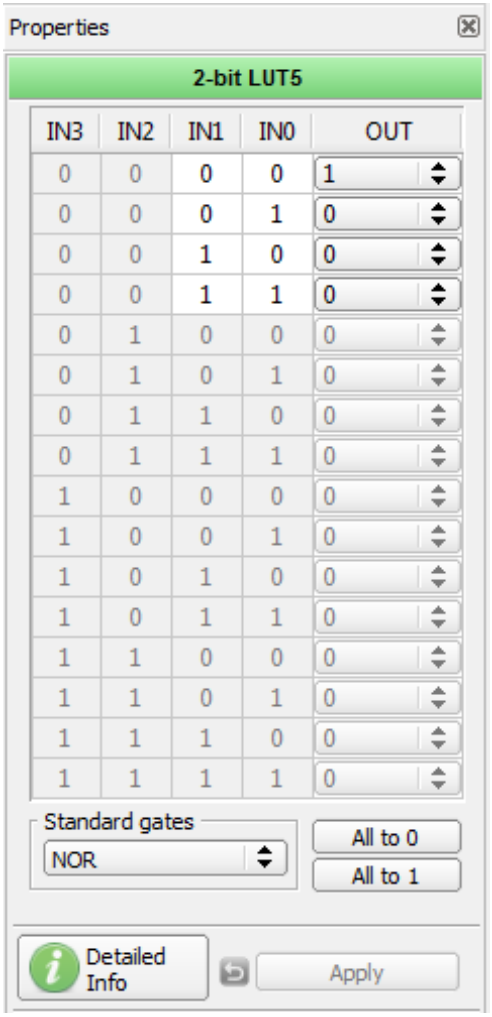


Figure 13. Look-Up Table Properties Configured as NOR Gate

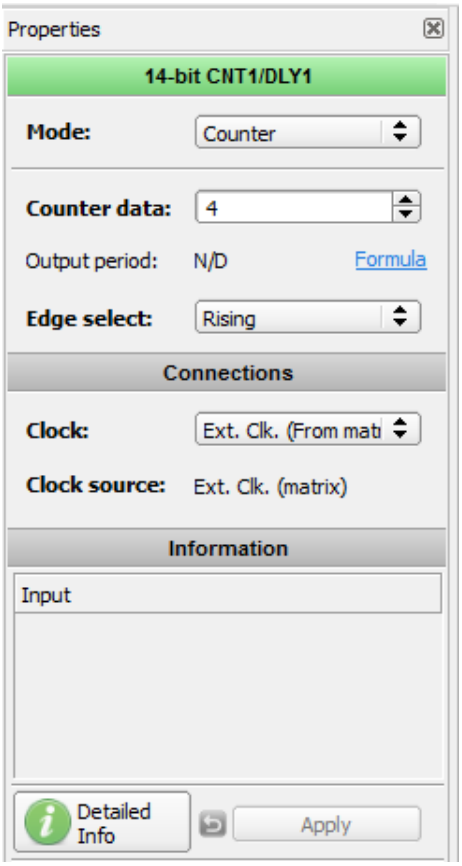


Figure 14. Counter Properties

The final step is to connect used components. Use Wire tool to perform this action. To connect two pins select “Set Wire” 

and then click on the first and the second pin of the module or modules that you want to connect. The trace will be automatically routed.

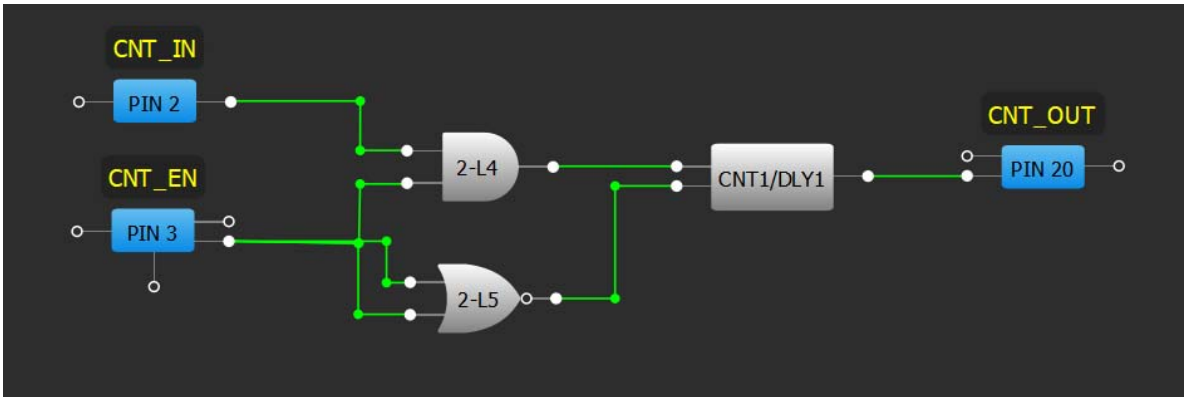


Figure 15. GreenPAK Designer

Figure 15 displays ready project with configured blocks and wire connections.

Use the GreenPAK Advanced Development Board to test this project. Connect the GreenPAK Advanced Development Board to the PC and press “Emulation” button. This will load the code of your project to the chip and will enable Test functionality of your Development Board.

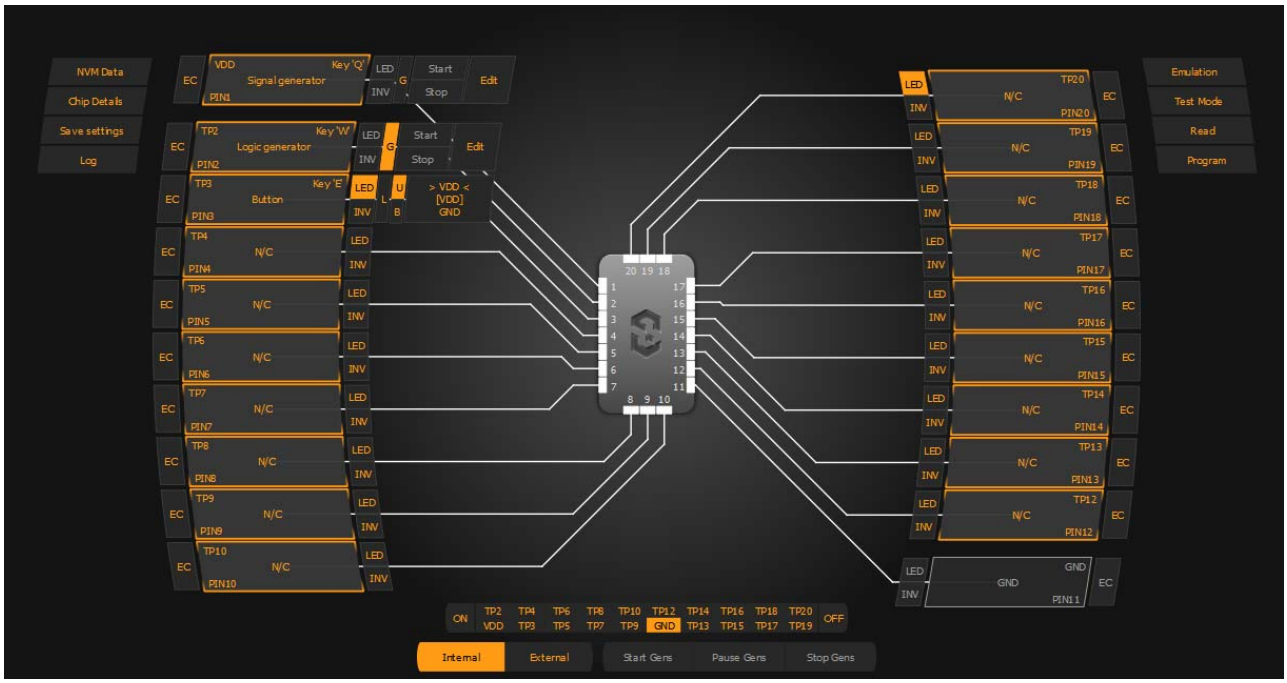


Figure 16. GreenPAK Designer, Emulation Tool

To test this project we will use the following tools:

- Signal generator. Signal generator is applied to VDD pin to power GreenPAK chip
- Logic generator. Logic generator serves as clock source
- Button is a software simulation of the real button. It switches PIN between VDD and GND signal levels
- Inverted buffered LED
- Buffered LED

Figure 17. Signal Generator Connected to VDD Pin

Signal generator is presented as a power source for GreenPAK chip. It's configured to output source constant 3.3 V.

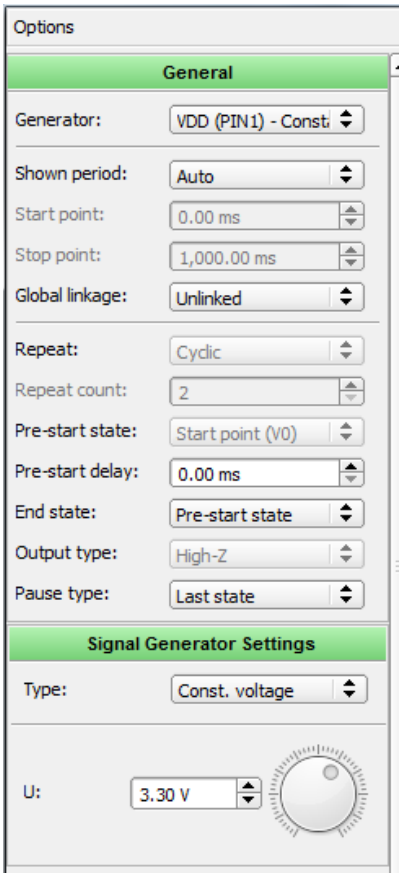


Figure 18. Signal Generator Settings

The purpose of the logic generator is to provide clock pulses for the Counter block. It is configured for 10 Hz clock source as shown in the *Figure 19.*

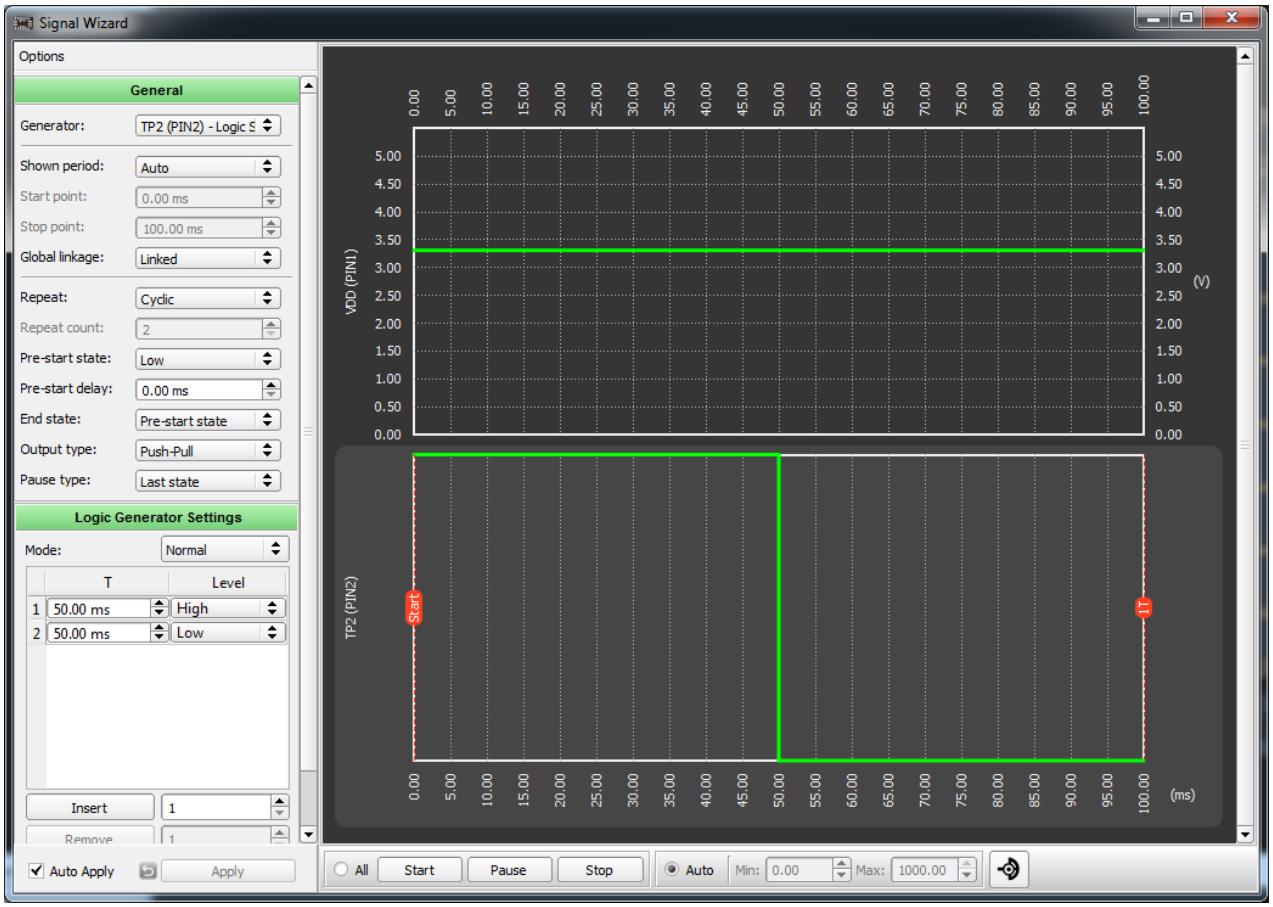


Figure 19. Logic Generator Properties

Functionality Waveform
Channel 1 (yellow/top) – Logic generator
Channel 2 (light blue/2nd line) – Button, 1 - enable Counter; 0 - disable Counter
Channel 3 (magenta/3rd line) – Counter output

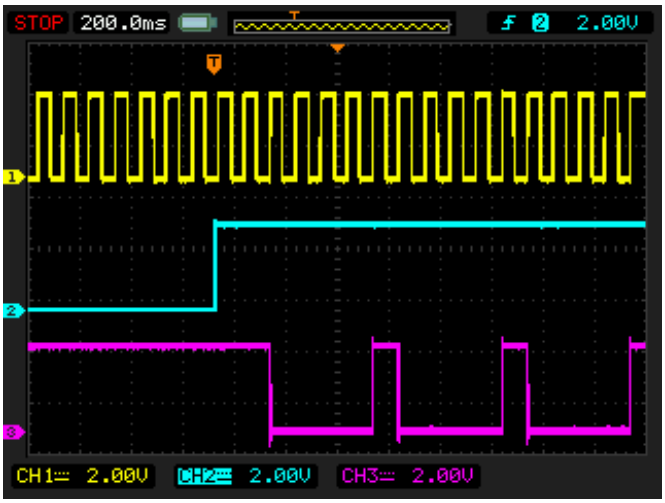


Figure 20. Waveform, Triggered on Button Pressed

Channel 1 (yellow/top) – Logic generator
Channel 2 (light blue/2nd line) – Button, 1 - enable Counter; 0 - disable Counter
Channel 3 (magenta/3rd line) – Counter output

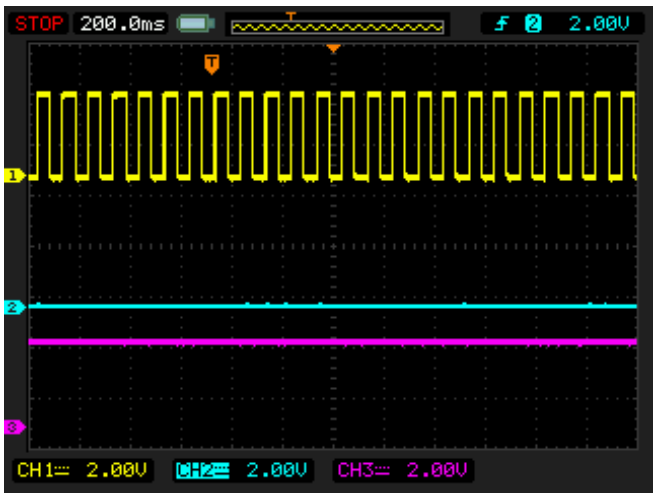


Figure 21. Waveform, no Triggered on Button Released

Channel 1 (yellow/top) – Logic generator
Channel 2 (light blue/2nd line) – Button, 1 - enable Counter; 0 - disable Counter
Channel 3 (magenta/3rd line) – Counter output

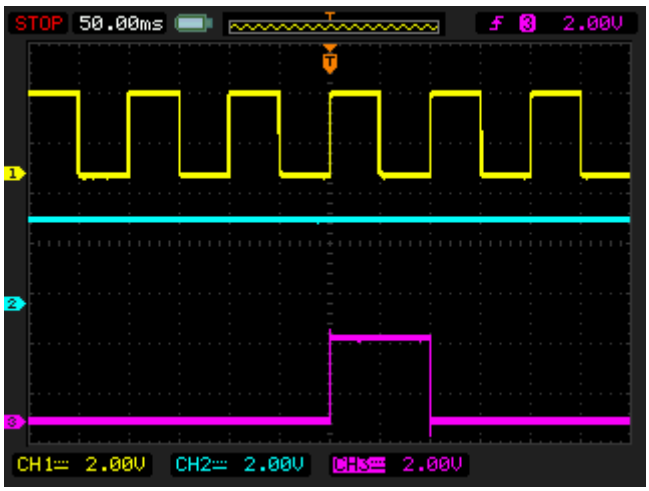


Figure 22. Waveform of the Pulse Width of the Logic Generator and Count End Signal

As shown in *Figure 21* and *Figure 22* Counter works only when the button is pressed.

4.2 Project: LED String with Direction

For this project we will need:

- Analog pin for input data
- Digital pin for PWM output
- ADC block
- PWM block

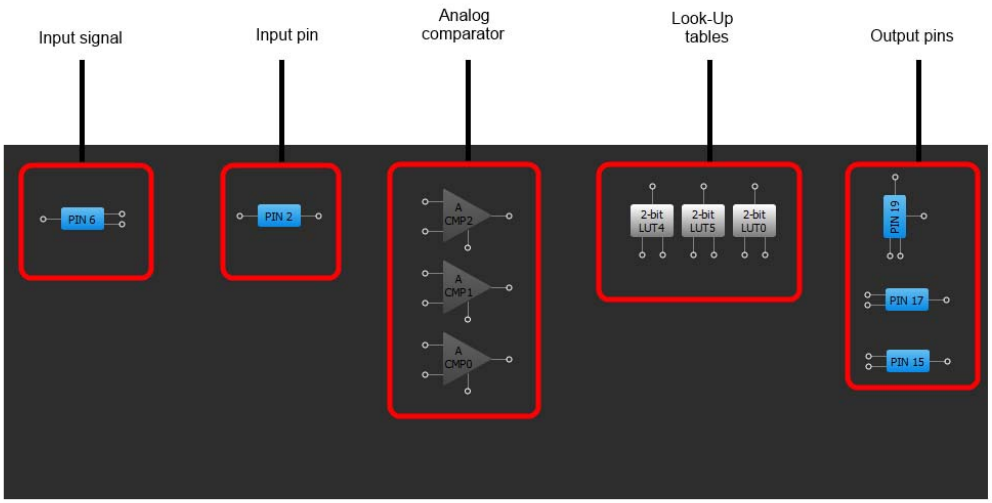


Figure 23. Used Blocks for Current Project

For testing this project, the Signal generator with sine waveform is used.

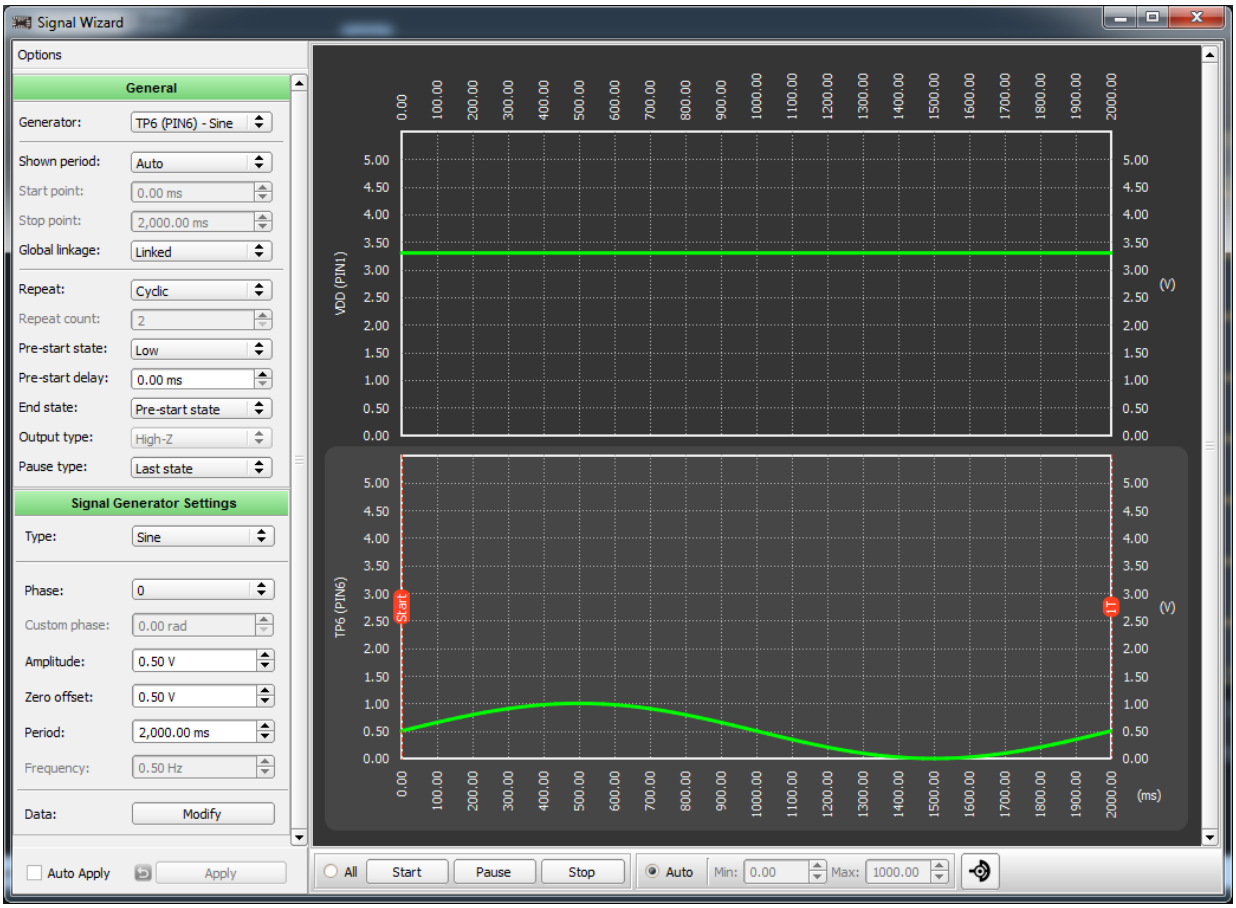


Figure 24. Sine Waveform Generated with Signal Generator

Figure 25. Emulation Window, with Buffered LED and Signal Generator

Pin configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
2	DIRECTION	Input	Controls direction
6	SIGNAL	Input	Analog Input
11	GND	GND	Ground
15	LED_A	Output	LED
17	LED_B	Output	LED
19	LED_C	Output	LED

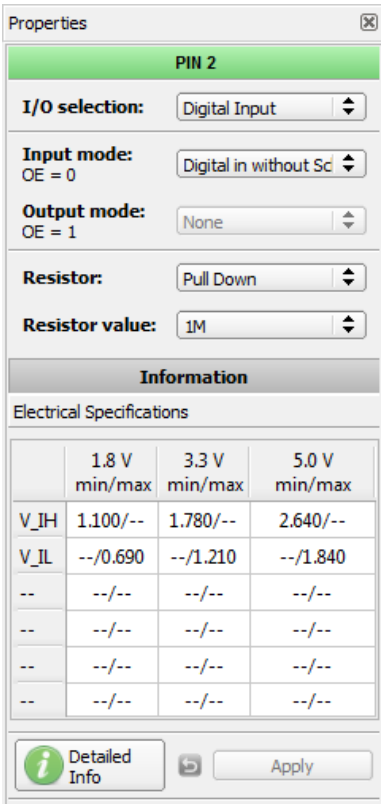


Figure 26. Pin Properties

Pin 6 is configured as analog input-output. This pin is used for generating SINE waveform.

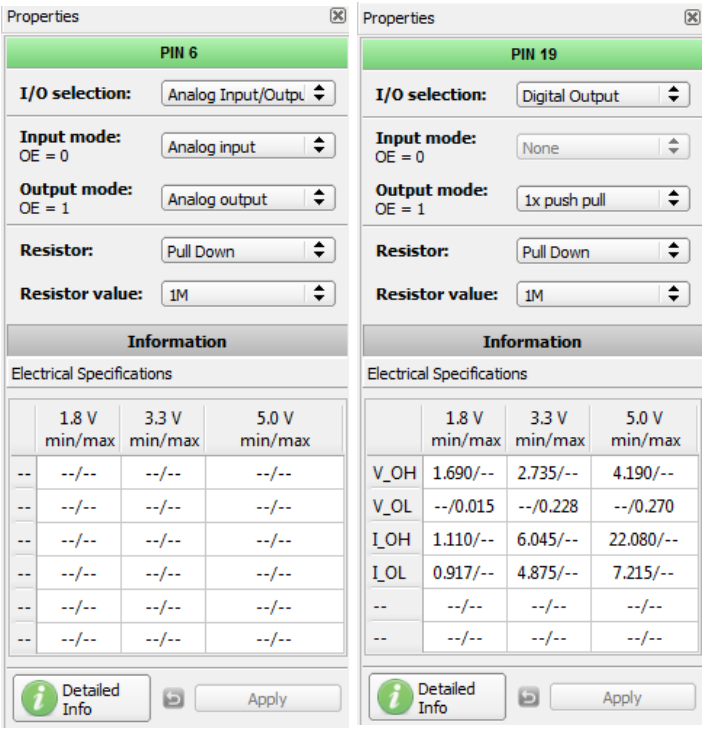


Figure 27. Pin Properties

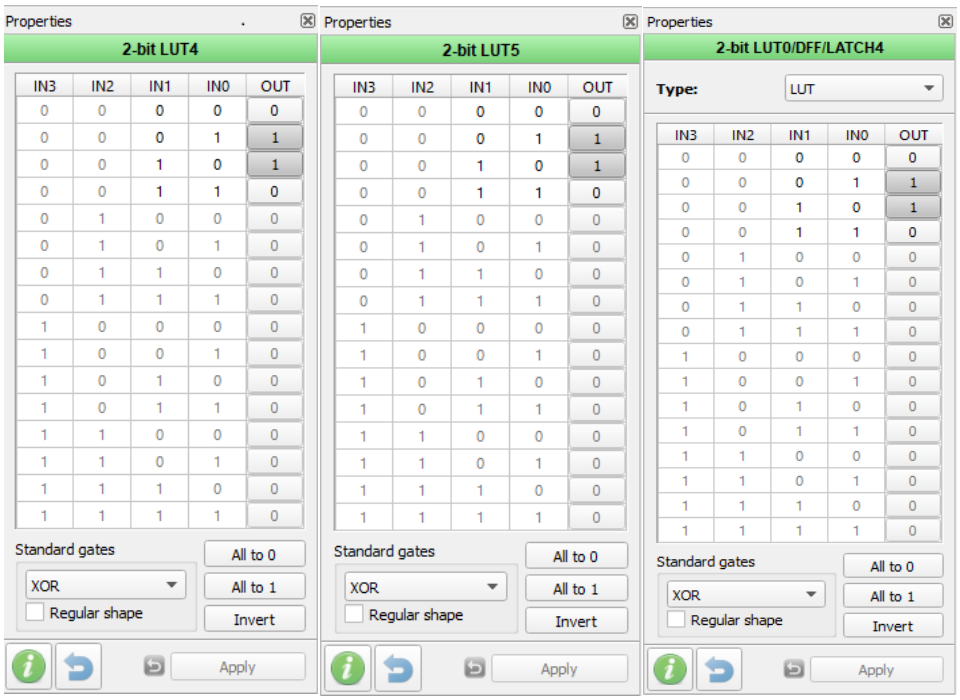


Figure 28. Look-Up Tables Properties Configured as XOR Gate

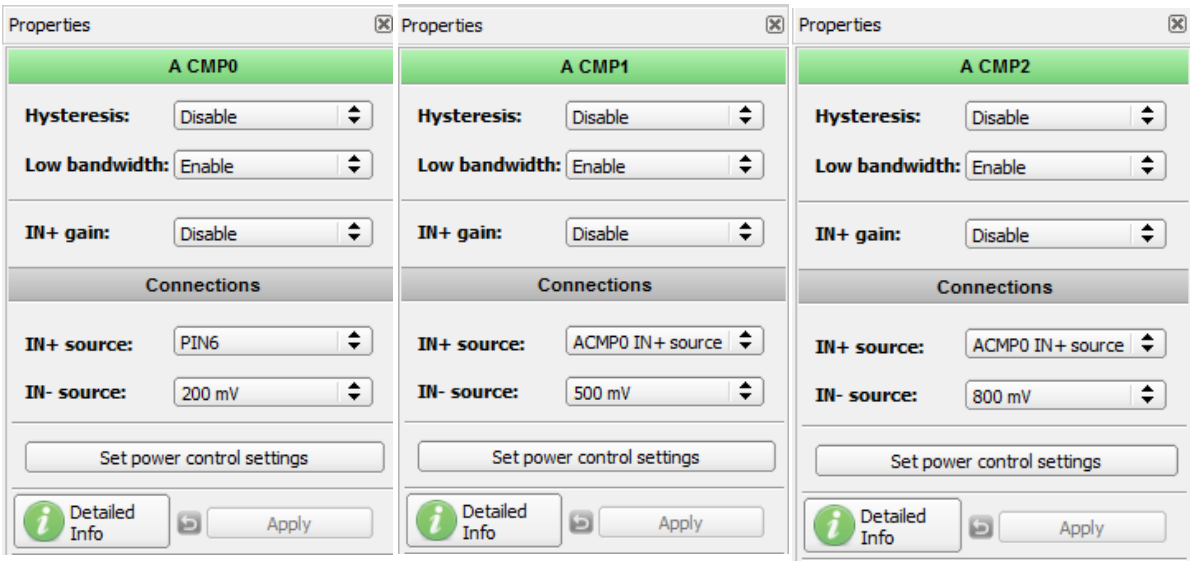


Figure 29. ACMP Properties

Pin 15, 17, 19 - configured as output with 1x push pull. They are used for testing purpose.

All comparators positive inputs are connected to the Pin 6 analog input. When the voltage on the positive input is higher than the voltage on the negative input, comparator will set logic “1” on its output. ACMP0 positive input is 200 mV, ACMP1 is 500 mV, and ACMP2 is 800 mV, creating 4 states:

- All LEDs are off
- LED_A is on
- LED_A and LED_B are on
- All LEDs are on

If Pin 2 logic level is set to “1”, these states will transform into:

- All LEDs are on
- LED_A and LED_B are on
- LED_A is on
- All LEDs are off

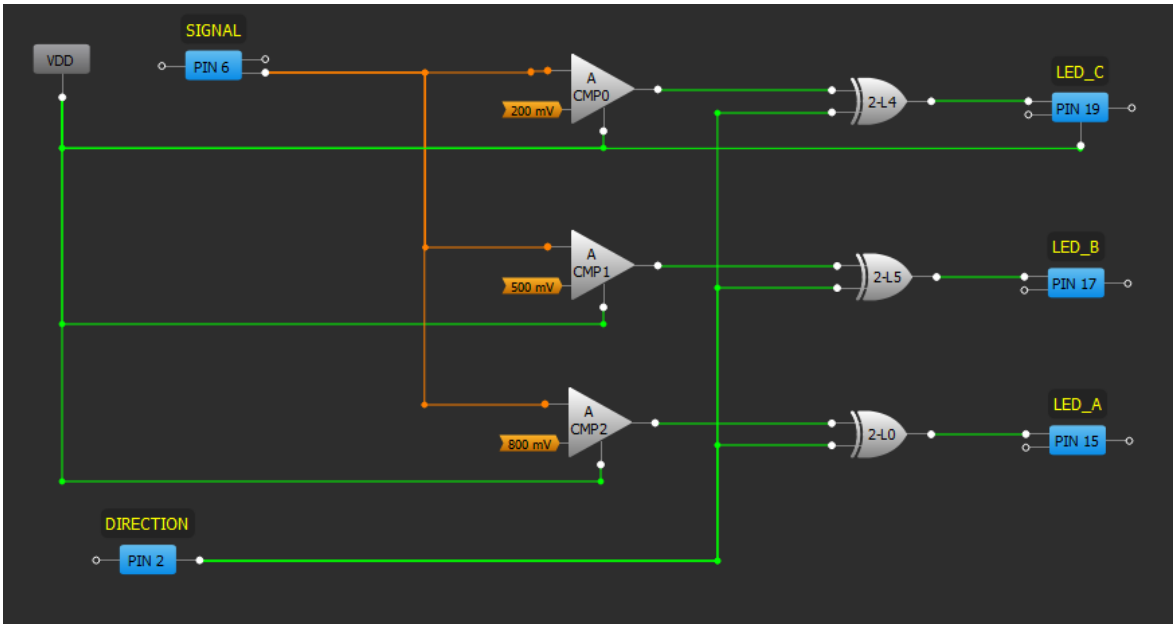


Figure 30. GreenPAK Designer

Functionality Waveform
Channel 1 (yellow/top) – Direction
Channel 2 (light blue /2nd line) – LED_A
Channel 3 (magenta/3rd line) – LED_B
Channel 4 (blue / 4rth line) – LED_C

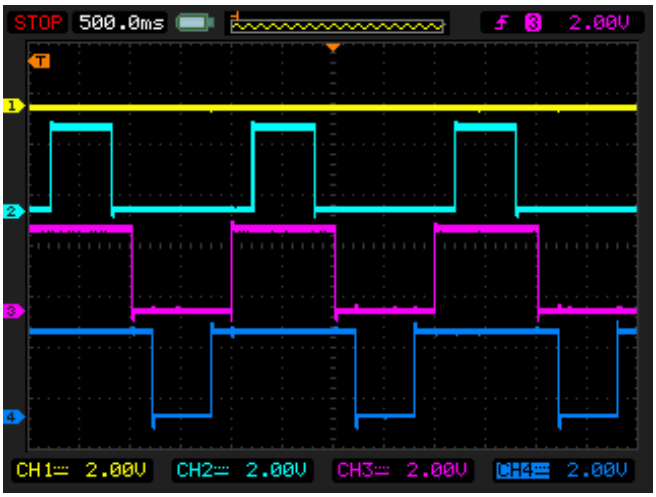


Figure 31. LED Output with Direction (PIN2) Low

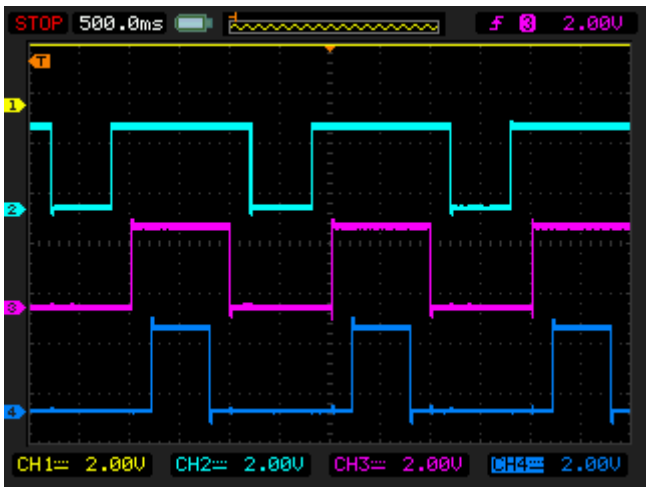


Figure 32. LED Output with Direction (PIN2) High

The PWM duty cycle rises up to 100% when analog signal is close to 1 V.

Conclusion

This Development Platform is a truly versatile tool. It allows the designer to create a custom project within minutes, without using additional devices (except oscilloscope).

For more information please visit our website http://www.silego.com/.

5 Appendix A - Electrical Specification

Mode	Parameter	Min.	Typ.	Max.	Units
General	Test Point Capacitance	19.5	--	--	pF
	Input Leakage Current	--	--	14	nA
	Max. Current through Protection Diode to VDD	--	--	200	mA
	Ripple & Noise	20	--	40	mVp-p
VDD Power Supply Generator (VDD)	Voltage Range	1.5	--	5.5	V
	VDD Max. Current	--	--	70	mA
	Voltage Output Total Error	--	±30	--	mV
Logic generator	Number of Channels (TP2...TP10, TP12...TP20)	--	--	18	--
	Output Voltage High	--	VDD	--	V
	Output Voltage Low	0.4	--	0.8	V
	Max. Current per TP	--	--	30	mA
	Max. Total Current per TPs	--	--	250	mA
	Rise Time	4	--	75	ns
	Fall Time	4	--	60	ns
	Full-Scale Settling Time (0 to 5.5 V)	30	40	75	ns
	Max. Output Frequency	0.152	--	5000	Hz
	Max. Number of Points	--	--	180	--
	Sample Rate	--	10	--	kSPS
Signal Generator	Number of Channels (TP3...TP10, TP12...TP18)	--	--	15	--
	Output Voltage Range	0	--	5.5	V
	DC Output Impedance	--	0.5	--	Ω
	Short-Circuit Current	--	--	30	mA
	Min. Output Voltage	--	--	19	mV
	Output Total Error	--	--	±7	mV
	Output Frequency (SINE)	0.01	--	2500	Hz
	Max. Number of Points	--	--	60	--
	Sample Rate	--	10	--	kSPS
Virtual Button, VDD/GND, Pull Up/Down Driver	Output Level High	--	VDD	--	--
	Output Level Low	--	GND	--	--
	Strong Drive (VDD/GND) Resistance	--	100	--	Ω
	Pull Up/Down Resistance	3.5	5.6	8.5	kΩ

Mode	Parameter	Min.	Typ.	Max.	Units
Expansion Connector Switch	Max. Voltage	--	--	5.5	V
	Continuous Current through Any Terminal	--	--	±30	mA
	Switch On-Resistance	--	20	40	Ω
	External VDD Switch On-Resistance	--	10	20	Ω
	On Leakage Current	-20	--	20	nA
	Off Leakage Current	-10	--	10	nA
	Bandwidth	--	--	10	MHz
	Max. VDD Supply from External Source	--	--	5.66	V

6 Appendix B - Schematic Diagram

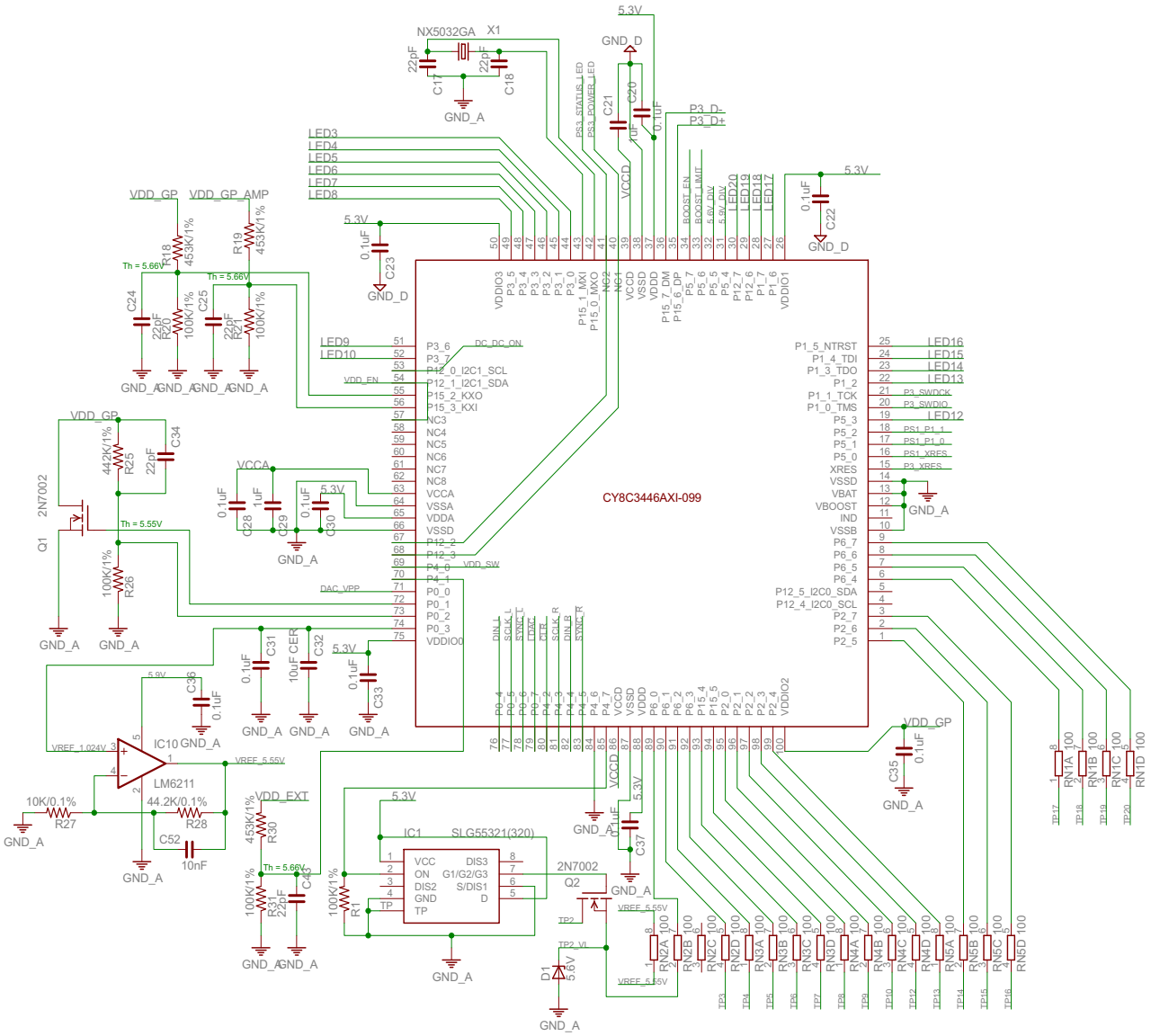


Figure 33. MCU

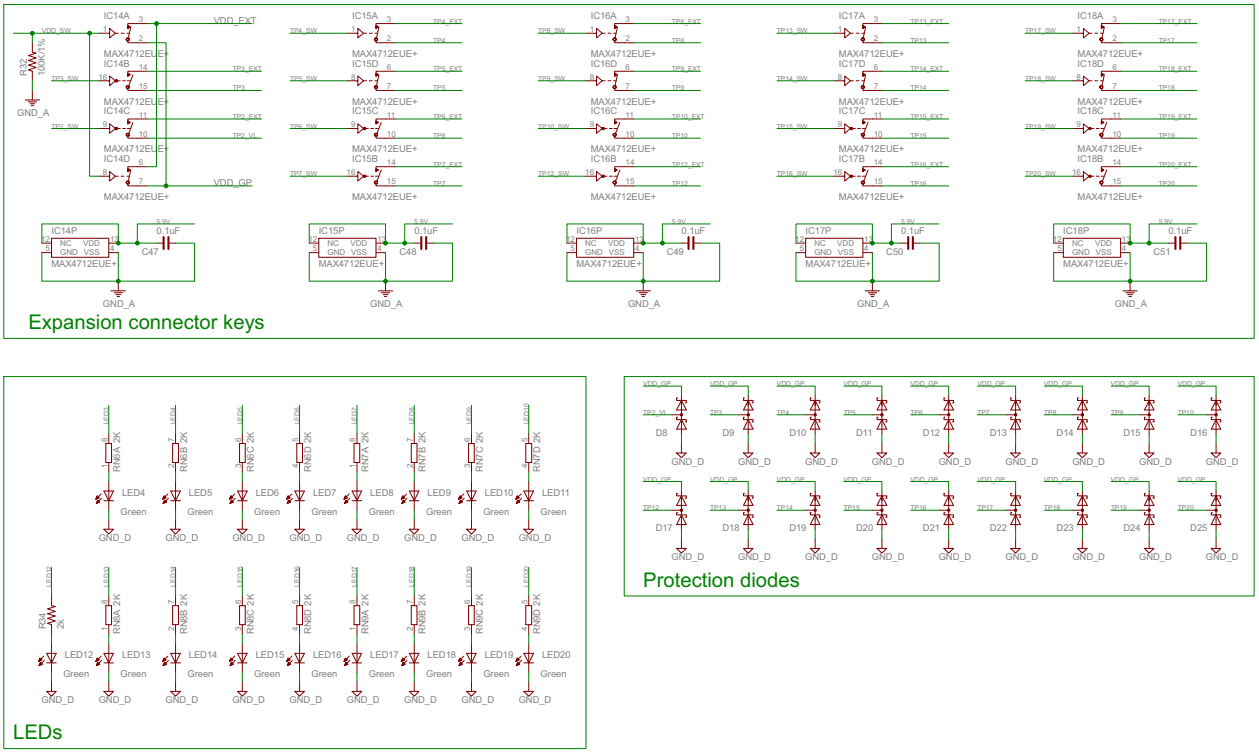


Figure 34. Analog Switches, Protection Diodes and LEDs

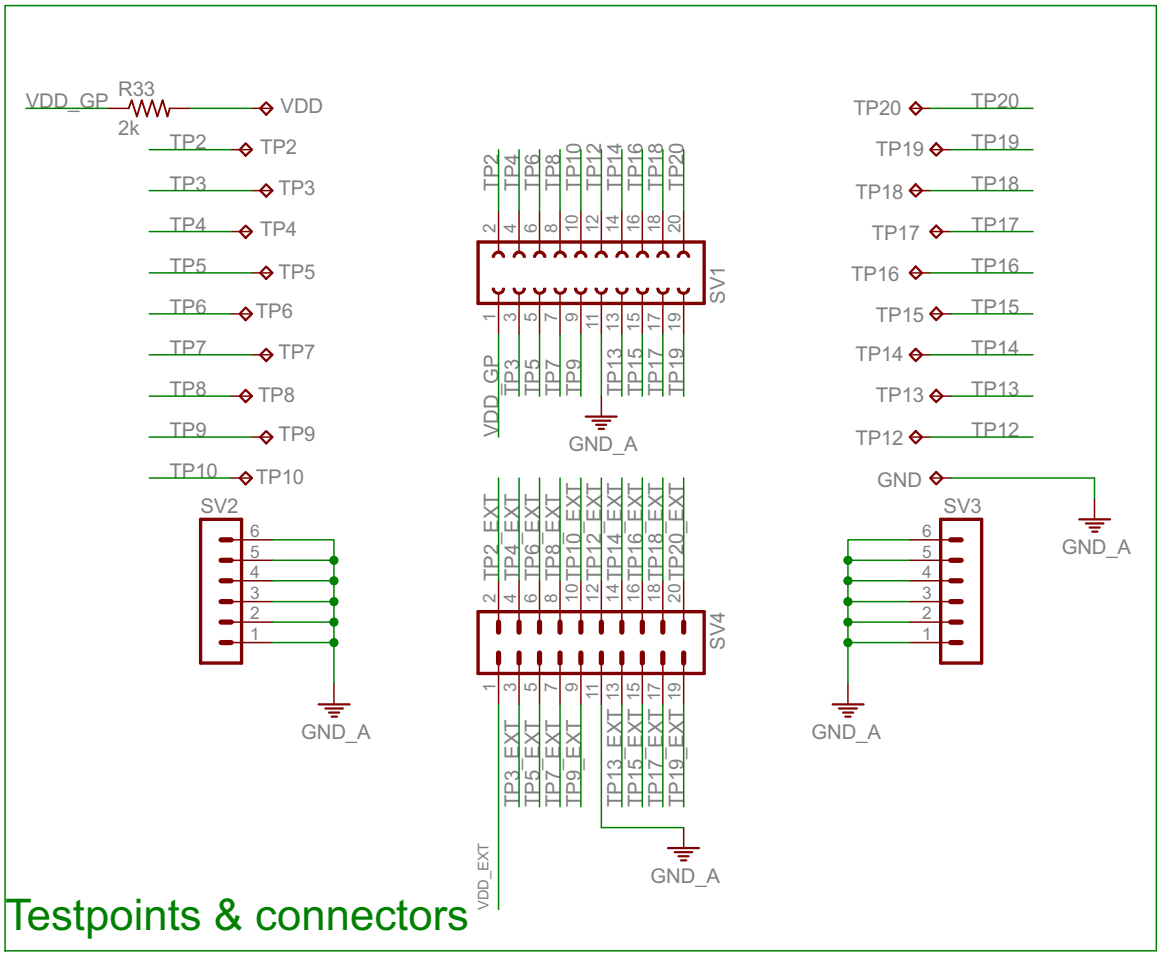


Figure 35. Socket and Expansion Connectors

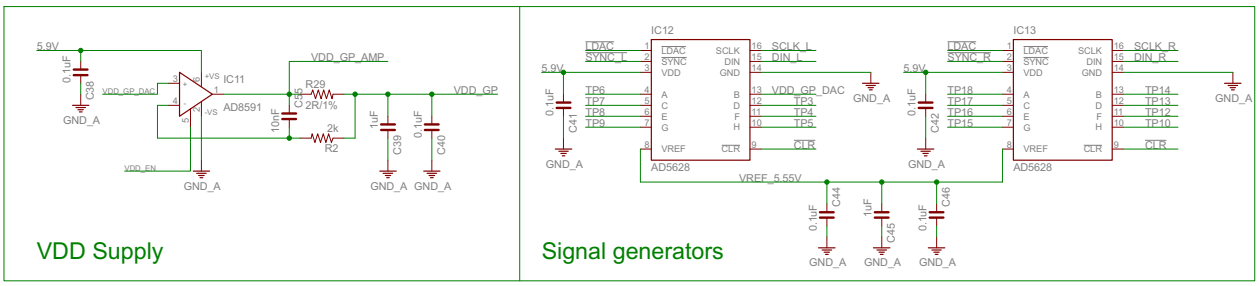


Figure 36. Signal Generators

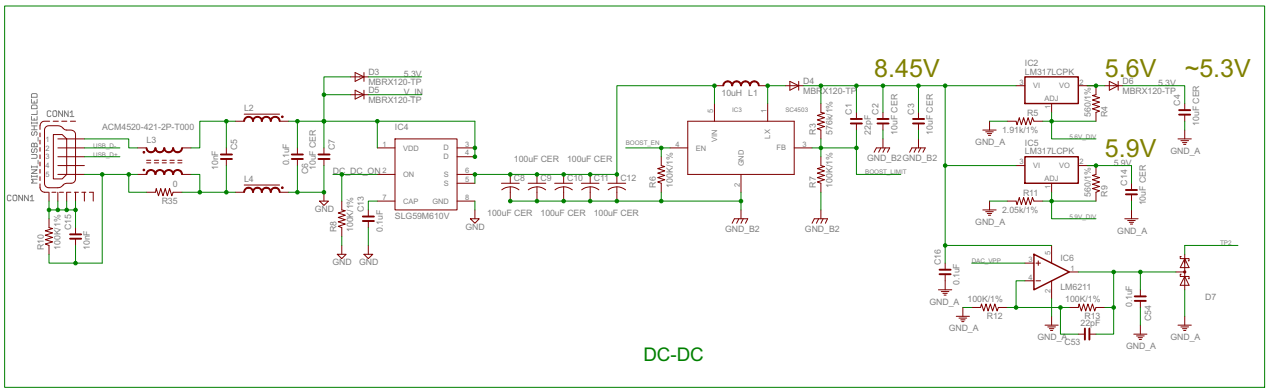


Figure 37. Boost Converter USB Interface

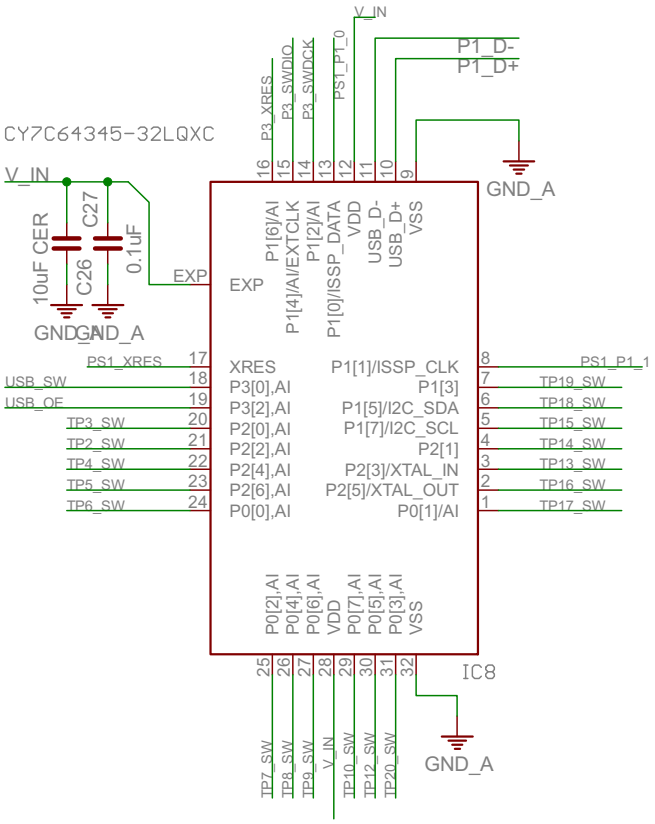


Figure 38. Port Extender

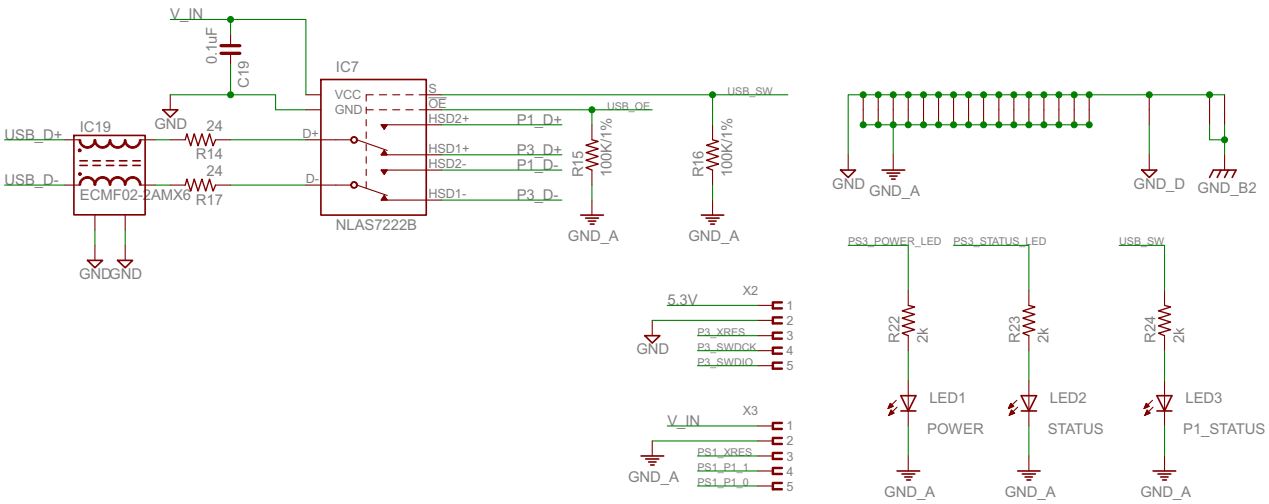


Figure 39. USB Protection

7 Appendix C - BOM

#	Items	Package	Quantity per Development Board	Symbol
1	N/A	TQFN20	1	
2	MCU	TQFN-100	1	IC9
3	CY7C64345-32LQXC	QFN-32	1	IC8
4	AD5628BRUZ-2	16TSSOP	2	IC12, IC13
5	NLAS7222BMUTBG	10-UFQFN	1	IC7
6	MAX4712EUE+	16TSSOP	5	IC14-IC18
7	BAS21SLT1G	SOT-23-3	19	D7-D25
8	GM1JS35200AE	0603 (1608 Metric)	1	LED1
9	LB Q39E-N1P1-35-1	0603 (1608 Metric)	1	LED2
10	LW Q38G-Q1S1-3K6L-1	0603 (1608 Metric)	1	LED3
11	LTST-C193KGKT-5A	0603 (1608 Metric)	17	LED4-LED20
12	NX5032-GA -25.0MHz-LN-CD-1	2-SMD	1	X1
13	SC4503TSKTRT	TSOT23-5	1	IC3
14	USB-M26FTR		1	CONN1
15	2N7002	SOT-23-3	2	Q1, Q2
16	MBRX120-TP	SOD-123	4	D3-D6
17	SLG59M610V	TDFN-8	1	IC4
18	AD8591	SOT-23-6	1	IC11
19	ECMF02 -2AMX6	6-UFQFN	1	IC19
20	NRS4018T100MDGJ	4.00x4.00x1.8mm	1	L1
21	BLM18KG260TN1	0603 (1608 Metric)	2	L2, L4
22	RESISTOR 10k OHM 1/10W 1%	0603 (1608 Metric)	1	R27
23	RESISTOR 44.2k OHM 1/10W 1%	0603 (1608 Metric)	1	R28
24	ACM4520-421-2P-T000	4.70x4.50mm	1	L3
25	GRM31CF50J107ZE01L	1206 (3216 Metric)	5	C8-C12
26	LM317LCPK	SOT89-3	2	IC2, IC5
27	LM6211MF/NOPB	SOT23-5	2	IC6, IC10
28	GRM155F51C104ZA01D	0402 (1005 Metric)	28	C6, C13, C16, C19, C20, C22, C23, C27, C28, C30, C31, C33, C35, C36, C37, C38, C40, C41, C42, C44, C46, C47, C48, C49, C50, C51, C54, Csoc
29	EMK316BJ106KL-T	1206 (3216 Metric)	7	C2, C3, C4, C7, C14, C26, C32
30	C2012X7R1C105K/1.25	0805 (2012 Metric)	4	C21, C29, C39, C45
31	CC0402KRX7R9BB103	0402 (1005 Metric)	4	C5, C15, C52, C55

#	Items	Package	Quantity per Development Board	Pull down
32	CC0402JRNPO9BN220	0402 (1005 Metric)	8	C1, C17, C18, C24, C25, C34, C43, C53
33	RESISTOR 442k 1/16W 1%	0402 (1005 Metric)	1	R25
34	RESISTOR 100k 1/16W 1%	0402 (1005 Metric)	14	R1, R6, R7, R8, R10, R12, R13, R15, R16, R20, R21, R26, R31, R32
35	RESISTOR 453k 1/16W 1%	0402 (1005 Metric)	3	R18, R19, R30
36	RESISTOR 576k 1/16W 1%	0402 (1005 Metric)	1	R3
37	RESISTOR 560 1/16W 1%	0402 (1005 Metric)	2	R4, R9
38	RESISTOR 2.05 1/16W 1%	0402 (1005 Metric)	1	R11
39	RESISTOR 1.91k 1/16W 1%	0402 (1005 Metric)	1	R5
40	RESISTOR 2k 1/16W	0402 (1005 Metric)	6	R2, R22, R23, R24, R33, R34
41	RESISTOR 24 Ω	0402 (1005 Metric)	2	R14, R17
42	RESISTOR 2 Ω	0805 (2012 Metric)	1	R29
43	YC164-JR-072KL	1206 (3216 Metric)	4	RN6, RN7, RN8, RN9
44	YC164-JR-07100RL	1206 (3216 Metric)	5	RN1, RN2, RN3, RN4, RN5
45	5000_		1	VDD
46	5001_		1	GND
47	5002_		18	TP2-TP10, TP12-TP20
48	SJ61A6		5	
49	TSW-110-08-L-D-RA	0.100" (2.54mm)	2	SV4, SVsoc
50	SSQ-110-02-T-D-RA	0.100" (2.54mm)	1	SV1
51	961106-6404-AR	0.100" (2.54mm)	2	SV2, SV3
52	3021009-06		1	
53	RESISTOR 0 Ω	1206 (3216 Metric)	1	R35
54	SLG55321	TDFN-8	1	IC1
55	BZV55C5V6-TP	SOD-80C	1	D1