Product Change Notification - SYST-14LBXL167

Date:

15 Feb 2019

Product Category:

16-Bit - Microcontrollers and Digital Signal Controllers

Affected CPNs:

Notification subject:

ERRATA - PIC24FJ256GA705 Family Silicon Errata and Data Sheet Clarification

Notification text:

SYST-14LBXL167

Microchip has released a new DeviceDoc for the PIC24FJ256GA705 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at PIC24FJ256GA705 Family Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: 1) Added silicon errata issue 16 (ADC) 2) Added data sheet clarifications 1 (Power-Saving Features), 2 (Flash Program Memory) 3 (Memory Organization) and 4 (Capture/Compare/PWM/Timer Modules (MCCP).

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 15 Feb 2019

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

PIC24FJ256GA705 Family Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

PIC24FJ128GA704-E/PT
PIC24FJ128GA704-I/PT
PIC24FJ128GA704-I/PTC01
PIC24FJ128GA704T-I/PT
PIC24FJ128GA704T-I/PTC01
PIC24FJ128GA705-E/M4
PIC24FJ128GA705-E/PT
PIC24FJ128GA705-I/M4
PIC24FJ128GA705-I/PT
PIC24FJ128GA705T-I/M4
PIC24FJ128GA705T-I/PT
PIC24FJ256GA705-E/M4
PIC24FJ256GA705-E/PT
PIC24FJ256GA705-I/M4
PIC24FJ256GA705-I/PT
PIC24FJ256GA705T-I/M4
PIC24FJ256GA705T-I/PT
PIC24FJ64GA704-E/PT
PIC24FJ64GA704-I/PT
PIC24FJ64GA704T-I/PT
PIC24FJ64GA705-E/M4
PIC24FJ64GA705-E/PT
PIC24FJ64GA705-I/M4
PIC24FJ64GA705-I/PT
PIC24FJ64GA705T-I/M4
PIC24FJ64GA705T-I/PT

PIC24FJ256GA705 Family Silicon Errata and Data Sheet Clarification

The PIC24FJ256GA705 family devices that you have received conform functionally to the current Device Data Sheet (DS30010118**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24FJ256GA705 family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on Page 9, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24FJ256GA705 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	
		A3	A4			A3	A4
PIC24FJ64GA705	0x7507	0x03	0x04	PIC24FJ256GA704	0x750D	0x03	0x04
PIC24FJ128GA705	0x750B			PIC24FJ64GA702	0x7506		
PIC24FJ256GA705	0x750F			PIC24FJ128GA702	0x750A		
PIC24FJ64GA704	0x7505			PIC24FJ256GA702	0x750E		
PIC24FJ128GA704	0x7509			—			

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC24FJ256GA705 Family Flash Programming Specification"* (DS30010102) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)	
				A3	A4
I2C	Address Hold	1.	In Slave mode when AHEN = 1 (Address Hold Enable), if ACKDT (Acknowledge Data bit) is set at the beginning of address reception, clock stretching will not happen after the 8th clock.	X	X
Reset	Trap Conflict	2.	The TRAPR bit is not getting set when a hard trap conflict occurs.	X	X
I2C	Data Hold	3.	In Slave mode when DHEN = 1 (Data Hold Enable), if ACKDT (Acknowledge Data bit) is set at the beginning of data reception, then a slave interrupt will not occur after the 8th clock.	X	X
Primary XT and HS Oscillator (POSC)	Primary Oscillator Start-up Timer (OST)	4.	OST may indicate oscillator is ready for use too early.	X	X
Power	Retention Sleep	5.	When the device wakes up from Retention Sleep mode (RETEN bit (RCON[12]) = 1, $\overline{\text{LPCFG}}$ bit (FPOR[2]) = 0), a device Reset may occur. The BOR, POR and EXTR bits in the RCON register are set erroneously for this Reset.	X	
Power	Power BOR	6.	The main BOR may not function on some devices.	X	
I2C	Slave Mode	7.	Bus data can get corrupted when it matches with one of the slave addresses connected to the bus.	X	X
I2C	Slave Mode	8.	In 10-Bit Addressing Slave mode, on receiving the upper address byte (A9 and A8 bits), the Acknowledge Time Status bit (ACKTIM) is not asserted during the Acknowledgment sequence.	X	X
I2C	Slave Receive Mode	9.	The Acknowledge Time Status bit (ACKTIM) is asserted only if the Address Hold Enable (AHEN) or Data Hold Enable (DHEN) bit is enabled.	X	X
I2C	Bus Collisions	10.	In Slave mode, false bus collision triggers are generated when bus collision is enabled (SBCDE = 1).	X	X
I2C	Hold Time	11.	Minimum hold time of 300 ns is not achieved when the SDAx Hold Time Selection bit (SDAHT) is set.	X	X
I2C	Slave Mode	12.	In Slave mode, the Bus Collision Detect bit (BCL) cannot be cleared when bus collision detection is enabled (SBCDE = 1).	X	X
I2C	Slave Mode	13.	In Slave mode, an address cannot be received when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = 1).	X	X
UART	Break Character Transmission	14.	The Transmit Shift Register Empty (TRMT) bit is unreliable when there are back-to-back Break character transmissions.	X	X
ADC	Differential Nonlinearity	15.	Increase DNL specification on the positive side.		X
ADC	Current	16.	ADC draws additional current when enabled.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: I^2C

In Slave mode when AHEN = 1 (Address Hold Enable), if the ACKDT bit (Acknowledge Data) is set at the beginning of address reception, clock stretching will not happen after the 8th clock.

Work around

In Slave mode, user software should clear ACKDT on receiving the Start bit.

Affected Silicon Revisions

A3	A4						
X	X						

2. Module: Reset

If a lower priority address error trap occurs while a higher priority oscillator failure trap is being processed, the TRAPR bit (RCON[15]) is not set. A Trap Conflict Reset does not occur as expected and the device may stop executing code.

Work around

None. However, a $\overline{\text{MCLR}}$/POR Reset will recover the device.

Affected Silicon Revisions

A3	A4						
X	X						

3. Module: I^2C

In Slave mode when DHEN = 1 (Data Hold Enable), if the ACKDT bit (Acknowledge Data) is set at the beginning of data reception, then the slave interrupt will not occur after the 8th clock.

Work around

In Slave mode, user software should clear ACKDT on receiving the Start bit.

Affected Silicon Revisions

A3	A4						
X	X						

4. Module: Primary XT and HS Oscillator (POSC)

The Primary Oscillator Start-up Timer (OST) may indicate the oscillator is ready for use too early. Clocking the device before the oscillator is ready may result in incorrect execution and exceptions. This issue exists when the POSC is requested at power-on, during clock switching, when waking from Sleep or when a peripheral module requests the POSC directly. This issue affects XT and HS modes only.

Work around

Make sure that the Primary Oscillator clock is ready before using it by following these steps:

1. Running on a non-POSC source, request the POSC clock using a peripheral such as REFO.
2. Provide a delay to stabilize the POSC.
3. Switch to the POSC source.

Example 1 shows a work around for the device power-on and Example 2 explains the work around when the device wakes from Sleep.

EXAMPLE 1: USING POSC AT POWER-ON

```
#pragma config FNOSC = FRC            // Oscillator Selection bits (Fast RC oscillator (FRC))
// Clock Switching Enabled (Failsafe Clock Monitor can be enabled or disabled)
#pragma config FCKSM = CSECMD
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
int     main()
{
    // configure REFO to request POSC
    REFOCONLbits.ROSEL = 2;           // POSC
    REFOCONLbits.ROOUT = 0;           // disable output
    REFOCONLbits.ROEN = 1;            // enable module

    // wait for POSC stable clock
    // this delay may vary depending on different application conditions
    // such as voltage, temperature, layout, XT or HS mode and components
    {   // delay for 9 ms
        unsigned int delayms = 9;
        while(delayms--) asm volatile("repeat #(8000000/1000/2) \n nop");
    }

    // switch to POSC = 2
    __builtin_write_OSCCONH(2);
    __builtin_write_OSCCONL(1);
    while(OSCCONbits.OSWEN == 1);     // wait for switch
```

EXAMPLE 2: USING POSC WHEN WAKING FROM SLEEP

```
// Clock Switching Enabled (Failsafe Clock Monitor can be enabled or disabled)
#pragma config FCKSM = CSECMD
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
    // switch to FRC = 0 before entering sleep
    __builtin_write_OSCCONH(0);
    __builtin_write_OSCCONL(1);
    while(OSCCONbits.OSWEN == 1);     // wait for switch

    // enter sleep mode
    Sleep();

    // configure REFO to request POSC
    REFOCONLbits.ROSEL = 2;           // POSC
    REFOCONLbits.ROOUT = 0;           // disable output
    REFOCONLbits.ROEN = 1;            // enable module

    // wait for POSC stable clock
    // this delay may vary depending on different application conditions
    // such as voltage, temperature, layout, XT or HS mode and components
    {   // delay for 9 ms
        unsigned int delayms = 9;
        while(delayms--) asm volatile("repeat #(8000000/1000/2) \n nop");
    }

    // switch to POSC = 2
    __builtin_write_OSCCONH(2);
    __builtin_write_OSCCONL(1);
    while(OSCCONbits.OSWEN == 1);     // wait for switch
```

Affected Silicon Revisions

A3	A4						
X	X						

5. Module: Power

When the device wakes up from Retention Sleep mode (RETEN bit (RCON[12]) = 1, $\overline{\text{LPCFG}}$ bit (FPOR[2]) = 0), occasionally a device reset may occur. The BOR, POR and EXTR bits in the RCON register are set erroneously for this Reset.

Work around

To provide a consistent behavior when the device wakes up from Retention Sleep mode, a software RESET instruction (RESET) should be inserted following the SLEEP instruction. In this case, a Reset will be always be generated when the device wakes up from Retention Sleep. Example 3 shows the software RESET instruction implementation:

EXAMPLE 3: SOFTWARE RESET AFTER SLEEP INSTRUCTION

```
// ENTER SLEEP MODE.
asm volatile ("pwrsav #0");
// SOFTWARE RESET RIGHT AFTER SLEEP.
asm volatile("reset");
```

Affected Silicon Revisions

A3	A4						
X							

6. Module: Power

The main BOR may not occur when the operating voltage drops below the BOR trip voltage.

Work around

Ensure the device operating voltage does not violate the specified values. Use an external supervisor circuit to reset the device if the operating voltage can be outside the specified values.

Affected Silicon Revisions

A3	A4						
X							

7. Module: I²C

In applications with multiple I²C slaves, bus data can become corrupted when the data payload sent to an addressed slave device matches the bus address of another (unaddressed) slave device.

Work around

Keep track of the bus address and data phases in software. When Address Hold Enable is used (the AHEN bit is set), the application can assert a NACK for any of the received bytes (invalid addresses and data bytes for other slave devices) until a Stop bit is received.

Affected Silicon Revisions

A3	A4						
X	X						

8. Module: I²C

In I²C 10-Bit Slave Addressing mode, on receiving the upper address byte (A9 and A8 bits), the Acknowledge Time Status bit (ACKTIM) is not asserted during the Acknowledgment sequence. This issue is not seen during the reception of the lower address byte (A7 to A0) and data bytes. The hardware asserts the ACKTIM bit on the falling edge of the eighth clock and deasserts on the rising edge of the ninth clock. In this case, ACKTIM is not asserted on upper address byte reception. When AHEN = 1, the clock is stretched after the 8th falling edge and the ACKTIM bit is asserted until the clock is released. If AHEN = 0, the clock is not stretched and ACKTIM is asserted during the Acknowledgment sequence, which is of a short duration. Therefore, the user application can see this issue of the ACKTIM bit not getting asserted when AHEN = 1.

Work around

Instead of polling for ACKTIM to be asserted, poll for the RBF flag.

Affected Silicon Revisions

A3	A4						
X	X						

9. Module: I²C

In I²C Slave Receive mode, the Acknowledge Time Status bit (ACKTIM) has no effect if the Address Hold Enable (AHEN) and Data Hold Enable (DHEN) bits are disabled (AHEN = 0 and DHEN = 0). The Acknowledge Time Status bit (ACKTIM) is asserted only if the Address Hold Enable (AHEN) or Data Hold Enable (DHEN) bit is enabled.

Work around

Instead of polling for the ACKTIM bit to be asserted, poll for the RBF flag.

Affected Silicon Revisions

A3	A4						
X	X						

10. Module: I²C

In Slave mode, false bus collision triggers are generated when the bus collision is enabled (SBCDE = 1).

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

11. Module: I²C

A minimum hold time of 300 ns on SDAx, after the falling edge of SCLx, is not achieved when the SDAx Data Hold Time Selection bit (SDAHT) is set.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

12. Module: I²C

In Slave mode, the Bus Collision Detect bit (BCL) cannot be cleared when bus collision detection is enabled (SBCDE = 1).

Work around

Disable the I²C module and then re-enable the module.

Affected Silicon Revisions

A3	A4						
X	X						

13. Module: I²C

In Slave mode, an address cannot be received when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = 1).

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

14. Module: UART

The Transmit Shift Register Empty (TRMT) bit is unreliable when there are back-to-back Break character transmissions.

For back-to-back Break characters, the TRMT bit may not reflect the actual status. If user software is polling for this bit to be set, it may result in dummy bytes getting transmitted instead of Break characters.

Work around

Poll the UARTx Transmit Break bit, UTXBRK (UxSTA[11]), to be cleared instead of the TRMT bit (U1STA[8]) to be set. The UTXBRK status bit will be cleared after a Break character transmission.

Affected Silicon Revisions

A3	A4						
X	X						

15. Module: ADC

As shown in the following table, the ADC Differential Nonlinearity (DNL) specification on the positive side changes (changes shown in **bold**).

TABLE 32-24: A/D MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
A/D Accuracy							
AD22B	DNL	Differential Nonlinearity	—	—	**< +2** **< -1**	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V

Work around

None.

Affected Silicon Revisions

A3	A4						
	X						

16. Module: ADC

On some devices, the current drawn may increase when the ADC is enabled. The power-saving modes or ADC configuration cannot stop the additional current being drawn. However, the additional current does not affect the performance of either the ADC or the device.

Work around

Disable the ADC when it is not used in the application.

Affected Silicon Revisions

A3	A4						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS30010118**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Power-Saving Features

The VREGS column in Table 10-1: Low-Power Sleep Modes of the device data sheet should be read as the one given in the following table. .

TABLE 10-1: LOW-POWER SLEEP MODES

RETEN	VREGS	MODE	Relative Power
0	**0**	Sleep	A Few µA Range
0	**1**	Fast Wake-up	100 µA Range
1	**0**	Retention Sleep	Less than 1 µA
1	**1**	Fast Retention	A Few µA Range

2. Module: Flash Program Memory

The following Note has to be added below the text in **Section 6.4 "Enhanced In-Circuit Serial Programming"** of the device data sheet.

Note:	The PGD2/PGC2 port on 28-pin packages supports ICSP™ only, so Enhanced ICSP programming does not work.

3. Module: Memory Organization

Section 4.1.2 "Hard Memory Vectors" of the device data sheet has to be appended with a paragraph; the section should now read as:

All PIC24F devices reserve the addresses between 000000h and 000200h for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on a device Reset to the actual start of code. A `GOTO` instruction is programmed by the user at 000000h, with the actual address for the start of code at 000002h.

The PIC24FJ256GA705 family devices can have up to two Interrupt Vector Tables (IVTs). The first is located from addresses, 000004h to 0000FFh. The Alternate Interrupt Vector Table (AIVT) can be enabled by the AIVTDIS Configuration bit if the Boot Segment (BS) is present and at least two pages in size. If the user has configured a Boot Segment, the AIVT will be located at the address, (BSLIM[12:0] – 1) x 0x800. These vector tables allow each of the many device interrupt sources to be handled by separate Interrupt Service Routines (ISRs). A more detailed discussion of the Interrupt Vector Tables is provided in **Section 8.1 "Interrupt Vector Table"**.

4. Module: Capture/Compare/PWM/Timer Modules (MCCP)

Register 16-8: CCPxSTATH: CCPx Status Register High is not implemented.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (10/2016)

Initial release of this document; issued for Revision A3.

Rev B Document (12/2016)

Added silicon errata issue 5 (Power).

Rev C Document (6/2017)

Added silicon errata issue 6 (Power).

Added data sheet clarifications 1 (Referenced Sources), 2 (Device Overview), 3 (Power-Saving Features), 4 (Capture/Compare/PWM/Timer Modules (MCCP)), 5 (Serial Peripheral Interface), 6 (Serial Peripheral Interface), 7 (Comparator Voltage Reference), 8 (High/Low-Voltage Detect (HLVD)), 9 (High/Low-Voltage Detect (HLVD)), 10 (Electrical Characteristics) and 11 (Packaging Information.

Rev D Document (3/2018)

Rev D is updated for the silicon revision A4.

Added silicon errata issues 7 (I^2C), 8 (I^2C), 9 (I^2C), 10 (I^2C), 11 (I^2C), 12 (I^2C), 13 (I^2C), 14 (UART) and 15 (ADC).

Incorporated all data sheet clarifications into the *"PIC24FJ256GA705 Family Data Sheet"* (DS30010118**C**).

Rev E Document (2/2019)

Added silicon errata issue 16 (ADC)

Added data sheet clarifications 1 (Power-Saving Features), 2 (Flash Program Memory) 3 (Memory Organization) and 4 (Capture/Compare/PWM/Timer Modules (MCCP)).

Note the following details of the code protection feature on Microchip devices:

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ISBN: 978-1-5224-4150-2

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