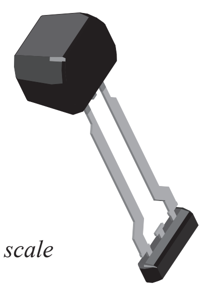
Vibration-Tolerant Hall-Effect Transmission Speed and Direction Gear Tooth Sensor IC

FEATURES AND BENEFITS

- **Differential Hall-effect sensor** measures ferrous targets with inherent stray field immunity
- **SolidSpeed Digital Architecture™** provides robust, adaptive performance with advanced algorithms that provide vibration immunity over the full target pitch
- **Integrated solution** includes a back-bias magnet and capacitor in a single overmolded package
- **ISO 26262:2011 ASIL B** with integrated diagnostics and certified safety design process (pending assessment)
- **Two-wire current source output** pulse-width protocol supporting speed, direction, and ASIL error reporting
- **EEPROM** enables factory traceability

PACKAGE: 3-pin SIP (suffix SN)



Not to scale

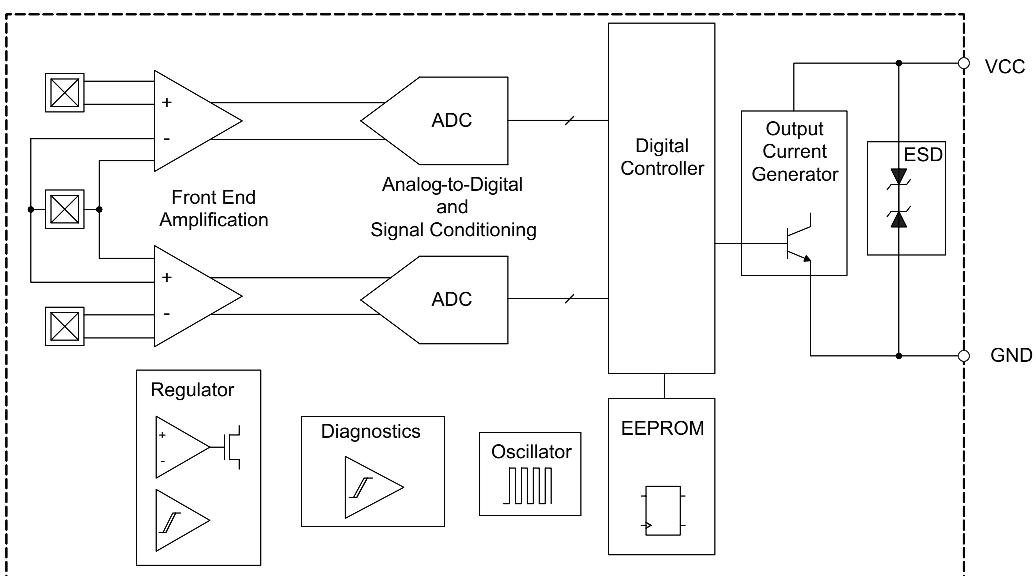
DESCRIPTION

The ATS19520 is an advanced Hall-effect integrated circuit (IC) that uses an integrated back-bias magnet to measure the speed and direction of rotating ferrous targets. The package features an integrated capacitor for electromagnetic compatibility (EMC).

The ATS19520 employs intelligent algorithms that allow stable operation during vibration and highly dynamic air gap environments common to transmission applications. In addition, the differential sensing offers inherent rejection of interfering common-mode magnetic fields.

The ATS19520 was developed in accordance with ISO 26262:2011 as a hardware safety element out of context with ASIL B capability (pending assessment) for use in automotive safety-related systems when integrated and used in the manner prescribed in the applicable safety manual and datasheet.

The ATS19520 is provided in a 3-pin SIP package (suffix SN) that is lead (Pb) free, with tin leadframe plating. The SN package includes an IC, magnet, and capacitor integrated into a single overmold, with an additional molded lead-stabilizing bar for robust shipping and ease of assembly.



Functional Block Diagram

SELECTION GUIDE*

Part Number	Packing
ATS19520LSNBTN-RSWHPYU	Tape and reel, 13-in. reel, 800 pieces per reel

* Not all combinations are available. Contact Allegro sales for availability and pricing of custom programming options.

Configuration Options

ATS19520 L SN □ TN - □ □ □ □ □ □ □ - □

ASIL Protocol:
A – ASIL Protocol Enabled
Blank – ASIL Protocol Disabled

Extended Sudden Air Gap Options
K – Timed Resets Enabled
U – Feature Not Enabled

Calibration Mode Non-Direction Pulses
O – Blanked, no output during calibration
Y – Pulses allowed during calibration

Running Mode Non-Direction Pulses
B – Blanked, no output during Running mode
P – Pulses allowed during Running mode

Vibration Immunity/Direction Change
L – Low vibration immunity with immediate direction-change detection
H – High vibration immunity

Pulse Widths (Typical)
I – Intermediate, Forward = 60 µs, Reverse = 120 µs, Non-Direction = 30 µs
N – Narrow, Forward = 45 µs, Reverse = 90 µs, Non-Direction = 180 µs
W – Wide, Forward = 45 µs, Reverse = 180 µs, Non-Direction = 360 µs

Number of Pulses
S – Single, one pulse per tooth-valley pair

Rotation Direction
F – Forward, pin 1 to pin 3
R – Forward, pin 3 to pin 1

Packing Type

Internal Capacitor
B – 10 nF capactitor
L – 22 nF capacitor

Package Designation

Operating Temperature Range

Allegro Identifier and Device Type

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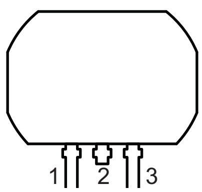
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}	Refer to Power Derating section	28	V
Reverse Supply Voltage	V_{RCC}		–18	V
Operating Ambient Temperature	T_A	Range L	–40 to 150	ºC
Maximum Junction Temperature	$T_{J(max)}$		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

PINOUT DIAGRAM AND TERMINAL LIST



Package SN, 3-Pin SIP Pinout Diagram

Terminal List Table

Number	Name	Function
1	VCC	Supply voltage
2	VCC	Supply voltage
3	GND	Ground

Internal Discrete Capacitor Ratings

Characteristic	Symbol	Notes		Rating	Units
Nominal Capacitance	C_{SUPPLY}	Connected between VCC and GND; refer to Figure 1	B	10	nF
			L	22	nF

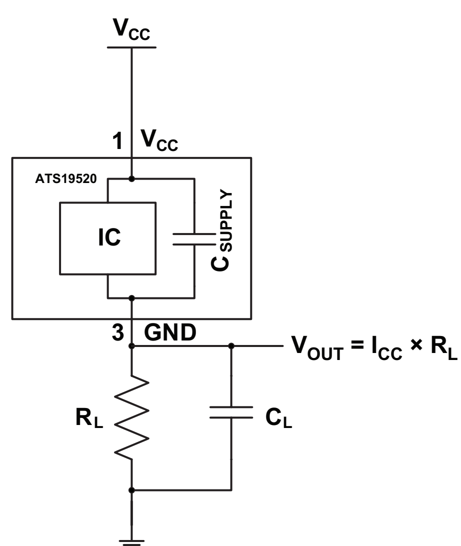


Figure 1: Typical Application Circuit

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OPERATING CHARACTERISTICS: Valid throughout full operating and temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ. [1]	Max.	Unit
GENERAL							
Supply Voltage [2]	V_{CC}	Operating, $T_J < T_{J(max)}$, voltage across pin 1 and pin 3; does not include voltage across R_L		4	–	24	V
Undervoltage Lockout	$V_{CC(UV)}$	V_{CC} 0 V → 5 V or 5 V → 0 V		–	3.6	3.95	V
Reverse Supply Current [3]	I_{RCC}	$V_{CC} = V_{RCC(max)}$		–10	–	–	mA
Supply Current	$I_{CC(LOW)}$	Low-current state		5.9	7	8	mA
	$I_{CC(HIGH)}$	High-current state		12	14	16	mA
	$I_{CC(HIGH)}$ / $I_{CC(LOW)}$	Ratio of high current to low current (isothermal)		1.9	–	–	–
ASIL Safety Current	I_{RESET}	Refer to Figure 7		1.5	–	3.9	mA
PROTECTION CIRCUITS							
Supply Zener Clamp Voltage	$V_{Zsupply}$	I_{CC} = 19 mA, T_A = 25°C		28	–	–	V
POWER-ON CHARACTERISTICS							
Power-On State	POS	$V_{CC} > V_{CC(min)}$, as connected in Figure 1			$I_{CC(LOW)}$		mA
Power-On Time [4]	t_{PO}	Time from $V_{CC} > V_{CC(min)}$, until device has entered calibration		–	–	1	ms
OUTPUT PULSE CHARACTERISTICS, PULSE PROTOCOL [5]							
Output Rise Time	t_r	Voltage measured at pin 2 in Figure 1, R_L = 100 Ω, C_L = 10 pF, measured between 10% and 90% of signal	SNL variant	0	4.5	8	μs
			SNB variant	0	2	4	μs
Output Fall Time	t_r	Voltage measured at pin 3 in Figure 1, R_L = 100 Ω, C_L = 10 pF, measured between 10% and 90% of signal	SNL variant	0	4.5	8	μs
			SNB variant	0	2	4	μs
Pulse Width, ASIL Warning	$t_{w(ASILwarn)}$	Refer to Figure 7		63	–	121	μs
Pulse Width, ASIL Critical	$t_{w(ASILcrit)}$	Refer to Figure 7		4	–	8	ms

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OPERATING CHARACTERISTICS (continued): Valid throughout full operating temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
INTERMEDIATE PULSE WIDTH OPTION (PART NUMBER -xxIxxxx)						
Threshold to Enter High-Speed Mode	f_{HIGH}	T_{CYCLE} frequency increasing	0.935	1.1	1.265	kHz
Threshold to Exit High-Speed Mode	f_{LOW}	T_{CYCLE} frequency decreasing	0.85	1	1.15	kHz
Pulse Width, Forward Rotation	$t_{w(FWD)}$	T_{CYCLE} frequency < f_{LOW}	51	60	69	μs
Pulse Width, Reverse Rotation	$t_{w(REV)}$	T_{CYCLE} frequency < f_{LOW}	102	120	138	μs
Pulse Width, High-Speed	$t_{w(HS)}$	T_{CYCLE} frequency > f_{HIGH}	25	30	35	μs
Pulse Width, Non-Direction	$t_{w(ND)}$		25	30	35	μs
Operating Frequency, Forward Rotation [6][7][8]	f_{FWD}		0	–	12	kHz
Operating Frequency, Reverse Rotation [6][7][8]	f_{REV}		0	–	12	kHz
Operating Frequency, Non-Direction Pulses [6][8]	f_{ND}		0	–	12	kHz
NARROW PULSE WIDTH OPTION (PART NUMBER -xxNxxxx)						
Pulse Width, Forward Rotation	$t_{w(FWD)}$		38	45	52	μs
Pulse Width, Reverse Rotation	$t_{w(REV)}$		76	90	104	μs
Pulse Width, Non-Direction	$t_{w(ND)}$		153	180	207	μs
Operating Frequency, Forward Rotation [6][8]	f_{FWD}		0	–	12	kHz
Operating Frequency, Reverse Rotation [6][8]	f_{REV}		0	–	7	kHz
Operating Frequency, Non-Direction Pulses [6][8]	f_{ND}		0	–	4	kHz
WIDE PULSE WIDTH OPTION (PART NUMBER -xxWxxxx)						
Pulse Width, Forward Rotation	$t_{w(FWD)}$		38	45	52	μs
Pulse Width, Reverse Rotation	$t_{w(REV)}$		153	180	207	μs
Pulse Width, Non-Direction	$t_{w(ND)}$		306	360	414	μs
Operating Frequency, Forward Rotation [6][8]	f_{FWD}		0	–	12	kHz
Operating Frequency, Reverse Rotation [6][8]	f_{REV}		0	–	4	kHz
Operating Frequency, Non-Direction Pulses [6][8]	f_{ND}		0	–	2.2	kHz

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OPERATING CHARACTERISTICS (continued): Valid throughout full operating temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
INPUT CHARACTERISTICS AND PERFORMANCE						
Air Gap Range		Using Allegro 60-0 reference target; tested at 1000 rpm [9]	0.5	–	2.8	mm
User-Induced Offset		Differential Magnitude valid for both differential magnetic channels.	–400	–	400	G
Operate Point	B_{OP}	% of peak-to-peak IC-processed signal	–	70	–	%
Release Point	B_{RP}	% of peak-to-peak IC-processed signal	–	30	–	%
Switch Point Separation	$B_{DIFF(SP-SEP)}$	Required amount of amplitude separation between channels at each B_{OP} and B_{RP} occurrence; refer to Figure 4	20	–	–	$\%B_{DIFF(pk-pk)}$
Allowable Differential Sequential Signal Variation	$B_{SEQ(n+1)}$ / $B_{SEQ(n)}$	Signal cycle-to-cycle variation (refer to Figure 2)	0.7	–	1.3	–
	$B_{SEQ(n+i)}$ / $B_{SEQ(n)}$	Overall signal variation (refer to Figure 2)	0.1	–	–	–
Initial Calibration	T_{CAL}	Periods after t_{PO} completed and first valid speed and direction output. Constant direction of rotation. Refer to Figure 3 for definition of T_{CYCLE}.	–	–	4 × T_{CYCLE}	–
Vibration Immunity (Startup)		High Vibration (-xxxHxxxx variant)	1 × T_{CYCLE}	–	–	–
		Low Vibration (-xxxLxxxx variant)	1 × T_{CYCLE}	–	–	–
Vibration Immunity (Running Mode)		High Vibration (-xxxHxxxx variant)	1 × T_{CYCLE}	–	–	–
		Low Vibration (-xxxLxxxx variant)	0.12 × T_{CYCLE}	–	–	–
Timer Period		Timed reset intervals with no output pulses (-xxxxxxxK variant)	–	0.5	–	s
THERMAL CHARACTERISTICS						
Package Thermal Resistance [10]	$R_{\theta JA}$	Single-layer PCB with copper limited to solder pads	–	150	–	°C/W

[1] Typical values are at T_A = 25°C and V_{CC} = 12 V. Performance may vary for individual units, within the specified maximum and minimum limits.
[2] Maximum voltage must be adjusted for power dissipation and junction temperature; see representative for Power Derating discussions.
[3] Negative current is defined as conventional current coming out of (sourced from) the specified device terminal.
[4] Output transients prior to t_{PO} should be ignored.
[5] Timing from start of rising output transition. Measured pulse width will vary on load circuit configurations and thresholds. Pulse width measured at threshold of ($I_{CC(HIGH)}$ + $I_{CC(LOW)}$) / 2 for non-ASIL pulses and (I_{RESET} + $I_{CC(LOW)}$) / 2 for ASIL pulses.
[6] Maximum Operating Frequency is determined by satisfactory separation of output pulses. If shorter low-state durations can be resolved, the maximum f_{REV} and f_{ND} may be higher. Does not appy to -xxIxxxx variant or f_{FWD}.
[7] Direction information is not available when frequency > f_{HIGH} for the Intermediate Pulse Width option.
[8] Zero-speed is not met when the xxxxxxK-variant is implemented due to the inclusion of a timed reset.
[9] Speed-related effects on maximum air gap are highly dependent upon specific target geometry. Consult with Allegro field applications engineering for aid with assessment of target geometries.
[10] Additional thermal information is available on the Allegro website.

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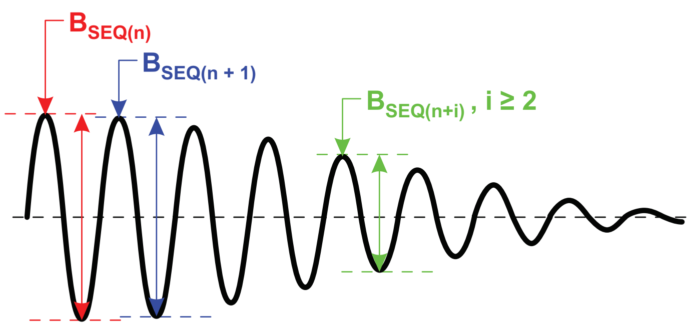
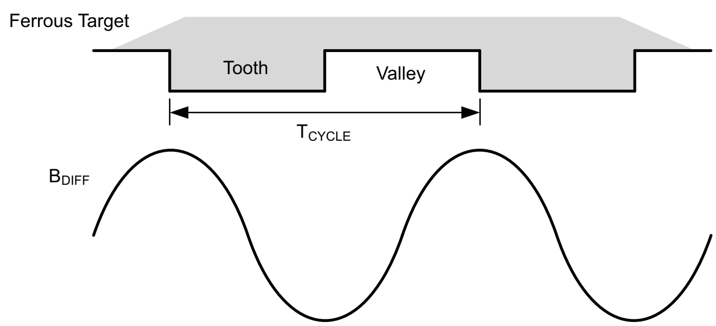


Figure 2: Differential Signal Variation



T_{CYCLE} = Target Cycle; the amount of rotation that moves one tooth and valley across the sensor.

B_{DIFF} = The differential magnetic flux density sensed by the sensor.

Figure 3: Definition of T_{CYCLE}

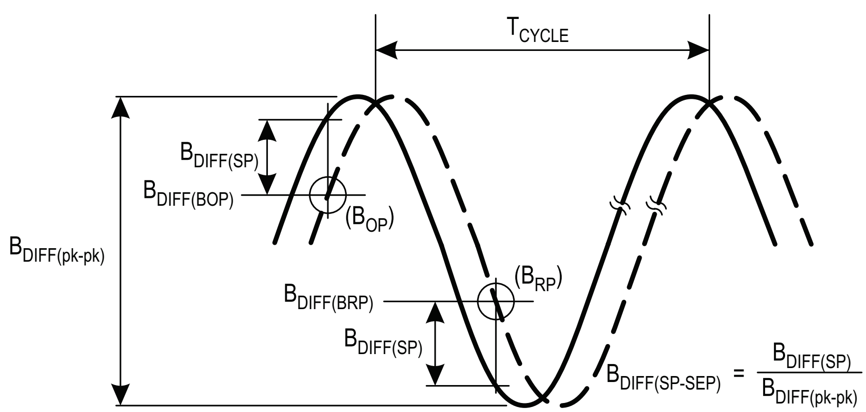


Figure 4: Definition of Switch Point Separation

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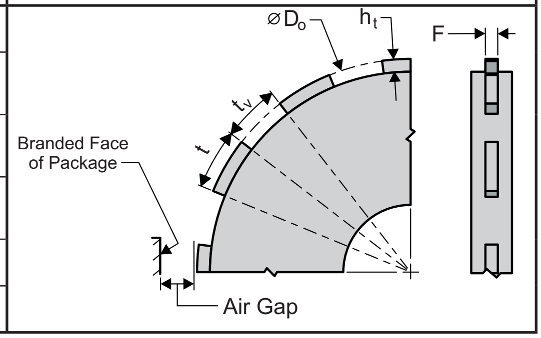
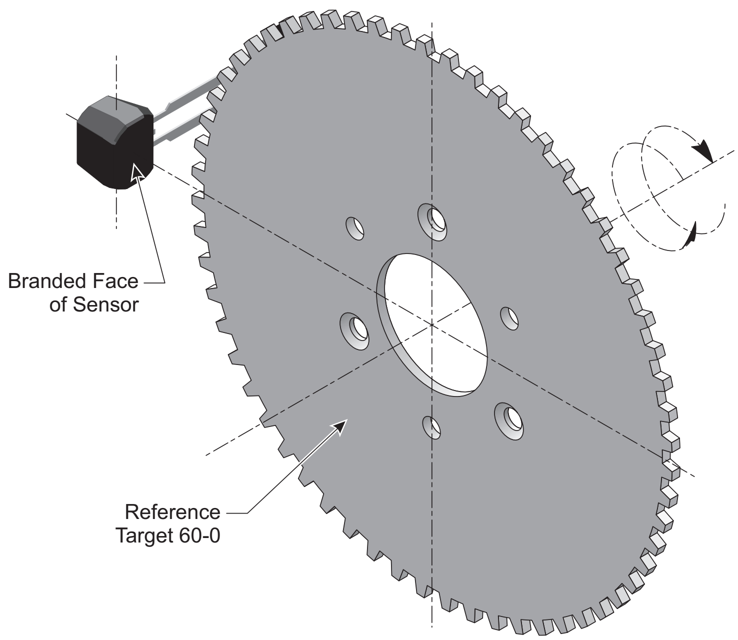
Reference Target 60-0 (60 Tooth Target)

Characteristics	Symbol	Test Conditions	Typ.	Units	Symbol Key
Outside Diameter	D_o	Outside diameter of target	120	mm	
Face Width	F	Breadth of tooth, with respect to branded face	6	mm	
Circular Tooth Length	t	Length of tooth, with respect to branded face	3	deg.	
Circular Valley Width	t_v	Length of valley, with respect to branded face	3	deg.	
Tooth Whole Depth	h_t		3	mm	
Material		Low Carbon Steel	–	–	



FUNCTIONAL DESCRIPTION

Sensing Technology

The sensor IC contains a single-chip Hall-effect circuit that supports a trio of Hall elements. These are used in differential pairs to provide electrical signals containing information regarding edge position and direction of target rotation. The ATS19520 is intended for use with ferrous targets.

After proper power is applied to the sensor IC, it is capable of providing digital information that is representative of the magnetic features of a rotating target. The waveform diagrams in Figure 5 present the automatic translation of the target profiles, through their induced magnetic profiles, to the digital output signal of the sensor IC.

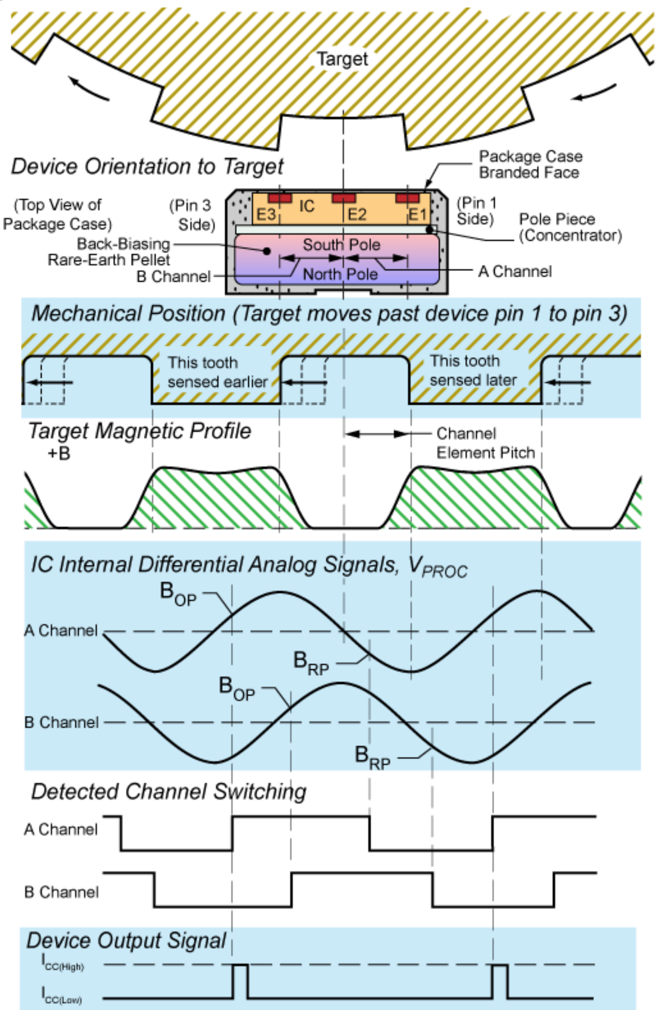


Figure 5: Magnetic Profile

The magnetic profile reflects the features of the target, allowing the sensor IC to present an accurate digital output.

Direction Detection

The sensor IC compares the relative phase of its two differential channels to determine which direction the target is moving. The relative switching order is used to determine the direction, which is communicated through the output protocol.

Data Protocol Description

When a target passes in front of the device (opposite the branded face of the package case), the ATS19520 generates an output pulse for each tooth of the target. Speed information is provided by the output pulse rate, while direction of target rotation is provided by the duration of the output pulses. The sensor IC can sense target movement in both the forward and reverse directions.

FORWARD ROTATION

As shown in panel A in Figure 6, when the target is rotating such that a tooth near the sensor IC – of -Fxxxxxx variant – passes from pin 1 to pin 3, this is referred to as forward rotation. This direction is opposite for the -Rxxxxxx variant. Forward rotation is indicated by output pulse widths of $t_{w(FWD)}$.

REVERSE ROTATION

As shown in panel B in Figure 6, when the target is rotating such that a tooth passes from pin 3 to pin 1, it is referred to as reverse rotation for the -Fxxxxxx variant. Reverse rotation is indicated by output pulse widths of $t_{w(REV)}$.

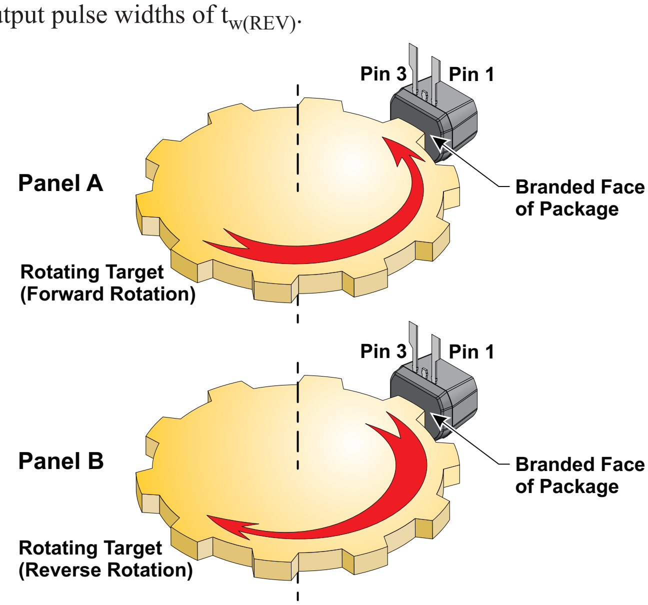


Figure 6: Target Rotation (F Variant Shown)

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ASIL Protocol

The -xxxxxxx-A variant contains diagnostic circuitry that will continuously monitor occurrences of failure defects within the IC. Refer to Figure 7 for the output protocol of the ASIL Safe State after an internal defect has been detected. Error Protocol will result from faults which cause incorrect signal transmission (i.e., too few or too many output pulses).

Note: If a fault exists continuously, the device will attempt recovery indefinitely. Refer to the ATS19520 Safety Manual for additional details on the ASIL Safe State Output Protocol.

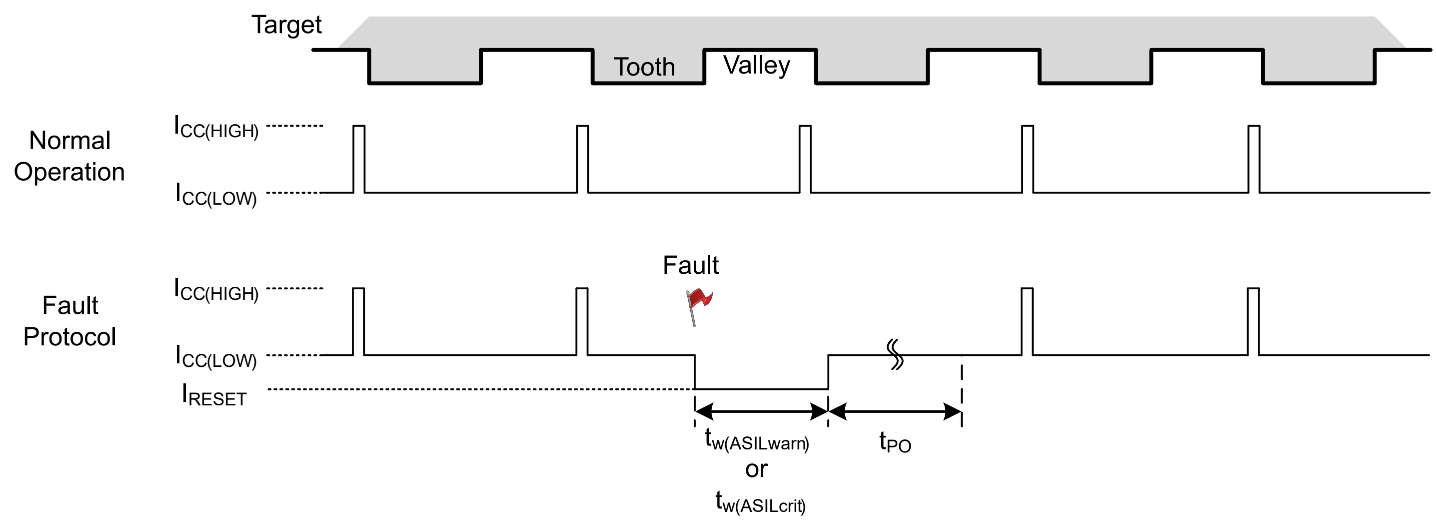


Figure 7: Output Protocol (ASIL Safe State)

POWER DERATING

The device must be operated below the maximum junction temperature of the device ($T_{J(max)}$). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro website.)

The Package Thermal Resistance ($R_{\theta JA}$) is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity (K) of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case ($R_{\theta JC}$) is relatively small component of $R_{\theta JA}$. Ambient air temperature (T_A) and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 14 mA, and $R_{\theta JA}$ = 150°C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 14\ mA = 168\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 168\ mW \times 150°C/W = 25.2°C$$

$$T_J = T_A + \Delta T = 25°C + 25.2°C = 50.2°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)}$, $I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A

Example: Reliability for V_{CC} at T_A=150°C, package SN, using a single-layer PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$ =150°C/W, $T_{J(max)}$ =165°C, $V_{CC(max)}$ = 24 V, and $I_{CC(avg)}$ = 14.6 mA. $I_{CC(avg)}$ is computed using $I_{CC(LOW)(max)}$ and $I_{CC(HIGH)(max)}$, with a duty cycle of 83% computed from $t_{w(REV)(max)}$ on-time at 4 kHz maximum operating frequency.

Calculate the maximum allowable power level, $P_{D(max)}$. First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

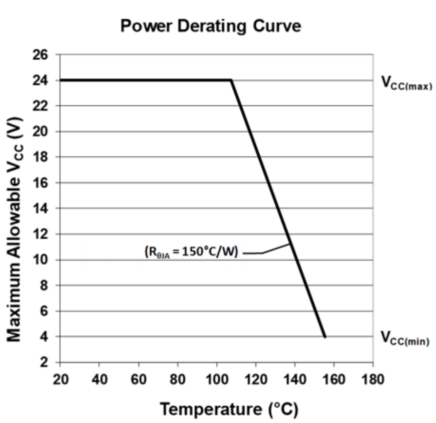
$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 150°C/W = 100\ mW$$

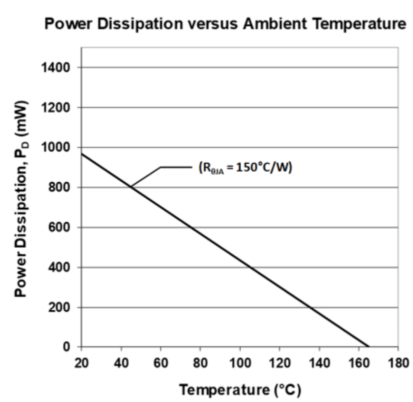
Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(avg)} = 100\ mW \div 14.6\ mA = 6.8\ V$$

The result indicates that, at T_A, the application and device cannot dissipate adequate amounts of heat at operating voltages above 6.8 V at 150°C.

Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \leq V_{CC(max)}$, then reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these conditions.





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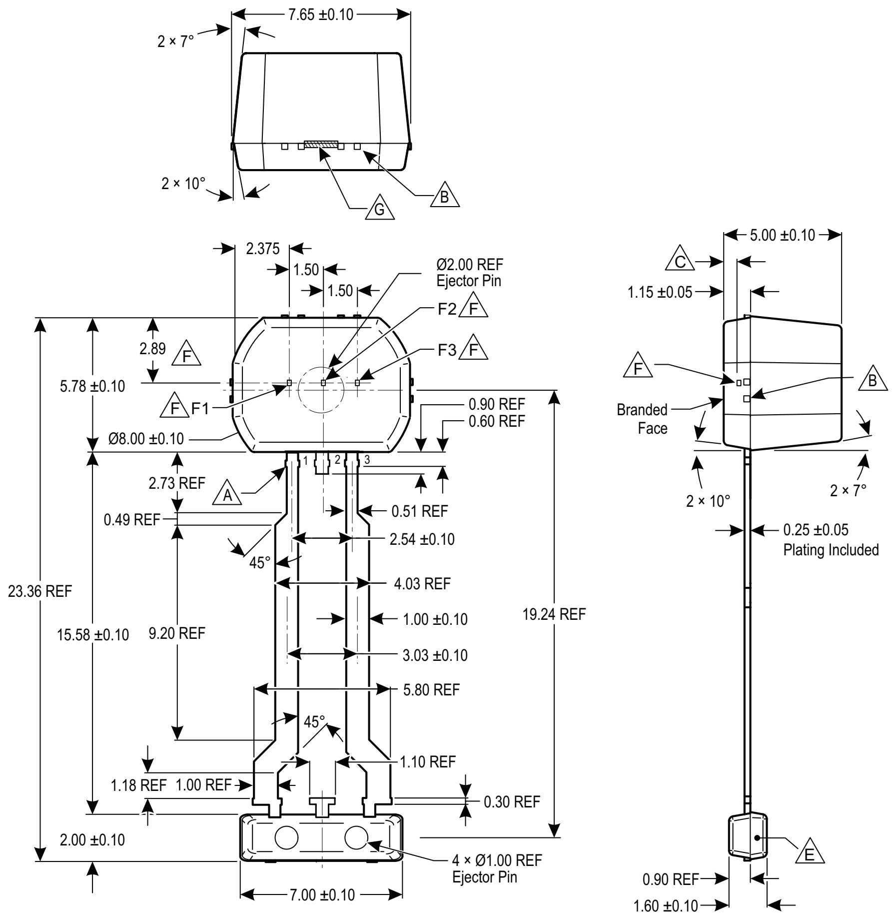
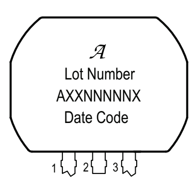
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-0000429, Rev. 4)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown





D Standard Branding Reference View

Lines 1, 2, 3, 4: Up to 10 characters, centered

Line 1: Logo A
Line 2: Characters 5, 6, 7, 8, 9, 10, 11 of Assembly Lot Number
Line 3: 3 Character Prefix, 5 Digit Part Number, Package Variant
Line 4: 4 digit Date Code

Notes:

- A Dambar removal protrusion (12×)
- B Tie bars (8×)
- C Active Area Depth, 0.40 ±0.05 mm
- D Branding scale and appearance at supplier discretion
- E Molded lead bar for preventing damage to leads during shipment
- F Hall elements (F1, F2, F3); not to scale
- G Gate location

Figure 8: Package SN, 3-Pin SIP

Revision History

Number	Date	Description
–	January 31, 2019	Initial release
1	March 29, 2019	Updated Features and Benefits (page 1), selection guide (page 2), and ASIL Protocol section (page 10).
2	April 5, 2019	Updated ASIL status (page 1) and figure references (page 4).

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