190314496 Updated Errata for CP2114

Bulletin Issue Date: 3/14/2019   **Effective Date:**   3/14/2019

Description of Change

Silicon Labs is releasing updated Errata v0.2 for the CP2114.

The following errata items have been added and are active:
CP2114_E113 - Configuration write files when SYSCLK is driven by the internal 49.152 MHz oscillator
CP2114_E114 - Left-justified ADC data is incorrect for signals greater than -6 dBFS
CP2114_E115 - Failure to switch back to using external clock after resuming from USB suspend mode

The following errata have been resolved:
CP2114_E101 - Dropouts in asynchronous-mode playback audio on 64-bit systems
CP2114_E102 - Record sample values intermittently corrupted
CP2114_E103 - Playback mute-by-zero can cause record corruption
CP2114_E104 - USB descriptor not correct for synchronous mode
CP2114_E105 - Resume may fail on externally-clocked systems
CP2114_E106 - UART is unusable if GPIO.9 is reconfigured
CP2114_E107 - Record can fail after rebooting PC
CP2114_E108 - UART can deliver duplicated RX character
CP2114_E109 - Failure to enumerate with unprogrammed configuration when external clock is missing
CP2114_E110 - Host PC record mute icon controls CP2114 playback muting
CP2114_E111 - GPIO and suspend
CP2114_E112 - Right-channel ADC data lags by one sample

Reason for Change

Added and updated errata items

Product Identification

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Existing Part #
CP2114-B01-GM
CP2114-B01-GMR
CP2114-B02-GM
CP2114-B02-GMR
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This change is considered a minor change which does not affect form, fit, function, quality, or reliability. The information is being provided as a customer courtesy.

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Customer Actions Needed:

None.

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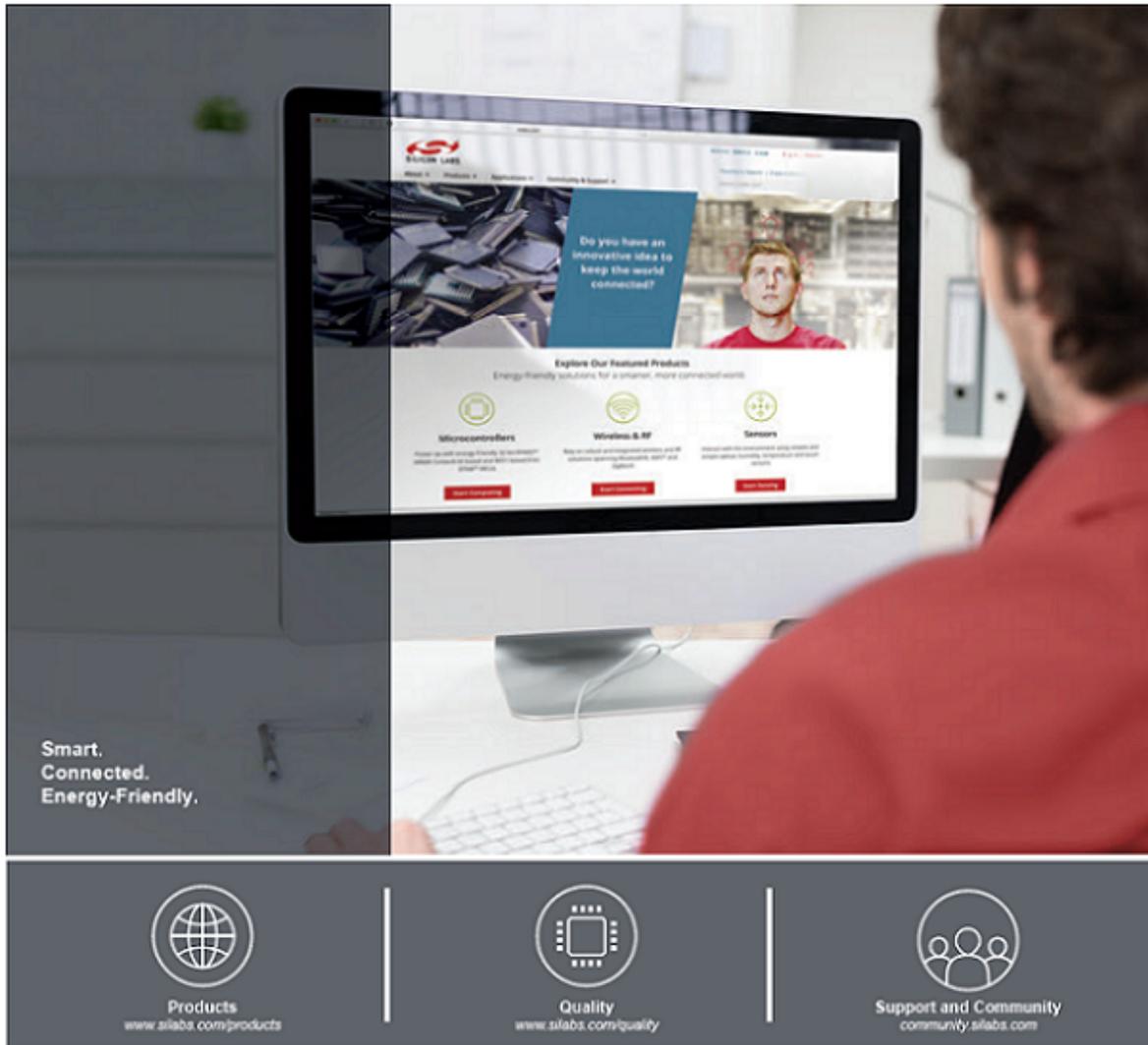
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