MDE029A128296RBW	128 x 296	3-Wire SPI Interface	E-Ink Module

Specification		
Version: 1	Date: 12/02/2019	
Revision		
1	11/02/2019	First Issue.

Display Features	
Display Size	2.9"
Resolution	128 x 296
Orientation	Portrait
Appearance	Black, White, Red
Logic Voltage	3.3V
Interface	SPI
Touchscreen	N/A
Module Size	91.00 x 77.00 x 1.25 mm
Operating Temperature	0°C ~ +30°C
Pinout	24 - Way FFC
Pitch	0.5mm

RoHS compliant

	Box Quantity	Weight / Display
Pinout	---	---
Pitch		

* - For full design functionality, please use this specification in conjunction with the SSD1619A specification.(Provided Separately)

Display Accessories	
Part Number	**Description**

Optional Variants	
Appearances	**Voltage**

Overview

MDE029A128296RBW is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The display is capable to display image at 1-bit white,black and red full display capabilities. The 2.9inch active area contains 296×128 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.
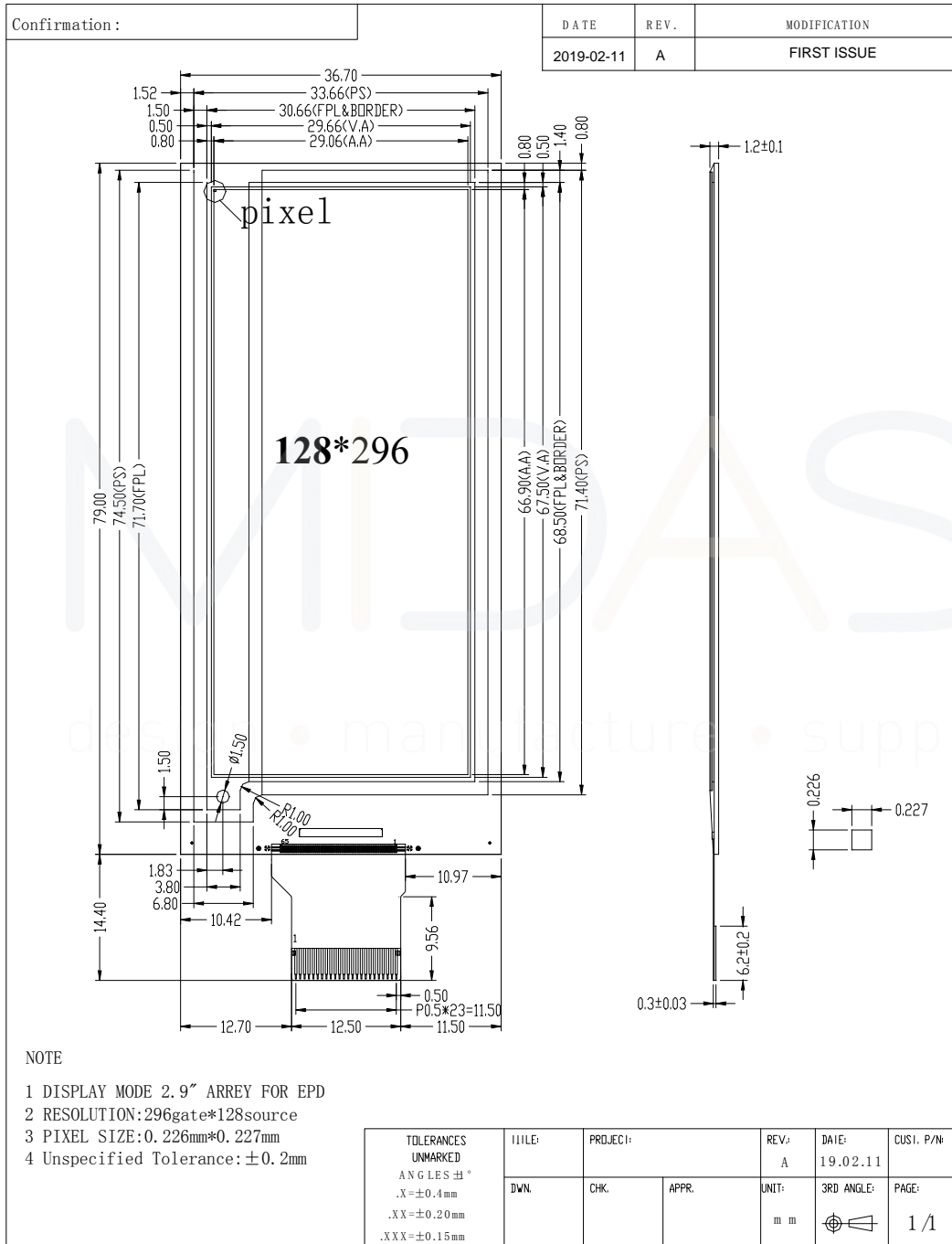
Features

◆296×128 pixels display

◆High contrast High reflectance

◆Ultra wide viewing angle Ultra low power consumption

◆Pure reflective mode

◆Bi-stable display

◆Commercial temperature range

◆Landscape portrait modes

◆Hard-coat antiglare display surface

◆Ultra Low current deep sleep mode

◆On chip display RAM

◆Waveform can stored in On-chip OTP or written by MCU

◆Serial peripheral interface available

◆On-chip oscillator

◆On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage

◆I^2C signal master interface to read external temperature sensor

◆Built-in temperature sensor

◆Support partial update mode

Mechanical Specification

Parameter	Specifications	Unit	Remark
Screen Size	2.9	Inch	
Display Resolution	128(H)×296(V)	Pixel	DPI:112
Active Area	29.06×66.90	mm	
Pixel Pitch	0.227×0.226	mm	
Pixel Configuration	Rectangle		
Outline Dimension	36.7(H)×79.0 (V) ×1.20(D)	mm	
Weight	5.5±0.5	g	

Confirmation:

DATE	REV.	MODIFICATION
2019-02-11	A	FIRST ISSUE

36.70
33.66(PS)
1.52
1.50
30.66(FPL&BORDER)
0.50
29.66(V.A)
0.80
29.06(A.A)

0.80
0.50
1.40
0.80

1.2±0.1

pixel

128*296

66.90(A.A)
67.50(V.A)
68.50(FPL&BORDER)
71.40(PS)

79.00(PS)
74.50(PS)
71.70(FPL)

0.226

0.227

1.50
Ø1.50

R1.00
R1.00

1.83
3.80
6.80
10.42

10.97

9.56

14.40

6.2±0.2

0.3±0.03

0.50
P0.5*23=11.50

12.70
12.50
11.50

NOTE

1 DISPLAY MODE 2.9″ ARREY FOR EPD
2 RESOLUTION:296gate*128source
3 PIXEL SIZE:0.226mm*0.227mm
4 Unspecified Tolerance:±0.2mm

TOLERANCES UNMARKED ANGLES±° .X=±0.4mm .XX=±0.20mm .XXX=±0.15mm	TITLE:	PROJECT:		REV.: A	DATE: 19.02.11	CUST. P/N:
	DWN.	CHK.	APPR.	UNIT: m m	3RD ANGLE:	PAGE: 1/1

Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage(Red)	
6	TSCL	O	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I2C Interface to digital temperature sensor Data pin	
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	Keep Open
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, /O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU.   The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode.   When the pin is pulled HIGH, the data at SDA will be interpreted as data.   When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin.   When Busy is High, the operation of chip should not be interrupted, command should not be sent.   The chip would put Busy pin High when -Outputting display waveform -Communicating with digital temperature sensor

Note 5-5: Bus interface selection pin

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

Electrical Characteristics

1. Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI	-0.5 to +4.0	V
Logic Input voltage	VIN	-0.5 to VCI +0.5	V
Logic Output voltage	VOUT	-0.5 to VCI +0.5	V
Operating Temp range	TOPR	10 to +40	℃.
Storage Temp range	TSTG	-25 to+40	℃.
Operating Temp range Max	TOPRm	0 to +40	℃.
Optimal Storage Temp	TSTGo	23±2	℃.
Optimal StorageHumidity	HSTGo	55±10	%RH

Note:

   1.Maximum ratings are those values beyond which damages to the device may occur.   Functional operation should be restricted to the limits in the Panel DC Characteristics tables.
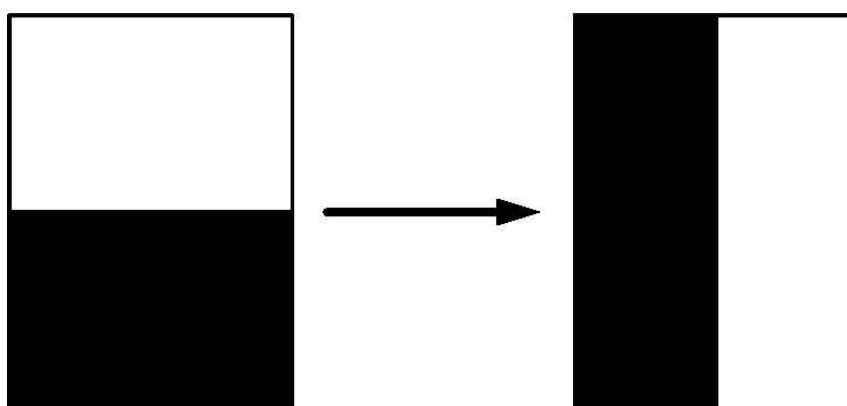
2. Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	V_{SS}	-		-	0	-	V
Logic supply voltage	V_{CI}	-	VCI	2.2	3.0	3.7	V
Core logic voltage	V_{DD}		VDD	1.7	1.8	1.9	V
High level input voltage	V_{IH}	-	-	0.8 V_{CI}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2 V_{CI}	V
High level output voltage	V_{OH}	IOH = -100uA	-	0.9 V_{CI}	-	-	V
Low level output voltage	V_{OL}	IOL = 100uA	-	-	-	0.1 V_{CI}	V
Typical power	P_{TYP}	V_{CI} =3.0V	-	-	12.9	-	mW
Deep sleep mode	P_{STPY}	V_{CI} =3.0V	-	-	0.003	-	mW
Typical operating current	Iopr_VCI	V_{CI} =3.0V	-	-	4.3	-	mA
Image update time	-	23 ºC	-	-	12	-	sec
Sleep mode current	Islp_V_{CI}	DC/DC off No clock No input load Ram data retain	-	-	20	-	uA
Deep sleep mode current	Idslp_V_{CI}	DC/DC off No clock No input load Ram data not retain	-	-	1	5	uA

Notes: 1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.

2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Midas.

3. Panel DC Characteristics(Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCOM output voltage	VCOM	-	VCOM	-	TBD	-	V
Positive Source output voltage	V_{SH}	-	$S_0{\sim}S_{127}$	+14.5	+15	+15.5	V
Negative Source output voltage	V_{SL}	-	$S_0{\sim}S_{127}$	-15.5	-15	-14.5	V
Positive gate output voltage	Vgh	-	$G_0{\sim}G_{295}$	+21	+22	+23	V
Negative gate output voltage	Vgl	-	$G_0{\sim}G_{295}$	-21	-20	-19	V

4. Panel AC Characteristics

4.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-4-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDA	SCL	CS#	L	RES#

4.2 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#.   This interface supports Write mode and Read mode.

Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

In the write mode SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte . The data byte in the shift register is written to the Graphic Display Data RAM /Data Byte register or command Byte register according to D/C# pin.
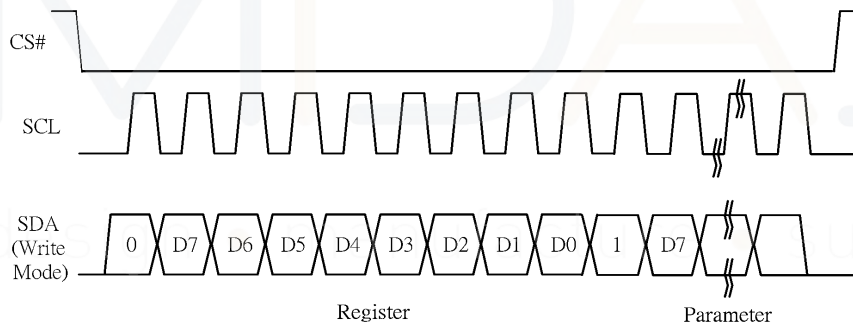
Figure 6-1: Write procedure in 4-wire SPI mode
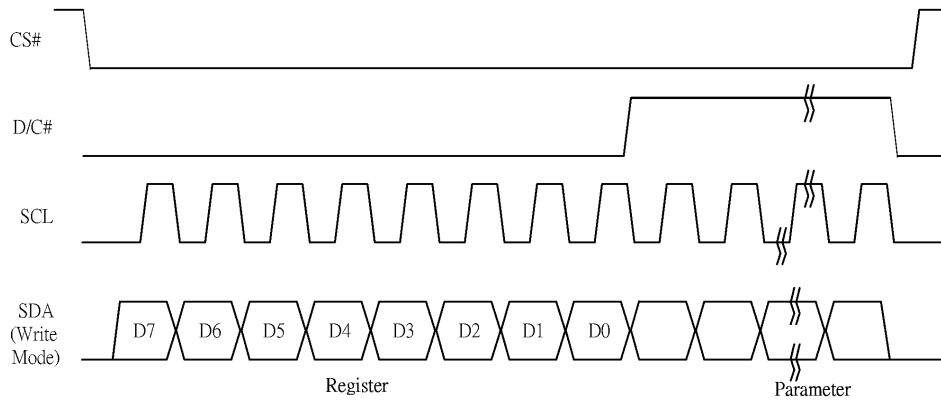
In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.

2. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0 with D/C# keep low.

3. After SCL change to low for the last bit of register, D/C# need to drive to high.

4. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, … D0.

5. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

Figure 6-2: Read procedure in 4-wire SPI mode
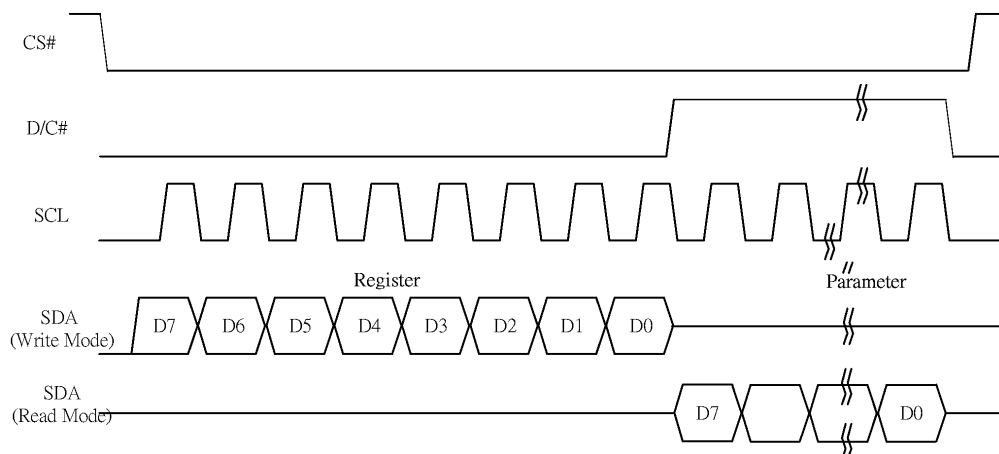
4.3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCL, serial data SDA and CS#. This interface also supports Write mode and Read mode.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

Function	CS#	D/C#	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

Note：↑ stands for rising edge of signal

Figure 6-3: Write procedure in 3-wire SPI mode

In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. D/C=0 is shifted thru SDA with one rising edge of SCL
3. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0.
4. D/C=1 is shifted thru SDA with one rising edge of SCL
5. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, … D0.
6. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

Figure 6-4: Read procedure in 3-wire SPI mode
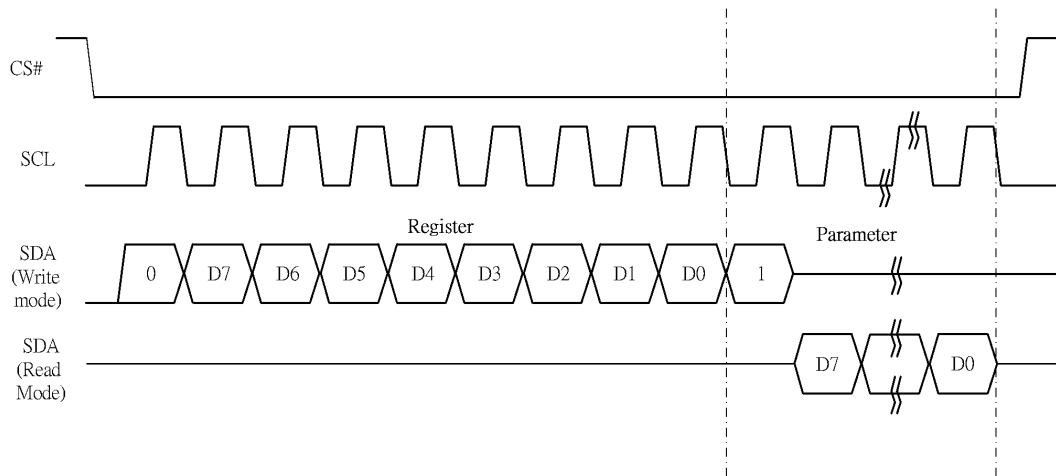
4.4 Interface Timing

The following specifications apply for: VSS=0V, VCI=3.0V, T_{OPR} =23ºC.
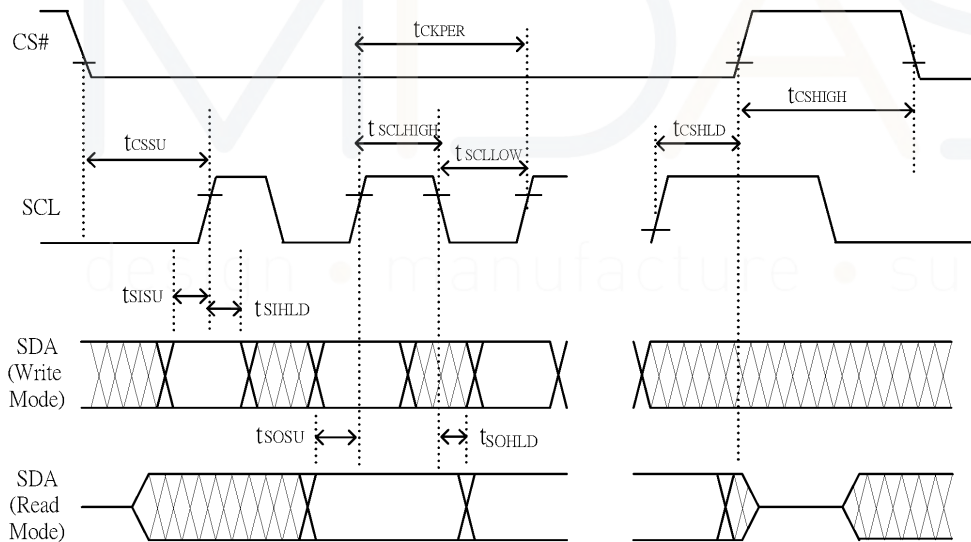
Changed Diagram

Serial Interface Timing Characteristics

(VCI - VSS = 2.2V to 3.7V, TOPR = 23°C, CL=20pF)

Write mode

Symbol	Parameter	Min	Typ.	Max	Unit
fSCL	SCL frequency (Write Mode)			20	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	20			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	20			ns
tCSHIGH	Time CS# has to remain high between two transfers	100			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	25			ns
tSCLLOW	Part of the clock period where SCL has to remain low	25			ns
tSISU	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
tSIHLD	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ.	Max	Unit
fSCL	SCL frequency (Read Mode)			2.5	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	100			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	50			ns
tCSHIGH	Time CS# has to remain high between two transfers	250			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	180			ns
tSCLLOW	Part of the clock period where SCL has to remain low	180			ns
tSOSU	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
tSOHLD	Time SO (SDA Read Mode) will remain stable after the rising edge of SCL		70		ns

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting
0	1		A7	A6	A5	A4	A3	A2	A1	A0		Set A[8:0]=0127h
0	1		0	0	0	0	0	0	0	A8		Set B[8:0]=00h
0	1		0	0	0	0	0	B2	B1	B0		
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage control	SetGate Driving voltage
0	1		0	0	0	A4	A3	A2	A1	A0		A[4:0]=17h[POR],VGH at 20V[POR] VGH setting from 10V to 21V
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage control	SetSource Driving voltage
0	1		A7	A6	A5	A4	A3	A2	A1	A0		A[7:0]= 41h[POR],VSH1 at 15V
0	1		B7	B6	B5	B4	B3	B2	B1	B0		B[7:0]=A Ch[POR],VSH2 at 5.4V
0	1		C7	C6	C5	C4	C3	C2	C1	C0		C[7:0]= 32h[POR], VSL at -15V
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control
0	1		0	0	0	0	0	0	0	A0		A[0] : / Description 0 / Normal Mode [POR] 1 / Enter Deep Sleep Mode
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence
0	1		0	0	0	0	0	A_2	A_1	A_0		A [1:0] = ID[1:0]Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	0	12	0	0	0	1	0	0	1	0	SWRESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode Note: RAM are unaffected by this command.
0	0	18	0	0	0	1	1	0	0	0	Temperature Sensor Control	Temperature Sensor Selection A[7:0]= 48h [POR] external temperature

			A7	A6	A5	A4	A3	A2	A1	A0		
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[7:0] – MSByte 01111111[POR] B[7:0] – LSByte 11110000[POR]
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		B7	B6	B5	B4	0	0	0	0		
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence. The Display Update Sequence Option is located at R22h. User should not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	RAM content option for Display Update BW RAM option A[7:4]=0100 (For BW) A[3:0]=0000[POR] Normal A[3:0]=0100 Bypass RAM content as 0 A[3:0]=0100 Inverse RAM content
0	1		0	0	0	0	A3	A2	A1	A0		
0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation
	1		A7	A6	A5	A4	A3	A2	A1	A0		

Display Update Control 2 description:

Setting for LUT from MCU	
Enable Clock Signal, Then Enable Analog Then PATTERN DISPLAY Then Disable Analog Then Disable OSC	C7
Setting for LUT from OTP according to external Temperature Sensor operation	
Then Enable Analog Then Load LUT	90
Enable Analog Then PATTERN DISPLAY Then Disable Analog Then Disable OSC	47

0	0	24	0	0	1	0	0	1	0	0	Write RAM (BW)	After this command, data entries will be written into the 1RAM until another command is written. Address pointers will advance accordingly. For Write pixel: Content of write RAM(BW)=1 For Black pixel: Content of write RAM(BW)=0
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED)	After this command, data entries will be written into the 2 RAM until another command is written. Address pointers will advance accordingly. For RED pixel: Content of write RAM(RED)=1 For White/Black pixel: Content of write RAM(RED)=0
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Set A[7:0]=2Fh
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read	Read Register stored in OTP: 1. A[7:0]~ B[7:0]: VCOM Information 3. C[7:0]~F[7:0]: Reserved 4. G[7:0]~H[7:0]: Module ID/ Waveform Version [2bytes]
1	1		A7	A6	A5	A4	A3	A2	A1	A0		
1	1		B7	B6	B5	B4	B3	B2	B1	B0		
1	1		C7	C6	C5	C4	C3	C2	C1	C0		
1	1		D7	D6	D5	D4	D3	D2	D1	D0		
1	1		E7	E6	E5	E4	E3	E2	E1	E0		
1	1		F7	F6	F5	F4	F3	F2	F1	F0		
1	1		G7	G6	G5	G4	G3	G2	G1	G0		
1	1		H7	H6	H5	H4	H3	H2	H1	H0		
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	Read IC status Bit [POR 0x21] A[5]: HV Ready Detection flag [POR=1] 0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01] Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively.
1	1		0	0	A5	A4	0	0	A1	A0		

0	0	32	0	0	1	1	0	0	1	0	WriteLUT register	Write LUT register from MCU interface [70 bytes].
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		:	:	:	:	:	:	:	:		
0	1		:	:	:	:	:	:	:	:		
0	1		:	:	:	:	:	:	:	:		
0	1		:	:	:	:	:	:	:	:		
0	0	3A	0	0	1	1	1	0	1	0	Set dummy line period	Set A[6:0]=30h
0	1		0	A6	A5	A4	A3	A2	A1	A0		Default value will give 50Hz Frame frequency
0	0	3B	0	0	1	1	1	0	1	1	Set Gate line width	Set A[3:0]=0Ah
0	1		0	0	0	0	A3	A2	A1	A0		Default value will give 50Hz Frame frequency
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	
0	1		A7	A6	A5	A4	0	0	A1	A0		Select border waveform for VBD A [7:6] Select VBD

A[7:6]	Select VBD as
00[POR]	GS Transition Define A[1:0]
01	Fix Level Define A [5:4]
10	VCOM
11	HIZ

A [5:4] Fix Level Setting for VBD

A[5:4]	VBD level
00[POR]	VSS
01	VSH1
10	VSL
11	VSH2

A[1:0]) BW Transition setting for VBD

A[1:0]	VBD Transition
00 [POR]	LUT0
01	LUT1
10	LUT2
11	LUT3

0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit A[4:0]: XSA[4:0], X Start, POR = 00h B[4:0]: XEA[4:0], X End, POR = 0Fh
0	1		0	0	0	A4	A3	A2	A1	A0		
0	1		0	0	0	B4	B3	B2	B1	B0		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y-address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit A[8:0]: YSA[8:0], Y Start, POR = 0127h B[8:0]: YEA[8:0], Y End, POR = 0000h
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	0	A8		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		0	0	0	0	0	0	0	B8		
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X	Make initial settings for the RAM X

0	1		0	0	0	A_4	A_3	A_2	A_1	A_0	address counter	address in the address counter (AC) $A[4:0]$: XAD[4:0], POR is 00h
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) $A[8:0]$: YAD8:0], POR is 0127h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	0	74	0	1	1	1	0	1	0	0	Set Analog Block control	$A[7:0] = 54h$
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	7E	0	1	1	1	1	1	1	0	Set Digital Block control	$A[7:0] = 3Bh$
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Optical Specification

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	8-1
CR	Contrast Ratio	indoor	8:1		-		8-2
GN	2Grey Level	-	-	DS+(WS-DS)*n(m-1)			8-3
T update	Image update time	at 23 °C	-	12	-	sec	
Life		Topr		1000000times or 5years			

Notes: 8-1.   Luminance meter: Eye-One Pro Spectrophotometer.

8-2.   CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

8-3   WS: White state, DS: Dark state

Handling, Safety, and Environment Requirements

Warning

The display glass may break when it is dropped or bumped on a hard surface.   Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.   Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged.   Moreover the display is sensitive to static electricity and other rough environmental conditions.

Product specification	This data sheet contains final product specifications.

Reliability Test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=60ºC，RH=40%，240h Test in white pattern
3	High-Temperature Operation	T=40ºC，RH=35%，240h
4	Low-Temperature Operation	0ºC，240h
5	High-Temperature, High-Humidity Operation	T=40ºC，RH=80%，168h
6	High Temperature, High Humidity Storage	T=50ºC，RH=80%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25°C 30min]→[+60 °C 30 min] : 50 cycles Test in white pattern
8	UV exposure Resistance	765W/m² for 168hrs,40 °C Test in white pattern

9	ESD Gun	Air+/-15KV;Contact+/-8KV
		  (Test finished product shell,not display only)
		Air+/-8KV;Contact+/-6KV
		  (Naked EPD display,no including IC and FPC area)
		Air+/-4KV;Contact+/-2KV
		  (Naked EPD display,including IC and FPC area)

Note: Put in normal temperature for 1hour after test finished, display performance is ok.

Block Diagram
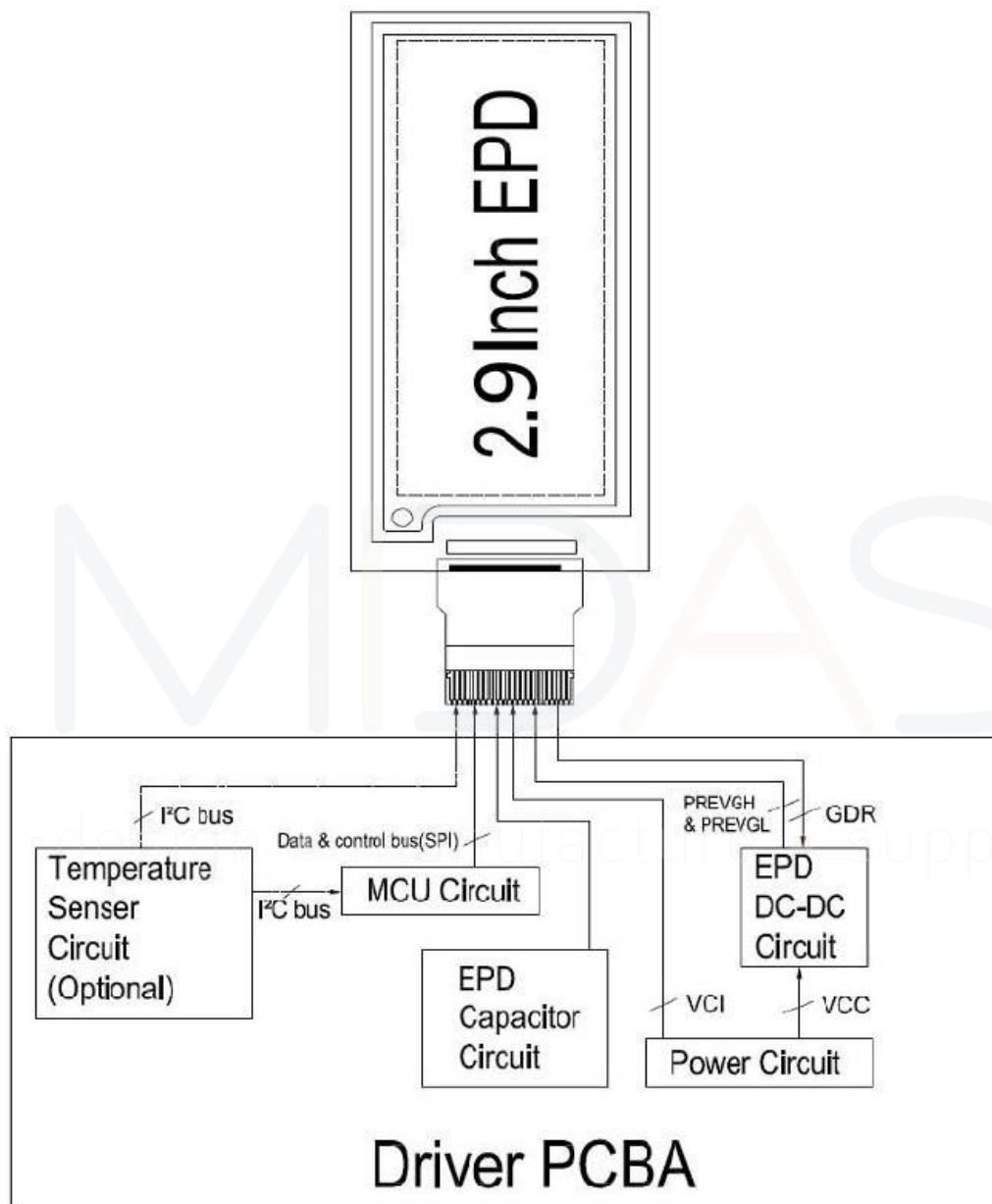
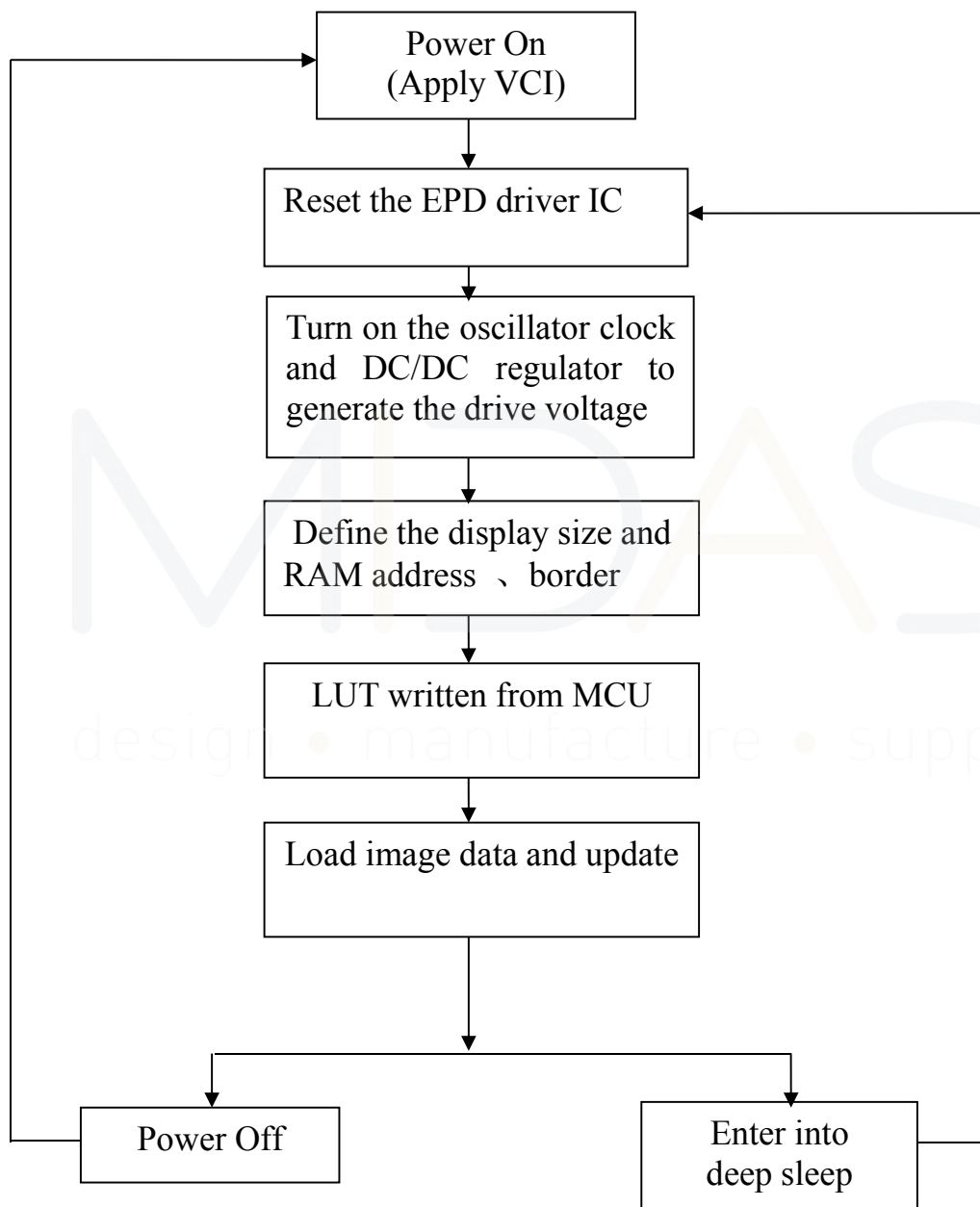# Typical Application Circuit with SPI Interface
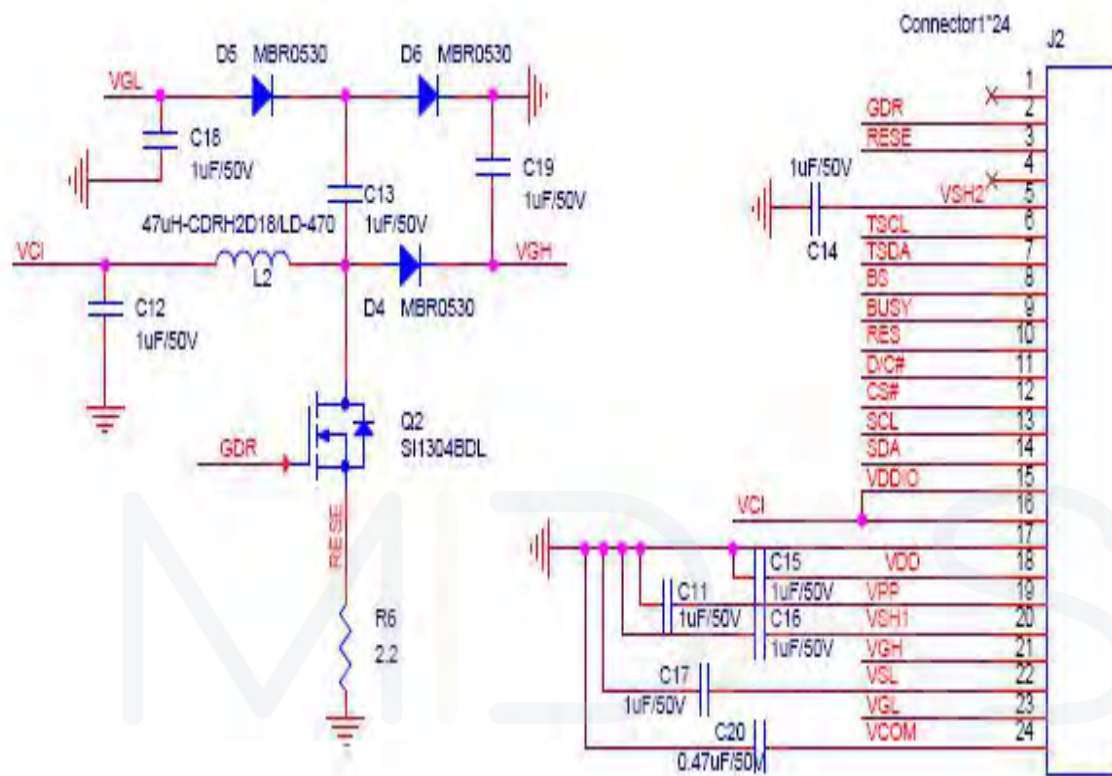
Typical Operating Sequence

1. Normal Operation Flow

```
          Power On
         (Apply VCI)
              |
              v
     Reset the EPD driver IC
              |
              v
   Turn on the oscillator clock
   and DC/DC regulator to
   generate the drive voltage
              |
              v
    Define the display size and
    RAM address 、border
              |
              v
     LUT written from MCU
              |
              v
    Load image data and update
              |
       +------+------+
       |             |
       v             v
   Power Off    Enter into
                deep sleep
```

2. Normal Operation Reference Program Code

| ACTION	VALUE/DATA	COMMENT
POWER ON		
delay	10ms	
PIN CONFIG		
RESE#	high	Hardware reset
delay	200us	
RESE#	low	
delay	200us	
Read busy pin		Wait for busy low
Command 0x12		Software reset
Read busy pin		Wait for busy low
Command 0x74	Data 0x54	Set Analog Block Control
Command 0x7E	Data 0x3B	Set Digital Block Control
Command 0x01	Data 0x27 0x01 0x00	Set display size and driver output control
Command 0x11	Data 0x01	Ram data entry mode
Command 0x44	Data 0x00 0x0F	Set Ram X address
Command 0x45	Data 0x27 0x01 0x00 0x00	Set Ram Y address
Command 0x3C	Data 0x01	Set border
SET VOLTAGE AND LOAD LUT		
Command 0x2C	Data 0x2F	Set VCOM value
Command 0x03	Data 0x17	Gate voltage setting
Command 0x04	Data 0x41 0xAC 0x32	Source voltage setting
Command 0x3A	Data 0x30	Frame setting 50hz
Command 0x3B	Data 0x0A	
Command 0x32	Write 70bytes LUT	Load LUT
LOAD IMAGE AND UPDATE		
Command 0x4E	Data 0x00	Set Ram X address counter
Command 0x4F	Data 0x27 0x01	Set Ram Y address counter
Command 0x24	4736bytes	Load BW image (128/8*296)
Command 0x4E	Data 0x00	Set Ram X address counter
Command 0x4F	Data 0x27 0x01	Set Ram Y address counter
Command 0x26	4736bytes	Load RED image (128/8*296)
Command 0x22	Data 0XC7	Image update
Command 0x20		
Read busy pin		Wait for busy low
Command 0x10	Data 0X01	Enter deep sleep mode
POWER OFF		

Inspection condition

1. Environment
Temperature：　25±3℃
　　　　Humidity：　55±10%RH
2. Illuminance
　　　Brightness:1200～1500LUX;distance:20-30CM;Angle:Relate 30°surround.
3. Inspect method
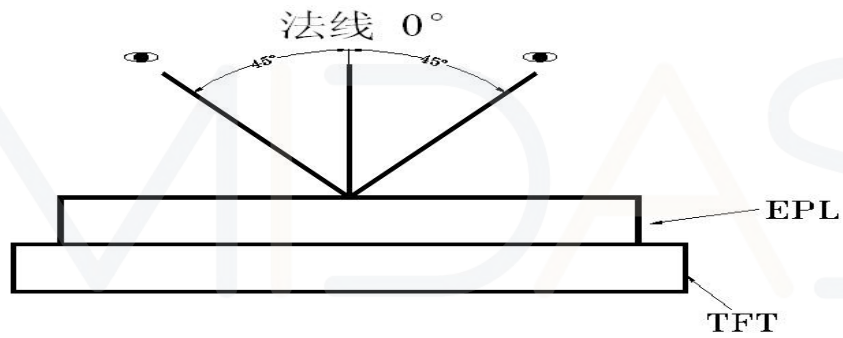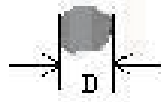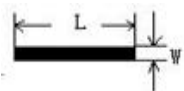
4. Display area
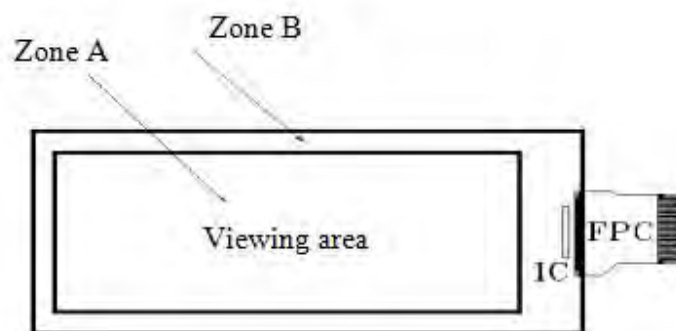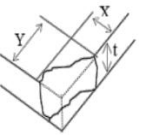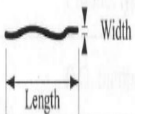
5. Inspection standard

5.1 Electric inspection standard
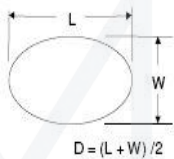
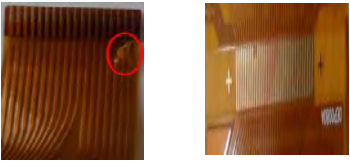| NO.	Item	Standard	Defect level	Method	Scope
1	Display	Display complete Display uniform	MA		
2	Black/White spots	D≤0.25mm，Allowed 0.25mm＜D≤0.4mm。N≤3，and Distance≥5mm 0.4mm＜D　Not Allow	MI	Visual inspection	
3	Black/White spots (No switch)	L≤0.6mm，W≤0.2mm，N≤1 L≤2.0mm,W＞0.2mm，Not Allow L＞0.6mm，Not Allow		Visual/ Inspection card	Zone A
4	Ghost image	Allowed in switching process	MI	Visual inspection	

5	Flash spots/ Larger FPL size	Flash spots in switching, Allowed FPL size larger than viewing area, Allowed	MI	Visual/ Inspection card	Zone A Zone B
6	Display wrong/Missing	All appointed displays are showed correct	MA	Visual inspection	Zone A
6	Short circuit/ Circuit break/ Display abnormal	Not Allow			

5.2 Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	D≤0.25mm，Allowed 0.25mm＜D≤0.4mm，N≤3 D＞0.4mm，Not Allow	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A Zone B
3	Dirty	Allowed if can be removed	MI		Zone A Zone B
4	Chips/Scratch/ Edge crown	X≤3mm,Y≤0.5mm 2mm≤X or 2mm≤Y Allow W≤0.1mm,L≤5mm, n≤ 2 Edge crown：X≤0.3mm，Y≤3mm	MI	Visual / Microscope	Zone A Zone B

5	Substrate color difference	Allowed			
6	FPC broken/ Goldfingers oxidation/ scratch	Not Allow	MA	Visual / Microscope	Zone B
7	PCB damaged/ Poor welding/ Curl	PCB（Circuit area）damaged Not Allow PCB Poor welding Not Allow PCB Curl≤1%			
8	Edge Adhesives height/FPL/ Edge adhesives bubble	Edge Adhesives height ≤ Display surface Edge adhesives seep in≤1/2 Margin width FPL tolerance ±0.3mm Edge adhesives bubble：bubble Width ≤1/2 Margin width；Length ≤0.5mm。n≤3	MI	Visual / Ruler	Zone B
9	Protect film	Surface scratch but not effect protect function, Allowed		Visual Inspection	