Electra House, 32 Southtown Road
Great Yarmouth, Norfolk
NR31 0DU, England

Telephone +44 (0)1493 602602
Fax +44 (0)1493 665111
Email:sales@midasdisplays.com
www.midasdisplays.com

MDE042A400300RBW	400 x 300	3-Wire SPI Interface	E-Ink Module
Specification			
Version: 1		Date: 25/04/2018	
Revision			
1	24/04/2018	First Issue.	

Display Features	
Display Size	4.2”
Resolution	400 x 300
Orientation	Landscape
Appearance	Black, White, Red
Logic Voltage	3.3V
Interface	SPI
Touchscreen	N/A
Module Size	91.00 x 77.00 x 1.25 mm
Operating Temperature	0°C ~ +30°C
Pinout	24 - Way FFC
Pitch	0.5mm

RoHS compliant

Box Quantity	Weight / Display
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* - For full design functionality, please use this specification in conjunction with the SSD1619A specification.(Provided Separately)

Display Accessories	
Part Number	**Description**

Optional Variants	
Appearances	**Voltage**

General Description

MDE042A400300RBW is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The 4.2" active area contains 400×300 pixels, and has 1-bit B/W/R full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

Features

- 400×300 pixels display
- White reflectance above 35%
- Contrast ratio above 10:1
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor/ built-in temperature sensor

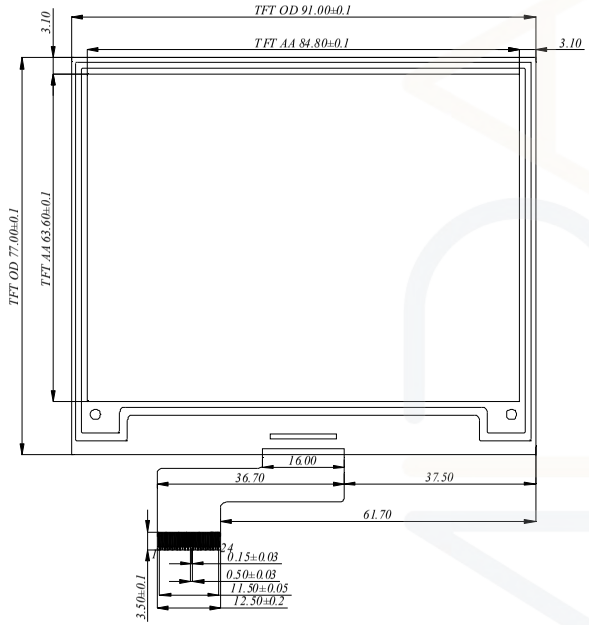
Application

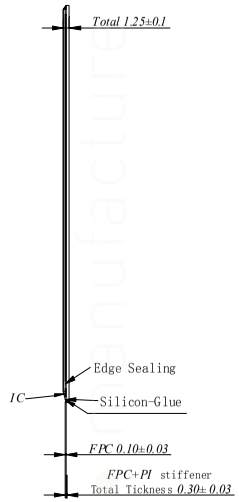
Electronic Shelf Label System

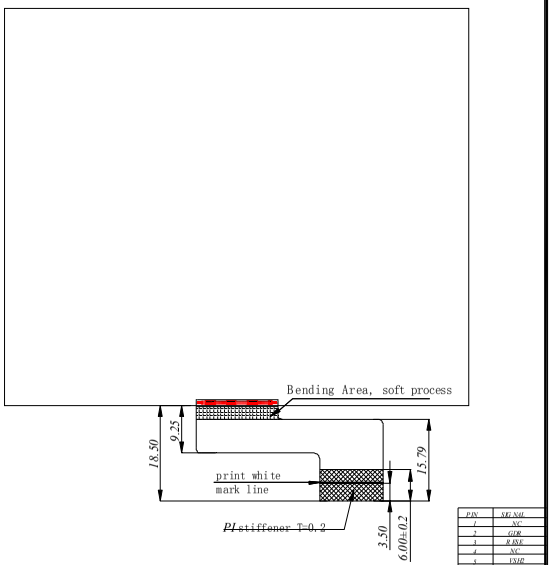
Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	4.2	Inch	
Display Resolution	400(H)×300(V)	Pixel	Dpi:119
Active Area	84.8(H)×63.6 (V)	mm	
Pixel Pitch	0.212×0.212	mm	
Pixel Configuration	Square		
Outline Dimension	91.00(H)× 77.00(V) × 1.25(D)	mm	
Weight	15±0.2	g	

Mechanical Drawing of EPD module







PIN	SIGNAL
1	NC
2	GDR
3	RESE
4	NC
5	VSH2
6	TSCL
7	TSCA
8	BS1
9	BUSY
10	RESN
11	D/CN
12	CSB
13	SCL
14	SDA
15	VDD3D
16	VCI
17	VSL
18	VDD
19	VDF
20	VSH1
21	VGH
22	VSL
23	VGL
24	VCOM

NOTES:
1. DISPALY MODE 4.2 ARREY FOR EPD;
2. DRIVE IC: SSD1619
3. RESOLUTION:300gate X 400source;
4. pixel pitch:0.212mm X 0.212mm;
5. Unspecified Tolerance:±0.20;
6. Material conform to the ROHS standar

Midas Displays

ALL UNITS: mm	DATE	MODEL NUMBER : MDE042A400300RBW		SHEET:
DWN:				
CHK: Alan		CUSTOMER NO:		
APP: Donlin		P/N	PROJECTION	

Input/Output Terminals

Pin #	Single	Description	Remark
1	NC	No connection and do not connect with other NC pins NC	Keep Open
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	NC	No connection and do not connect with other NC pins	Keep Open
5	VSH2	Positive Source driving voltage	
6	TSCL	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I2C Interface to digital temperature sensor Date pin	
8	BS1	Bus selection pin	Note 6-5
9	BUSY	Busy state output pin	Note 6-4
10	RES #	Reset	Note 6-3
11	D/C #	Data /Command control pin	Note 6-2
12	CS #	Chip Select input pin	Note 6-1
13	SCL	serial clock pin (SPI)	
14	SDA	serial data pin (SPI)	
15	VDDIO	Power for interface logic pins	
16	VCI	Power Supply pin for the chip	
17	VSS	Ground	
18	VDD	Core logic power pin	
19	VPP	Power Supply for OTP Programming	
20	VSH1	Positive Source driving voltage	
21	VGH	Power Supply pin for Positive Gate driving voltage and VSH	
22	VSL	Negative Source driving voltage	
23	VGL	Power Supply pin for Negative Gate driving voltage, VCOM and VSL	
24	VCOM	VCOM driving voltage	

Note 6-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication: only when CS# is pulled LOW.
Note 6-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulle set is active low.
Note 6-4: This pin (BUSY) is Busy state output pin. When Busy is High the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin High when the driver IC is working such as:
- Outputting display waveform; or
- Communicating with digital temperature sensor

Note 6-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected.

MCU Interface

MCU Interface selection

The SSD1619A can support 3-wire/4-wire serial peripheral. In the SSD1619A, the MCU interface is pin selectable by BS1 shown in Table7-1.

Note

(1) L is connected to VSS

(2) H is connected to VDDIO

Table 1 : Interface pins assignment under different MCU interface

MCU Interface	Pin Name					
	BS1	RES#	CS#	D/C#	SCL	SDA
4-wire serial peripheral interface (SPI)	Connect to VSS	Required	Required	Required	SCL	SDA
3-wire serial peripheral interface (SPI) – 9 bits SPI	Connect to VDDIO	Required	Required	Connect to VSS	SCL	SDA

2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C# and CS#. The control pins status in 4-wire SPI in writing command/data is shown in Table 7-2 and the write procedure 4-wire SPI is shown in Table 7-2

Table 7-2 : Control pins status of 4-wire SPI

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

Note:

(1) L is connected to VSS and H is connected to VDDIO

(2) ↑ stands for rising edge of signal

(3) SDA(Write Mode) is shifted into an 8-bit shift register on each rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

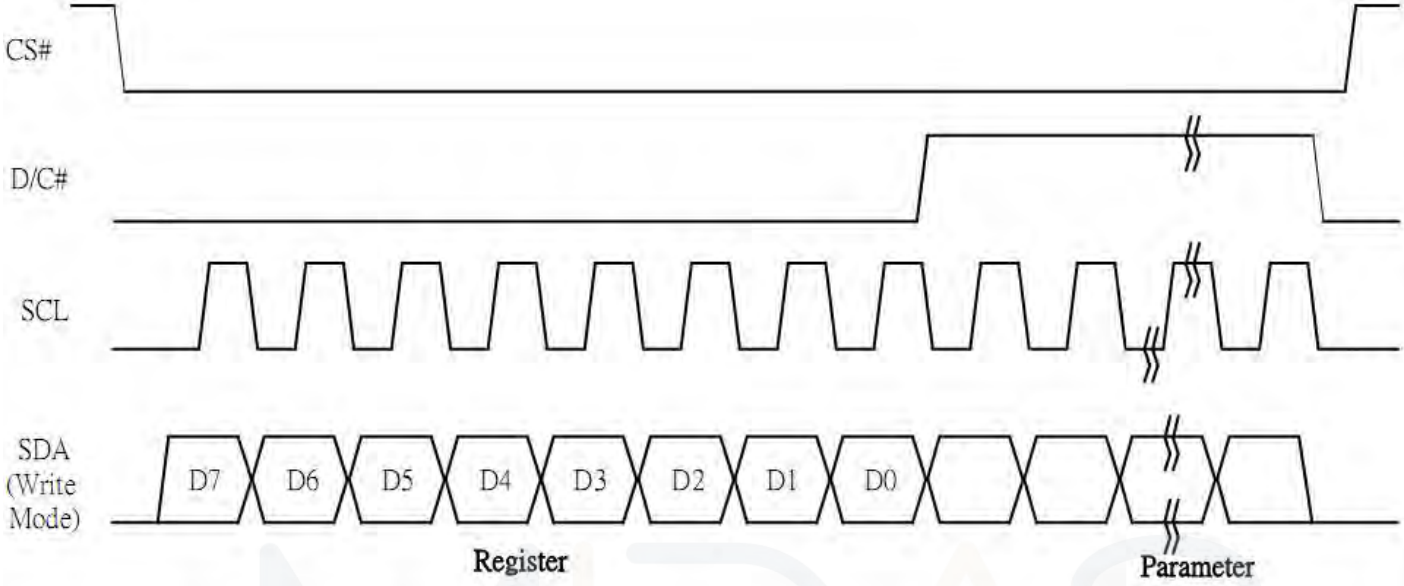


Figure 7-2 : Write procedure in 4-wire SPI mode

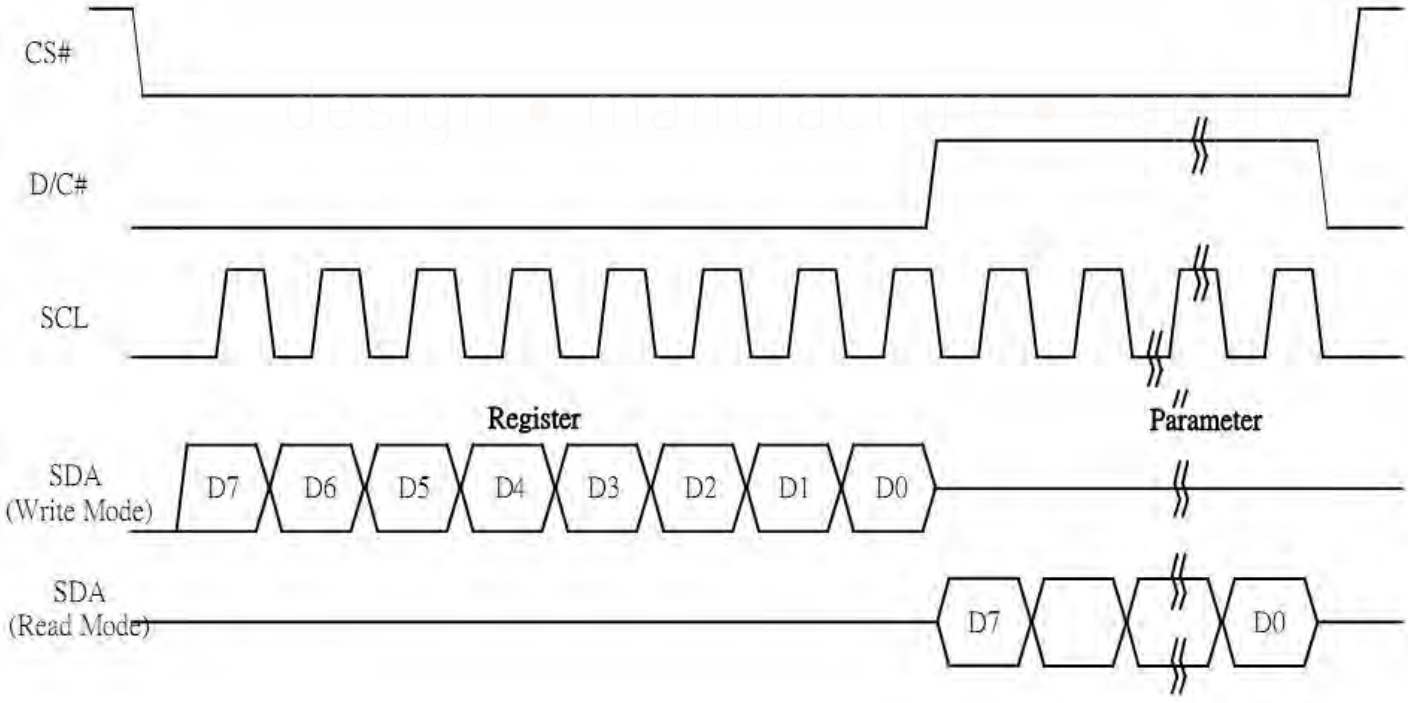


Figure 7-2 : Read procedure in 4-wire SPI mode

3 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data SDA and CS#. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table7-3.

In the write operation, a 9-bit data will be shifted into the shift register on each clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or write data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data. Table 7-3 shows the write procedure in 3-wire SPI

Table 7-3 : Control pins status of 3-wire SPI

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

Note:

(1) L is connected to VSS and H is connected to VDDIO

(2) ↑ stands for rising edge of signal

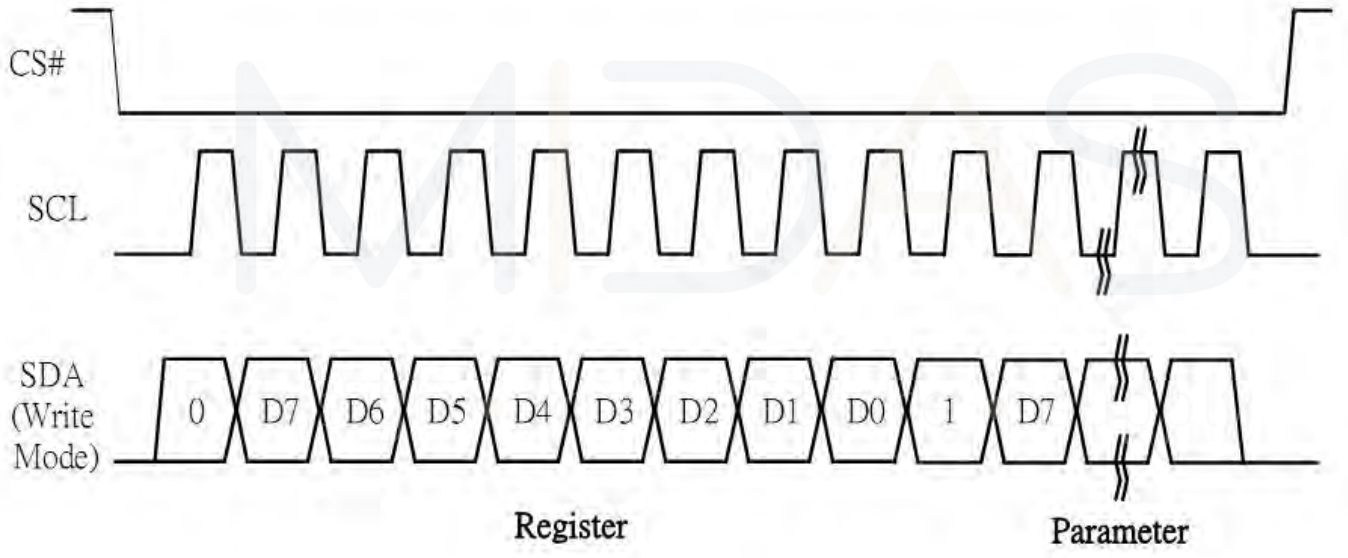


Figure 7-3 : Write procedure in 3-wire SPI

In the read operation (Register 0x1B, 0x27, 0x2D, 0x2E, 0x2F, 0x35), SDA data are transferred in the unit of 9 bits. After CS# pull low, the first byte is command byte, the D/C# bit is as 0 and following with the register byte. After command byte send, the following byte(s) are data byte(s), with D/C# bit is 1. After D/C# bit sending from MCU, an 8-bit data will be shifted out on each clock falling edge. The serial data SDA bit shifting sequence is D7, D6, to D0 bit. Figure 7-4 shows the read procedure in 3-wire SPI.

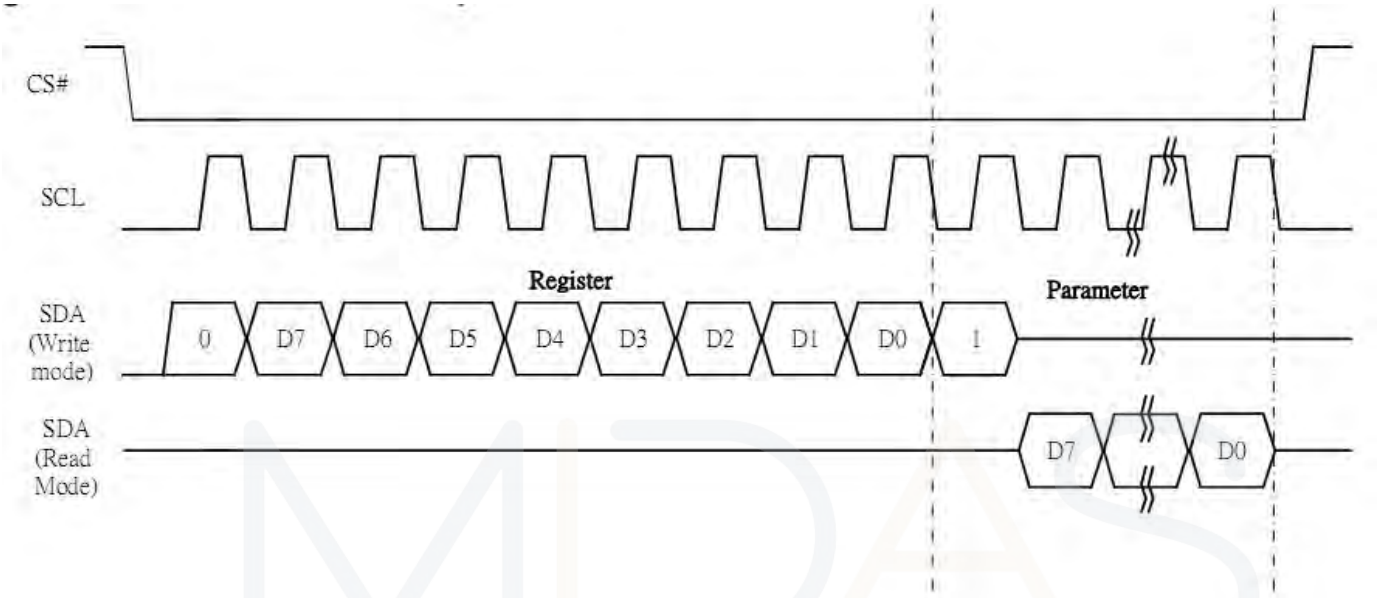


Figure 7-3 : Read procedure in 3-wire SPI mode

COMMAND TABLE

Command Table

R/W #	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting A[8:0]= 12Bh [POR], 300 MUX MUX Gate lines setting as (A[8:0] + 1). B[2:0] = 000 [POR]. Gate scanning sequence and direction B[2]: GD Selects the 1st output Gate GD=0 [POR], G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, … GD=1, G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, … B[1]: SM Change scanning order of gate driver. SM=0 [POR], G0, G1, G2, G3…299 (left and right gate interlaced) SM=1, G0, G2, G4 …G298, G1, G3, …G299 B[0]: TB TB = 0 [POR], scan from G0 to G299 TB = 1, scan from G299 to G0.
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	0	A8		
0	0	0	03	0	0	0	0	0	1	1	Gate Driving voltage Control	Set Gate driving voltage A[4:0] = 19h [POR] VGH setting from 10V to 20V
0	1		0	0	0	A4	A3	A2	A1	A0		

A[4:0]	VGH	A[4:0]	VGH
03h	10	0Fh	16
04h	10.5	10h	16.5
05h	11	11h	17
06h	11.5	12h	17.5
07h	12	13h	18
08h	12.5	14h	18.5
09h	13	15h	19
0Ah	13.5	16h	19.5
0Bh	14	17h	20
0Ch	14.5	0Fh	NA
0Dh	15		
0Eh	15.5		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source driving voltage
0	1		A7	A6	A5	A4	A3	A2	A1	A0		A[7:0] = 41h [POR], VSH1 at 15V
0	1		B7	B6	B5	B4	B3	B2	B1	B0		B[7:0] = A8h [POR], VSH2 at 5V.
0	1		C7	C6	C5	C4	C3	C2	C1	C0		C[7:0] = 32h [POR], VSL at -15V

A[7]/B[7] = 1,
VSH1/VSH2 voltage setting from 2.4V to 8.8V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
8Eh	2.4	AFh	5.7
8Fh	2.5	B0h	5.8
90h	2.6	B1h	5.9
91h	2.7	B2h	6
92h	2.8	B3h	6.1
93h	2.9	B4h	6.2
94h	3	B5h	6.3
95h	3.1	B6h	6.4
96h	3.2	B7h	6.5
97h	3.3	B8h	6.6
98h	3.4	B9h	6.7
99h	3.5	BAh	6.8
9Ah	3.6	BBh	6.9
9Bh	3.7	BCh	7
9Ch	3.8	BDh	7.1
9Dh	3.9	BEh	7.2
9Eh	4	BFh	7.3
9Fh	4.1	C0h	7.4
A0h	4.2	C1h	7.5
A1h	4.3	C2h	7.6
A2h	4.4	C3h	7.7
A3h	4.5	C4h	7.8
A4h	4.6	C5h	7.9
A5h	4.7	C6h	8
A6h	4.8	C7h	8.1
A7h	4.9	C8h	8.2
A8h	5	C9h	8.3
A9h	5.1	CAh	8.4
AAh	5.2	CBh	8.5
ABh	5.3	CCh	8.6
ACh	5.4	CDh	8.7
ADh	5.5	CEh	8.8
AEh	5.6	Oher	NA

A[7]/B[7] = 0,
VSH1/VSH2 voltage setting from 9V to 17V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
23h	9	3Ch	14
24h	9.2	3Dh	14.2
25h	9.4	3Eh	14.4
26h	9.6	3Fh	14.6
27h	9.8	40h	14.8
28h	10	41h	15
29h	10.2	42h	15.2
2Ah	10.4	43h	15.4
2Bh	10.6	44h	15.6
2Ch	10.8	45h	15.8
2Dh	11	46h	16
2Eh	11.2	47h	16.2
2Fh	11.4	48h	16.4
30h	11.6	49h	16.6
31h	11.8	4Ah	16.8
32h	12	4Bh	17
33h	12.2	Other	NA
34h	12.4		
35h	12.6		
36h	12.8		
37h	13		
38h	13.2		
39h	13.4		
3Ah	13.6		
3Bh	13.8		

C[7] = 0,
VSL setting from -9V to -17V

C[7:0]	VSL
1Ah	-9
1Ch	-9.5
1Eh	-10
20h	-10.5
22h	-11
24h	-11.5
26h	-12
28h	-12.5
2Ah	-13
2Ch	-13.5
2Eh	-14
30h	-14.5
32h	-15
34h	-15.5
36h	-16
38h	-16.5
3Ah	-17

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start Control	Booster Enable with Phase 1, Phase 2
0	1		1	A6	A5	A4	A3	A2	A1	A0		and Phase 3 for soft start current and duration setting.
0	1		1	B6	B5	B4	B3	B2	B1	B0		A[7:0] -> Soft start setting for Phase1= 8Bh [POR]
0	1		1	C6	C5	C4	C3	C2	C1	C0		B[7:0] -> Soft start setting for Phase2= 9Ch [POR]
0	1		0	0	D5	D4	D3	D2	D1	D0		C[7:0] -> Soft start setting for Phase3= 96h [POR]

D[7:0] -> Duration setting
= 0Fh [POR]
Bit Description of each byte:

A[6:0] / B[6:0] / C[6:0]:

Bit[6:4]	Driving Strength Selection
000	1(Weakest)
001	2
010	3
011	4
100	5
101	6
110	7
111	8(Strongest)

Bit[3:0]	Min Off Time Setting of GDR [Time unit]
0000~0011	NA
0100	2.6
0101	3.2
0110	3.9
0111	4.6
1000	5.4
1001	6.3
1010	7.3
1011	8.4
1100	9.8
1101	11.5
1110	13.8
1111	16.5

D[5:0]: duration setting of phase

D[5:4]: duration setting of phase 3

D[3:2]: duration setting of phase 2

D[1:0]: duration setting of phase 1

Bit[1:0]	Duration of Phase [Approximation]
00	10ms
01	20ms
10	30ms
11	40ms

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	0F	0	0	0	0	1	1	1	1	Gate scan start position	Set the scanning start position of the gate driver. The valid range is from 0 to 299. A[8:0] = 000h [POR] WhenTB=0,SCN [8:0] = A[8:0] When TB=1: SCN [8:0] = 299 - A[8:0]
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0		0	0	0	0	0	0	0	A8		
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control: A[1:0] : Description 00 Normal Mode [POR] 01 Enter Deep Sleep Mode 1 11 Enter Deep Sleep Mode 2 After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high. Remark: To Exit Deep Sleep mode, User required to send HWRESET to the driver
0	1		0	0	0	0	0	0	A1	A0		
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A[2:0] = 011 [POR] A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A2	A1	A0		
0	0	12		0	0	0	1	0	1	0	SW RESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation, BUSY pad will output high. Note: RAM are unaffected by this command.

<table>
<tr><td colspan="12">Command Table</td></tr>
<tr><td>R/W#</td><td>D/C#</td><td>Hex</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Command</td><td>Description</td></tr>
<tr><td>0</td><td>0</td><td>14</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>HV Ready Detection</td><td>HV ready detection

The command required CLKEN=1 and ANALOGEN=1
Refer to Register 0x22 for detail.
After this command initiated, HV Ready detection starts.
BUSY pad will output high during detection.
The detection result can be read from the Status Bit Read (Command 0x2F).</td></tr>
<tr><td colspan="12"></td></tr>
<tr><td>0</td><td>0</td><td>15</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td rowspan="2">VCI Detection</td><td rowspan="2">VCI Detection
A[2:0] = 100 [POR] , Detect level at 2.3V
A[2:0] : VCI level Detect
<table><tr><td>A[2:0]</td><td>VCI level</td></tr><tr><td>011</td><td>2.2V</td></tr><tr><td>100</td><td>2.3V</td></tr><tr><td>101</td><td>2.4V</td></tr><tr><td>110</td><td>2.5V</td></tr><tr><td>111</td><td>2.6V</td></tr><tr><td>Other</td><td>NA</td></tr></table>The command required CLKEN=1 and ANALOGEN=1
Refer to Register 0x22 for detail.
After this command initiated, VCI detection starts.
BUSY pad will output high during detection.
The detection result can be read from the Status Bit Read (Command 0x2F).</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A2</td><td>A1</td><td>A0</td></tr>
</table>

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	18	0	0	0	1	1	0	0	0	Temperature Sensor Control	Temperature Sensor Selection A[7:0] = 48h [POR], external temperatrure sensor A[7:0] = 80h Internal temperature sensor
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor	Write to temperature register. A[11:0] = 7FFh [POR]
0	0		A11	A10	A9	A8	A7	A6	A5	A4	Control (Write to	
0	1		A3	A2	A1	A0	0	0	0	0	temperature register)	
0	0	1B	0	0	0	1	1	0	1	1	Temperature Sensor	Read from temperature register.
0	0		A11	A10	A9	A8	A7	A6	A5	A4	Control (Read from	
0	1		A3	A2	A1	A0	0	0	0	0	temperature register)	
0	0	1C	0	0	0	1	0	1	0	0	Temperature Sensor	Write Command to External temperature sensor. A[7:0] = 00h [POR], B[7:0] = 00h [POR], C[7:0] = 00h [POR], A[7:6] A[5:0] – Pointer Setting B[7:0] – 1st parameter C[7:0] – 2nd parameter The command required CLKEN=1. Refer to Register 0x22 for detail. After this command initiated, Write Command to external temperature sensor starts. BUSY pad will output high during operation.
0	0		A7	A6	A5	A4	A3	A2	A1	A0	Control (Write	
0	1		B7	B6	B5	B4	B3	B2	B1	B0	Command to External	
0	1		C7	C6	C5	C4	C3	C2	C1	C0	temperature sensor)	

A[7:6]	Select no of byte to be sent
00	Address + pointer
01	Address + pointer + 1st parameter
10	Address + pointer + 1st parameter + 2nd pointer
11	Address

<table>
<tr><td colspan="12">Command Table</td></tr>
<tr><td>R/W#</td><td>D/C#</td><td>Hex</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Command</td><td>Description</td></tr>
<tr><td>0</td><td>0</td><td>20</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Master Activation</td><td>Activate Display Update Sequence

The Display Update Sequence Option is located at R22h.

BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images.</td></tr>
<tr><td colspan="12"></td></tr>
<tr><td>0</td><td>0</td><td>21</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Display Update</td><td rowspan="2">RAM content option for Display Update
A[7:0] = 00h [POR]

A[7:4] Red RAM option
<table><tr><td>0000</td><td>Normal</td></tr><tr><td>0100</td><td>Bypass RAM content as 0</td></tr><tr><td>1000</td><td>Inverse RAM content</td></tr></table>
A[3:0] BW RAM option
<table><tr><td>0000</td><td>Normal</td></tr><tr><td>0100</td><td>Bypass RAM content as 0</td></tr><tr><td>1000</td><td>Inverse RAM content</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>Control 1</td></tr>
</table>

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation A[7:0]= FFh (POR)

	Parameter(in Hex)
Enable Clock Signal, Then Enable ANALOG Then DISPLAY with DISPLAY Mode 1 Then Disable ANALOG Then Disable OSC	C7
Enable Clock Signal, Then Enable ANALOG Then DISPLAY with DISPLAY Mode 2 Then Disable ANALOG Then Disable OSC	CF
Enable Clock Signal, Then Load LUT with DISPLAY Mode 1	90
Enable Clock Signal, Then Load Temperature value from I2C Single Master Interface Then Load LUT with DISPLAY Mode 1	B0
Enable Clock Signal, Then Load LUT with DISPLAY Mode	98
Enable Clock Signal, Then Load Temperature value from I2C Single Master Interface Then Load LUT with DISPLAY Mode 2	B8
Enable Clock Signal, Then Load LUT with DISPLAY Mode 1 To Disable Clock Signal	91
Enable Clock Signal, Then Load Temperature value from I2C Single Master Interface Then Load LUT with DISPLAY Mode 1 To Disable Clock Signal	B1
Enable Clock Signal, Then Load LUT with DISPLAY Mode 2 To Disable Clock Signal	99
Enable Clock Signal, Then Load Temperature value	B9

from I2C Single Master Interface Then Load LUT with DISPLAY Mode 2 To Disable Clock Signal	
Enable ANALOG Then DISPLAY with DISPLAY Mode 1 Then Disable ANALOG Then Disable OSC	47
Enable ANALOG Then DISPLAY with DISPLAY Mode 2 Then Disable ANALOG Then Disable OSC	4F
To Enable Clock Signal (CLKEN=1)	80
To Enable Clock Signal, then Enable ANALOG (CLKEN=1, ANALOGEN=1)	C0
Enable ANALOG Then DISPLAY with DISPLAY Mode 1	44
Enable ANALOG Then DISPLAY with DISPLAY Mode 2	4C
To DISPLAY with DISPLAY Mode 1	04
To DISPLAY with DISPLAY Mode 2	0C
To Disable ANALOG, then Disable Clock Signal	03
(CLKEN=0, ANALOGEN=0) To Disable Clock Signal (CLKEN=0)	01

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	24	0	0	1	0	0	1	0	0	Write RAM (BW)	After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly For Write pixel: Content of Write RAM(BW) = 1 For Black pixel: Content of Write RAM(BW) = 0
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED)	After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly. For Red pixel: Content of Write RAM(RED) = 1 For non-Red pixel [Black or White]: Content of Write RAM(RED) = 0
0	0	27	0	0	1	0	0	1	1	1	Read RAM	After this command, data read on the MCU bus will fetch data from RAM [According to parameter of Register 41h to select reading RAM(BW) / RAM(RED)], until another command is written. Address pointers will advance accordingly. The 1st byte of data read is dummy data.
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value. The sensed VCOM voltage is stored in register The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	Stabling time between entering VCOM sensing mode and reading acquired. A[6]=1, Normal Mode A[6]=0, Reserve A[3:0] = 09h, duration = 10s. VCOM sense duration = Setting + 1 Seconds
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	2A	0	0	1	0	1	0	1	0	Program VCOM OTP	Program VCOM register into OTP The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Write VCOM register from MCU interface A[7:0] = 00h [POR]
0	1		A7	A6	A5	A4	A3	A2	A1	A0		

A[7:0]	VCOM	A[7:0]	VCOM
08h	-0.2	44h	-1.7
0Ch	-0.3	48h	-1.8
10h	-0.4	4Ch	-1.9
14h	-0.5	50h	-2
18h	-0.6	54h	-2.1
1Ch	-0.7	58h	-2.2
20h	-0.8	5Ch	-2.3
24h	-0.9	60h	-2.4
28h	-1	64h	-2.5
2Ch	-1.1	68h	-2.6
30h	-1.2	6Ch	-2.7
34h	-1.3	70h	-2.8
38h	-1.4	74h	-2.9
3Ch	-1.5	78h	-3
40h	-1.6	Other	NA

0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read for Display Option	Read Register stored in OTP for Display Option: 1. A[7:0]: VCOM OTP Selection (R37, Byte A) 2. B[7:0]: VCOM Register (R2C) 3. C[7:0]~F[7:0]: Display Mode (R37, Byte B and Byte E) [4 bytes] 4. G[7:0]~H[7:0]: Waveform Version (R37, Byte F and Byte G) [2 bytes]
1	1		A7	A6	A5	A4	A3	A2	A1	A0		
1	1		B7	B6	B5	B4	B3	B2	B1	B0		
1	1		C7	C6	C5	C4	C3	C2	C1	C0		
			D7	D6	D5	D4	D3	D2	D1	D0		
			E7	E6	E5	E4	E3	D2	E1	E0		
			F7	F6	F5	F4	F3	F2	F1	F0		
			G7	G6	G5	G4	G3	G2	G1	G0		
			H7	H6	H5	H4	H3	H2	H1	H0		

0	0	2E	0	0	1	0	1	1	1	0	User ID Read	Read 10 Byte User ID stored in OTP: A[7:0]]~J[7:0]: UserID (R38, Byte A and Byte J) [10 bytes]
1	1		A7	A6	A5	A4	A3	A2	A1	A0		
1	1		B7	B6	B5	B4	B3	B2	B1	B0		
1	1		C7	C6	C5	C4	C3	C2	C1	C0		
1	1		D7	D6	D5	D4	D3	D2	D1	D0		
1	1		E7	E6	E5	E4	E3	D2	E1	E0		
1	1		F7	F6	F5	F4	F3	F2	F1	F0		
1	1		G7	G6	G5	G4	G3	G2	G1	G0		
1	1		H7	H6	H5	H4	H3	H2	H1	H0		
1	1		I7	I6	I5	I4	I3	I2	I1	I0		
1	1		J7	J6	J5	J4	J3	J2	J1	J0		

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	Read IC status Bit [POR 0x21] A[5]: HV Ready Detection flag [POR=1] 0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01] Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively.
0	0	30	0	0	1	1	0	0	0	0	Program WS OTP	Program OTP of Waveform Setting The contents should be written into RAM before sending this command. The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	31	0	0	1	1	0	0	0	1	Load WS OTP	Load OTP of Waveform Setting The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [70 bytes], which contains the content of VS [nX-LUT], TP #[nX], RP#[n]). Refer to Session 6.7 Waveform Setting
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		..	..	..	..	..	..	..	..		
0	1		..	..	..	..	..	..	..	..		
0	0	34	0	0	1	1	0	1	0	0	CRC calculation	CRC calculation command BUSY pad will output high during operation.
0	0	35	0	0	1	1	0	1	0	1	CRC Status Read	CRC Status Read A[15:0] is the CRC read out value
1	1		A15	A14	A13	A12	A11	A10	A9	A8		
1	1		A7	A6	A5	A4	A3	A2	A1	A0		

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	36	0	0	1	1	0	1	1	0	Program OTP selection	Program OTP Selection according to the OTP Selection Control [R37h and R38h] The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	37	0	0	1	1	0	1	1	1	Write OTP selection	Write the OTP Selection: A[7]=1 spare VCOM OTP selection B[7:0]~E[7:0] reserved F[7:0]~G[7:0] module ID /waveform version.
0	1		A7	0	0	0	0	0	0	0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		C7	C6	C5	C4	C3	C2	C1	C0		
0	1		D7	D6	D5	D4	D3	D2	D1	D0		
0	1		E7	E6	E5	E4	E3	D2	E1	E0		
0	1		F7	F6	F5	F4	F3	F2	F1	F0		
0	1		G7	G6	G5	G4	G3	G2	G1	G0		
1	0	38	0	0	1	1	1	0	0	0	Write Register for User ID	Write Register for User ID A[7:0]]~J[7:0]: UserID [10 bytes]
1	1		A7	A6	A5	A4	A3	A2	A1	A0		
1	1		B7	B6	B5	B4	B3	B2	B1	B0		
1	1		C7	C6	C5	C4	C3	C2	C1	C0		
1	1		D7	D6	D5	D4	D3	D2	D1	D0		
1	1		E7	E6	E5	E4	E3	D2	E1	E0		
1	1		F7	F6	F5	F4	F3	F2	F1	F0		
1	1		G7	G6	G5	G4	G3	G2	G1	G0		
1	1		H7	H6	H5	H4	H3	H2	H1	H0		
1	1		I7	I6	I5	I4	I3	I2	I1	I0		
1	1		J7	J6	J5	J4	J3	J2	J1	J0		
0	0	39	0	0	1	1	1	0	0	1	OTP program mode	OTP program mode A[1:0] = 00: Normal Mode [POR] A[1:0] = 11: Internal generated OTP programming voltage Remark: User is required to EXACTLY follow the reference code sequences

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	3A	0	0	1	1	1	0	1	0	Set dummy line period	Set number of dummy line period
0	1		0	A6	A5	A4	A3	A2	A1	A0		A[6:0] = 2Ch [POR] Available setting 0 to 127.
0	0	3B	0	0	1	1	1	0	1	1	Set Gate line width	Set Gate line width (TGate) A[3:0] = 1010 [POR]
												Remark: Default value will give 50Hz Frame frequency under 44 dummy line pulse setting.

Resolution: 400x300

Frame Frequency [Hz]	Parameter of 0x3A	Parameter of 0x3B
15	0×79	0×0E
20	0×10	0×0E
25	0×26	0×0D
30	0×4E	0×0C
35	0×18	0×0C
40	0×43	0×0B
45	0×1A	0×0B
50	0×2C	0×0A
55	0×0D	0×0A
60	0×21	0×09
65	0×07	0×09
70	0×28	0×08
75	0×11	0×08
80	0×2F	0×07
85	0×1A	0×07
90	0×08	0×07
95	0×32	0×06
100	0×21	0×06
105	0×11	0×06
110	0×03	0×06
115	0×22	0×05
120	0×14	0×05
125	0×07	0×05
135	0×24	0×04
140	0×18	0×04
145	0×0D	0×04
150	0×03	0×04
155	0×27	0×03
160	0×1C	0×03
165	0×12	0×03
170	0×09	0×03
175	0×00	0×03
180	0×2F	0×02
185	0×25	0×02
190	0×1C	0×02
195	0×14	0×02
200	0×0C	0×02

Remark: Frame rate setting depends on resolution.

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A[7:0] = C0h [POR], set VBD as HIZ. A [7:6] :Select VBD option
0	1		A7	A6	A5	A4	0	0	A1	A0		

A[7:6]	Select VBD as
00	GS Transition,
01	Defined in A[1:0] Fix Level,
10	Defined in A[5:4] VCOM
11[POR]	HiZ

A [5:4]	Fix Level Setting for VBD
A[5:4]	VBD level
00[POR]	VSS
01	VSH1
10	VSL
11	VSH2

A [1:0] GS Transition setting for VBD

A[1:0]	VBD Transition
00[POR]	LUT0
01	LUT1
10	LUT2
11	LUT3

0	0	41	0	1	0	0	0	0	0	1	Read RAM Option	Read RAM Option A[0]= 0 [POR] 0 : Read RAM corresponding to 24h 1 : Read RAM corresponding to 26h
0	1		0	0	0	0	0	0	0	A0		
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address	Specify the start/end positions of the window address in the X direction by an address unit for RAM A[5:0]: XSA[5:0], XStart, 00h [POR] B[5:0]: XEA[5:0], XEnd, 31h [POR]
0	1		0	0	A5	A4	A3	A2	A1	A0	Start / End position	
0	1		0	0	B5	B4	B3	B2	B1	B0		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address	Specify the start/end positions of the window address in the Y direction by an address unit for RAM A[8:0]: YSA[8:0], YStart, 000h [POR] B[8:0]: YEA[8:0], YEnd, 12Bh [POR]
0	1		A7	A6	A5	A4	A3	A2	A1	A0	Start / End position	
0	1		0	0	0	0	0	0	0	A8		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		0	0	0	0	0	0	0	B8		

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[5:0]: 00h [POR].
0	1		0	0	A5	A4	A3	A2	A1	A0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: 000h [POR].
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	0	A8		
0	1	74	0	1	1	1	0	1	0	0	Set Analog Block Control	A[7:0]: 54h
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1	7E	0	1	1	1	1	1	1	0	Set Digital Block Control	A[7:0]: 3Bh
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1	7F	0	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read Commands.

Command Table

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>46</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td rowspan="2">Auto Write RED RAM for Regular Pattern</td><td rowspan="2">Auto Write RED RAM for Regular Pattern
A[7:0] = 00h [POR]
A[7]: The 1st step value, POR = 0
A[6:4]: Step Hieght, POR= 000
Step of alter RAM in Y-direction according to Gate
<table>
<tr><th>A[6:4]</th><th>Height</th><th>A[6:4]</th><th>Height</th></tr>
<tr><td>000</td><td>8</td><td>100</td><td>128</td></tr>
<tr><td>001</td><td>16</td><td>101</td><td>256</td></tr>
<tr><td>010</td><td>32</td><td>110</td><td>300</td></tr>
<tr><td>011</td><td>64</td><td>111</td><td>NA</td></tr>
</table>
A[2:0]: Step Width, POR= 000
Step of alter RAM in X-direction according to Source
<table>
<tr><th>A[2:0]</th><th>Width</th><th>A[2:0]</th><th>Width</th></tr>
<tr><td>000</td><td>8</td><td>100</td><td>128</td></tr>
<tr><td>001</td><td>16</td><td>101</td><td>256</td></tr>
<tr><td>010</td><td>32</td><td>110</td><td>400</td></tr>
<tr><td>011</td><td>64</td><td>111</td><td>NA</td></tr>
</table>
BUSY pad will output high during operation.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>47</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td rowspan="2">Auto Write B/W RAM for Regular Pattern</td><td rowspan="2">Auto Write B/W RAM for Regular Pattern
A[7:0] = 00h [POR]
A[7]: The 1st step value, POR = 0
A[6:4]: Step Hieght, POR= 000
Step of alter RAM in Y-direction according to Gate
<table>
<tr><th>A[6:4]</th><th>Height</th><th>A[6:4]</th><th>Height</th></tr>
<tr><td>000</td><td>8</td><td>100</td><td>128</td></tr>
<tr><td>001</td><td>16</td><td>101</td><td>256</td></tr>
<tr><td>010</td><td>32</td><td>110</td><td>400</td></tr>
<tr><td>011</td><td>64</td><td>111</td><td>NA</td></tr>
</table>
A[2:0]: Step Width, POR= 000
Step of alter RAM in X-direction according to Source
<table>
<tr><th>A[2:0]</th><th>Width</th><th>A[2:0]</th><th>Width</th></tr>
<tr><td>000</td><td>8</td><td>100</td><td>128</td></tr>
<tr><td>001</td><td>16</td><td>101</td><td>256</td></tr>
<tr><td>010</td><td>32</td><td>110</td><td>400</td></tr>
<tr><td>011</td><td>64</td><td>111</td><td>NA</td></tr>
</table>
During operation, BUSY pad will output high.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
</table>

Reference Circuit

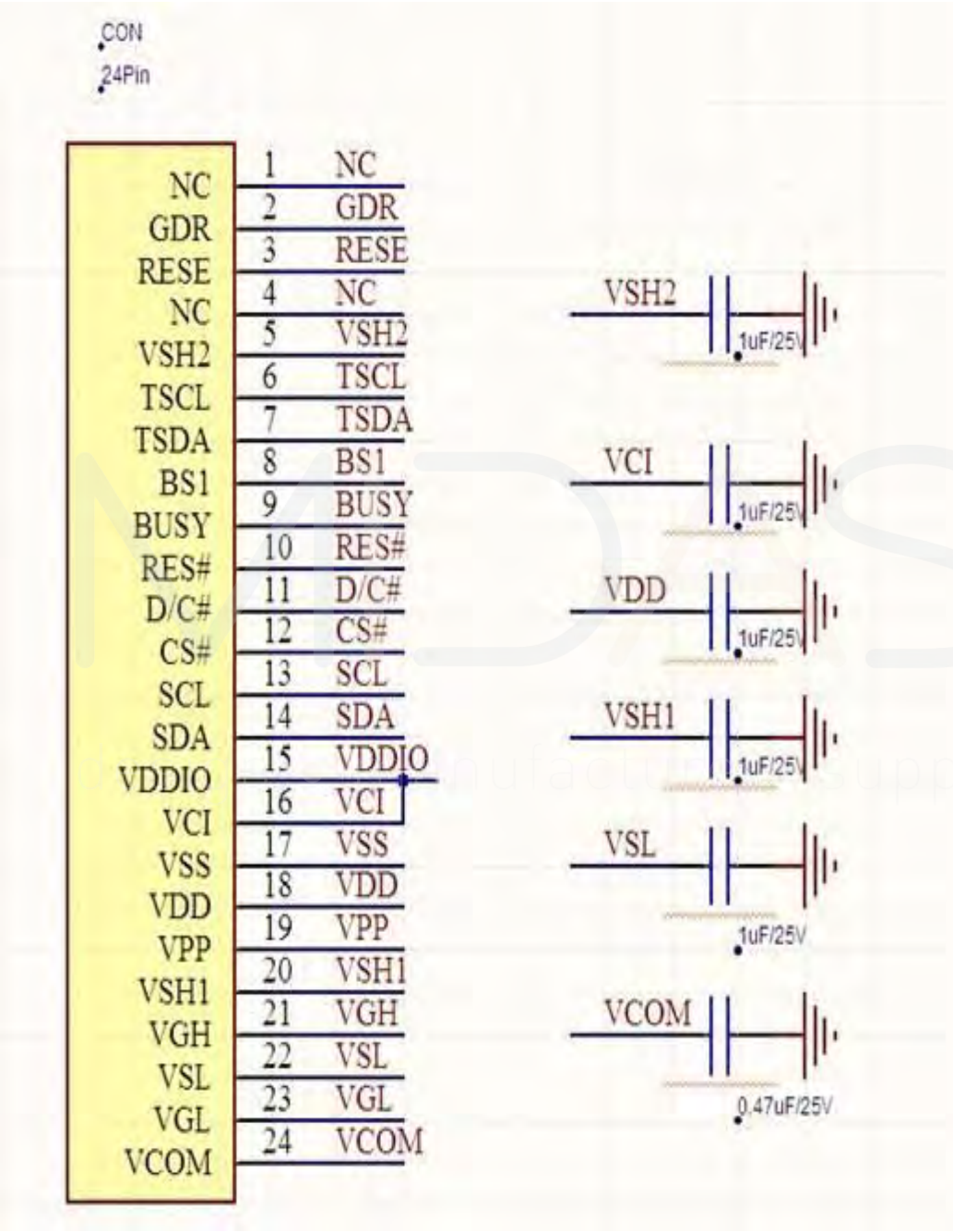


Figure. 9-1

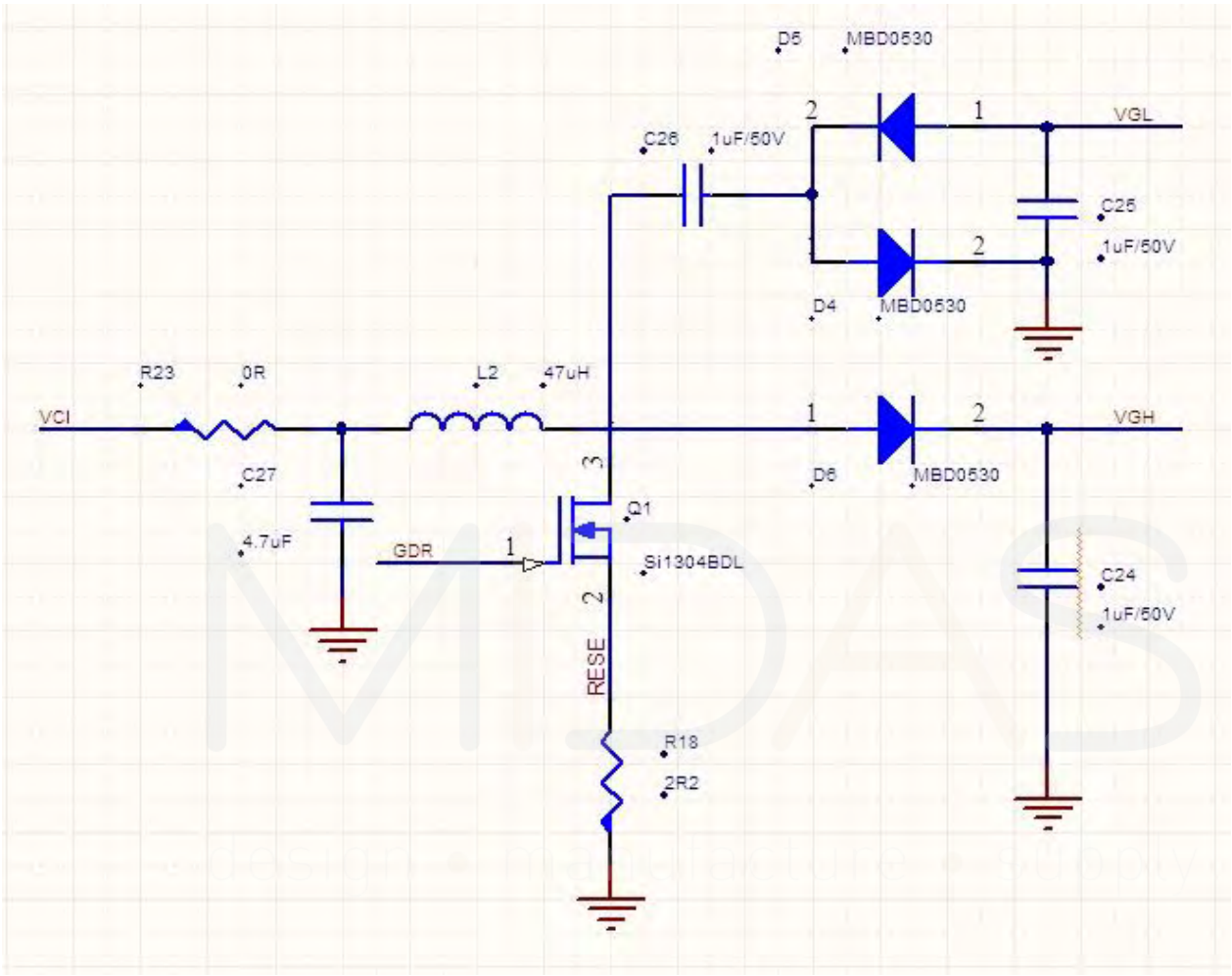

D5
MBD0530
2
1
VGL
C26
1uF/50V
C25
1uF/50V
D4
MBD0530
R23
0R
L2
47uH
VCI
1
2
VGH
C27
3
D6
MBD0530
Q1
4.7uF
GDR
1
Si1304BDL
C24
1uF/50V
2
RESE
R18
2R2

Figure. 9-2

Absolute Maximum Rating

Table 10-1 : Maximum Ratings

Symbol	Parameter	Rating	Unit
VCI	Logic supply voltage	-0.5 to +6.0	V
TOPR	Operation temperature range	0 to 30	℃
TSTG	Storage temperature range	-25 to 60	℃

DC CHARACTERISTICS

The following specifications apply for: VSS=0V, VCI=3.3V, T_{OPR}=25℃.

Table 11-1: DC Characteristics

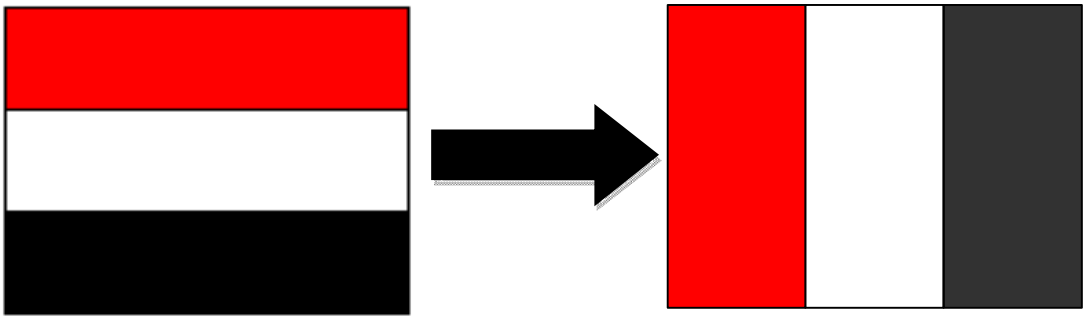
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VCI	VCI operation voltage	-	2.2	3.3	3.7	V
VIH	High level input voltage	Digital input pins	0.7VDDIO	-	-	V
VIL	Low level input voltage	Digital input pins	-		0.3VDDIO	V
VOH	High level output voltage	IOH = 400uA	VDDIO-0.4O	-	-	V
VOL	Low level output voltage	IOL = -400uA	-		0.1VDDIO	V
Iupdate	Module operating current	-	-	10	-	mA
Isleep	Deep sleep mode	VCI=3.3V	-	0.73	-	uA

- The Typical power consumption is measured using associated 25℃ waveform with following pattern transition: from horizontal scan pattern to vertical scan pattern. (Note 11-1)
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Midas.

- Vcom value will be OTP before in factory or present on the label sticker.

Note 11-1

The Typical power consumption



AC Characteristics

1 Oscillator frequency

The following specifications apply for: VSS=0V, VDD=1.8V, TOPR=25ºC.

Table12-1: Oscillator Frequency

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
Fosc	Internal Oscillator frequency	VCI=2.2 to 3.7V	CL	0.95	1	1.05	MHz

2 Serial Peripheral Interface

The following specifications apply for: VDDIO - VSS = 2.2V to 3.7V, TOPR = 25℃

Table 12-2 : Serial Peripheral Interface Timing Characteristics

Write mode

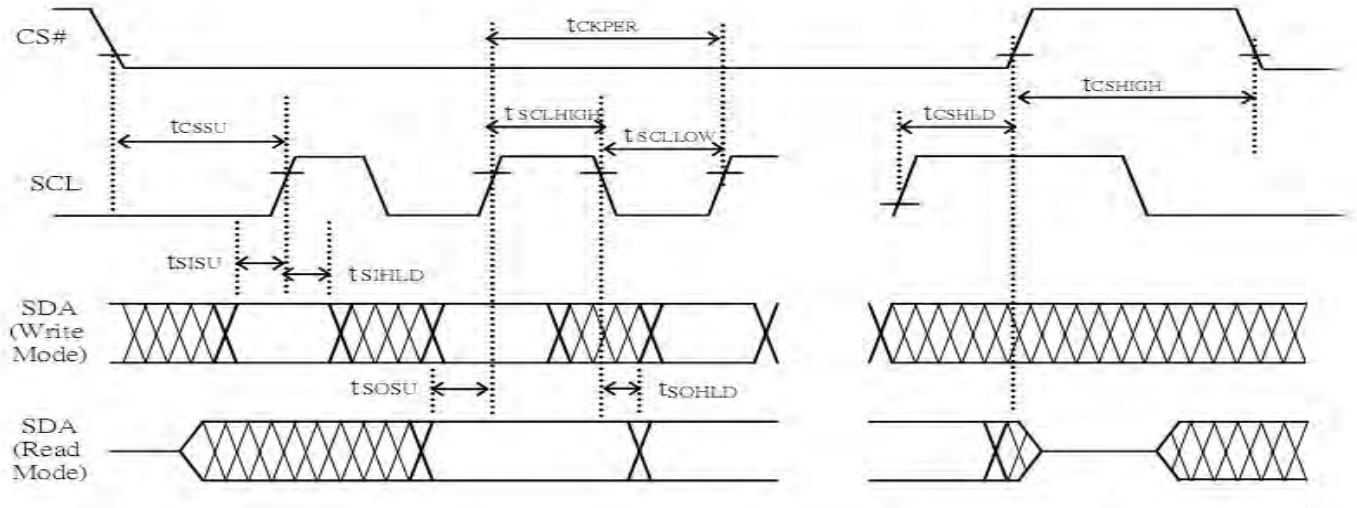
Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Write Mode)			20	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	20			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	20			ns
tCSHIGH	Time CS# has to remain high between two transfers	100			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	25			ns
tSCLLOW	Part of the clock period where SCL has to remain low	25			ns
tSISU	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
tSIHLD	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Read Mode)			2.5	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	100			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	50			ns
tCSHIGH	Time CS# has to remain high between two transfers	250			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	180			ns
tSCLLOW	Part of the clock period where SCL has to remain low	180			ns
tSOSU	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
tSOHLD	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

Note: All timings are based on 20% to 80% of VDDIO-VSS

Figure 12-2: SPI timing diagram



Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25℃	110	-	mAs	-
Deep sleep mode	-	25℃	0.73	-	uA	-

Typical Operating Sequence

1 Normal Operation Flow

Sequence	Action by	Command	Action Description	Remark
1	User	-	Power on (VCI supply);	-
2	User	-	HW Reset	-
	IC	-	After HW reset, the IC will be ready for command input	-
	User	C 12	Command: SW Reset	--
	IC	-	After SW reset, the IC will have Registers load with POR value VCOM register loaded with OTP value IC enter idle mode	BUSY = H
	User	-	Wait until BUSY = L	-
3	-	-	Send initial code to driver including setting of	-
	User	C 74 D 54	Command: Set Analog Block Control	-
	User	C 7E D 3B	Command: Set Digital Block Control	-
	User	C 01	Command: Driver Output Control (MUX, Source gate scanning direction)	-
	User	C 3A	Command: Set dummy line period	-
	User	C 3B	Command: Set Gate line width	-
	User	C 3C	Command: Border waveform control	-
4	-	-	Data operations for Black White	-
	User	C 11	Command: Data Entry mode setting	-
	User	C 44	Command: RAM X address start /end position	-
	User	C 45	Command: RAM Y address start /end position	-
	User	C 4E	Command: RAM X address counter	-
	User	C 4F	Command: RAM Y address counter	-
	User	C 24	Command: write BW RAM	-
	-	-	Ram Content for Display	-
5	-	-	Data operations for RED	-
	User	C 11	Command: Data Entry mode setting	-
	User	C 44	Command: RAM X address start /end position	-
	User	C 45	Command: RAM Y address start /end position	-
	User	C 4E	Command: RAM X address counter	-
	User	C 4F	Command: RAM Y address counter	-
	User	C 26	Command: write RED RAM	-
			Ram Content for Display	-

6	User	C 22	Command: Display Update Control 2	BUSY=H
	User	C 20	Command: Master Activation	
	IC	-	Booster and regulators turn on	
	IC	-	Load LUT register with corresponding waveform setting stored in OTP)	
	IC	-	Send output waveform according RAM content and LUT.	
	IC	-	Booster and Regulators turn off	
	IC	-	Back to idle mode	
	User	-	Wait until BUSY = L	-
7	User	-	IC power off;	-

Optical characteristics

1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25℃

SYMBOL	PARAMETER	CONDITIONS	MIN	TYPE	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 15-1
Gn	2Grey Level	-	-	DS+(WS-DS)×n(m-1)	-	L*	-
RS_a*	Red State a* value	Red	35	45	48	-	Note 15-1
CR	Contrast Ratio	indoor	-	10	-	-	-
Panel's life	-	0℃～30℃		5years or 1000000 times	-	-	Note 15-2-
Panel	Image Update	Storage and transportation	-	Update the white screen	-	-	-
	Update Time	Operation	-	at least update 1 time per day	-	-	-

WS: White state, DS : Dark state

m: 2

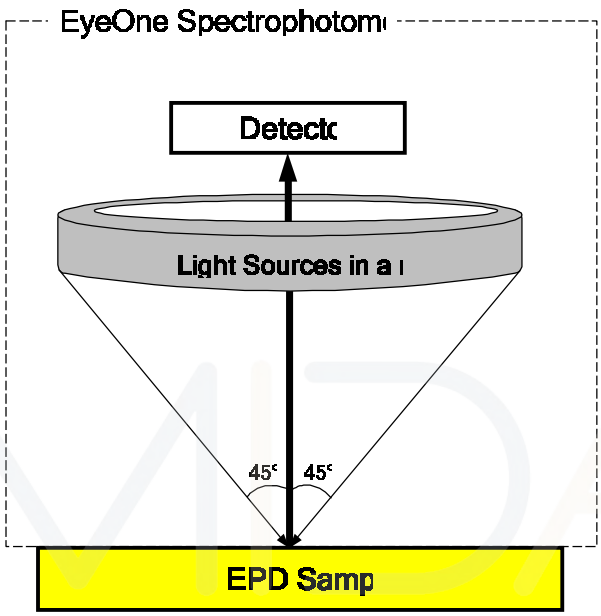
Note 15-1: Luminance meter : Eye - One Pro Spectrophotometer

Note 15-2: we guarantee 1 pixel display quality from 0 ℃~ 27 ℃, and we don't guarantee 1 pixels display quality for 27℃~ 30℃ ,but we can read 0℃~ 30℃ plus from the barcode.

2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd):

$$CR = Rl/Rd$$

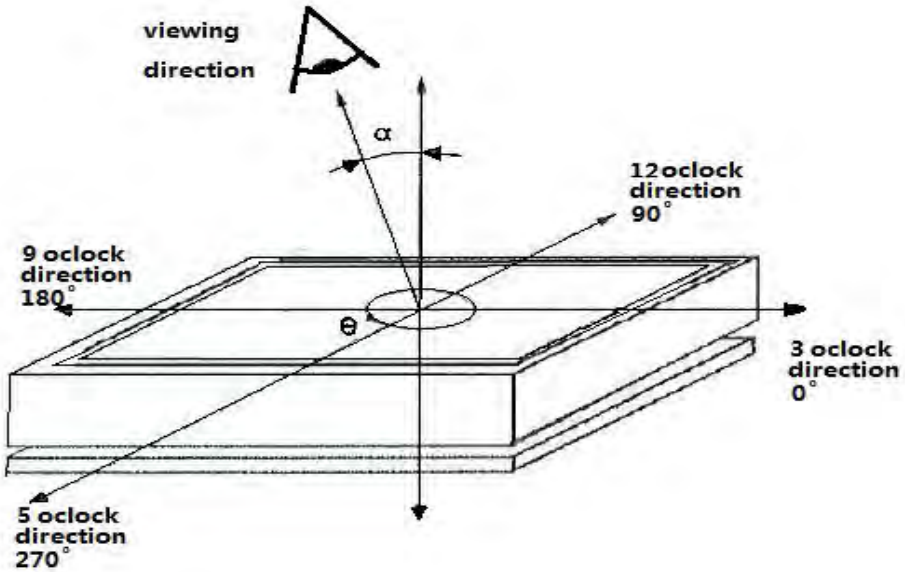


3 Reflection Ratio

The reflection ratio is expressed as:

$R = \text{Reflectance Factor}_{\text{white board}} \times (L_{\text{center}} / L_{\text{white board}})$

L_{center} is the luminance measured at center in a white area (R=G =B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Product specification	The data sheet contains final product specifications.

Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.
Application information
Where application information is given, it is advisory and dose not form part of the specification.

Product Environmental certification
ROHS

REMARK
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T=40℃，RH=35%RH，For 240Hr	IEC 60 068-2-2Bb	
2	Low-Temperature Operation	T = 0℃ for 240 hrs	IEC 60 068-2-2Ab	
3	High-Temperature Storage	T=60℃ RH=35%RH For 240Hr Test in white pattern	IEC 60 068-2-2Bb	
4	Low-Temperature Storage	T = -25℃ for 240 hrs Test in white pattern	IEC 60 068-2-2Ab	
5	High Temperature, High-Humidity Operation	T=40℃，RH=80%RH，For 168Hr	IEC 60 068-2-3CA	
6	High Temperature, High-Humidity Storage	T=50℃，RH=80%RH，For 240Hr Test in white pattern	IEC 60 068-2-3CA	
7	Temperature Cycle	-25℃(30min)~60℃(30min)，50 Cycle Test in white pattern	IEC 60 068-2-14NB	
8	Package Vibration	1.04G,Frequency : 10~500Hz Direction : X,Y,Z Duration:1hours in each direction	Full packed for shipment	
9	Package Drop Impact	Drop from height of 122 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment	
10	UV exposure Resistance	765 W/㎡ for 168hrs,40℃	IEC 60068-2-5 Sa	
11	Electrostatic discharge	Machine model: +/-250V,0Ω,200pF	IEC61000-4-2	

Actual EMC level to be measured on customer application.

Note1: The protective film must be removed before temperature test.

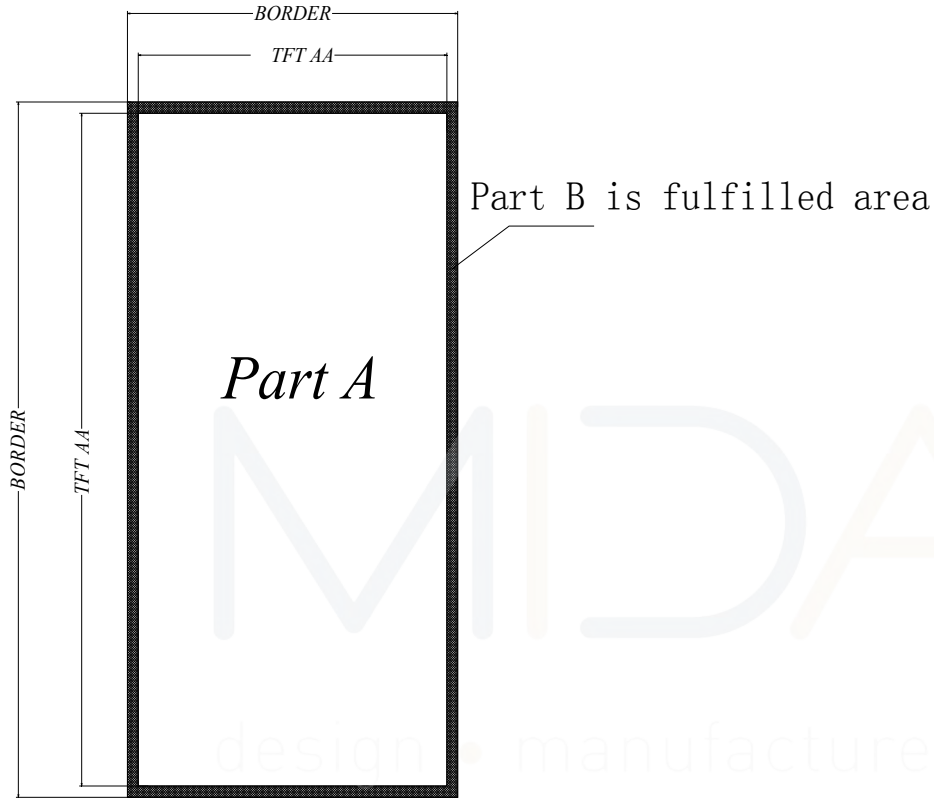
Note2： Stay white pattern for storage and non-operation test.

Note3： Operation is black/white/red pattern , hold time is 150S.

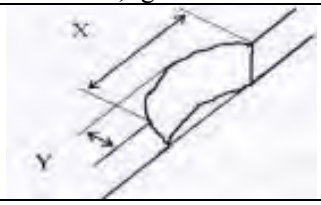
Note4： The function,appearence,opticals should meet the requirements of the test before and after the test.

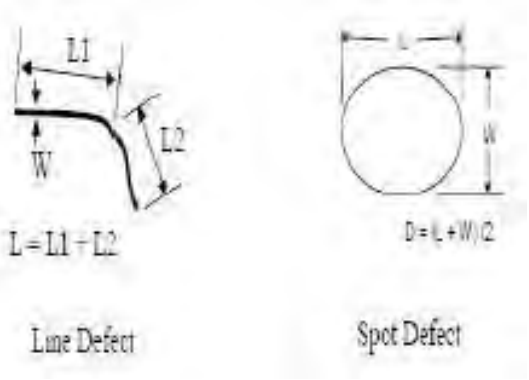
Note5： Keep testing after 2 hours placing at 20℃-25℃.

PartA/PartB specification



Point and line standard

Shipment Inspection Standard						
Equipment：Electrical test fixture, Point gauge						
Outline dimension	91 (H) × 77(V) × 1.25(D)	Unit：㎜	Part-A	Active area	Part-B	Border area
Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
	19℃～25℃	55%±5%RH	800～1300Lux	300 ㎜	35Sec	
Defet type	Inspection method	Standard		Part-A		Part-B
Spot	Electric Display	D≤0.25 ㎜		Ignore		Ignore
		0.25 ㎜＜D≤0.4 ㎜		N≤4		Ignore
		0.40 ㎜＜D≤0.5 ㎜		N≤1		Ignore
		D＞0.5 ㎜		Not Allow		Ignore
Display unwork	Electric Display	Not Allow		Not Allow		Ignore
Display error	Electric Display	Not Allow		Not Allow		Ignore
Scratch or line defect(include dirt)	Visual/Film card	L≤2 ㎜，W≤0.2 ㎜		Ignore		Ignore
		2.0mm＜L≤8.0mm，0.2＜W≤0.5mm,		N≤2		Ignore
		L＞8.0 ㎜，W＞0.5 ㎜		Not Allow		Ignore
PS Bubble	Visual/Film card	D≤0.25mm		Ignore		Ignore
		0.25mm≤D≤0.40mm		N≤4		Ignore
		D＞0.40 mm		Not Allow		Ignore
Side Fragment	Visual/Film card	X≤6mm，Y≤0.5mm, Do not affect the electrode circuit , Ignore				
						
Remark	1.Cannot be defect & failure cause by appearance defect；					
	2.Cannot be larger size cause by appearance defect；					
	L=long W=wide D=point size N=Defects NO					



L=long W=wide D=point size