

FSB50825B/FSB50825BS

Motion SPM[®] 5 Series

Description

The FSB50825B / FSB50825BS is an advanced Motion SPM 5 module providing a fully-featured, high-performance inverter output for AC Induction, BLDC and PMSM motors such as refrigerators, fans and pumps. These modules integrate optimized gate drive of the built-in MOSFETs (FRFET technology) to minimize EMI and losses, while also providing multiple on-module protection features including under-voltage lockouts and thermal monitoring. The built-in high-speed HVIC requires only a single supply voltage and translates the incoming logic-level gate inputs to the high-voltage, high-current drive signals required to properly drive the module's internal MOSFETs. Separate open-source MOSFET terminals are available for each phase to support the widest variety of control algorithms.

Features

- UL Certified No. E209204 (UL1557)
- Optimized for Over 10 kHz Switching Frequency
- 250 V $R_{DS(ON)} = 0.55 \Omega(\text{Max})$ FRFET MOSFET 3-Phase Inverter with Gate Drivers and Protection
- Built-In Bootstrap Diodes Simplify PCB Layout
- Separate Open-Source Pins from Low-Side MOSFETs for Three-Phase Current-Sensing
- Active-HIGH Interface, Works with 3.3 / 5 V Logic, Schmitt-trigger Input
- Optimized for Low Electromagnetic Interference
- HVIC for Gate Driving and Under-Voltage Protection
- Isolation Rating: 1500 V_{rms} / min
- RoHS Compliant
- Moisture Sensitive Level (MSL) 3 for SMD PKG

Applications

- 3-Phase Inverter Driver for Small Power AC Motor Drives



ON Semiconductor[®]

www.onsemi.com

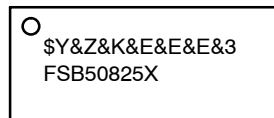


SPM5E-023 / 23LD, PDD STD
CASE MODEJ



SPM5H-023 / 23LD, PDD STD,
SPM23-BD
CASE MODEM

MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
FSB50825X	= Specific Device Code
	X = B or BS

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

FSB50825B/FSB50825BS

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter	Conditions	Rating	Unit
V _{PN}	DC Link Input Voltage, Drain-Source Voltage of Each MOSFET		250	V
BV _{DSS}	Drain-Source Voltage	V _{IN} = 0V, I _D = 250 μA	250	V
I _{PN}	Zero-Bias Static Leakage Current	V _{PN} = 200V, V _{IN} = 0V, V _{DD} = V _{BS} = 0V, T _C = T _J = 25°C for all phase	40	μA
I _{D 25} (Note 2)	Each MOSFET Drain Current, Continuous	T _C = 25°C	3.6	A
I _{D 80} (Note 2)	Each MOSFET Drain Current, Continuous	T _C = 80°C	2.7	A
I _{DP} (Note 2)	Each MOSFET Drain Current, Peak	T _C = 25°C, PW < 100 μs	9.0	A
I _{DRMS} (Note 2)	Each FRFET Drain Current, Rms	T _C = 80°C, F _{PWM} < 20 kHz	1.9	A _{rms}
P _D (Note 2)	Maximum Power Dissipation	T _C = 25°C, For Each MOSFET	14.2	W

CONTROL PART (Each HVIC Unless Otherwise Specified)

Symbol	Parameter	Conditions	Rating	Unit
V _{DD}	Control Supply Voltage	Applied Between V _{DD} and COM	20	V
V _{BS}	High-side Bias Voltage	Applied Between V _B and V _S	20	V
V _{IN}	Input Signal Voltage	Applied Between IN and COM	-0.3 ~ V _{DD} +0.3	V

BOOTSTRAP DIODE PART (Each Bootstrap Diode Unless Otherwise Specified)

Symbol	Parameter	Conditions	Rating	Unit
V _{RRMB}	Maximum Repetitive Reverse Voltage		250	V
I _{FB} (Note 2)	Forward Current	T _C = 25°C	0.5	A
I _{FPB} (Note 2)	Forward Current (Peak)	T _C = 25°C, Under 1ms Pulse Width	1.5	A

THERMAL RESISTANCE

Symbol	Parameter	Conditions	Rating	Unit
R _{th(j-c)Q}	Junction to Case Thermal Resistance (Note1)	Inverter MOSFET part, (Per Module)	1.7	°C/W

TOTAL SYSTEM

Symbol	Parameter	Conditions	Rating	Unit
T _J	Operating Junction Temperature		-40 ~ 150	°C
T _{STG}	Storage Temperature		-40 ~ 125	°C
V _{ISO}	Isolation Voltage	60 Hz, Sinusoidal, 1 minute, Connection Pins to Heatsink	1500	V _{rms}

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- For the Measurement Point of Case Temperature T_C, Please refer to Figure 4.
- Calculation Value or Design Factor.
- Using continuously under heavy loads or excessive assembly conditions (e.g. the application of high temperature/ current/ voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/ current/ voltage, etc.) are within the absolute maximum ratings and the operating ranges.

FSB50825B/FSB50825BS

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Packing Type	Reel Size	Quantity
FSB50825B	FSB50825B	SPM5P-023	Rail	N/A	15
FSB50825BS	FSB50825BS	SPM5Q-023	Tape & Reel	330 mm	450

PIN DESCRIPTION

Pin No.	Pin Name	Pin Description
1	COM	IC Common Supply Ground
2	V _{B(U)}	Bias Voltage for U Phase High Side FRFET Driving
3	V _{DD(U)}	Bias Voltage for U Phase IC and Low Side FRFET Driving
4	IN _(UH)	Signal Input for U Phase High-side
5	IN _(UL)	Signal Input for U Phase Low-side
6	N.C	N.C
7	V _{B(V)}	Bias Voltage for V Phase High Side FRFET Driving
8	V _{DD(V)}	Bias Voltage for V Phase IC and Low Side FRFET Driving
9	IN _(VH)	Signal Input for V Phase High-side
10	IN _(VL)	Signal Input for V Phase Low-side
11	V _{TS}	Output for HVIC Temperature Sensing
12	V _{B(W)}	Bias Voltage for W Phase High Side FRFET Driving
13	V _{DD(W)}	Bias Voltage for W Phase IC and Low Side FRFET Driving
14	IN _(WH)	Signal Input for W Phase High-side
15	IN _(WL)	Signal Input for W Phase Low-side
16	N.C	N.C
17	P	Positive DC-Link Input
18	U, V _{S(U)}	Output for U Phase & Bias Voltage Ground for High Side FRFET Driving
19	N _U	Negative DC-Link Input for U Phase
20	N _V	Negative DC-Link Input for V Phase
21	V, V _{S(V)}	Output for V Phase & Bias Voltage Ground for High Side FRFET Driving
22	N _W	Negative DC-Link Input for W Phase
23	W, V _{S(W)}	Output for W Phase & Bias Voltage Ground for High Side FRFET Driving

FSB50825B/FSB50825BS

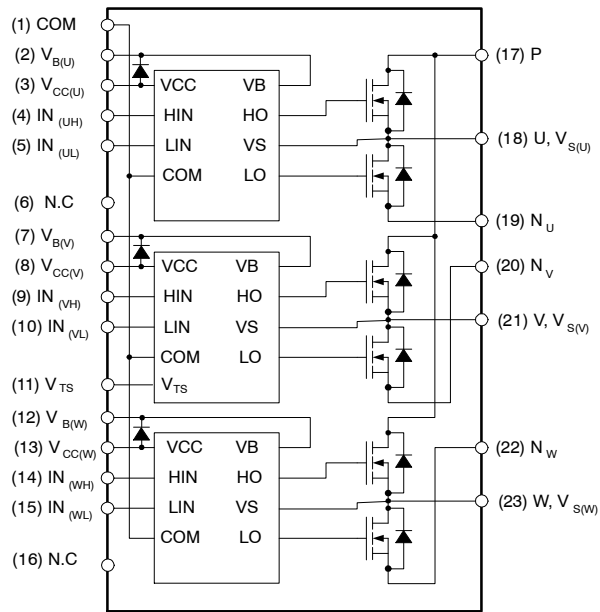


Figure 1. Pin Configuration and Internal Block Diagram (Bottom View)

NOTE: 4. Source Terminal of Each Low-Side MOSFET is Not Connected to Supply Ground or Bias Voltage Ground Inside Motion SPM 5 product. External Connections Should be Made as Indicated in Figure 3

FSB50825B/FSB50825BS

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, $V_{DD} = V_{BS} = 15\text{ V}$ Unless Otherwise Specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
--------	-----------	-----------------	------	------	------	------

INVERTER PART (Each MOSFET Unless Otherwise Specified)

BV _{DSS}	Drain-Source Breakdown Voltage	V _{IN} = 0 V, I _D = 1 mA (Note 5)	250	–	–	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{IN} = 0 V, V _{DS} = 250 V	–	–	1	mA
R _{DS(on)}	Static Drain-Source On-Resistance	V _{DD} = V _{BS} = 15 V, V _{IN} = 5 V, I _D = 2 A	–	0.37	0.55	Ω
V _{SD}	Drain-Source Diode Forward Voltage	V _{DD} = V _{BS} = 15 V, V _{IN} = 0 V, I _D = –2 A	–	–	1.1	V
t _{ON}	Switching Times	V _{PN} = 150 V, V _{DD} = V _{BS} = 15 V, I _D = 2 A ON / OFF R _G = 800 Ω / 200 Ω V _{IN} = 0 V ↔ 5 V, Inductive Load L = 3 mH High and Low-Side MOSFET Switching (Note 6)	–	330	–	ns
t _{OFF}			–	530	–	ns
t _{rr}			–	100	–	ns
E _{ON}			–	40	–	μJ
E _{OFF}			–	15	–	μJ
RBSOA	Reverse-Bias Safe Operating Area	V _{PN} = 200 V, V _{DD} = V _{BS} = 15 V, I _D = I _{DR} , V _{DS} = BV _{DSS} , T _J = 150°C High- and Low-Side MOSFET Switching (Note 7)	Full Square			

CONTROL PART (Each HVIC Unless Otherwise Specified)

I _{QDD}	Quiescent V _{DD} Current	V _{DD} = 15 V, V _{IN} = 0 V	Applied Between V _{DD} and COM	–	–	200	μA
I _{QBS}	Quiescent V _{BS} Current	V _{BS} = 15 V, V _{IN} = 0 V	Applied Between V _{B(U)-U} , V _{B(V)-V} , V _{B(W)-W}	–	–	100	μA
I _{PDD}	Operating V _{DD} Supply Current	V _{DD} – COM	V _{DD} = 15 V, f _{PWM} = 20 kHz, duty = 50%, Applied to One PWM Signal Input for Low-Side			900	μA
I _{PBS}	Operating V _{BS} Supply Current	V _{B(U) – VS(U)} , V _{B(V) – VS(V)} , V _{B(W) – VS(W)}	V _{DD} = V _{BS} = 15 V, f _{PWM} = 20 kHz, Duty = 50%, Applied to One PWM Signal Input for High-Side			800	μA
UV _{DDD}	Low-Side Undervoltage Protection (Figure 8)	V _{DD} Undervoltage Protection Detection Level		7.4	8.0	9.4	V
UV _{DDR}		V _{DD} Undervoltage Protection Reset Level		8.0	8.9	9.8	V
UV _{BSD}	High-Side Undervoltage Protection (Figure 9)	V _{BS} Undervoltage Protection Detection Level		7.4	8.0	9.4	V
UV _{BSR}		V _{BS} Undervoltage Protection Reset Level		8.0	8.9	9.8	V
V _{TS}	HVIC Temperature sensing voltage output	V _{DD} = 15 V, T _{HVIC} = 25°C (Note 8)		600	790	980	mV
V _{IH}	ON Threshold Voltage	Logic High Level	Applied between IN and COM	–	–	2.9	V
V _{IL}	OFF Threshold Voltage	Logic Low Level		0.8	–	–	V

FSB50825B/FSB50825BS

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, $V_{DD} = V_{BS} = 15\text{ V}$ Unless Otherwise Specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
--------	-----------	-----------------	------	------	------	------

BOOTSTRAP DIODE PART (Each Bootstrap Diode Unless Otherwise Specified)

V_{FB}	Forward Voltage	$I_F = 0.1\text{ A}$, $T_C = 25^\circ\text{C}$ (Note 9)	–	2.5	–	V
t_{rrB}	Reverse Recovery Time	$I_F = 0.1\text{ A}$, $T_C = 25^\circ\text{C}$	–	80	–	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

FSB50825B/FSB50825BS

RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{PN}	Supply Voltage	Applied Between P and N	–	150	200	V
V_{DD}	Control Supply Voltage	Applied Between V_{DD} and COM	13.5	15	16.5	V
V_{BS}	High-Side Bias Voltage	Applied Between V_B and V_S	13.5	15	16.5	V
$V_{IN(ON)}$	Input ON Threshold Voltage	Applied Between IN and COM	3.0	–	V_{DD}	V
$V_{IN(OFF)}$	Input OFF Threshold Voltage		0	–	0.6	V
t_{dead}	Blanking Time for Preventing Arm-Short	$V_{DD} = V_{BS} = 13.5 \sim 16.5 \text{ V}$, $T_J \leq 150^\circ\text{C}$	1.0	–	–	μS
f_{PWM}	PWM Switching Frequency	$T_J \leq 150^\circ\text{C}$	–	15	–	kHz

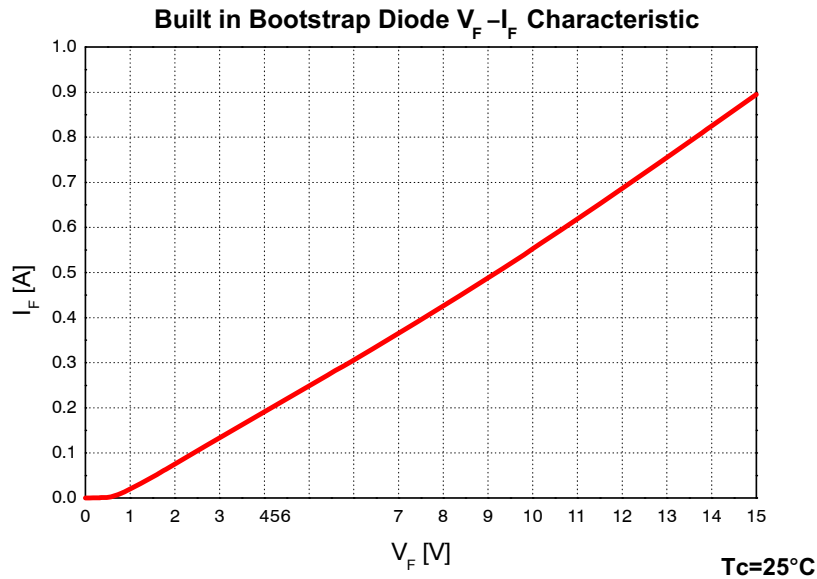


Figure 2. Built in Bootstrap Diode Characteristics (Typ.)

- NOTE:
5. BV_{DSS} is the Absolute Maximum Voltage Rating Between Drain and Source Terminal of Each MOSFET Inside Motion SPM 5 product. V_{PN} Should be Sufficiently Less Than This Value Considering the Effect of the Stray Inductance so that V_{DS} Should Not Exceed BV_{DSS} in Any Case.
 6. t_{ON} and t_{OFF} Include the Propagation Delay Time of the Internal Drive IC. Listed Values are Measured at the Laboratory Test Condition, and They Can be Different According to the Field Applications Due to the Effect of Different Printed Circuit Boards and Wirings. Please see Figure 6 for the Switching Time Definition with the Switching Test Circuit of Figure 7.
 7. The peak current and voltage of each MOSFET during the switching operation should be included in the Safe Operating Area (SOA). Please see Figure 7 for the RBSOA test circuit that is same as the switching test circuit.
 8. V_{TS} is only for sensing temperature of module and cannot shutdown MOSFETs automatically.
 9. Built in bootstrap diode includes around 15 Ω resistance characteristic. Please refer to Figure 2.

FSB50825B/FSB50825BS

These values depend on PWM control algorithm

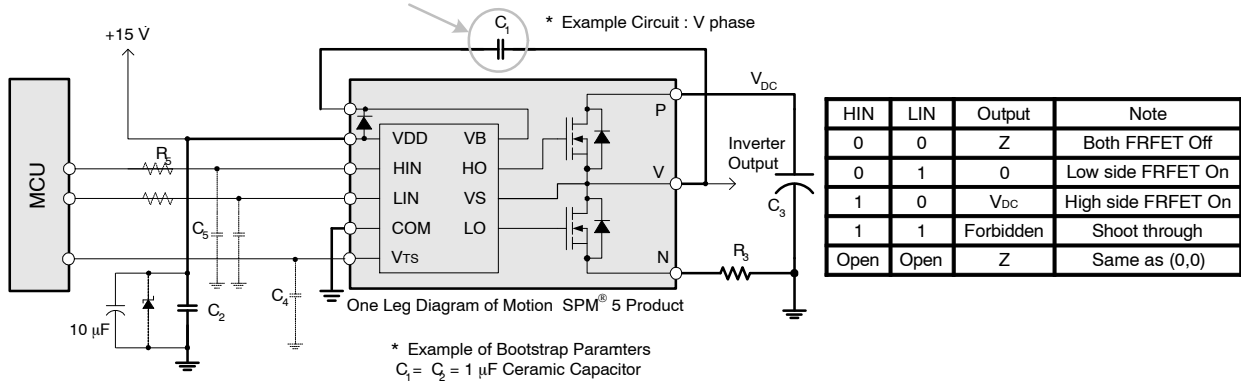


Figure 3. Recommended MCU Interface and Bootstrap Circuit with Parameters

- NOTE: 10. Parameters for bootstrap circuit elements are dependent on PWM algorithm. For 15 kHz of switching frequency, typical example of parameters is shown above.
11. RC-coupling (R₅ and C₅) and C₄ at each input of Motion SPM 5 product and MCU (Indicated as Dotted Lines) may be used to prevent improper signal due to surge-noise.
12. Bold lines should be short and thick in PCB pattern to have small stray inductance of circuit, which results in the reduction of surge-voltage. Bypass capacitors such as C₁, C₂ and C₃ should have good high-frequency characteristics to absorb high-frequency ripple-current.

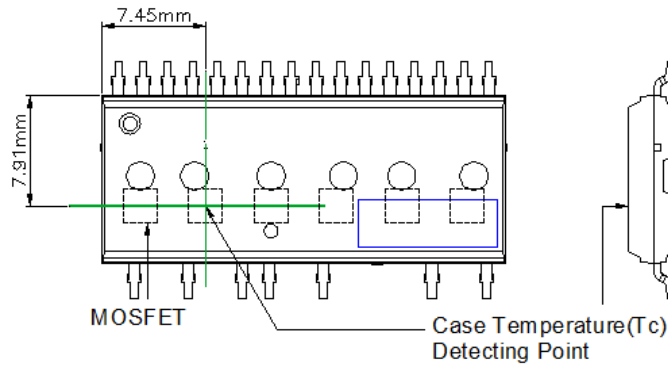


Figure 4. Case Temperature Measurement

- NOTE: 13. Attach the thermocouple on top of the heat-sink of SPM 5 package (between SPM 5 package and heatsink if applied) to get the correct temperature measurement.

FSB50825B/FSB50825BS

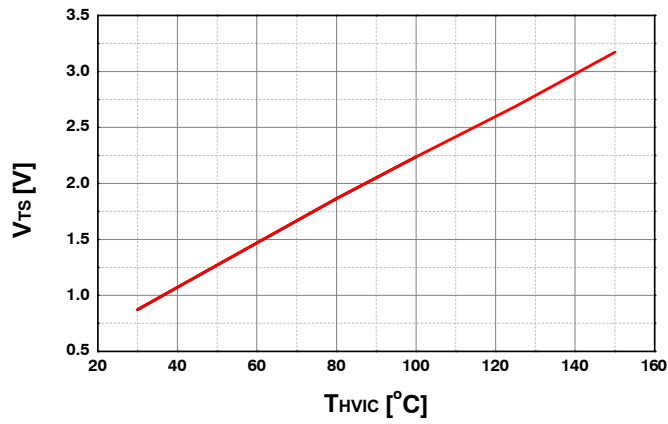


Figure 5. Temperature Profile of V_{TS} (Typical)

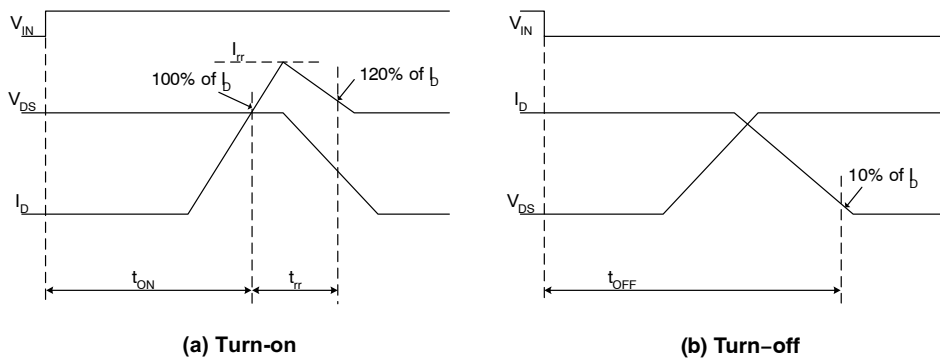


Figure 6. Switching Time Definitions

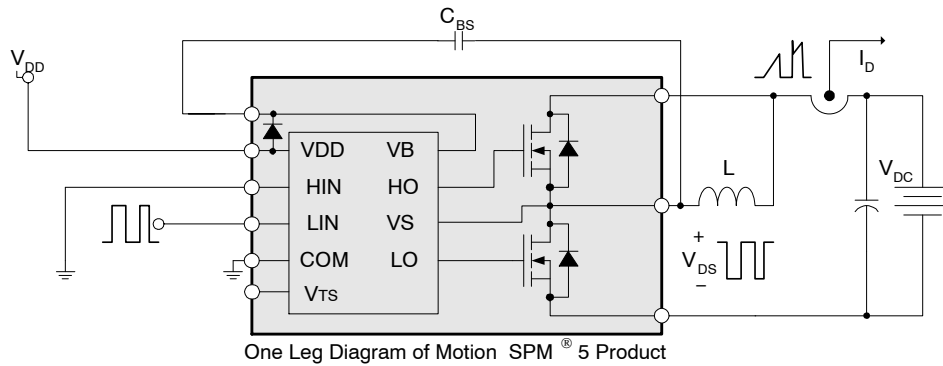


Figure 7. Switching and RBSOA (Single-Pulse) Test Circuit (Low-side)

FSB50825B/FSB50825BS

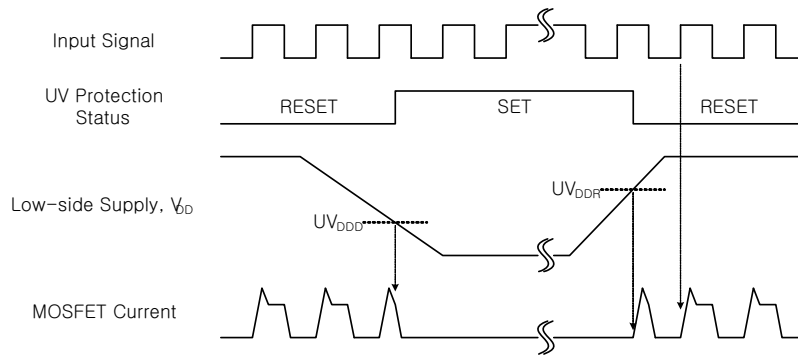


Figure 8. Under-Voltage Protection (Low-Side)

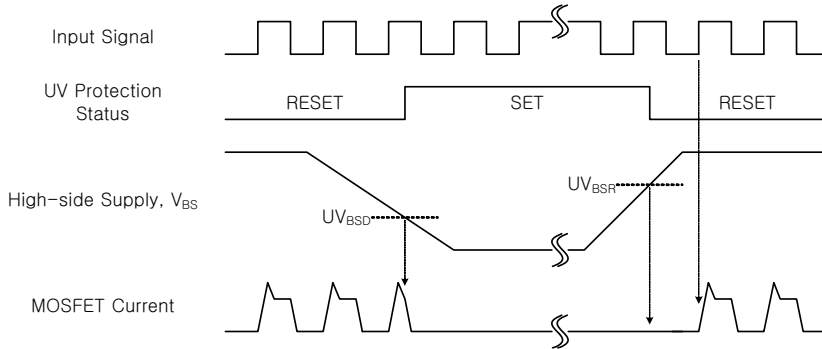


Figure 9. Under-Voltage Protection (High-Side)

FSB50825B/FSB50825BS

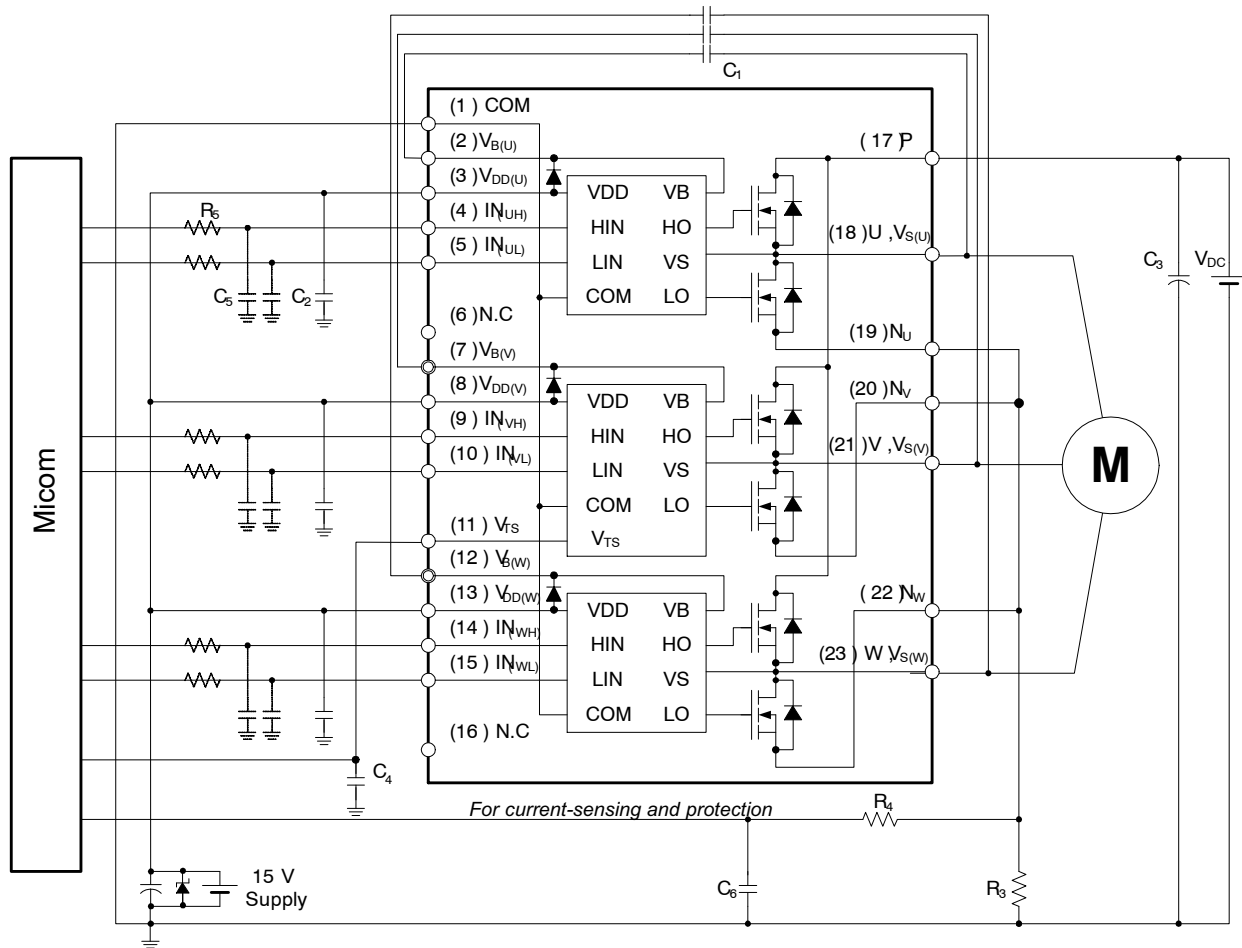


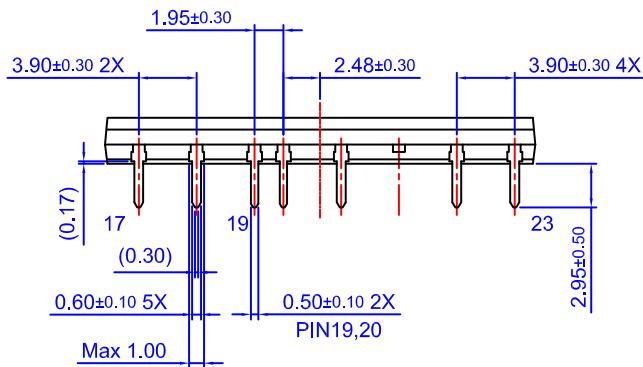
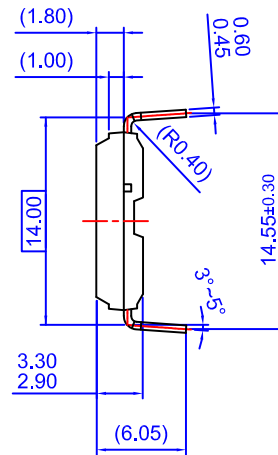
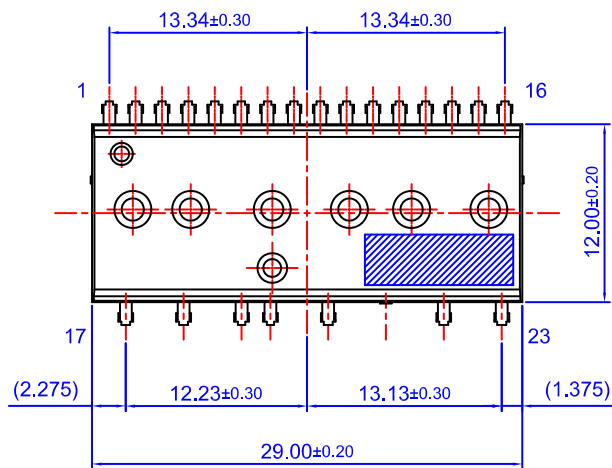
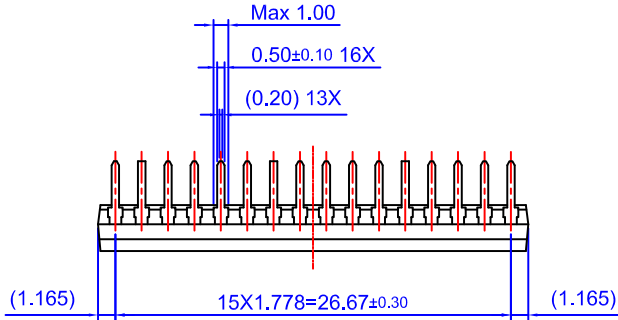
Figure 10. Example of Application Circuit

- NOTE:
14. About pin position, refer to Figure 1.
 15. RC-coupling (R_5 and C_5 , R_4 and C_6) and C_4 at each input of Motion SPM 5 product and MCU are useful to prevent improper input signal caused by surge-noise.
 16. The voltage-drop across R_3 affects the low-side switching performance and the bootstrap characteristics since it is placed between COM and the source terminal of the low-side MOSFET. For this reason, the voltage-drop across R_3 should be less than 1 V in the steady-state.
 17. Ground-wires and output terminals, should be thick and short in order to avoid surge-voltage and malfunction of HVIC.
 18. All the filter capacitors should be connected close to Motion SPM 5 product, and they should have good characteristics for rejecting high-frequency ripple current.

FSB50825B/FSB50825BS

PACKAGE DIMENSIONS

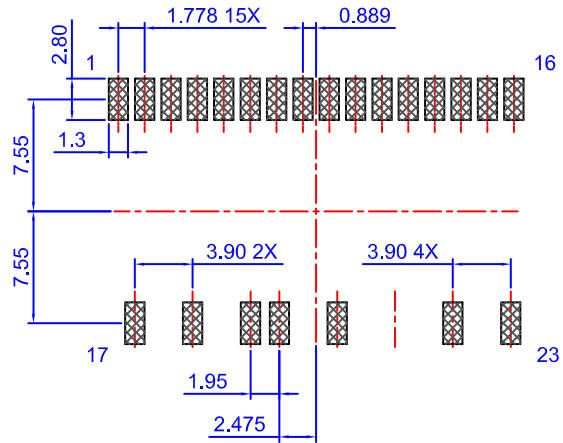
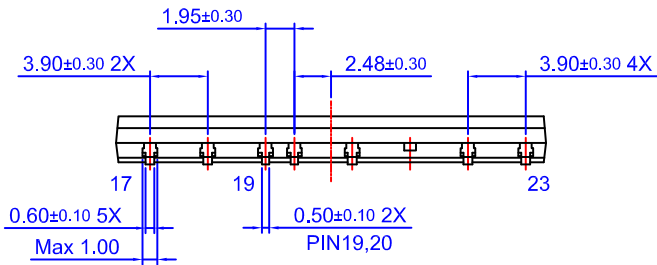
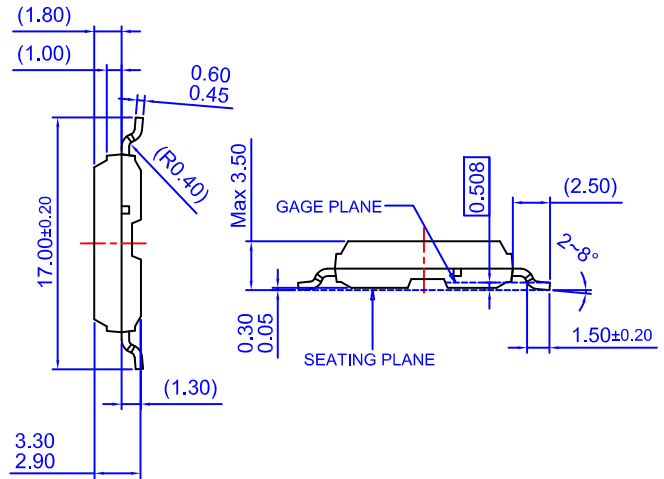
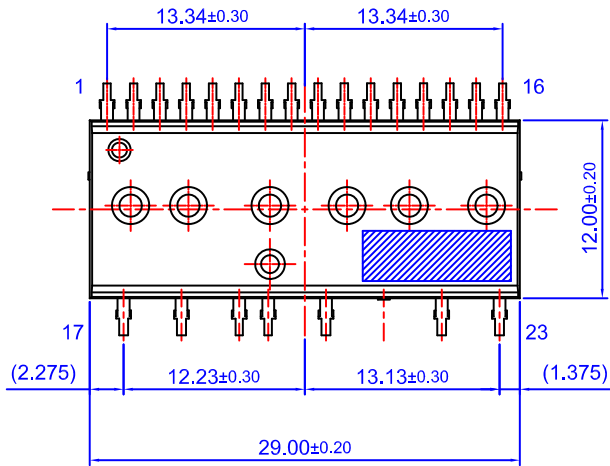
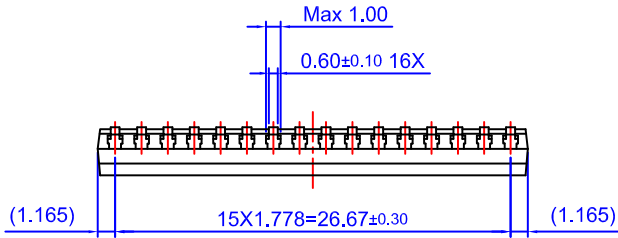
SPM5E-023 / 23LD, PDD STD, FULL PACK, DIP TYPE
CASE MODE J
ISSUE O



- NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
B) ALL DIMENSIONS ARE IN MILLIMETERS
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D) () IS REFERENCE

FSB50825B/FSB50825BS


SPM5H-023 / 23LD, PDD STD, SPM23-BD (Ver1.5) SMD TYPE
CASE MODEM
ISSUE O



- NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
B) ALL DIMENSIONS ARE IN MILLIMETERS
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D) () IS REFERENCE

LAND PATTERN RECOMMENDATIONS

SPM is a registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative