Product Change Notification - SYST-26RJWS405

Date:
29 Mar 2019
Product Category:
8-bit Microcontrollers
Affected CPNs:

Notification subject:
ERRATA - PIC18(L)F26/45/46/55/56K42 Silicon Errata and Data Sheet Clarification
Notification text:
SYST-26RJWS405
Microchip has released a new DeviceDoc for the PIC18(L)F26/45/46/55/56K42 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at PIC18(L)F26/45/46/55/56K42 Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change:
1) Added silicone rev A3
2) Updated Module 5.1
3) Added sections 4.3, 8.3 and 9.1.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Estimated First Ship Date: 29 March 2019
NOTE: Please be advised that after the estimated first ship date customers may receive pre and post change parts.

Markings to Distinguish Revised from Unrevised Devices: Traceability Code
Attachment(s):
PIC18(L)F26/45/46/55/56K42 Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

PIC18F26K42-E/ML
PIC18F26K42-E/MX
PIC18F26K42-E/SO
PIC18F26K42-E/SP
PIC18F26K42-E/SS
PIC18F26K42-I/ML
PIC18F26K42-I/MX
PIC18F26K42-I/SO
PIC18F26K42-I/SP
PIC18F26K42-I/SS
PIC18F26K42T-I/ML
PIC18F26K42T-I/MX
PIC18F26K42T-I/SO
PIC18F26K42T-I/SS
PIC18F45K42-E/ML
PIC18F45K42-E/MV
PIC18F45K42-E/MVV01
PIC18F45K42-E/P
PIC18F45K42-E/PT
PIC18F45K42-I/ML
PIC18F45K42-I/MV
PIC18F45K42-I/P
PIC18F45K42-I/PT
PIC18F45K42T-E/MVV01
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PIC18(L)F26/45/46/55/56K42 Family Silicon Errata and Data Sheet Clarification

The PIC18(L)F26/45/46/55/56K42 family devices that you have received conform functionally to the current Device Data Sheet (DS40001919**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18(L)F26/45/46/55/56K42 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A3**).

Data Sheet clarifications and corrections start on page 7, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVID/REVID values for the various PIC18(L)F26/45/46/55/56K42 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID<13:0>(1), (2)	Revision ID for Silicon Revision		
		A1	A2	A3
PIC18F26K42	6C60h	A001	A002	A003
PIC18F45K42	6C20h	A001	A002	A003
PIC18F46K42	6C00h	A001	A002	A003
PIC18F55K42	6BC0h	A001	A002	A003
PIC18F56K42	6BA0h	A001	A002	A003
PIC18LF26K42	6DA0h	A001	A002	A003
PIC18LF45K42	6D60h	A001	A002	A003
PIC18LF46K42	6D40h	A001	A002	A003
PIC18LF55K42	6D00h	A001	A002	A003
PIC18LF56K42	6CE0h	A001	A002	A003

Note 1: The Revision ID is located in addresses 3FFFFCh-3FFFFDh and Device ID is located in addresses 3FFFFEh-3FFFFFh.

2: Refer to the *"PIC18(L)F26/45/46/55/56K42 Memory Programming Specification"* (DS40001886) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item No.	Issue Summary	Affected Revisions(1)		
				A1	A2	A3
Electrical Specifications	SMBus 2.0	1.1	SMBus 2.0 logic levels.	X		
	SMBus 3.0	1.2	SMBus 3.0 logic levels.	X	X	X
	Min VDD Specification for LF Devices	1.3	NVM access on LF devices may not work properly at specified voltage levels and temperatures.	X	X	X
Signal Measurement Timer (SMT)	MFINTOSC Clock Sources into SMT	2.1	MFINTOSC clock sources into the SMT are not functional.	X	X	X
Direct Memory Access (DMA)	DMA Reads from Data EEPROM	3.1	DMA reads from Data EEPROM does not operate.	X		
	DMA in Doze mode	3.2	DMA transfers may not work when CPU is in Doze mode.	X	X	
Universal Asynchronous Receiver Transmitter (UART)	BRGS Select	4.1	BRGS Select feature not functional in DALI mode.		X	X
	Stop Bit Interrupt Flag	4.2	Stop Bit interrupt flag functionality not available.	X		
	Autobaud	4.3	The first character after autobaud may be corrupted.	X	X	X
Nonvolatile Memory (NVM) Control	WRERR Bit Functionality	5.1	WRERR bit cannot be cleared in hardware after being set once.	X	X	
Windowed Watchdog Timer (WWDT)	WWDT Operation in Doze mode	6.1	Window violation occurs when WWDT operated in Doze mode.	X	X	
Power-Saving Operation Modes	Low-Power Sleep mode	7.1	Low-power Sleep mode does not operate at 3.1v<VDD<3.3v.	X	X	
Analog-to-Digital Converter with Computation (ADC2)	ADC Conversion	8.1	The 12-bit ADC shorts briefly at the beginning of the ADC conversion stage.	X		
	Burst Average mode Double Sampling	8.2	The ADC^2 does not trigger the second conversion when operated in non-continuous double-sampling Burst Average mode.	X	X	
	ADC Conversion in FOSC mode	8.3	ADC does not complete conversion successfully in FOSC mode.	X	X	
Instruction Set	MOVFF/MOVSF Instruction	9.1	MOVFF/MOVSF may corrupt destination.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A2**).

1. Module: Electrical Specifications

1.1 SMBus 2.0

The SMBus 2.0 VIL specification (Parameter D304) at 125°C is 0.7V.

Work around

None.

Affected Silicon Revisions

A1	A2	A3					
X							

1.2 SMBus 3.0

The SMBus 3.0 VIL specification (Parameter D305) is temperature and VDD dependent. Refer to the table below.

Temperature	VDD	D305 SMBus 3.0 VIL Specification
-40°C	1.8V	0.6V
-40°C	5.5V	0.8V
25°C	1.8V	0.6V
25°C	5.5V	0.8V
85°C	1.8V	0.6V
85°C	5.5V	0.7V
125°C	1.8V	0.5V
125°C	5.5V	0.7V

Work around

None.

Affected Silicon Revisions

A1	A2	A3					
X	X	X					

1.3 Min VDD Specification for LF Devices for A3 Rev

V_{DDMIN} for LF devices has changed for temperatures below +25°C as shown below in **bold**.

PIC18LF26/45/46/55/56K42			Standard Operating Conditions (unless otherwise stated)				
PIC18F26/45/46/55/56K42							
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
Supply Voltage							
D002	VDD		**2.0** 1.8 2.5 2.7	— — — —	3.6 3.6 3.6 3.6	V V V V	FOSC ≤ 16 MHz **(-40°C to <+25°C)** FOSC ≤ 16 MHz **(≥+25°C to +125°C)** FOSC > 16 MHz and FOSC ≤ 32 MHz FOSC > 32 MHz
D002	VDD		2.3 2.5 2.7	— — —	5.5 5.5 5.5	V V V	FOSC ≤ 16 MHz FOSC > 16 MHz and FOSC ≤ 32 MHz FOSC > 32 MHz

Work around

None.

Affected Silicon Revisions

A1	A2	A3					
X	X	X					

2. Module: Signal Measurement Timer (SMT)

2.1 MFINTOSC Clock Sources into SMT

The Signal Measurement Timer does not operate when MFINTOSC is selected as the clock source (i.e. CSEL = 0b100 and 0b101).

Work around

The MFINTOSC does not start up automatically. User software needs to manually enable the MFINTOSC by setting the MFOEN bit in the OSCCEN register. The MFINTOSC will remain enabled as long as MFOEN bit is set.

Affected Silicon Revisions

A1	A2	A3					
X	X	X					

3. Module: Direct Memory Access (DMA)

3.1 DMA Reads from Data EEPROM

The DMA modules do not operate when configured to access the Data EEPROM (i.e., SMR<1:0> = 1x). The destination gets written to 0x00.

Work around

None. NVMCON reads work as described.

Affected Silicon Revisions

A1	A2	A3					
X							

3.2 DMA in Doze Mode

When the CPU is operated in Doze mode, DMA transfers may not work as expected.

Work around

None.

Affected Silicon Revisions

A1	A2	A3					
X	X						

4. Module: Universal Asynchronous Receiver Transmitter (UART)

4.1 Baud Rate Generator Speed Select

The Baud Rate Generator Speed Select feature (BRGS bit in the UxCON0 register) in DALI mode is not functional. The Baud Rate Generator always operates at normal speed with 16 baud clocks per bit in DALI mode.

Work around

When using UART in DALI mode, operate the Baud Rate Generator in normal speed (BRGS = 0) only and use the following formula to calculate the UxBRGH:L register value:

$$UxBRGH:L = \frac{FOSC}{16 \times Desired\ Baud\ Rate} - 1$$

Example: To obtain the desired baud rate of 1200 at FOSC = 64 MHz,

$$UxBRGH:L = \frac{64,000,000}{16 \times 1200} - 1 = 3332$$

Affected Silicon Revisions

A1	A2	A3					
	X	X					

4.2 Stop Bit Interrupt Flag

Stop Bit Interrupt flag functionality is not available in the CERIF bit in revision A1.

Work around

Use Timer2 with HLT and connect the UART RX port to the timer Reset trigger. Set the time-out period to the desired Stop bit time (for DALI mode, this is equivalent to two Stop bits at 1200 baud = 1.66 ms). When the Stop bit is received, the timer times out notifying end of data.

Affected Silicon Revisions

A1	A2	A3					
X							

4.3 Autobaud

When the UART is configured as follows, then the first character received after autobaud may be corrupted.

- The UBRG registers are cleared.
- The BRGS bit is set (fast baud rate mode).
- The Stop bits are configured for two Stop bits (STP = 0b1x).

Work around

a) In asynchronous modes other than LIN: the transmitter should delay the first character by at least one character period after sending auto-baud.

b) In all asynchronous modes including LIN: Clear the BRGS bit to select the normal baud rate mode.

Affected Silicon Revisions

A1	A2	A3					
X	X	X					

5. Module: Nonvolatile Memory (NVM) Control

5.1 WRERR Bit Functionality

When a Reset is issued while an NVM high-voltage operation is in progress, the WRERR bit in the NVMCON1 register is set as expected. After clearing the WRERR bit, if a Reset reoccurs, the WRERR bit is set again regardless of whether an NVM operation is in progress or not. A successful write operation will clear the WRERR condition.

Work around

None.

Affected Silicon Revisions

A1	A2	A3					
X	X						

6. Module: Windowed Watchdog Timer (WWDT)

6.1 WWDT Operation in Doze Mode

When the CLRWDT instruction is issued in Doze mode, a window violation error occurs in WWDT even though the window is open and armed.

Work around

Do not operate the WWDT in Doze mode.

Affected Silicon Revisions

A1	A2	A3					
X	X						

7. Module: Power-Saving Operation Modes

7.1 Low-Power Sleep Mode in F Devices

The F device resets when waking up from Sleep while in Low-Power mode (VREGPM = 1 in VREGCON register) at 3.1V < VDD < 3.3V.

Work around

c) If wake-up from Sleep is needed at 3.1V < VDD < 3.3V, operate the F device in Normal Power mode (VREGPM = 0).

d) If wake-up from Sleep is needed at 3.1V < VDD < 3.3V, enable the Fixed Voltage Reference (EN = 1 in FVRCON register). This increases the current in Sleep mode by typically 7 µA.

Affected Silicon Revisions

A1	A2	A3					
X	X						

8. Module: Analog-to-Digital Converter with Computation (ADC^2)

8.1 ADC Conversion

At the very beginning of the ADC conversion, the input signal may briefly be pulled to ground, which in turn may take some charge out of the internal sample and hold capacitor. The problem is more pronounced on inputs with an impedance greater than 1K ohm.

This issue will be seen when sampling the following internal channel inputs: FVR, DAC, and Temperature Indicator and when sampling external sources on an analog pin, including the CVD.

Work around

a) When sampling the internal channel inputs, FVR, DAC, and Temperature Indicator, increase the minimum TAD time to 4 µs to increase accuracy.

b) When sampling an external source through an analog pin, keep the input impedance below 1K ohm.

c) When using the ADC in CVD mode, there is no work around.

Affected Silicon Revisions

A1	A2	A3					
X							

8.2 Burst Average Mode Double Sampling

When the ADC^2 is operated in Burst Average mode (MD = 0b011 in ADCON2 register) while enabling non-continuous operation and double-sampling (CONT = 0 in the ADCON0 register and DSEN = 1 in the ADCON1 register), the value in the ADCNT register does not increment beyond 0b1 toward the value in the ADRPT register.

Work around

When operating the ADC^2 in Burst Average mode with double-sampling, enable continuous operation of the module (CONT = 1 in the ADCON0 register) and set the stop-on-interrupt bit (SOI bit in the ADCON3 register). After the interrupt occurs, perform appropriate threshold calculations in the software and retrigger ADC^2 as necessary.

If the CPU is in Low-Power Sleep mode, alternatively the ADC^2 in non-continuous Burst Average mode can be operated with single ADC conversion (DSEN = 0 in the ADCON1 register) compromising noise immunity for lower power consumption by preventing the device from waking up to perform threshold calculations in the software.

Affected Silicon Revisions

A1	A2	A3					
X	X						

8.3 ADC Conversion in Fosc Mode

The ADCON0.GO bit remains set and the conversion does not complete successfully when configured to operate in FOSC mode (ADCON0.CS=0) with FOSC > 40 MHz.

Work around

Use ADCRC as the ADC clock source (ADCON0.CS=1).

Affected Silicon Revisions

A1	A2	A3					
X	X						

9. Module: Instruction Set

9.1 MOVFF/MOVSF Instruction

When the BSR points to the last bank of the SFR region (BSR=0x3F) and the low byte of the source or destination address of a MOVFF/MOVSF instruction equals the low byte of an indirect addressing operation register address (INDFx, POSTINCx, POSTDECx, PREINCx, PLUSWx), the operation will not be completed as expected. Either, one or more of the destination, FSR value, or location pointed to by the FSR will be corrupted, or the move will simply not occur.

Work around

Ensure that the BSR does not point to the last bank if the SFR region (BSR=0x3F) when MOVFF/MOVSF instruction is being executed.

Affected Silicon Revisions

A1	A2	A3					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001919**C**):

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev F Document (3/2019)

Added silicone rev. A3. Updated Module 5.1. Added sections 4.3, 8.3 and 9.1.

Rev E Document (11/2018)

Updated Modules 3.1 and 4.1.

Data Sheet Clarifications: Deleted Module 1: Electrical Specifications.

Rev D Document (9/2018)

Updated Table 2. Updated Item 8.1.

Rev C Document (06/2018)

Updated Table 1 and Table 2; Added Module 4: UART; Module 3.2; Module 5: NVM Control; Module 6: WWDT; Module 7: Power-Saving Operation Modes; Added Module 8: ADC

Data Sheet Clarifications: Added Module 1: Electrical Specifications.

Other minor corrections.

Rev B Document (10/2017)

Added Module 3: DMA to Silicon Errata Issues. Other minor corrections.

Rev A Document (06/2017)

Initial release of this document.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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