# Product Change Notification - SYST-04NMLU519

**Date:**
08 Apr 2019
**Product Category:**
USB Hubs
**Affected CPNs:**

**Notification subject:**
ERRATA - USB251xB/xBi Family Silicon Errata
**Notification text:**
SYST-04NMLU519
Microchip has released a new DeviceDoc for the USB251xB/xBi Family Silicon Errata of devices. If you are using one of these devices please read the document located at USB251xB/xBi Family Silicon Errata.

**Notification Status:** Final

**Description of Change:**
1) Added new errata module “Detach detection failure”.
2) Updated layout to standard Microchip format.

**Impacts to Data Sheet:** None

**Reason for Change:** To Improve Productivity

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 8 Apr 2019

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

**Markings to Distinguish Revised from Unrevised Devices:** N/A
**Attachment(s):**
USB251xB/xBi Family Silicon Errata

Please contact your local Microchip sales office with questions or concerns regarding this notification.

**Terms and Conditions:**

If you wish to receive Microchip PCNs via email please register for our PCN email service at our PCN home page select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the PCN FAQ section.
If you wish to change your PCN profile, including opt out, please go to the PCN home page select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Affected Catalog Part Numbers (CPN)

USB2512B-AEZG
USB2512B-AEZG-BYC
USB2512B-AEZG-TR
USB2512B-I/M2
USB2512B/M2
USB2512BI-AEZG
USB2512BI-AEZG-TR
USB2512BT-I/M2
USB2512BT/M2
USB2513B-AEZC
USB2513B-AEZC-TR
USB2513B-AEZG
USB2513B-AEZG-TR
USB2513B-AEZG-TR-CD0
USB2513B-I/M2
USB2513B/M2
USB2513BI-AEZG
USB2513BI-AEZG-TR
USB2513BT-I/M2
USB2513BT/M2
USB2514B-AEZC
USB2514B-AEZC-TR
USB2514B-AEZG
USB2514B-AEZG-TR
USB2514B-I/M2
USB2514B/M2
USB2514BI-AEZG
USB2514BI-AEZG-TR
USB2514BT-I/M2
USB2514BT/M2

# MIC5800/1

## 4/8-Bit Parallel-Input Latched Drivers

### Features

- 4.4 MHz Minimum Data Input Rate
- High-Voltage, High-Current Sink Outputs
- Output Transient Protection
- CMOS, PMOS, NMOS, and TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches

### General Description

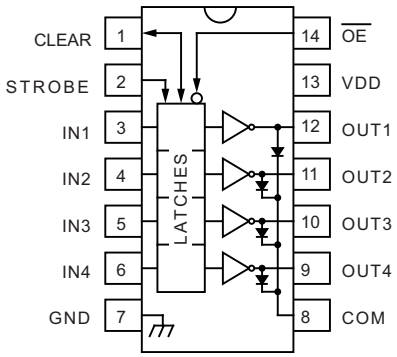
The MIC5800 and MIC5801 latched drivers are high-voltage, high-current integrated circuits comprised of four or eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions.

The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility. MIC5800 contains four latched drivers; MIC5801 contains eight latched drivers.

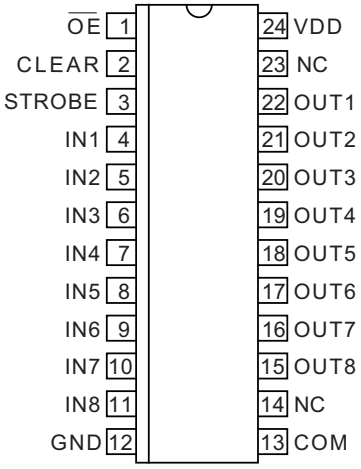
Data input rates are greatly improved in these devices. With a 5V supply, they will typically operate at better than 5 MHz. With a 12V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors. The bipolar outputs are suitable for use with relays, solenoids, stepping motors, LED or incandescent displays, and other high-power loads. Both units have open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 500 mA and will sustain at least 50V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be connected in parallel for higher load current capability.

### Package Types

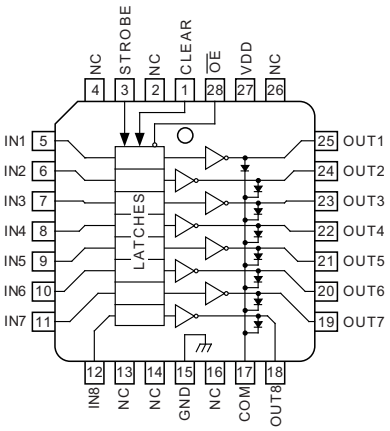
**MIC5800YM**
14-Lead SOIC (M)
(Top View)



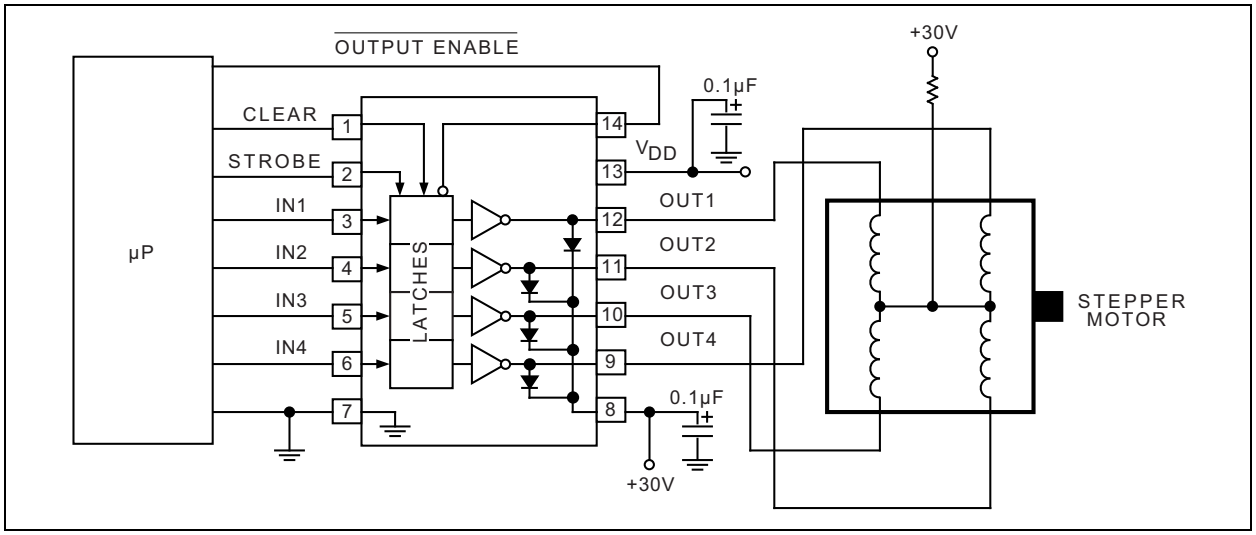

**MIC5801YWM**
24-Lead SOIC (WM)
(Top View)



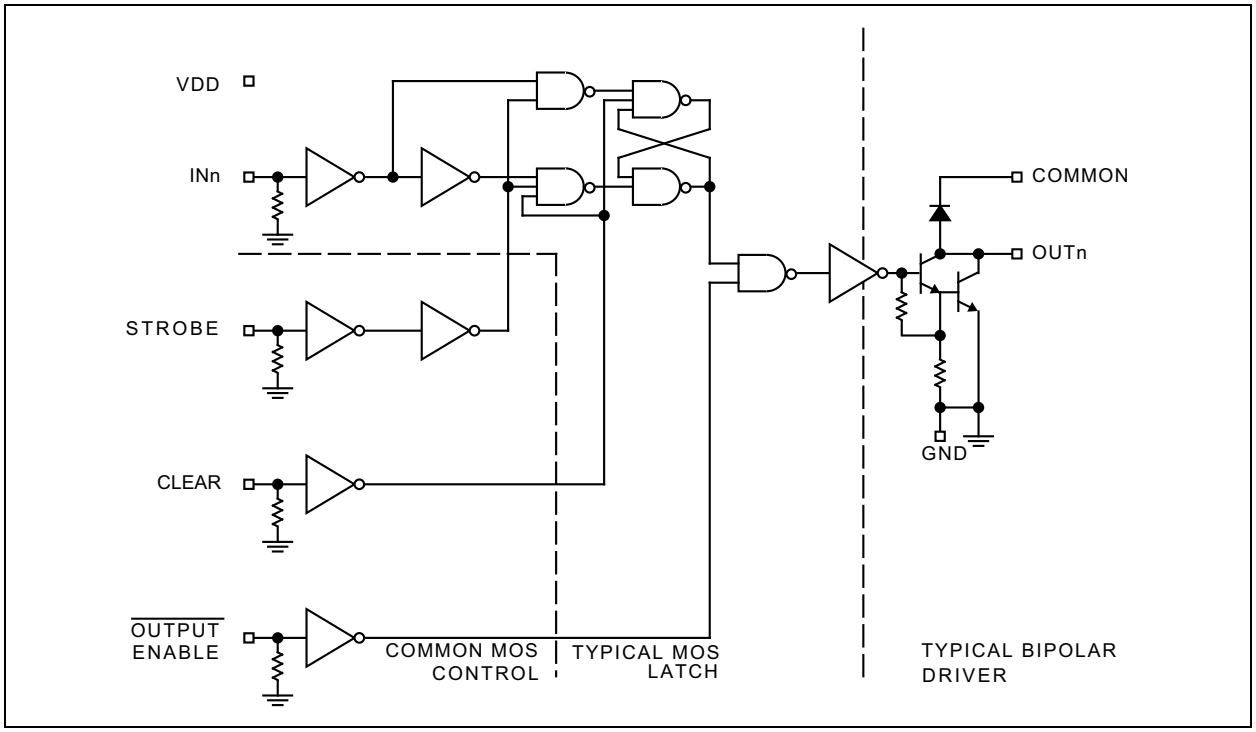

**MIC5801YV**
28-Lead PLCC (V)
(Top View)



## Typical Application Circuit




## Functional Block Diagram



# 1.0 ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings †

Output Voltage ($V_{CE}$) ..... +50V
Supply Voltage ($V_{DD}$) ..... +15V
Input Voltage Range ($V_{IN}$) ..... –0.3V to $V_{DD}$ + 0.3V
Continuous Collector Current ($I_C$) ..... 500 mA
ESD Rating (Note 1) ..... ESD Sensitive

## Operating Ratings ††

Package Power Dissipation ($P_D$)
MIC5800 SOIC ..... 1.0W
Derate above $T_A$ = +25°C ..... 8.5 mW/°C
MIC5801 PLCC ..... 2.25W
Derate above $T_A$ = +25°C ..... 18.2 mW/°C
MIC5801 Wide SOIC ..... 1.4W
Derate above $T_A$ = +25°C ..... 11 mW/°C

**† Notice:** Exceeding the absolute maximum ratings may damage the device.

**†† Notice:** The device is not guaranteed to function outside its operating ratings.

**Note 1:** Microchip CMOS devices have input-static protection, but are susceptible to damage when exposed to extremely high static electrical charges.

## ELECTRICAL CHARACTERISTICS

**Electrical Characteristics:** $V_{DD}$ = 5V, $T_A$ = +25°C, $V_A$ ≤ +85°C unless otherwise noted. Note 1

| Parameter | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Output Leakage Current | $I_{CEX}$ | — | — | 50 | µA | $V_{CE}$ = 50V, $T_A$ = +25°C |
| | | — | — | 100 | | $V_{CE}$ = 50V, $T_A$ = +70°C |
| Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$ | — | 0.9 | 1.1 | V | $I_C$ = 100 mA |
| | | — | 1.1 | 1.3 | | $I_C$ = 200 mA |
| | | — | 1.3 | 1.6 | | $I_C$ = 350 mA, $V_{DD}$ = 7.0V |
| Input Voltage (Low) | $V_{IN(0)}$ | — | — | 1.0 | V | — |
| Input Voltage (High) | $V_{IN(1)}$ | 10.5 | — | — | V | $V_{DD}$ = 12V |
| | | 8.5 | — | — | | $V_{DD}$ = 10V |
| | | 3.5 | — | — | | $V_{DD}$ = 5V, Note 2 |
| Input Resistance | $R_{IN}$ | 50 | 200 | — | kΩ | $V_{DD}$ = 12V |
| | | 50 | 300 | — | | $V_{DD}$ = 10V |
| | | 50 | 600 | — | | $V_{DD}$ = 5V |
| Supply Current ON (Each Stage) | $I_{DD(ON)}$ | — | 1.0 | 2.0 | mA | $V_{DD}$ = 12V, Outputs Open |
| | | — | 0.9 | 1.7 | | $V_{DD}$ = 10V, Outputs Open |
| | | — | 0.7 | 1.0 | | $V_{DD}$ = 5V, Outputs Open |
| Supply Current OFF (Total) | $I_{DD(OFF)}$ | — | — | 200 | µA | $V_{DD}$ = 12V, Outputs Open, Inputs = 0V |
| | | — | 50 | 100 | | $V_{DD}$ = 5V, Outputs Open, Inputs = 0V |

**Note 1:** Specification for packaged product only.

**2:** Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure a minimum logic “1”.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

| **Electrical Characteristics:** $V_{DD}$ = 5V, $T_A$ = +25°C, $V_A \le$ +85°C unless otherwise noted. Note 1 | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Sym.** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| Clamp Diode Leakage Current | $I_R$ | — | — | 50 | µA | $V_R$ = 50V, $T_A$ = +25°C |
| | | — | — | 100 | | $V_R$ = 50V, $T_A$ = +70°C |
| Clamp Diode Forward Voltage | $V_F$ | — | 1.7 | 2.0 | V | $I_F$ = 350 mA |

**Note 1:** Specification for packaged product only.

**2:** Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure a minimum logic “1”.

## TRUTH TABLE

| **$IN_N$** | **Strobe** | **Clear** | **/OE** | **$OUT_N$** | |
|---|---|---|---|---|---|
| | | | | **t – 1** | **t** |
| 0 | 1 | 0 | 0 | X | OFF |
| 1 | 1 | 0 | 0 | X | ON |
| X | X | 1 | X | X | OFF |
| X | X | X | 1 | X | OFF |
| X | 0 | 0 | 0 | ON | ON |
| X | 0 | 0 | 0 | OFF | OFF |

**Legend:** X = Irrelevant; t – 1 = Previous output state; t = Present output state.

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high /OE will set all outputs to the off condition, regardless of any other input conditions. When the /OE is low, the outputs depend on the state of their respective latches.

## TEMPERATURE SPECIFICATIONS

| **Parameters** | **Sym.** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
|---|---|---|---|---|---|---|
| **Temperature Ranges** | | | | | | |
| Storage Temperature Range | $T_S$ | –65 | — | +125 | °C | — |
| Operating Temperature Range | $T_A$ | –40 | — | +85 | °C | — |

**Note 1:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., $T_A$, $T_J$, $\theta_{JA}$). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1 and Table 2-2.

**TABLE 2-1: MIC5800 PIN FUNCTION TABLE**

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | CLEAR | Resets all latches and turns all outputs OFF (open). |
| 2 | STROBE | Input strobe pin. Loads output latches when high. |
| 3, 4, 5, 6 | $IN_N$ | Parallel inputs, 1 through 4. |
| 7 | GND | Logic and Output Ground pin. |
| 8 | COM | Transient suppression diode common cathode pin. |
| 9, 10, 11, 12 | $OUT_N$ | Parallel outputs, 4 through 1. |
| 13 | VDD | Logic Supply Voltage. |
| 14 | /OE | Output Enable. When low, outputs are active. When high, outputs are inactive and device is reset from a fault condition. An undervoltage condition emulates a high OE input. |

**TABLE 2-2: MIC5801 PIN FUNCTION TABLE**

| Pin Number SOIC | Pin Number PLCC | Pin Name | Description |
|---|---|---|---|
| 1 | 28 | /OE | Output Enable. When low, outputs are active. When high, outputs are inactive and device is reset from a fault condition. An undervoltage condition emulates a high OE input. |
| 2 | 1 | CLEAR | Resets all latches and turns all outputs OFF (open). |
| 3 | 3 | STROBE | Input strobe pin. Loads output latches when high. |
| 4, 5, 6, 7, 8, 9, 10, 11 | 5, 6, 7, 8, 9, 10, 11, 12 | $IN_N$ | Parallel inputs, 1 through 8. |
| 12 | 15 | GND | Logic and Output Ground pin. |
| 13 | 17 | COM | Transient suppression diode common cathode pin. |
| 14, 23 | 2, 4, 13, 14, 16, 26 | NC | No Connection. Leave floating. |
| 15, 16, 17, 18, 19, 20, 21, 22 | 18, 19, 20, 21, 22, 23, 24, 25 | $OUT_N$ | Parallel outputs, 8 through 1. |
| 24 | 27 | VDD | Logic Supply Voltage. |

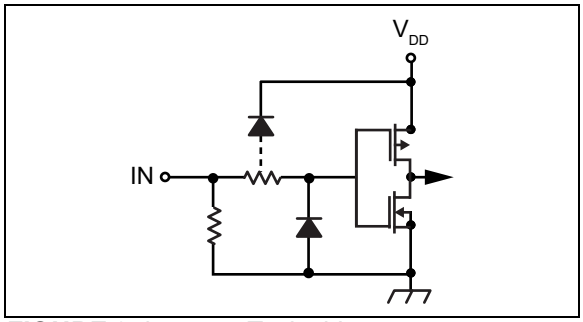



***FIGURE 2-1:*** *Typical Input.*

## 3.0 TIMING

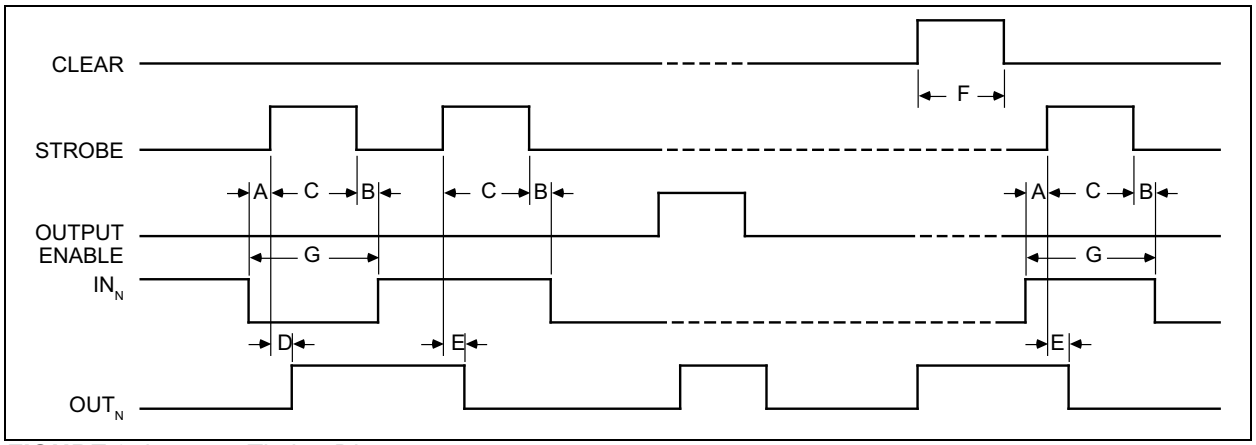



***FIGURE 3-1:*** *Timing Diagram.*

**TABLE 3-1: TIMING CONDITIONS**

| **Characteristics:** $T_A$ = +25°C; Logic levels are $V_{DD}$ and Ground; $V_{DD}$ = 5V. | | | |
|---|---|---|---|
| **Condition** | **Min.** | **Typ.** | **Max.** |
| A. Minimum data active time before strobe enabled (data set-up time) | 50 ns | — | — |
| B. Minimum data active time after strobe disabled (data hold time) | 50 ns | — | — |
| C. Minimum strobe pulse width | 125 ns | — | — |
| D. Typical time between strobe activation and output on to off transition | — | 500 ns | — |
| E. Typical time between strobe activation and output off to on transition | — | 500 ns | — |
| F. Minimum clear pulse width | 300 ns | — | — |
| G. Minimum data pulse width | 225 ns | — | — |

## 4.0 TYPICAL APPLICATIONS

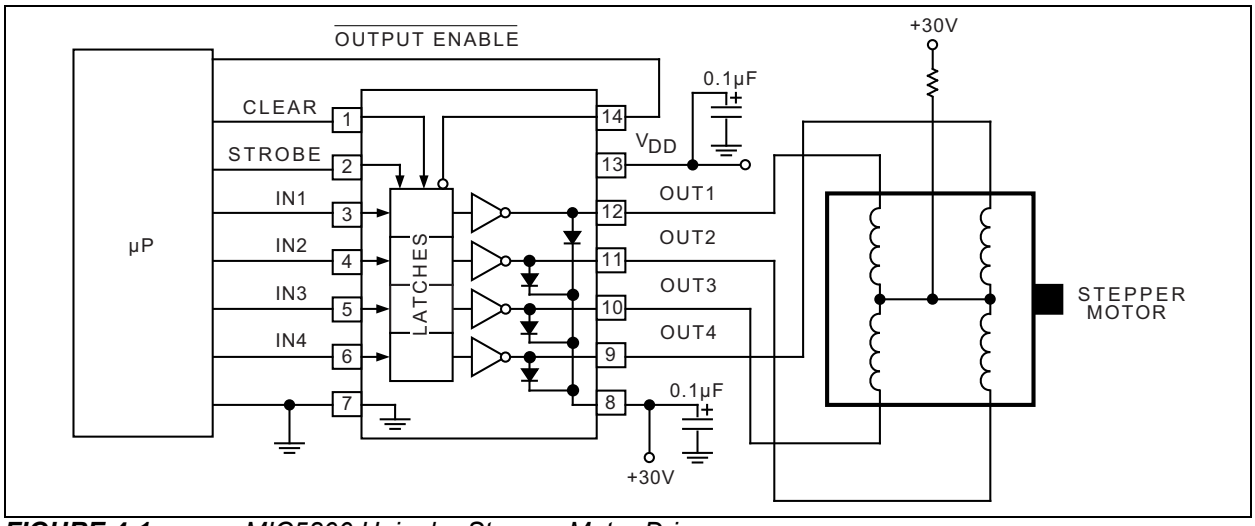



***FIGURE 4-1:*** *MIC5800 Unipolar Stepper-Motor Drive.*

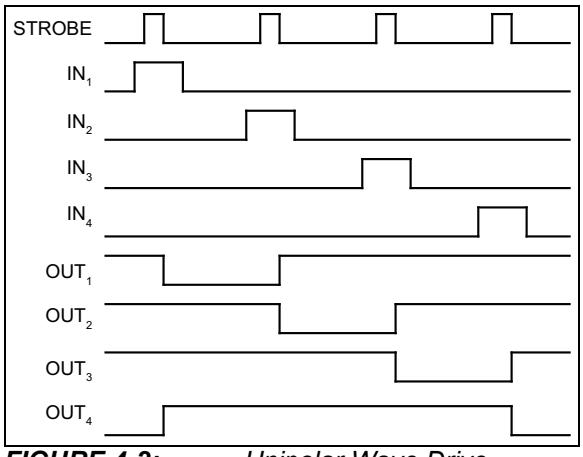



***FIGURE 4-2:*** *Unipolar Wave Drive.*

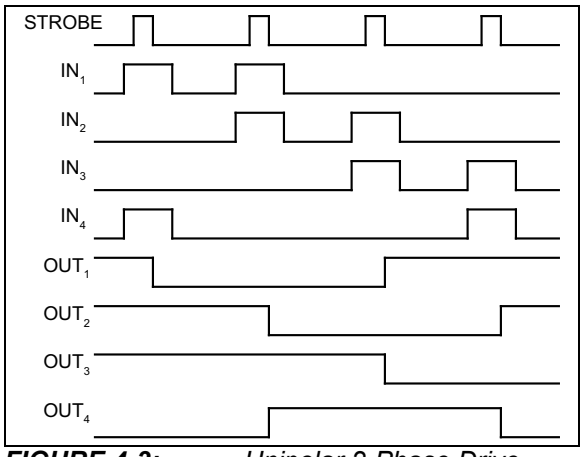



***FIGURE 4-3:*** *Unipolar 2-Phase Drive.*

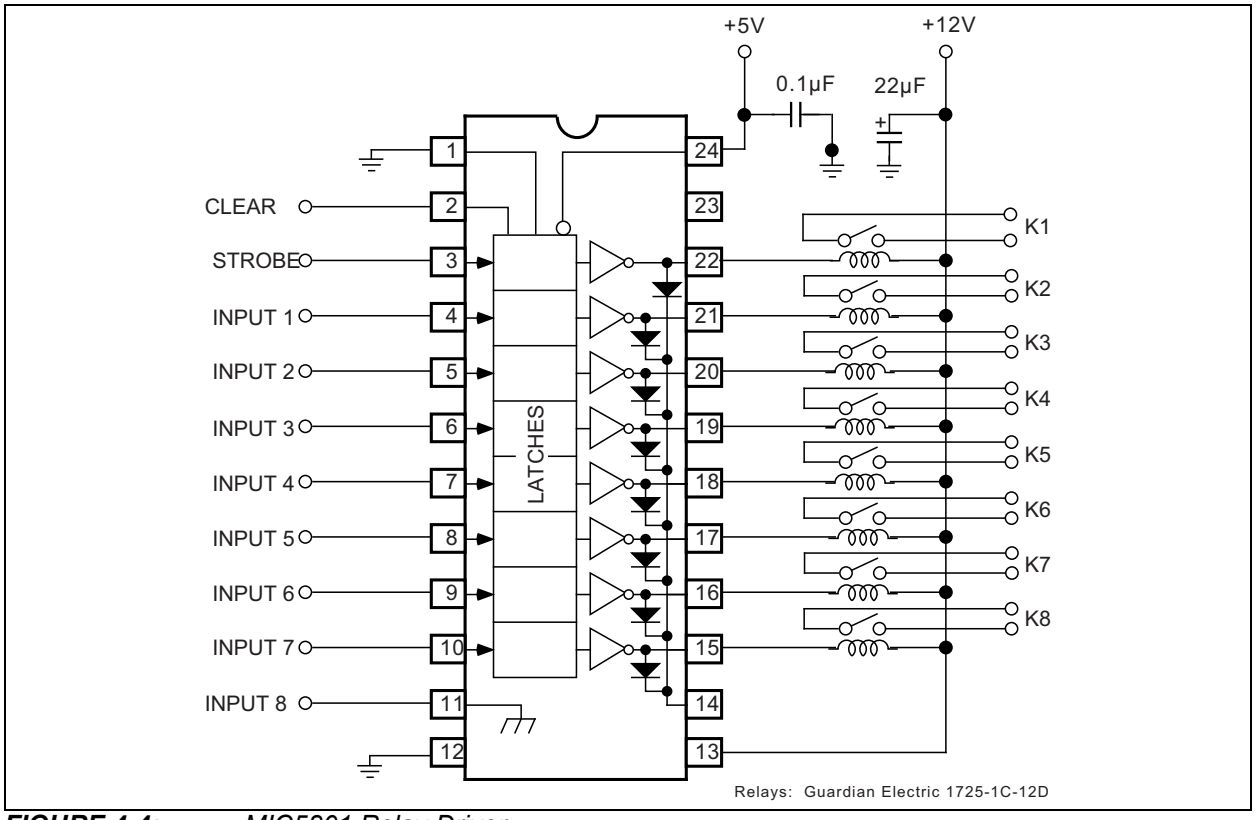



***FIGURE 4-4:*** *MIC5801 Relay Driver.*

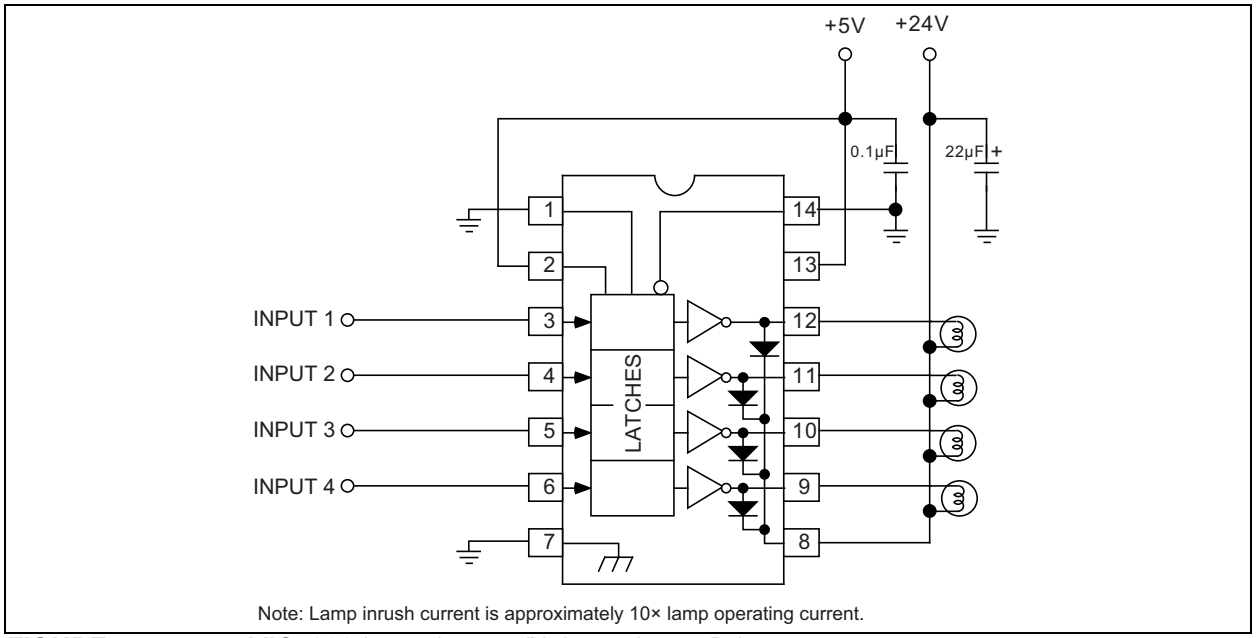
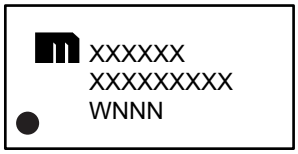



***FIGURE 4-5:*** *MIC5800 Incandescent/Halogen Lamp Driver.*

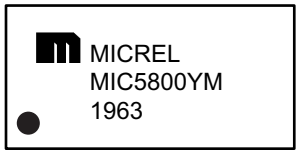
## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

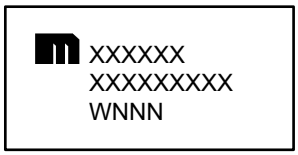
14-Lead SOIC*



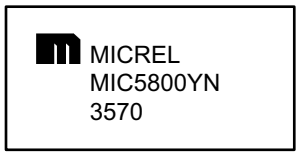

Example



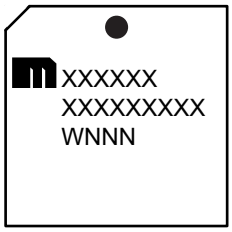

14-Lead PDIP*




Example

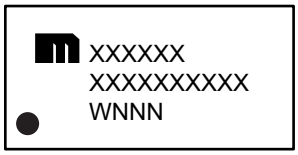



28-Lead PLCC*




Example


24-Lead SOICW*



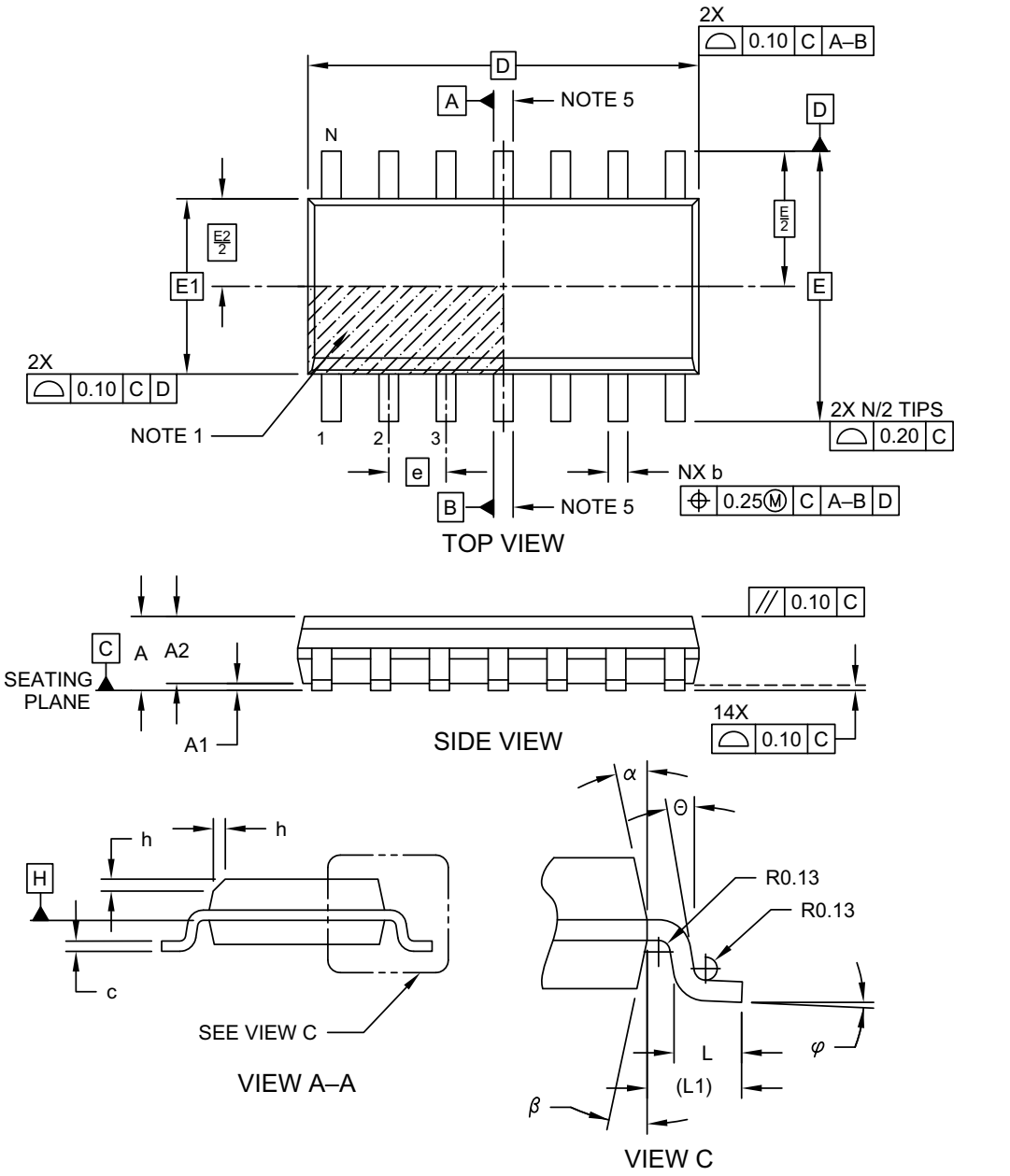

Example


| | | |
|---|---|---|
| **Legend:** | XX...X | Product code or customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |
| | ●, ▲, ▼ | Pin one index is identified by a dot, delta up, or delta down (triangle mark). |
| **Note**: | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo. | |
| | Underbar (_) and/or Overbar (¯) symbol may not be to scale. | |

## 14-Lead Plastic Small Outline SOIC Package Outline and Recommended Land Pattern

**14-Lead Plastic Small Outline (D3X, UEB, M5B, UEB) - Narrow, 3.90 mm Body [SOIC]**
**Atmel Legacy Global Package Code SVQ**

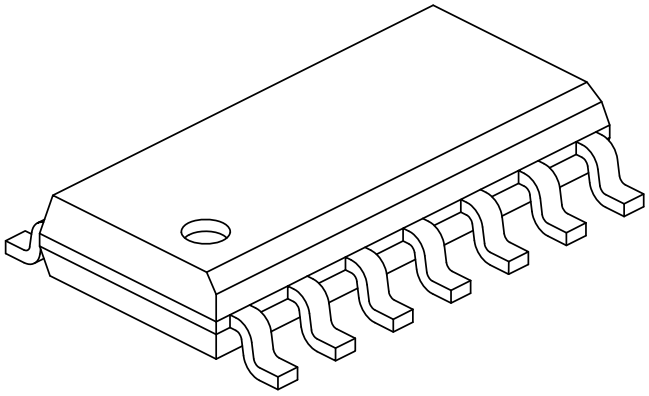
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing No. C04-065-D3X Rev D

**14-Lead Plastic Small Outline (D3X, UEB, M5B, UEB) - Narrow, 3.90 mm Body [SOIC]**
**Atmel Legacy Global Package Code SVQ**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 14 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | - | - | 1.75 |
| Molded Package Thickness | A2 | 1.25 | - | - |
| Standoff § | A1 | 0.10 | - | 0.25 |
| Overall Width | E | | 6.00 BSC | |
| Molded Package Width | E1 | | 3.90 BSC | |
| Overall Length | D | | 8.65 BSC | |
| Chamfer (Optional) | h | 0.25 | - | 0.50 |
| Foot Length | L | 0.40 | - | 1.27 |
| Footprint | L1 | | 1.04 REF | |
| Lead Angle | Θ | 0° | - | - |
| Foot Angle | φ | 0° | - | 8° |
| Lead Thickness | c | 0.10 | - | 0.25 |
| Lead Width | b | 0.31 | - | 0.51 |
| Mold Draft Angle Top | α | 5° | - | 15° |
| Mold Draft Angle Bottom | β | 5° | - | 15° |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

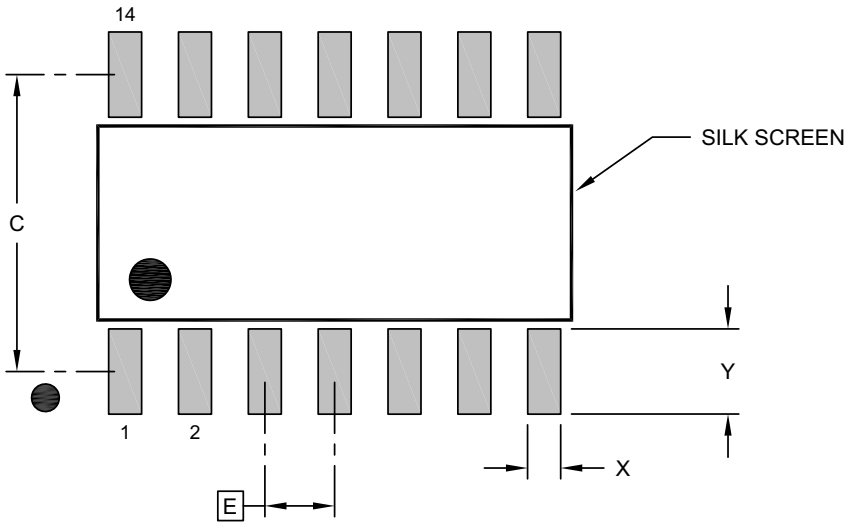
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065-D3X Rev D Sheet 2 of 2

**14-Lead Plastic Small Outline (D3X, UEB, M5B, UEB) - Narrow, 3.90 mm Body [SOIC]**
**Atmel Legacy Global Package Code SVQ**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X14) | X | | | 0.60 |
| Contact Pad Length (X14) | Y | | | 1.55 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

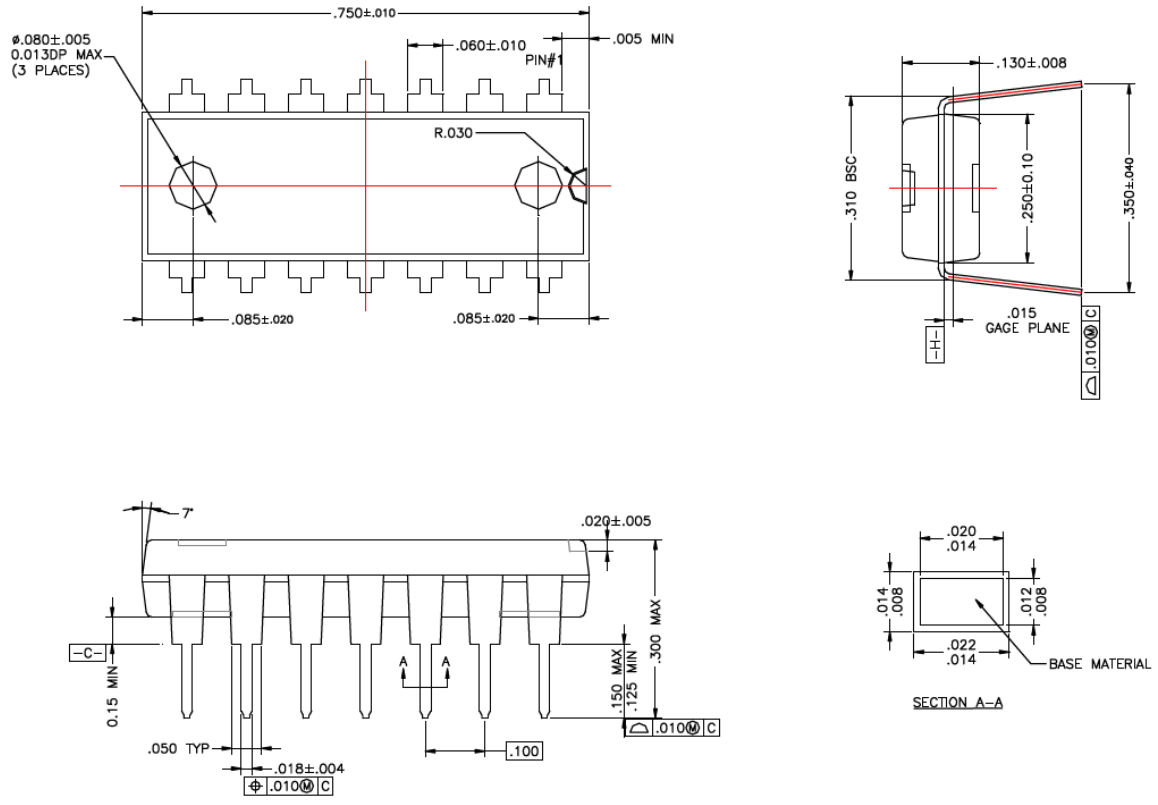
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065-D3X Rev D

## 14-Lead PDIP Package Outline and Recommended Land Pattern

**TITLE**
14 LEAD PDIP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

| | | | |
|---|---|---|---|
| **DRAWING #** | PDIP-14LD-PL-1 | **UNIT** | INCH |
| **LEAD FRAME** | Copper | **LEAD FINISH** | Matte Tin |

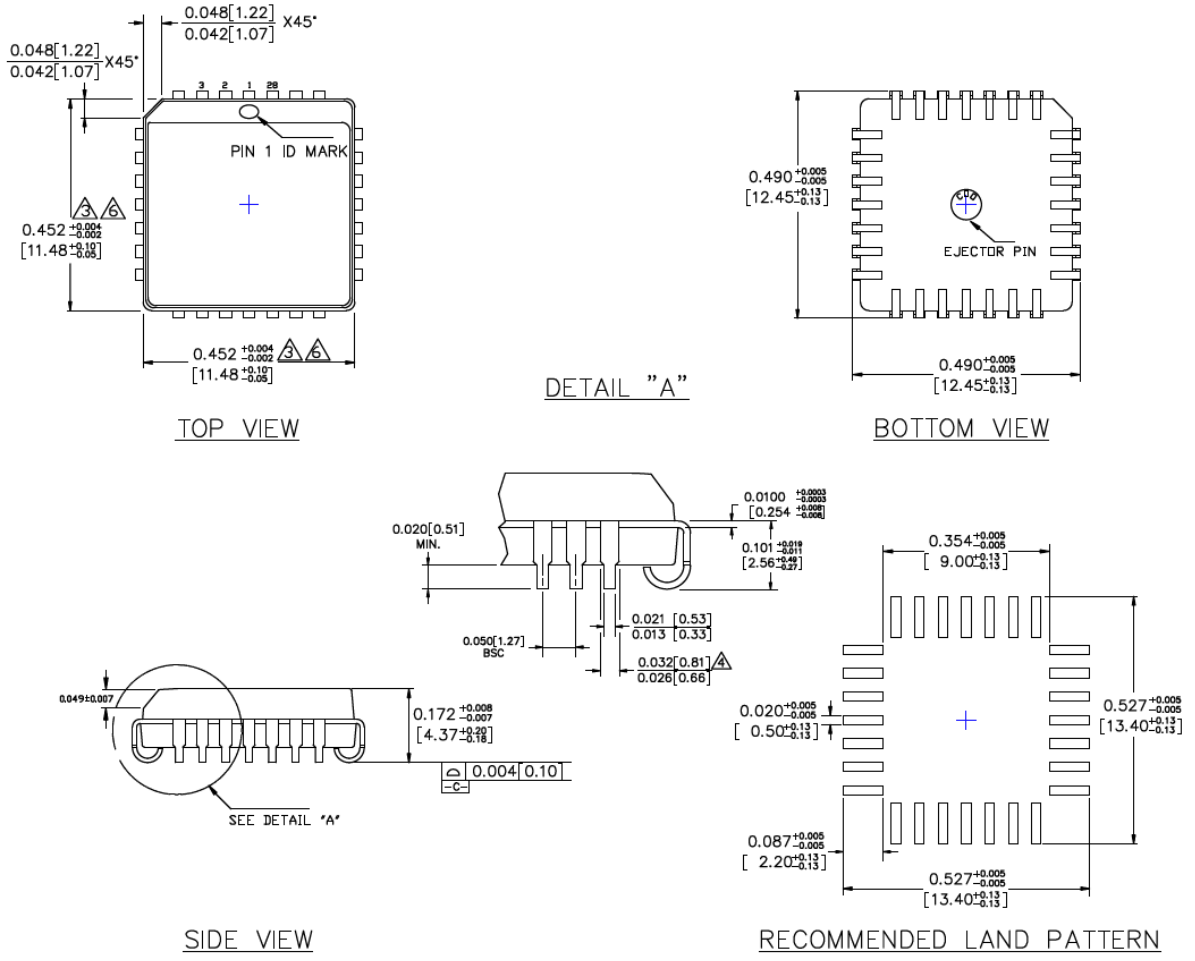



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

## 28-Lead PLCC Package Outline and Recommended Land Pattern

**TITLE**
28 LEAD PLCC PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

| DRAWING # | PLCC-28LD-PL-1 | UNIT | INCH [MM] |
|---|---|---|---|



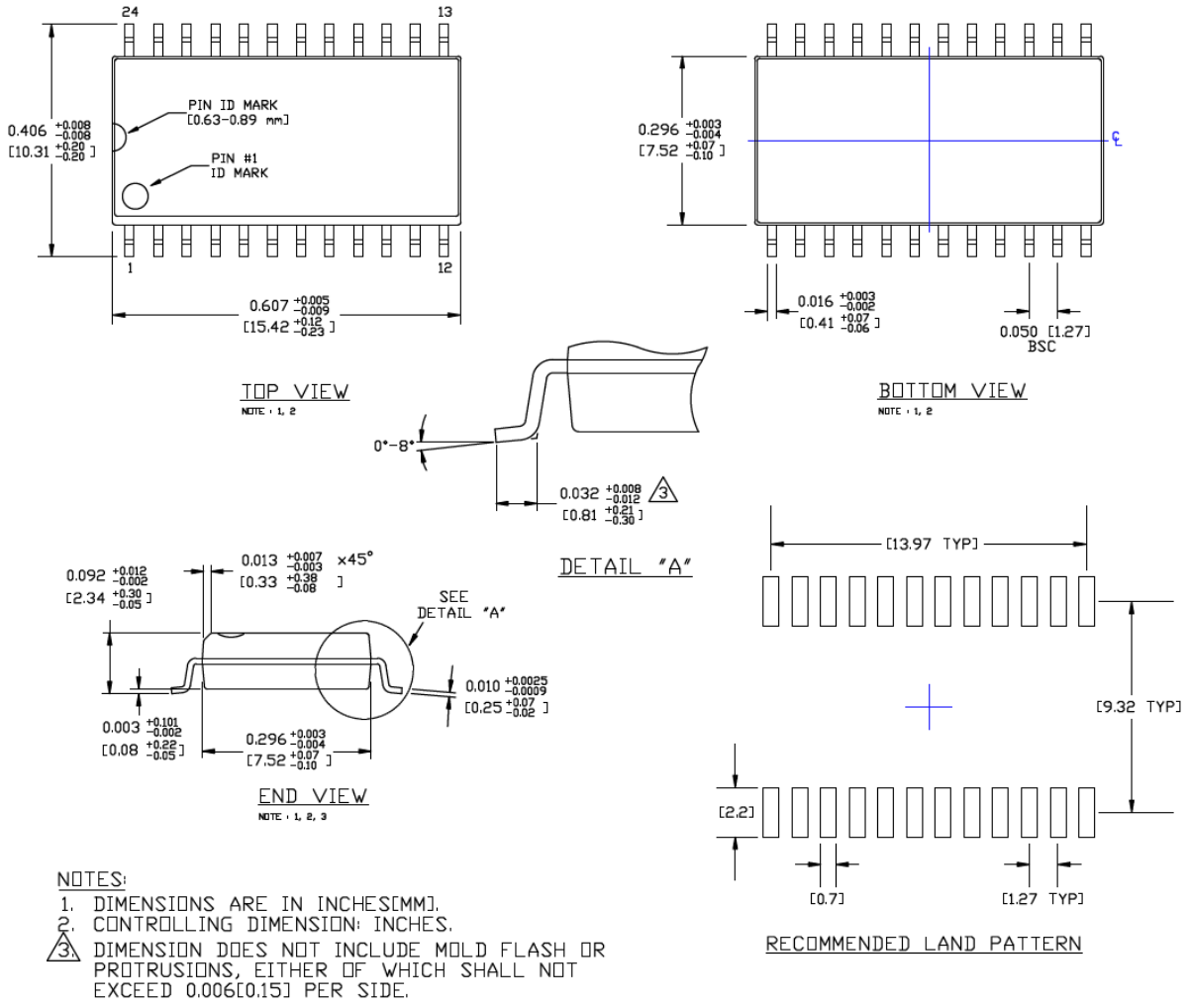

NOTES:
1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS : MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

## 24-Lead SOICW Package Outline and Recommended Land Pattern

**TITLE**
24 LEAD SOICW PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

| DRAWING # | SOICW-24LD-PL-1 | UNIT | INCH [MM] |
|---|---|---|---|




NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.15] PER SIDE.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

**NOTES:**

## APPENDIX A: REVISION HISTORY

### Revision A (April 2019)

- Converted Micrel document MIC5800/1 to Microchip data sheet template DS20006184A.
- Minor grammatical text changes throughout.

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| Device | X | XX | -XX |
|---|---|---|---|
| Part No. | Junction Temp. Range | Package | Media Type |

| | | |
|---|---|---|
| **Device:** | MIC5800: | 4-Bit Parallel-Input, High-Voltage, High-Current Latched Driver |
| | MIC5801: | 8-Bit Parallel-Input, High-Voltage, High-Current Latched Driver |
| **Junction Temperature Range:** | Y = | –40°C to +85°C, Industrial |
| **Package:** | M = | 14-Lead SOIC (MIC5800) |
| | N = | 14-Lead PDIP (MIC5800) |
| | V = | 28-Lead PLCC (MIC5801) |
| | WM = | 24-Lead Wide SOIC (MIC5801) |
| **Media Type:** | <blank>= | 54/Tube (M, MIC5800) |
| | <blank>= | 25/Tube (N, MIC5800) |
| | <blank>= | 38/Tube (V, MIC5801) |
| | <blank>= | 31/Tube (WM, MIC5801) |
| | TR = | 750/Reel (V, MIC5801) |
| | TR = | 1,000/Reel (WM, MIC5801) |
| | TR = | 2,500/Reel (M, MIC5800) |

**Examples:**

| | |
|---|---|
| a) MIC5800YM: | MIC5800, –40°C to +85°C Temperature Range, 14-Lead SOIC, 54/Tube |
| b) MIC5800YM-TR: | MIC5800, –40°C to +85°C Temperature Range, 14-Lead SOIC, 2,500/Reel |
| c) MIC5800YN: | MIC5800, –40°C to +85°C Temperature Range, 14-Lead PDIP, 25/Tube |
| d) MIC5801YV: | MIC5801, –40°C to +85°C Temperature Range, 28-Lead PLCC, 38/Tube |
| e) MIC5801YV-TR: | MIC5801, –40°C to +85°C Temperature Range, 28-Lead PLCC, 750/Reel |
| f) MIC5801YWM: | MIC5801, –40°C to +85°C Temperature Range, 24-Lead Wide SOIC, 31/Tube |
| g) MIC5801YWM-TR: | MIC5801, –40°C to +85°C Temperature Range, 24-Lead Wide SOIC, 1,000/Reel |

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**NOTES:**

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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# USB251xB/xBi

## USB251xB/xBi Family Silicon Errata

The USB251xB/xBi family devices that you have received conform functionally to the current Device Data Sheet (DS00001692A), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

**Note:** This document summarizes all silicon errata issues of the current silicon revision (**A2**).

The Engineering Device ID values for USB251xB/xBi silicon revision A2 is shown in Table 1.

**TABLE 1: SILICON DEVREV VALUES**

| Part Number | Engineer Device ID of A2 |
|---|---|
| USB2512B-AEZC | A2P10 |
| USB2512Bi-AEZC | A2P10 |
| USB2512B/M2 | A2P10 |
| USB2512BT/M2 | A2P10 |
| USB2512B-I/M2 | A2P10 |
| USB2512BT-I/M2 | A2P10 |
| USB2513B-AEZC | A2P10 |
| USB2513Bi-AEZC | A2P10 |
| USB2513B/M2 | A2P10 |
| USB2513BT/M2 | A2P10 |
| USB2513B-I/M2 | A2P10 |
| USB2513BT-I/M2 | A2P10 |
| USB2514B-AEZG | A2P10 |
| USB2514Bi-AEZG | A2P10 |
| USB2514B/M2 | A2P10 |
| USB2514BT/M2 | A2P10 |
| USB2514B-I/M2 | A2P10 |
| USB2514BT-I/M2 | A2P10 |

**TABLE 2: SILICON ISSUE SUMMARY**

| Item Number | Silicon Issue Summary | Affected Silicon Revisions |
|---|---|---|
| 1 | bcdDevice field (DID) has invalid characters | A2 |
| 2 | Selective Suspend command is ignored by the hub | A2 |
| 3 | Glitch on DP (and SD/SCL) during power-up | A2 |
| 4 | Detach detection failure | A2 |

## Silicon Errata Issues

### Module 1: bcdDevice field (DID) has invalid characters

DESCRIPTION

According to the USB2.0 specification, the bcdDevice field is specified to be binary-coded-decimal, which means only decimal characters are allowed. The hexadecimal digits A-F are not allowed.

END USER IMPLICATIONS

The presence of non-BCD characters will cause failures in some Command Verifier (CV) and Windows Hardware Certification tests, such as:

- USB (USBDEX) Verifier Test
- USB Device Connection S3 + S4
- USB Driver Level Re-Enumeration Test
- USB Enumeration Stress
- USB Serial Number

No end user functional impact.

**Work around**

This bcdDevice field can be changed through the configuration options by programming EEPROM via SMBus or $I^2C$ interface. Also, a Microsoft Contingency number 323 can be used to waive five mentioned tests above in the Windows Hardware Certification test suite.

PLAN

This erratum will not be corrected in a future revision.

### Module 2: Selective Suspend command is ignored by the hub

DESCRIPTION

If a SET_FEATURE (PORT_SUSPEND) command is sent right after the SOF command (microframe 0), the hub will not disable the port.

END USER IMPLICATIONS

The port will not suspend when a command is sent by the host. This will cause more current draw than if the port was suspended (~10mA).

**Work around**

It is recommended to use the Global Suspend function to put the entire hub into suspend to conserve power.

PLAN

This erratum will not be corrected in a future revision.

### Module 3: Glitch on DP (and SD/SCL) during power-up

DESCRIPTION

When the Hub is powering up, the DP pin is asserted before other internal logic has started. When the internal logic does start, it can cause a low pulse on the SMBus and DP pins.

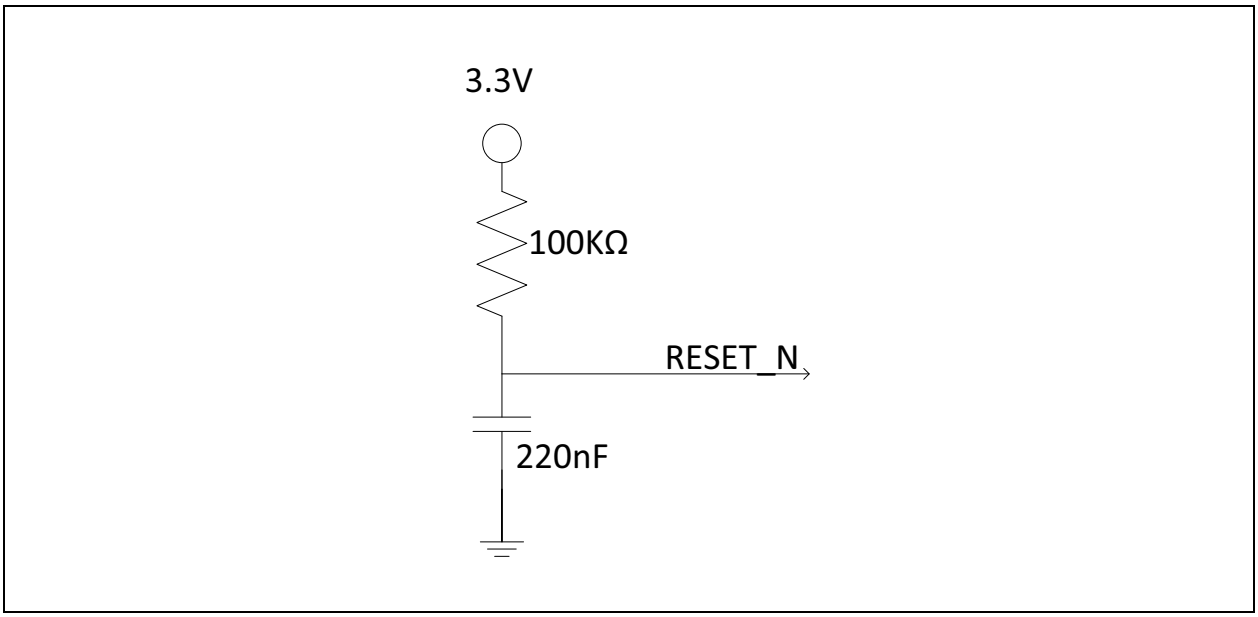
END USER IMPLICATIONS

The USB protocol can handle a glitch on DP, so no user impact on the USB lines. The SMBus glitch can impact the state machine of the SMBus Controller.

**Work around**

Keep the RESET_N pin low during POR to remove this glitch. Control RESET_N through a digital controller or an RC circuit by connecting a 100KΩ pull-up resistor to 3.3V and a 220nF capacitor to ground. See RC circuit diagram below.

**FIGURE 1: RC CIRCUIT DIAGRAM**




PLAN

This erratum will not be corrected in a future revision.

### Module 4: Detach detection failure

DESCRIPTION

When a Full-Speed/Low-Speed device detaches and quickly re-attaches, such as when issued a reset command over USB or other sideband control signal, there is a chance that the USB hub will not recognize the device detach and communicate the device detach event to the USB host. This may result in a failure to establish a connection with the device after the device is re-attached.

The hub requires 100us of uninterrupted SE0 line state (both D+ and D- lines below V_IL(min)) before a device detach is detected.

END USER IMPLICATIONS

This issue does not typically apply to a physical detach, as a physical device detach and re-attach typically involves much longer time scales.

This issue may be encountered when a device performs a self detach and re-attach as a result of some special command over USB or a reset due to some stimulus within the device's system (such as a button reset).

**Work around**

There are two possible work arounds:

1. Ensure that the hub port detects an SE0 line state for > 100us before re-attaching the device.
   a) The device must remove its D+ or D- pull-up resistor to ensure SE0 line state is achieved.
   b) There must be at least one 100µs gap in between packets while the device is in the detached state.
2. If the device is being commanded to detach and re-attach from USB host command (such as when instructing a device to re-enumerate in a different mode of operation), issue a Port Reset command to the hub for the respective port immediately after the detach command is issued to ensure that the device can be properly detected when it re-attaches.

PLAN

This erratum will not be corrected in a future revision.

## APPENDIX A: DOCUMENT REVISION HISTORY

**TABLE A-1: REVISION HISTORY**

| Revision Level & Date | Section/Figure/Entry | Correction |
|---|---|---|
| DS80000627D (03-19-19) | Module 4 | Added new errata module “Detach detection failure”. |
| | All | Updated layout to standard Microchip format. |
| DS80000627C (09-15-15) | Table 1 | Added additional device part numbers to table for SQFN package. No new errata added. |
| DS80000627B (11-07-14) | | Initial release. |

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