

## Product Change Notification - SYST-04NMLU519

#### Date:

 08 Apr 2019

 Product Category:

 USB Hubs

 Affected CPNs:

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 Notification subject:

 ERRATA - USB251xB/xBi Family Silicon Errata

 Notification text:

 SYST-04NMLU519

 Microchip has released a new DeviceDoc for the USB251xB/xBi Family Silicon Errata of devices. If you are using one of these devices please read the document located at USB251xB/xBi Family Silicon Errata.

 Notification Status: Final

## Description of Change:

- 1) Added new errata module &ldguo; Detach detection failure &rdguo;.
- 2) Updated layout to standard Microchip format.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 8 Apr 2019

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

## Markings to Distinguish Revised from Unrevised Devices: N/A Attachment(s):

USB251xB/xBi Family Silicon Errata

Please contact your local <u>Microchip sales office</u> with questions or concerns regarding this notification.

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login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Affected Catalog Part Numbers (CPN)

USB2512B-AEZG USB2512B-AEZG-BYC USB2512B-AEZG-TR USB2512B-I/M2 USB2512B/M2 USB2512BI-AEZG USB2512BI-AEZG-TR USB2512BT-I/M2 USB2512BT/M2 USB2513B-AEZC USB2513B-AEZC-TR USB2513B-AEZG USB2513B-AEZG-TR USB2513B-AEZG-TR-CD0 USB2513B-I/M2 USB2513B/M2 USB2513BI-AEZG USB2513BI-AEZG-TR USB2513BT-I/M2 USB2513BT/M2 USB2514B-AEZC USB2514B-AEZC-TR USB2514B-AEZG USB2514B-AEZG-TR USB2514B-I/M2 USB2514B/M2 USB2514BI-AEZG USB2514BI-AEZG-TR USB2514BT-I/M2 USB2514BT/M2



# **MIC5800/1**

## 4/8-Bit Parallel-Input Latched Drivers

#### Features

- 4.4 MHz Minimum Data Input Rate
- High-Voltage, High-Current Sink Outputs
- Output Transient Protection
- CMOS, PMOS, NMOS, and TTL Compatible
  Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches

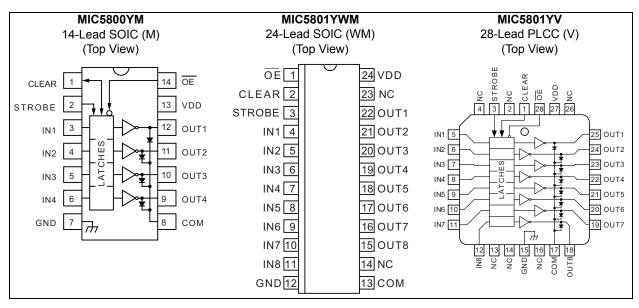
#### **General Description**

The MIC5800 and MIC5801 latched drivers are high-voltage, high-current integrated circuits comprised of four or eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions.

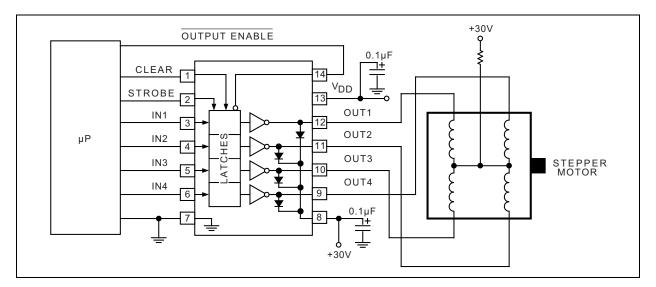
The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility. MIC5800 contains four latched drivers; MIC5801 contains eight latched drivers.

Data input rates are greatly improved in these devices. With a 5V supply, they will typically operate at better than 5 MHz. With a 12V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors. The bipolar outputs are suitable for use with relays, solenoids, stepping motors, LED or incandescent displays, and other high-power loads. Both units have open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 500 mA and will sustain at least 50V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be connected in parallel for higher load current capability.

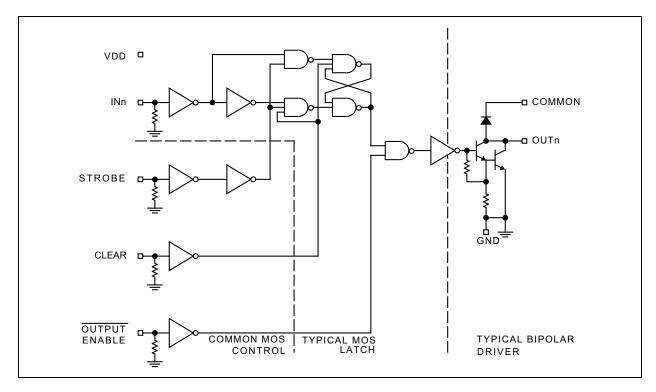
#### **Package Types**



### **Typical Application Circuit**



### **Functional Block Diagram**



## 1.0 ELECTRICAL CHARACTERISTICS

#### Absolute Maximum Ratings †

Output Voltage (V <sub>CE</sub> )	+50V
Supply Voltage (V <sub>DD</sub> )	
Input Voltage Range (V <sub>IN</sub> )	
Continuous Collector Current (I <sub>C</sub> )	
ESD Rating (Note 1)	

## **Operating Ratings ††**

Package Power Dissipation (P <sub>D</sub> )	
MIC5800 SOIC	1.0W
Derate above T <sub>A</sub> = +25°C	8.5 mW/°C
MIC5801 PLCC	
Derate above T <sub>A</sub> = +25°C	
MIC5801 Wide SOIC	
Derate above T <sub>A</sub> = +25°C	11 mW/°C

**† Notice:** Exceeding the absolute maximum ratings may damage the device.

**†† Notice:** The device is not guaranteed to function outside its operating ratings.

**Note 1:** Microchip CMOS devices have input-static protection, but are susceptible to damage when exposed to extremely high static electrical charges.

<b>Electrical Characteristics:</b> $V_{DD}$ = 5V, $T_A$ = +25°C, $V_A \le$ +85°C unless otherwise noted. Note 1								
Parameter	Sym.	Min.	Тур.	Max.	Units	Conditions		
			—	50		V <sub>CE</sub> = 50V, T <sub>A</sub> = +25°C		
Output Leakage Current	I <sub>CEX</sub>			100	μA	V <sub>CE</sub> = 50V, T <sub>A</sub> = +70°C		
			0.9	1.1		I <sub>C</sub> = 100 mA		
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	_	1.1	1.3	V	I <sub>C</sub> = 200 mA		
		_	1.3	1.6		I <sub>C</sub> = 350 mA, V <sub>DD</sub> = 7.0V		
Input Voltage (Low)	V <sub>IN(0)</sub>	_		1.0	V	—		
	V <sub>IN(1)</sub>	10.5		_	V	V <sub>DD</sub> = 12V		
Input Voltage (High)		8.5		_		V <sub>DD</sub> = 10V		
		3.5		_		V <sub>DD</sub> = 5V, Note 2		
		50	200	_		V <sub>DD</sub> = 12V		
Input Resistance	R <sub>IN</sub>	50	300	_	kΩ	V <sub>DD</sub> = 10V		
		50	600			V <sub>DD</sub> = 5V		
			1.0	2.0		V <sub>DD</sub> = 12V, Outputs Open		
Supply Current ON (Each Stage)	I <sub>DD(ON)</sub>		0.9	1.7	mA	V <sub>DD</sub> = 10V, Outputs Open		
			0.7	1.0		V <sub>DD</sub> = 5V, Outputs Open		
Supply Current OFF		_		200		V <sub>DD</sub> = 12V, Outputs Open, Inputs = 0V		
(Total)	I <sub>DD(OFF)</sub>	_	50	100	μA	V <sub>DD</sub> = 5V, Outputs Open, Inputs = 0V		

## **ELECTRICAL CHARACTERISTICS**

Note 1: Specification for packaged product only.

2: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure a minimum logic "1".

## ELECTRICAL CHARACTERISTICS (CONTINUED)

<b>Electrical Characteristics:</b> $V_{DD}$ = 5V, $T_A$ = +25°C, $V_A \le$ +85°C unless otherwise noted. Note 1									
Parameter	Sym.	Min.	Тур.	Max.	Units	Conditions			
Clamp Diode Leakage	I <sub>R</sub>	_		50		V <sub>R</sub> = 50V, T <sub>A</sub> = +25°C			
Current			_	100	μA	V <sub>R</sub> = 50V, T <sub>A</sub> = +70°C			
Clamp Diode Forward Voltage	V <sub>F</sub>	_	1.7	2.0	V	I <sub>F</sub> = 350 mA			

Note 1: Specification for packaged product only.

2: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure a minimum logic "1".

#### TRUTH TABLE

INI	Chucho	Clear	/OE	OUT <sub>N</sub>		
IN <sub>N</sub>	Strobe	Clear	/0E	t – 1	t	
0	1	0	0	Х	OFF	
1	1	0	0	Х	ON	
Х	Х	1	Х	Х	OFF	
Х	Х	Х	1	Х	OFF	
Х	0	0	0	ON	ON	
Х	0	0	0	OFF	OFF	

**Legend:** X = Irrelevant; t - 1 = Previous output state; t = Present output state.

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high /OE will set all outputs to the off condition, regardless of any other input conditions. When the /OE is low, the outputs depend on the state of their respective latches.

#### **TEMPERATURE SPECIFICATIONS**

Parameters	Sym.	Min.	Тур.	Max.	Units	Conditions		
Temperature Ranges								
Storage Temperature Range	Τ <sub>S</sub>	-65	—	+125	°C	—		
Operating Temperature Range	T <sub>A</sub>	-40	_	+85	°C	—		

**Note 1:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T<sub>A</sub>, T<sub>J</sub>, θ<sub>JA</sub>). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

## 2.0 PIN DESCRIPTIONS

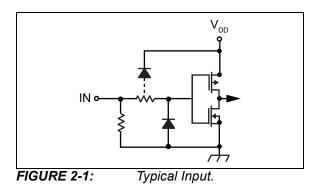
The descriptions of the pins are listed in Table 2-1 and Table 2-2.

TADLE 2-1.	ABEE 2-1. MICSOUV FINT UNCTION TABLE						
Pin Number	Pin Name	Description					
1	CLEAR	Resets all latches and turns all outputs OFF (open).					
2	STROBE	nput strobe pin. Loads output latches when high.					
3, 4, 5, 6	IN <sub>N</sub>	Parallel inputs, 1 through 4.					
7	GND	Logic and Output Ground pin.					
8	COM	Transient suppression diode common cathode pin.					
9, 10, 11, 12	OUT <sub>N</sub>	Parallel outputs, 4 through 1.					
13	VDD	Logic Supply Voltage.					
14	/OE	Output Enable. When low, outputs are active. When high, outputs are inactive and device is reset from a fault condition. An undervoltage condition emulates a high OE input.					

#### TABLE 2-1: MIC5800 PIN FUNCTION TABLE

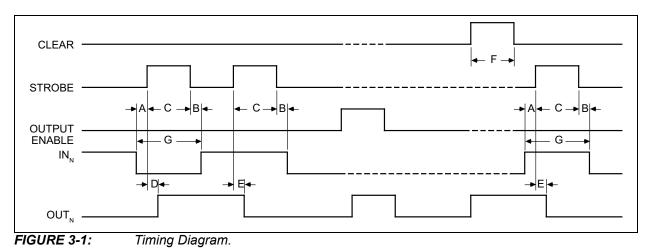
#### TABLE 2-2: MIC5801 PIN FUNCTION TABLE

Pin Number SOIC	Pin Number PLCC	Pin Name	Description
1	28	/OE	Output Enable. When low, outputs are active. When high, outputs are inactive and device is reset from a fault condition. An undervoltage condition emulates a high OE input.
2	1	CLEAR	Resets all latches and turns all outputs OFF (open).
3	3	STROBE	Input strobe pin. Loads output latches when high.
4, 5, 6, 7, 8, 9, 10, 11	5, 6, 7, 8, 9, 10, 11, 12	IN <sub>N</sub>	Parallel inputs, 1 through 8.
12	15	GND	Logic and Output Ground pin.
13	17	COM	Transient suppression diode common cathode pin.
14, 23	2, 4, 13, 14, 16, 26	NC	No Connection. Leave floating.
15, 16, 17, 18, 19, 20, 21, 22	18, 19, 20, 21, 22, 23, 24, 25	OUT <sub>N</sub>	Parallel outputs, 8 through 1.
24	27	VDD	Logic Supply Voltage.



## **MIC5800/1**

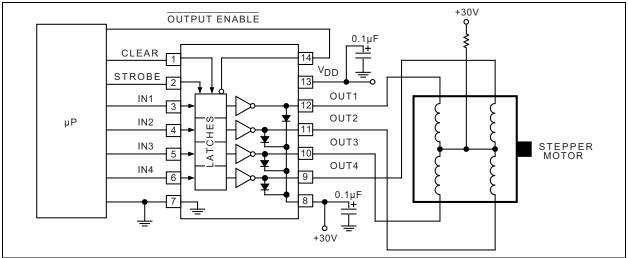
#### 3.0 TIMING



## TABLE 3-1: TIMING CONDITIONS

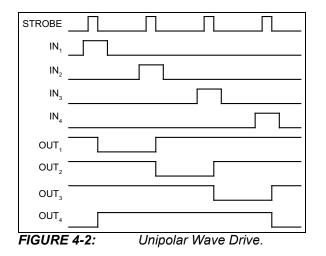
<b>Characteristics:</b> $T_A = +25^{\circ}C$ ; Logic levels are $V_{DD}$ and Ground; $V_{DD} = 5V$ .						
Condition	Min.	Тур.	Max.			
A. Minimum data active time before strobe enabled (data set-up time)	50 ns		-			
B. Minimum data active time after strobe disabled (data hold time)	50 ns		_			
C. Minimum strobe pulse width	125 ns		_			
D. Typical time between strobe activation and output on to off transition	—	500 ns	—			
E. Typical time between strobe activation and output off to on transition	_	500 ns	_			
F. Minimum clear pulse width	300 ns		_			
G. Minimum data pulse width	225 ns	_	_			

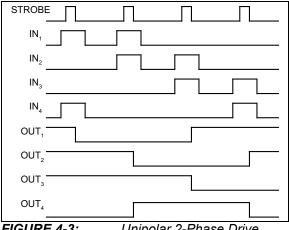
#### 4.0 **TYPICAL APPLICATIONS**

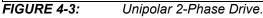


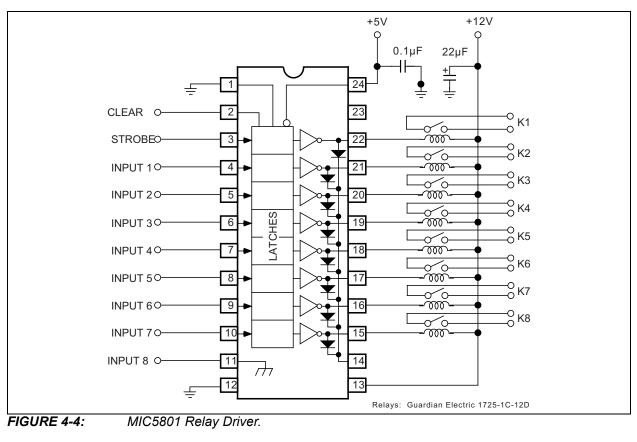


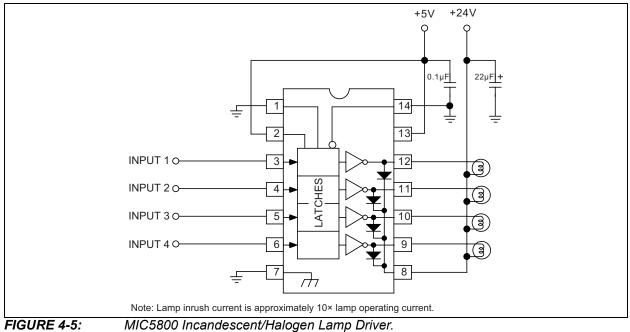
MIC5800 Unipolar Stepper-Motor Drive.





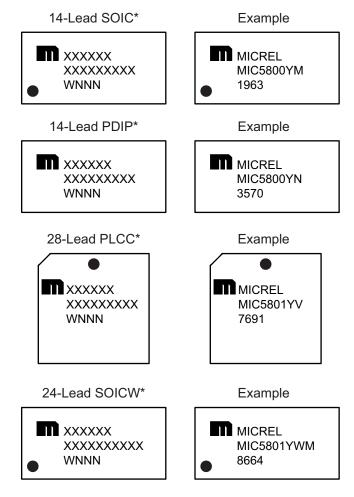






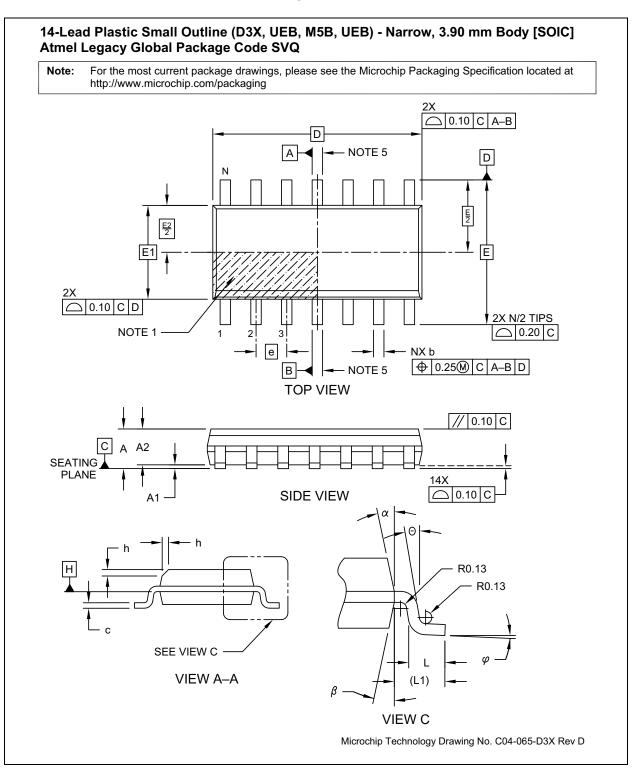
### 5.0 PACKAGING INFORMATION

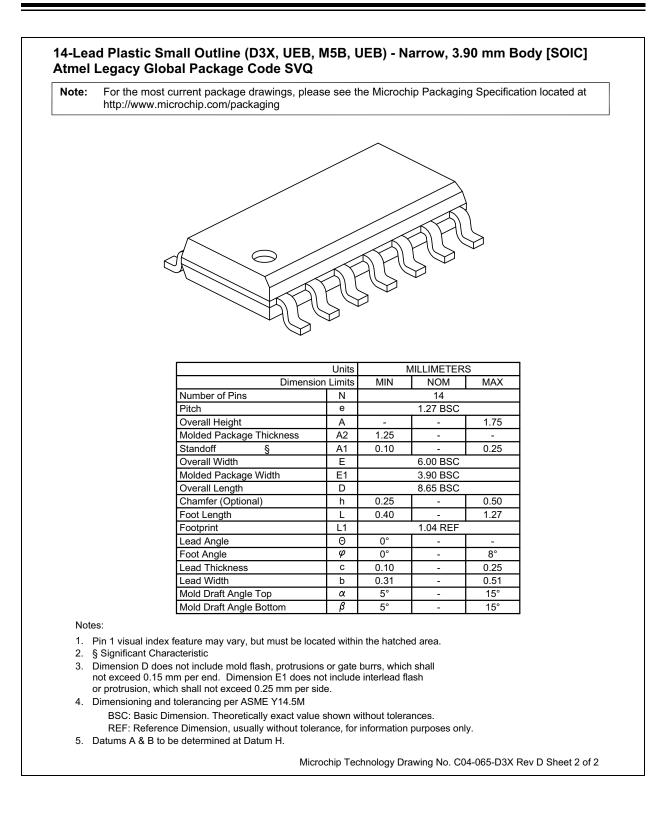
#### 5.1 Package Marking Information

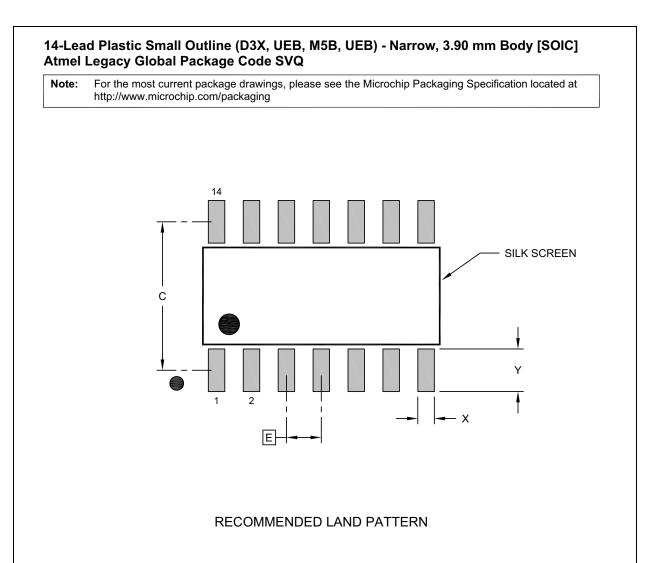


Legend:	Y YY WW NNN @3 *	Product code or customer-specific information Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code Pb-free JEDEC <sup>®</sup> designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. Pin one index is identified by a dot, delta up, or delta down (triangle
t c	be carried characters he corpora	nt the full Microchip part number cannot be marked on one line, it will d over to the next line, thus limiting the number of available for customer-specific information. Package may or may not include ate logo. (_) and/or Overbar ( <sup>-</sup> ) symbol may not be to scale.

#### 14-Lead Plastic Small Outline SOIC Package Outline and Recommended Land Pattern







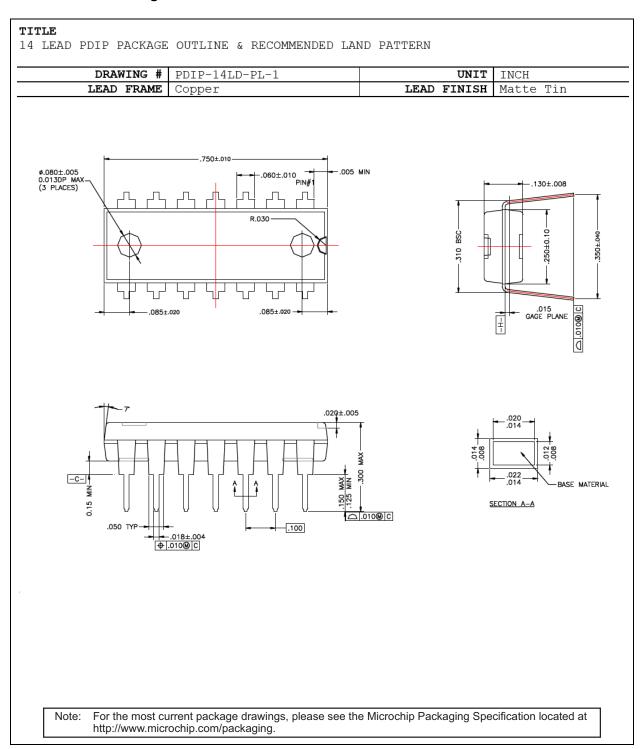
	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing C			5.40	
Contact Pad Width (X14)	Х			0.60
Contact Pad Length (X14)	Y			1.55

Notes:

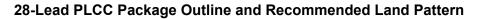
1. Dimensioning and tolerancing per ASME Y14.5M

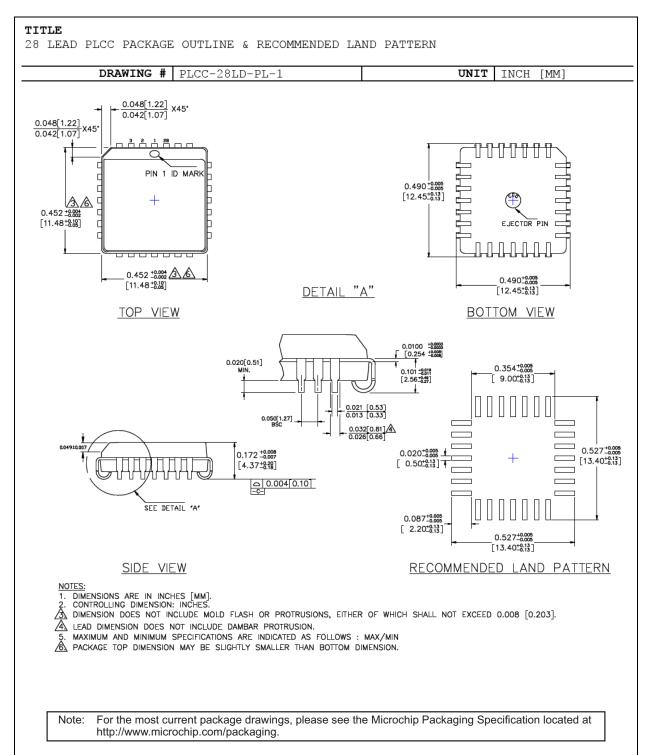
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

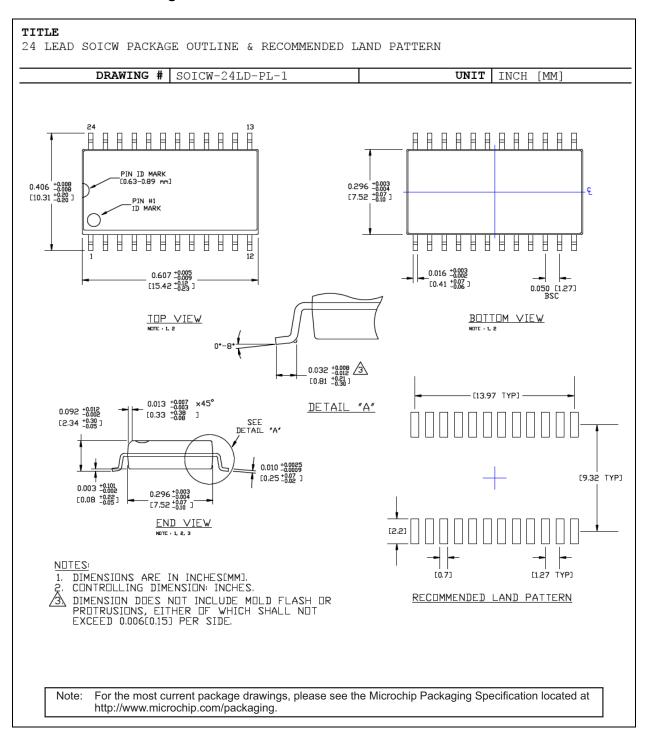
Microchip Technology Drawing No. C04-2065-D3X Rev D



#### 14-Lead PDIP Package Outline and Recommended Land Pattern







#### 24-Lead SOICW Package Outline and Recommended Land Pattern

## **MIC5800/1**

NOTES:

### APPENDIX A: REVISION HISTORY

### Revision A (April 2019)

- Converted Micrel document MIC5800/1 to Microchip data sheet template DS20006184A.
- Minor grammatical text changes throughout.

## **MIC5800/1**

NOTES:

## **PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

				Examples:	
Device Part No.	<u>X</u> Junction Temp. Range	<u>XX</u> Package	- <u>XX</u> Media Type	a) MIC5800YM:	MIC5800, –40°C to +85°C Temperature Range, 14-Lea SOIC, 54/Tube
Device:	(	4-Bit Parallel-Input, Hig Current Latched Driver		b) MIC5800YM-TR:	MIC5800, –40°C to +85°C Temperature Range, 14-Lea SOIC, 2,500/Reel
		8-Bit Parallel-Input, Hig Current Latched Driver		c) MIC5800YN:	MIC5800, –40°C to +85°C Temperature Range, 14-Lea PDIP, 25/Tube
Junction Temperature Range:	Y = -40°C	to +85°C, Industrial		d) MIC5801YV:	MIC5801, –40°C to +85°C Temperature Range, 28-Lea PLCC, 38/Tube
Package:	N = 14-Lea V = 28-Lea	ad SOIC (MIC5800) ad PDIP (MIC5800) ad PLCC (MIC5801)		e) MIC5801YV-TR:	MIC5801, –40°C to +85°C Temperature Range, 28-Lea PLCC, 750/Reel
	<blank>= 54/Tub</blank>		11)	f) MIC5801YWM:	MIC5801, –40°C to +85°C Temperature Range, 24-Lea Wide SOIC, 31/Tube
Media Type:	TR = 750/Re			g) MIC5801YWM-TR:	MIC5801, –40°C to +85°C Temperature Range, 24-Lea Wide SOIC, 1,000/Reel
		Reel (M, MIC5800)		catalog part used for ord the device p	eel identifier only appears in the number description. This identifier is ering purposes and is not printed on ackage. Check with your Microchip for package availability with the eel option.

## **MIC5800/1**

NOTES:

#### Note the following details of the code protection feature on Microchip devices:

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- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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## USB251xB/xBi Family Silicon Errata

The USB251xB/xBi family devices that you have received conform functionally to the current Device Data Sheet (DS00001692A), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

Note: This document summarizes all silicon errata issues of the current silicon revision (A2).

The Engineering Device ID values for USB251xB/xBi silicon revision A2 is shown in Table 1.

#### TABLE 1: SILICON DEVREV VALUES

Part Number	Engineer Device ID of A2
USB2512B-AEZC	A2P10
USB2512Bi-AEZC	A2P10
USB2512B/M2	A2P10
USB2512BT/M2	A2P10
USB2512B-I/M2	A2P10
USB2512BT-I/M2	A2P10
USB2513B-AEZC	A2P10
USB2513Bi-AEZC	A2P10
USB2513B/M2	A2P10
USB2513BT/M2	A2P10
USB2513B-I/M2	A2P10
USB2513BT-I/M2	A2P10
USB2514B-AEZG	A2P10
USB2514Bi-AEZG	A2P10
USB2514B/M2	A2P10
USB2514BT/M2	A2P10
USB2514B-I/M2	A2P10
USB2514BT-I/M2	A2P10

#### TABLE 2: SILICON ISSUE SUMMARY

ltem Number	Silicon Issue Summary	Affected Silicon Revisions
1	bcdDevice field (DID) has invalid characters	A2
2	Selective Suspend command is ignored by the hub	A2
3	Glitch on DP (and SD/SCL) during power-up	A2
4	Detach detection failure	A2

#### Silicon Errata Issues

#### Module 1: bcdDevice field (DID) has invalid characters

#### DESCRIPTION

According to the USB2.0 specification, the bcdDevice field is specified to be binary-coded-decimal, which means only decimal characters are allowed. The hexadecimal digits A-F are not allowed.

#### END USER IMPLICATIONS

The presence of non-BCD characters will cause failures in some Command Verifier (CV) and Windows Hardware Certification tests, such as:

- USB (USBDEX) Verifier Test
- USB Device Connection S3 + S4
- USB Driver Level Re-Enumeration Test
- USB Enumeration Stress
- USB Serial Number

No end user functional impact.

#### Work around

This bcdDevice field can be changed through the configuration options by programming EEPROM via SMBus or  $I^2C$  interface. Also, a Microsoft Contingency number 323 can be used to waive five mentioned tests above in the Windows Hardware Certification test suite.

#### PLAN

This erratum will not be corrected in a future revision.

#### Module 2: Selective Suspend command is ignored by the hub

#### DESCRIPTION

If a SET\_FEATURE (PORT\_SUSPEND) command is sent right after the SOF command (microframe 0), the hub will not disable the port.

#### END USER IMPLICATIONS

The port will not suspend when a command is sent by the host. This will cause more current draw than if the port was suspended (~10mA).

#### Work around

It is recommended to use the Global Suspend function to put the entire hub into suspend to conserve power.

#### PLAN

This erratum will not be corrected in a future revision.

#### Module 3: Glitch on DP (and SD/SCL) during power-up

#### DESCRIPTION

When the Hub is powering up, the DP pin is asserted before other internal logic has started. When the internal logic does start, it can cause a low pulse on the SMBus and DP pins.

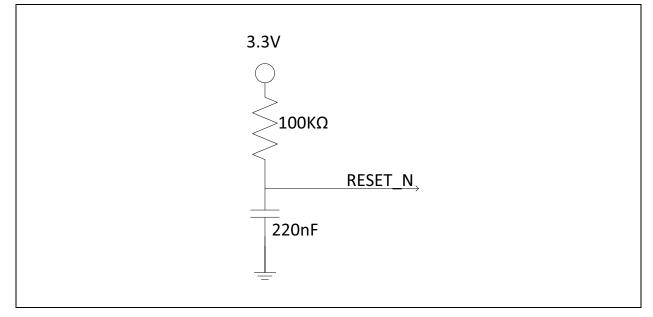
#### END USER IMPLICATIONS

The USB protocol can handle a glitch on DP, so no user impact on the USB lines. The SMBus glitch can impact the state machine of the SMBus Controller.

#### Work around

Keep the RESET\_N pin low during POR to remove this glitch. Control RESET\_N through a digital controller or an RC circuit by connecting a 100K $\Omega$  pull-up resistor to 3.3V and a 220nF capacitor to ground. See RC circuit diagram below.





#### PLAN

This erratum will not be corrected in a future revision.

#### Module 4: Detach detection failure

#### DESCRIPTION

When a Full-Speed/Low-Speed device detaches and quickly re-attaches, such as when issued a reset command over USB or other sideband control signal, there is a chance that the USB hub will not recognize the device detach and communicate the device detach event to the USB host. This may result in a failure to establish a connection with the device after the device is re-attached.

The hub requires 100us of uninterrupted SE0 line state (both D+ and D- lines below V\_IL(min)) before a device detach is detected.

#### END USER IMPLICATIONS

This issue does not typically apply to a physical detach, as a physical device detach and re-attach typically involves much longer time scales.

This issue may be encountered when a device performs a self detach and re-attach as a result of some special command over USB or a reset due to some stimulus within the device's system (such as a button reset).

#### Work around

There are two possible work arounds:

- 1. Ensure that the hub port detects an SE0 line state for > 100us before re-attaching the device.
  - a) The device must remove its D+ or D- pull-up resistor to ensure SE0 line state is achieved.
  - b) There must be at least one 100µs gap in between packets while the device is in the detached state.
- 2. If the device is being commanded to detach and re-attach from USB host command (such as when instructing a device to re-enumerate in a different mode of operation), issue a Port Reset command to the hub for the respective port immediately after the detach command is issued to ensure that the device can be properly detected when it re-attaches.

#### PLAN

This erratum will not be corrected in a future revision.

### APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction	
DS80000627D (03-19-19)	Module 4	Added new errata module "Detach detection failure".	
	All	Updated layout to standard Microchip format.	
DS80000627C (09-15-15)	Table 1	Added additional device part numbers to table for SQFN package. No new errata added.	
DS80000627B (11-07-14)		Initial release.	

#### TABLE A-1: REVISION HISTORY

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