

3A, 6.5V, Ultra Low Noise, Ultra Low Dropout Linear Regulator

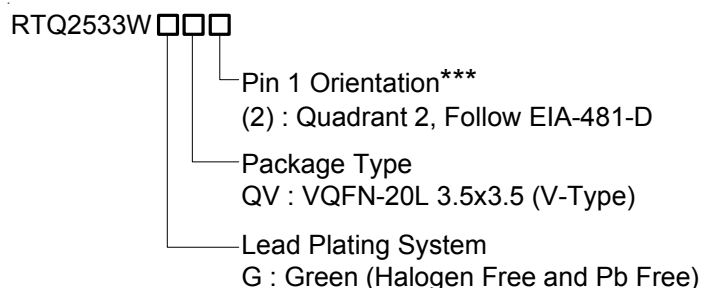
General Description

The RTQ2533W is a high-current (3A), low-noise ($6.8\mu\text{V}_{\text{RMS}}$), high accuracy (1% over line, load, and temperature), low-dropout linear regulator (LDO) capable of sourcing 3A with extremely low dropout (max. 180mV). The device output voltage is pin-selectable (up to 3.95V) using a PCB layout without the need of external resistors, thus reducing overall component count. Designers can achieve higher output voltage with the use of external resistor divider. The device supports single input supply voltage as low to 1.1V that makes it easy to use.

The low noise, high PSRR and high output current capability makes the RTQ2533W ideal to power noise-sensitive devices such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and RF components. With very high accuracy, remote sensing, and soft-start capabilities to reduce inrush current, the RTQ2533W is ideal for powering digital loads such as FPGAs, DSPs, and ASICs.

The external enable control and power good indicator function makes the control sequence easier. The output noise immunity is enhanced by adding external bypass capacitor on NR/SS pin. The device is fully specified over the temperature range of $T_J = -40^\circ\text{C}$ to 125°C and is offered in a VQFN-20L 3.5x3.5 package.

Ordering Information



Note :

***Empty means Pin1 orientation is Quadrant 1

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

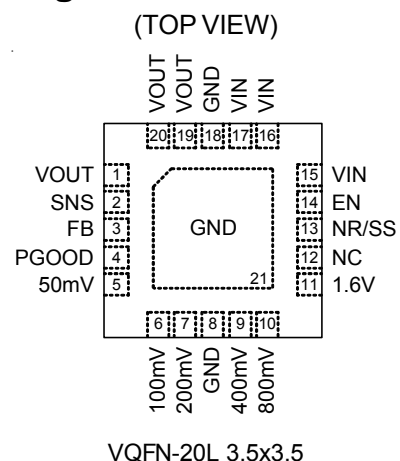
Features

- Input Voltage Range : 1.1V to 6.5V
- Two Output Voltage Modes
 - ▶ 0.8 V to 5.5V (Set by a Resistive Divider)
 - ▶ 0.8 V to 3.95V (Set via PCB Layout, No External Resistor Required)
- Accurate Output Voltage Accuracy (1%) Over Line, Load and Temperature
- Ultra High PSRR : 40dB at 500kHz
- Excellent Noise Immunity
 - ▶ $6.8\mu\text{V}_{\text{RMS}}$ at 0.8V Output
 - ▶ $10\mu\text{V}_{\text{RMS}}$ at 3.3V Output
- Ultra Low Dropout Voltage : 180mV at 3A
- Enable Control
- Programmable Soft-Start Output
- Stable with a $47\mu\text{F}$ or Larger Ceramic Output Capacitor
- Support Power-Good Indicator Function
- RoHS Compliant and Halogen Free

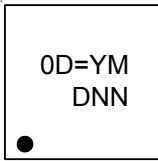
Applications

- Portable Electronic Device
- Wireless Infrastructure : SerDes, FPGA, DSP
- RF, IF Components : VCO, ADC, DAC, LVDS

Pin Configuration



Marking Information

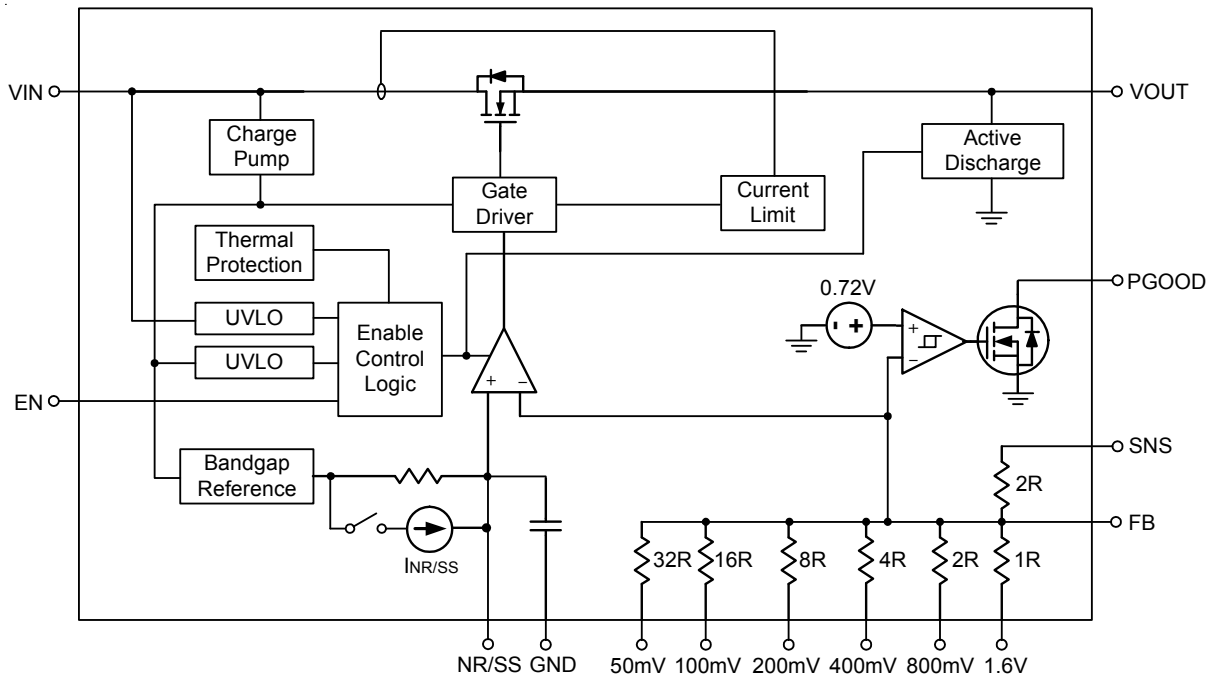


0D= : Product Code
 YMDNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 19, 20	VOUT	LDO output pins. A 47 μ F or larger ceramic capacitor (22 μ F or greater effective capacitance) is required for stability. Place the output capacitor as close to the device as possible and minimize the impedance between VOUT pin to load.
2	SNS	Output voltage sense input pin. Connect this pin only if using the configuration without external resistors. Keep SNS pin floating if the VOUT voltage is set by external resistor.
3	FB	Feedback voltage input. This pin is used to set the desired output voltage via an external resistive divider. The feedback reference voltage is 0.8V typically.
4	PGOOD	Power good indicator output. An open-drain output and active high when the output voltage reaches 88% of the target. The pin is pulled to ground when the output voltage is lower than its specified threshold, EN shutdown, OCP and OTP.
5, 6, 7, 9, 10, 11	50mV, 100mV, 200mV, 400mV, 800mV, 1.6V	Output voltage setting pins. Connect these pins to ground or leave floating. Connecting these pins to ground increases the output voltage by the value of the pin name; multiple pins can be simultaneously connected to GND to select the desired output voltage. Leave these pins floating (open) if the VOUT voltage is set by external resistor.
8, 18, 21 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
12	NC	No internal connection. Leaving these pins floating does not affect the chip functionality. By connecting these pins to GND, design engineers could extend the GND copper coverage on the PCB top layer to enhance the thermal convection.
13	NR/SS	Noise-reduction and soft-start pin. Decouple this pin to GND with an external capacitor C _{NR/SS} can not only reduce output noise to very low levels but also slow down the rising of VOUT, providing a soft-start behavior. For low noise applications, a 10nF to 1 μ F C _{NR/SS} is suggested.
14	EN	Enable control input. Connecting this pin to logic high enables the regulator, and driving this pin low puts it into shutdown mode. The device can have V _{IN} and V _{EN} sequenced in any order without causing damage to the device. However, for the soft-start function to work as intended, certain sequencing rules must be applied. Enabling the device after V _{IN} is present is preferred.
15, 16, 17	VIN	Supply input. A general 47 μ F ceramic capacitor should be placed as close as possible to this pin for better noise rejection.

Functional Block Diagram



Operation

The RTQ2533W operates with single supply input ranging from 1.1V to 6.5V and capable to deliver up to 3A current to the output. The device features high PSRR and low noise provides a clean supply to the application.

A low-noise reference and error amplifier are included to reduce device noise. The NR/SS capacitor filters the noise from the reference and feed-forward capacitor filters the noise from the error amplifier. The high power-supply rejection ratio (PSRR) of the RTQ2533W minimizes the coupling of input supply noise to the output.

Enable and Shutdown

The RTQ2533W provides an EN pin, as an external chip enable control, to enable or disable the device. V_{EN} below 0.5 V turns the regulator off and enters the shutdown mode, while V_{EN} above 1.1V turns the regulator on. When the regulator is shutdown, the ground current is reduced to a maximum of 25 μ A. The enable circuitry has hysteresis (typically 50mV) for use with relatively slowly ramping analog signals.

If not used, connect EN to the largest capacitance on the input as close as possible to prevent voltage droops on the VIN line from triggering the enable circuit.

VOUT Programming Pins

The built-in matched feedback resistor network of the RTQ2533W can set the output voltage. The output voltage can be programmed from 0.8V to 3.95V in 50mV steps when tying these programming pins (Pins 5 to 11) to ground. Tying any of the VOUT programming pins to SNS can lower the value of the upper resistor divider. Hence the VOUT programming resolution is increased.

Programmable Soft-Start

The noise-reduction capacitor ($C_{NR/SS}$) accomplishes the dual purpose of both noise-reduction and programming the soft-start ramp time during turn-on. When EN and UVLO exceed the respective threshold voltage, the RTQ2533W activates a quick-start circuit to charge the noise reduction capacitor ($C_{NR/SS}$) and then the output voltage ramps up.

Power Good

The power-good circuit monitors the feedback pin voltage to indicate the status of the output voltage. The open-drain PGOOD pin requires an external pull-up resistor to an external supply, any downstream device can receive power-good as a logic signal that can be used for sequencing. A pull-up resistor from 10k Ω to 100k Ω is recommended. Make sure that the external pull-up supply voltage results in a valid logic signal for the receiving device or devices.

After start-up, the PGOOD pin becomes high impedance when the feedback voltage exceeds V_{PGOOD_HYS} (Typically 90% of 0.8V reference voltage level). The PGOOD is pulled to GND when the feedback pin voltage falls below the V_{IT_PGOOD} , or either when En is low, the current limit or OTP levels are reached.

Under-Voltage Lockout (UVLO)

The UVLO circuit monitors the input voltage to prevent the device from turning on before VIN rises above the V_{UVLO} threshold. The UVLO circuit also disables the output of the device when VIN falls below the lockout voltage ($V_{UVLO} - \Delta V_{UVLO}$). The UVLO circuit responds quickly to glitches on VIN and attempts to disable the output of the device if VIN collapses.

Internal Current Limit (I_{LIM})

The RTQ2533W continuously monitors the output current to protect the device against high load current faults or shorting events. The current limit circuitry is not intended to allow operation above the rated current of the device. Continuously running the RTQ2533W above the rated current degrades device reliability.

During current limit, the output voltage falls when load impedance decreases. If the output voltage is low, excessive power may cause the output thermal shutdown.

A foldback feature limits the short-circuit current to protect the regulator from damage under all load conditions. If the load current demand exceeds the foldback current limit before EN goes high, the device does not start up.

Over-Temperature Protection (OTP)

The RTQ2533W implements thermal shutdown protection. The device is disabled when the junction temperature (T_J) exceeds 160°C (typical). The LDO automatically turns on again when the temperature falls to 140°C (typical).

For reliable operation, limit the junction temperature to a maximum of 125°C. Continuously running the RTQ2533W into thermal shutdown or above a junction temperature of 125°C reduces long-term reliability.

Output Active Discharge

When the device is disabled, the RTQ2533W discharges the LDO output (via VOUT pins) through an internal current sink to ground. Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input. External current protection should be added if the device may work at reverse voltage state.

Absolute Maximum Ratings (Note 1)

- VIN, PGOOD, EN ----- -0.3V to 7V
- VOUT ----- -0.3V to 7V
- NR/SS, FB ----- -0.3V to 3.6V
- Power Dissipation, PD @ TA = 25°C
- VQFN-20L 3.5x3.5 ----- 2.78W
- Package Thermal Resistance (Note 2)
- VQFN-20L 3.5x3.5, θJA ----- 36°C/W
- VQFN-20L 3.5x3.5, θJC ----- 7.9°C/W
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)
- HBM (Human Body Model) ----- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ----- 1.1V to 6.5V
- Junction Temperature Range ----- -40°C to 125°C

Electrical Characteristics

Over operating temperature range (TJ = -40°C to 125°C), (1.1V ≤ VIN < 6.5V and VIN ≥ VOUT(TARGET) + 0.3 V, VOUT(TARGET) = 0.8V, VOUT connected to 50Ω to GND, VEN = 1.1 V, CIN = 10μF, COUT = 47μF, CNR/SS = 0nF, CFF = 0nF, and PGOOD pin pulled up to VIN with 100kΩ, unless otherwise noted. (Note 5)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Input Voltage Range	VIN		1.1	--	6.5	V
Feedback Reference Voltage	VREF		--	0.8	--	V
NR/SS Pin Voltage	VNR/SS		--	0.8	---	V
Under-Voltage Lock-Out	VUVLO	VIN increasing	--	1.02	1.085	V
	ΔVUVLO	Hysteresis	--	100	--	mV
Output Voltage Range		Using voltage setting pins (50mV, 100mV, 200mV, 400mV, 800mV, and 1.6V)	0.8V -1%	--	3.95V + 1%	V
		Using external resistors	0.8V -1%	--	5V + 1%	V
Output Voltage Accuracy (Note 6)	VOUT	VIN = VOUT + 0.3V, 0.8V ≤ VOUT ≤ 5V, 1mA ≤ IOUT ≤ 3A	-1	--	1	%
Line Regulation	ΔVOUT/ΔVIN	IOUT = 1mA, 1.1V ≤ VIN ≤ 6.5 V	--	0.05	--	%/V
Load Regulation	ΔVOUT/ΔIOUT	1mA ≤ IOUT ≤ 3A	--	0.08	--	%/A
Dropout Voltage	VDROP	VIN = 1.1V to 6.5V, IOUT = 3A, VFB = 0.8V - 3%	--	110	180	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Output Current Limit	I _{LIM}	V _{OUT} = 90% V _{OUT(TARGET)} , V _{IN} = V _{OUT(TARGET)} + 400mV	3.5	4.2	4.8	A	
Short-Circuit Current Limit	I _{SC}	R _{LOAD} = 20mΩ, under foldback operation	--	1.5	--	A	
Ground Pin Current	I _{GND}	Minimum load, V _{IN} = 6.5V, I _{OUT} = 5mA	--	3	4	mA	
		Maximum load, V _{IN} = 1.4V, I _{OUT} = 3A	--	4.3	5.5		
		Shutdown, PGOOD = Open, V _{IN} = 6.5V, V _{EN} = 0.5V	--	1.2	25	μA	
EN Pin Current	I _{EN}	V _{IN} = 6.5V, V _{EN} = 0V and 6.5V	-0.1	--	0.1	μA	
EN Pin High-Level Input Voltage	V _{EN_H}	Enable device	1.1	--	6.5	V	
EN Pin Low-Level Input Voltage	V _{EN_L}	Disable device	0	--	0.5		
PGOOD Pin Threshold	V _{IT_PGOOD}	For the direction PGOOD signal falling with decreasing V _{OUT}	0.82 x V _{OUT}	0.883 x V _{OUT}	0.93 x V _{OUT}	V	
PGOOD Pin Hysteresis	V _{PGOOD_HYS}	For PGOOD signal rising	--	2% x V _{OUT}	--	V	
PGOOD Pin Low-Level Output Voltage	V _{PGOOD_L}	V _{OUT} < V _{IT_PGOOD} , I _{PGOOD} = -1mA (current into device)	--	--	0.4	V	
PGOOD Pin Leakage Current	I _{PGOOD_LK}	V _{OUT} > V _{IT_PGOOD} , V _{PGOOD} = 6.5V	--	--	1	μA	
NR/SS Pin Charging Current	I _{NR/SS}	V _{NR/SS} = GND, V _{IN} = 6.5V	4	--	9	μA	
FB Pin Leakage Current	I _{FB}	V _{IN} = 6.5V	-100	--	100	nA	
Power Supply Rejection Ratio	PSRR	V _{IN} - V _{OUT} = 0.4V, I _{OUT} = 3A, C _{NR/SS} = 100nF, C _{FF} = 10nF, C _{OUT} = 47μF//10μF//10μF	f = 10kHz, V _{OUT} = 0.8V	--	42	--	dB
			f = 500kHz, V _{OUT} = 0.8V	--	39	--	
			f = 10kHz, V _{OUT} = 5V	--	40	--	
			f = 500kHz, V _{OUT} = 5V	--	25	--	
Output Noise Voltage	e _{NO}	BW = 10Hz to 100kHz, I _{OUT} = 3A, C _{NR/SS} = 100nF, C _{FF} = 10nF, C _{OUT} = 47μF 10μF 10μF	V _{IN} = 1.1V, V _{OUT} = 0.8V	--	6.8	--	μV _{RMS}
			V _{IN} = 3.6V, V _{OUT} = 3.3V	--	10	--	
			V _{OUT} = 5V	--	16	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Shutdown Threshold	T _{SD}	Temperature increasing	--	160	--	°C
		Temperature decreasing	--	140	--	

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at $T_A = 25^\circ\text{C}$ on a high effective-thermal-conductivity four-layer test board in size of 70mm x 50mm with 1oz copper thickness. θ_{JC} is measured at the exposed pad of the package.

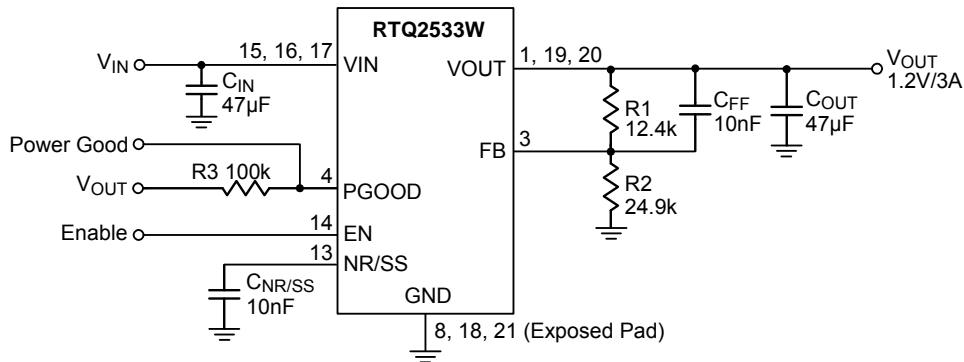
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. $V_{OUT(TARGET)}$ is the expected V_{OUT} value set by the external feedback resistors. The 50Ω load is disconnected when the test conditions specify an I_{OUT} value.

Note 6. External resistor tolerance is not taken into account.

Typical Application Circuit

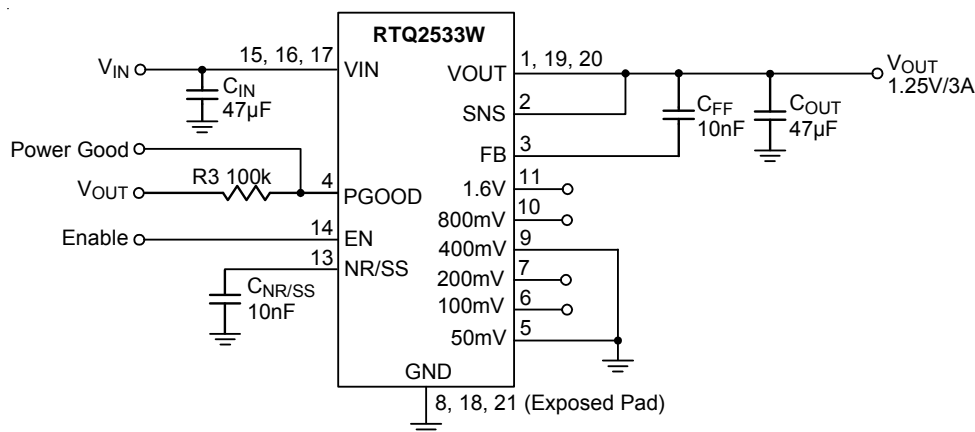


$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) = 0.8V \times \left(1 + \frac{12.4k}{24.9k}\right) = 1.2V$$

Figure 1. Configuration Circuit for V_{OUT} Adjusted by a Resistive Divider

Table 1. Recommended Feedback-Resistor Values

Output Voltage (V)	External Restive Divider Combinations	
	R1 (kΩ)	R2 (kΩ)
0.9	12.4	100
1	12.4	49.9
1.2	12.4	24.9
1.5	12.4	14.3
1.8	12.4	10
2.5	12.4	5.9
3.3	11.8	3.74
4.5	11.8	2.55
5	12.4	2.37



$$V_{OUT} = V_{REF} + 50mV + 400mV = 0.8V + 50mV + 400mV = 1.25V$$

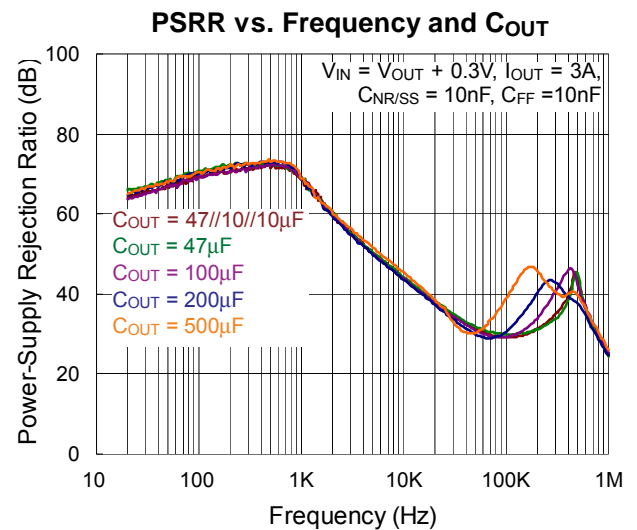
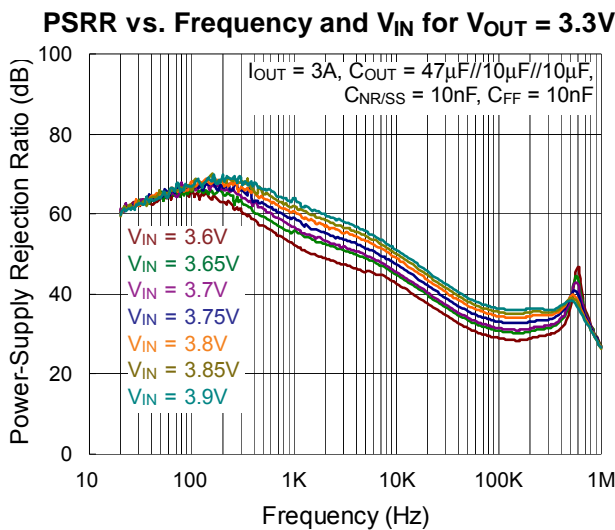
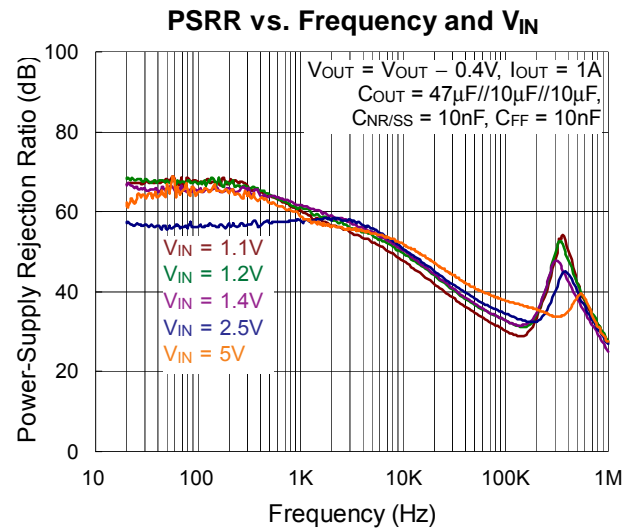
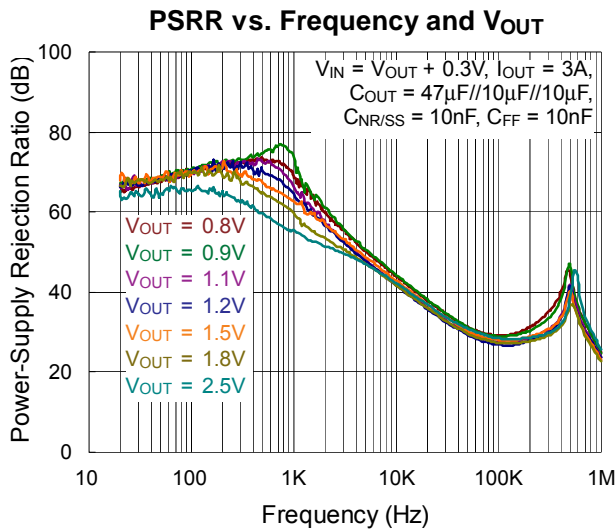
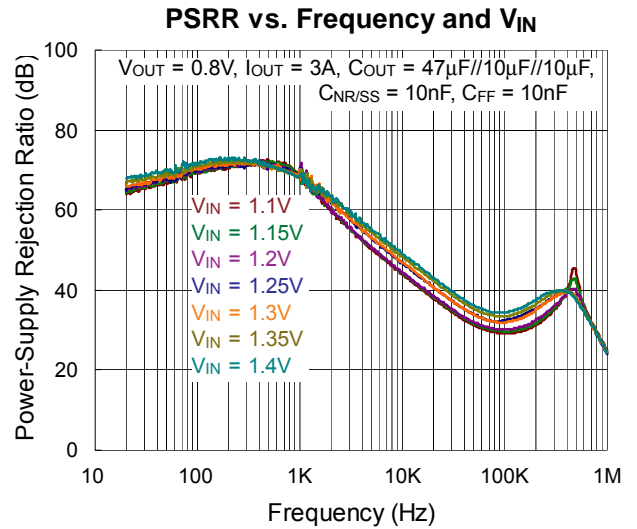
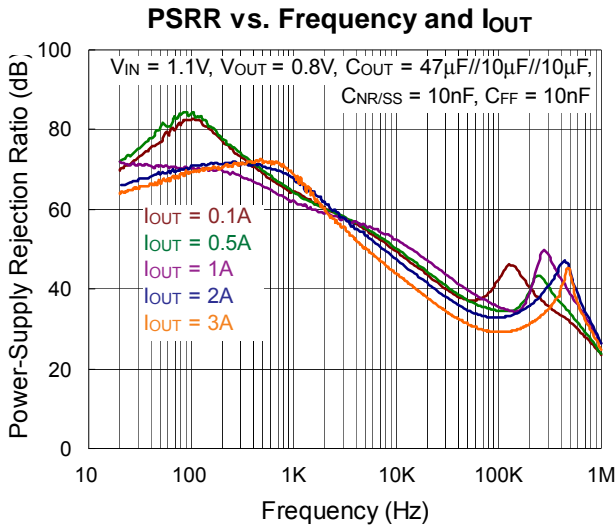
(Table 2. provides a full list for different V_{OUT} target and the corresponding pin settings.)

Figure 2. Configuration Circuit for V_{OUT} Adjusted via PCB Layout

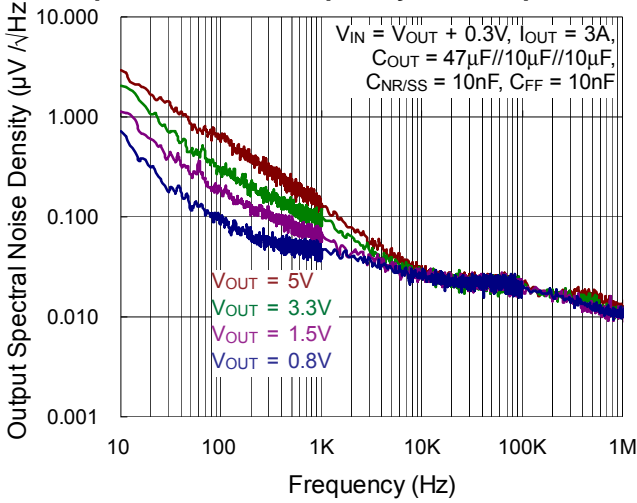
Table 2. V_{OUT} Select Pin Settings for Different Target

V _{OUT} (V)	50mV	100mV	200mV	400mV	800mV	1.6V	V _{OUT} (V)	50mV	100mV	200mV	400mV	800mV	1.6V
0.8	Open	Open	Open	Open	Open	Open	2.4	Open	Open	Open	Open	Open	GND
0.85	GND	Open	Open	Open	Open	Open	2.45	GND	Open	Open	Open	Open	GND
0.9	Open	GND	Open	Open	Open	Open	2.5	Open	GND	Open	Open	Open	GND
0.95	GND	GND	Open	Open	Open	Open	2.55	GND	GND	Open	Open	Open	GND
1	Open	Open	GND	Open	Open	Open	2.6	Open	Open	GND	Open	Open	GND
1.05	GND	Open	GND	Open	Open	Open	2.65	GND	Open	GND	Open	Open	GND
1.1	Open	GND	GND	Open	Open	Open	2.7	Open	GND	GND	Open	Open	GND
1.15	GND	GND	GND	Open	Open	Open	2.75	GND	GND	GND	Open	Open	GND
1.2	Open	Open	Open	GND	Open	Open	2.8	Open	Open	Open	GND	Open	GND
1.25	GND	Open	Open	GND	Open	Open	2.85	GND	Open	Open	GND	Open	GND
1.3	Open	GND	Open	GND	Open	Open	2.9	Open	GND	Open	GND	Open	GND
1.35	GND	GND	Open	GND	Open	Open	2.95	GND	GND	Open	GND	Open	GND
1.4	Open	Open	GND	GND	Open	Open	3	Open	Open	GND	GND	Open	GND
1.45	GND	Open	GND	GND	Open	Open	3.05	GND	Open	GND	GND	Open	GND
1.5	Open	GND	GND	GND	Open	Open	3.1	Open	GND	GND	GND	Open	GND
1.55	GND	GND	GND	GND	Open	Open	3.15	GND	GND	GND	GND	Open	GND
1.6	Open	Open	Open	Open	GND	Open	3.2	Open	Open	Open	Open	GND	GND
1.65	GND	Open	Open	Open	GND	Open	3.25	GND	Open	Open	Open	GND	GND
1.7	Open	GND	Open	Open	GND	Open	3.3	Open	GND	Open	Open	GND	GND
1.75	GND	GND	Open	Open	GND	Open	3.35	GND	GND	Open	Open	GND	GND
1.8	Open	Open	GND	Open	GND	Open	3.4	Open	Open	GND	Open	GND	GND
1.85	GND	Open	GND	Open	GND	Open	3.45	GND	Open	GND	Open	GND	GND
1.9	Open	GND	GND	Open	GND	Open	3.5	Open	GND	GND	Open	GND	GND
1.95	GND	GND	GND	Open	GND	Open	3.55	GND	GND	GND	Open	GND	GND
2	Open	Open	Open	GND	GND	Open	3.6	Open	Open	Open	GND	GND	GND
2.05	GND	Open	Open	GND	GND	Open	3.65	GND	Open	Open	GND	GND	GND
2.1	Open	GND	Open	GND	GND	Open	3.7	Open	GND	Open	GND	GND	GND
2.15	GND	GND	Open	GND	GND	Open	3.75	GND	GND	Open	GND	GND	GND
2.2	Open	Open	GND	GND	GND	Open	3.8	Open	Open	GND	GND	GND	GND
2.25	GND	Open	GND	GND	GND	Open	3.85	GND	Open	GND	GND	GND	GND
2.3	Open	GND	GND	GND	GND	Open	3.9	Open	GND	GND	GND	GND	GND
2.35	GND	GND	GND	GND	GND	Open	3.95	GND	GND	GND	GND	GND	GND

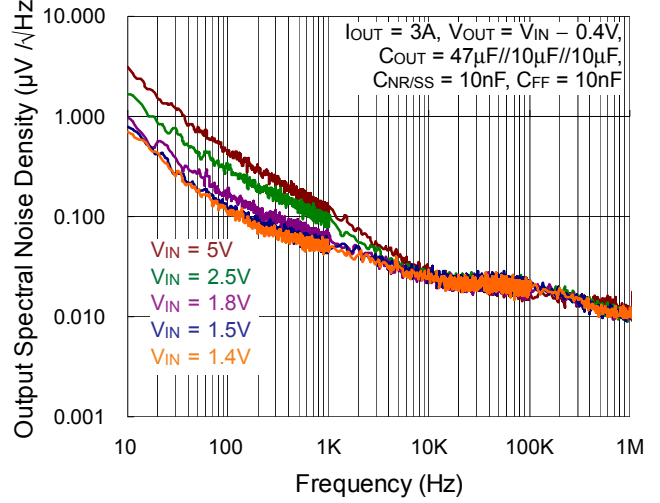
Typical Operating Characteristics



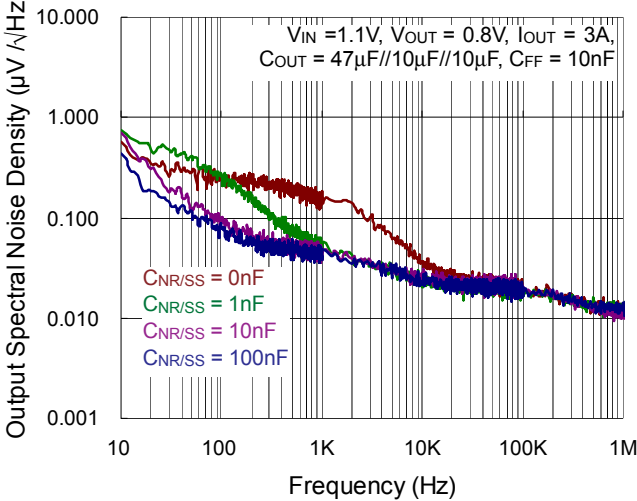
Output Noise vs. Frequency and Output Voltage



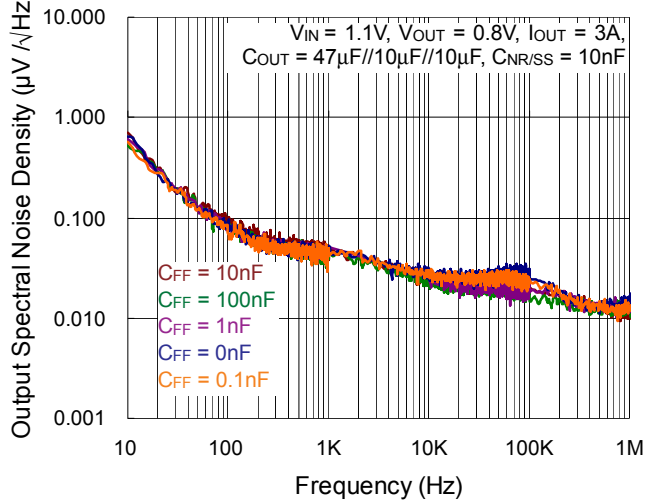
Output Noise vs. Frequency and Input Voltage



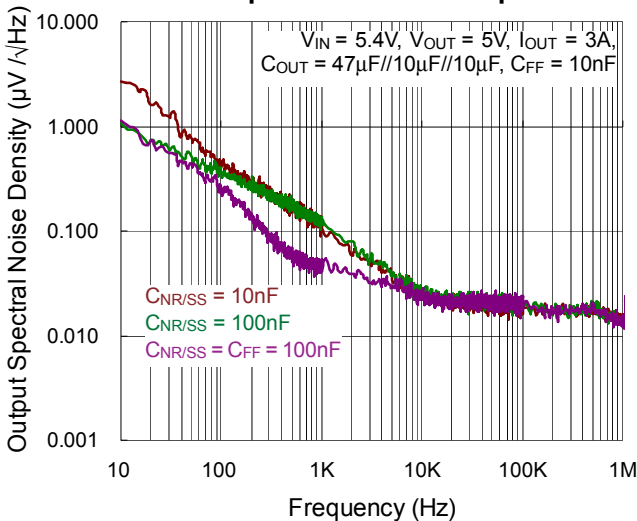
Output Noise vs. Frequency and CNR/SS



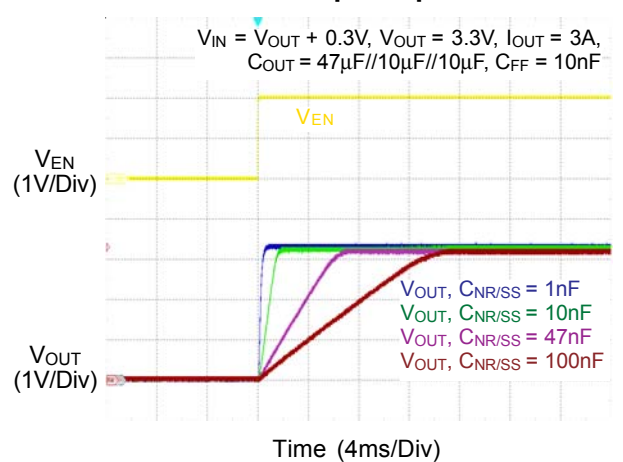
Output Noise vs. Frequency and CFF



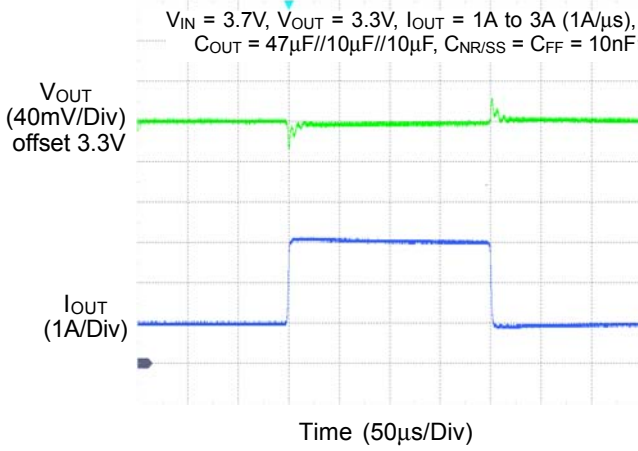
Output Noise at 5V Output



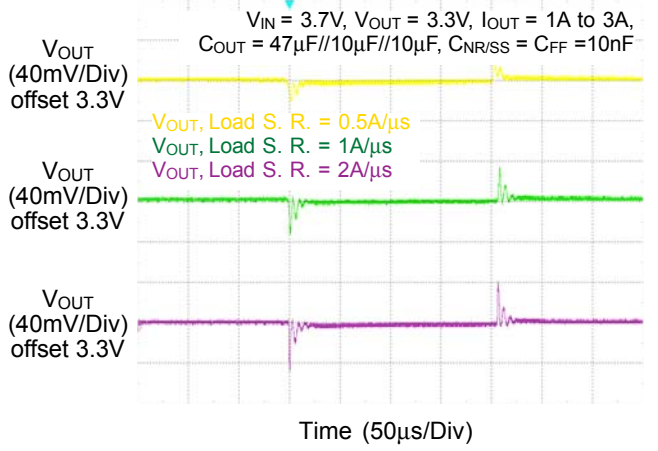
Power Up Response



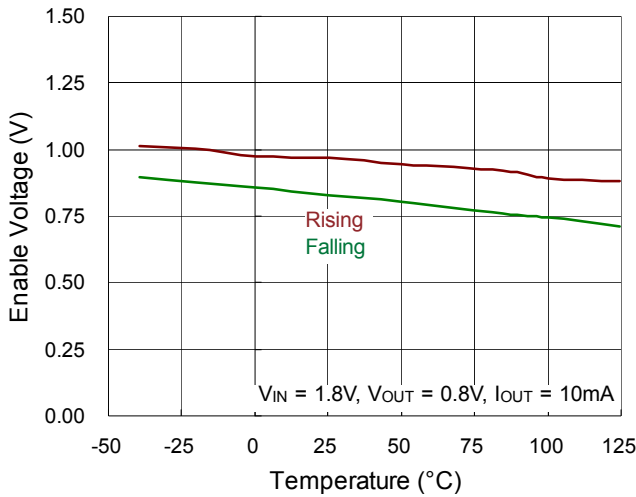
Load Transient Response



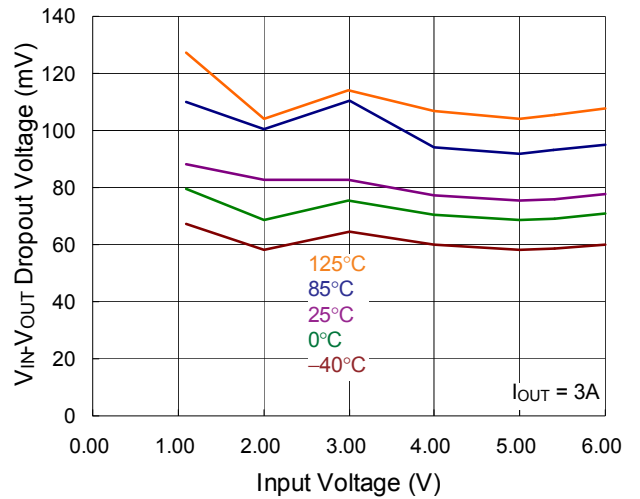
Load Transient Response vs. Load Slew Rate



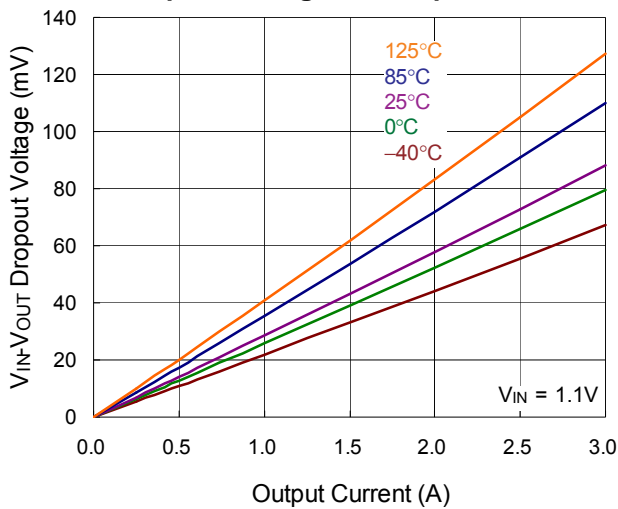
Enable Voltage vs. Temperature



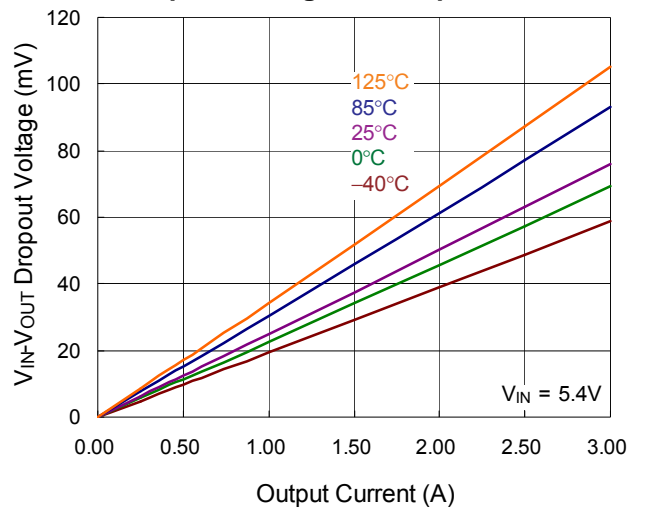
Dropout Voltage vs. Input Voltage



Dropout Voltage vs. Output Current



Dropout Voltage vs. Output Current



Application Information

The RTQ2533W is a high current, low-noise, high accuracy, low-dropout linear regulator which is capable of sourcing 3A with maximum dropout of 180mV. The input voltage operating range from 1.1V to 6.5V and adjustable output voltage from 0.8V to $(V_{IN} - V_{DROP})$ via external resistor setting or 0.8V to 3.95V via PCB Layout to short specific pins and get the required output target.

Output Voltage Setting

The output voltage of the RTQ2533W can be set by external resistors or by using the output voltage setting pins (50mV, 100mV, 200mV, 400mV, 800mV and 1.6V) to achieve different output targets.

Using external resistors, the output voltage is determined by the values of R1 and R2 as shown in Figure 3. The values of R1 and R2 can be calculated with any voltage value using the following formula :

$$V_{OUT} = 0.8 \times \frac{R1 + R2}{R2}$$

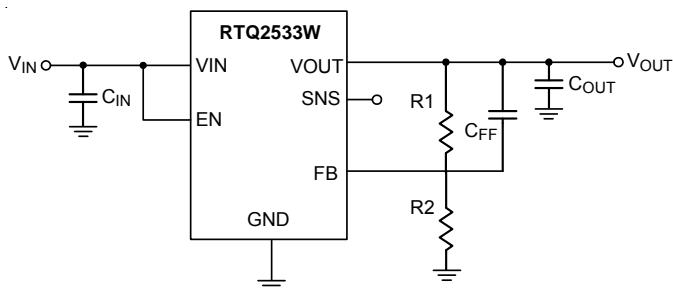


Figure 3. Output Voltage Set by External Resistors

The RTQ2533W can also short pins 5, 6, 7, 9, 10, and 11 to ground and program the regulated output voltage level without external resistors after the SNS pin is connected with the VOUT. Pins 5, 6, 7, 9, 10, and 11 are connected with internal resistor pairs, each pin is either connected to ground (active) or left open (floating).

Voltage programming is set as the sum of the internal reference voltage ($V_{REF} = 0.8V$) plus the accumulated sum of the respective voltages assigned to each active pin as illustrated in figure 4.

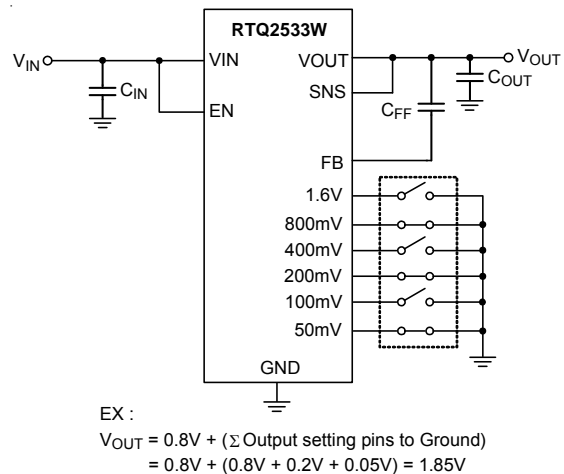


Figure 4. Output Setting without External Resistors

Table 2. summarizes these voltage values associated with each active pin setting for reference. By leaving all programming pins open, or floating, the output is thereby programmed to the minimum possible output voltage equal to V_{REF} (0.8V). The maximum output target can be supported up to 3.95V after all pins 5, 6, 7, 9, 10 are shorted with ground at the same time.

Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at a specific output current. The dropout voltage V_{DROP} also can be expressed as the voltage drop on the pass-FET at a specific output current (I_{RATED}) while the pass-FET is fully operating in the ohmic region and the pass-FET can be characterized as a resistance $R_{DS(ON)}$. Thus the dropout voltage can be defined as $(V_{DROP} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{RATED})$. For normal operation, the suggested LDO operating range is $(V_{IN} > V_{OUT} + V_{DROP})$ for good transient response and PSRR performance. Vice versa, operation in the ohmic region will degrade the performance severely.

CIN and COUT Selection

The RTQ2533W is designed to support low-series-resistance (ESR) ceramic capacitors. X7R, X5R, and COG-rated ceramic capacitors are recommended due to its good capacitive stability across different temperatures, whereas the use of Y5V-rated capacitors are discouraged because of large capacitance variations.

However, the capacitance of ceramic capacitors varies with

operating voltage and temperature and the design engineer must be aware of these characteristics. Ceramic capacitors are usually recommended to be derated by 50%. A 47µF or greater output ceramic capacitor (or 22µF effective capacitance) is suggested to ensure stability. Input capacitance is selected to minimize transient input drop during load current steps. For general applications, an input capacitor of at least 47µF is highly recommended for minimal input impedance. If the trace inductance between the RTQ2533W input supply is high, a fast load transient can cause VIN voltage level ringing above the absolute maximum voltage rating which damages the device. Adding more input capacitors is available to restrict the ringing and keep it below the device absolute maximum ratings.

Generally, a 47µF 0805-sized ceramic capacitor in parallel with two 10µF 0805-sized ceramic capacitor ensures the minimum effective capacitance at high input voltage and high output voltage requirement. Place these capacitors as close to the pins as possible for optimum performance and to ensure stability.

Feed-Forward Capacitor (C_{FF})

The RTQ2533W is designed to be stable without the external feed-forward capacitor (C_{FF}). However, a 10nF external feed-forward capacitor optimizes the transient, noise, and PSRR performances. A higher capacitance C_{FF} can be also used, but the start-up time is longer and the power-good signal can incorrectly indicate that the output voltage is settled.

Soft-Start and Noise Reduction (C_{NR/SS})

The RTQ2533W is designed for a programmable, monotonic soft-start time during the output rising, which can be achieved via an external capacitor (C_{NR/SS}) on NR/SS pin. Using an external C_{NR/SS} is recommended for general application, not only for the in-rush current minimization but also helps reduce the noise component from the internal reference.

During the monotonic start-up procedure, the error amplifier of the RTQ2533W tracks the voltage ramp of the external soft-start capacitor (C_{NR/SS}) until the voltage approaches the internal reference 0.8V. The soft-start ramp time can be calculated with Equation a1, which depends on the

soft-start charging current (I_{NR/SS}), the soft-start capacitance (C_{NR/SS}), and the internal reference 0.8V (V_{REF}).

$$t_{SS} = \frac{(V_{REF} \times C_{NR/SS})}{I_{NR/SS}} \quad (a1)$$

For noise-reduction, C_{NR/SS} in conjunction with an internal noise-reduction resistor forms a low-pass filter (LPF) and filters out the noise from the internal bandgap reference before being amplified via the error amplifier, thus reducing the total device noise floor.

Input Inrush Current

During start-up, the input inrush current into VIN pin consists of the sum of load current and the charging current of the output capacitor. The inrush current is difficult to measure because the input capacitor must be removed, which is not recommended. Generally, the soft-start inrush current can be estimated by Equation b1, where V_{OUT}(t) is the instantaneous output voltage of the power-on ramp, dV_{OUT}(t) / dt is the slope of the V_{OUT} ramp and R_{LOAD} is the resistive load impedance.

$$I_{OUT}(t) = \frac{(C_{OUT} \times dV_{OUT}(t))}{dt} + \left(\frac{V_{OUT}(t)}{R_{LOAD}} \right) \quad (b1)$$

Under-Voltage Lockout (UVLO)

The Under-Voltage Lockout (UVLO) threshold is the minimum input operational voltage range that ensures the device stays disabled. Figure 5 explain the UVLO circuits be triggered between three different input voltage events(duration a, b and c), assuming V_{EN} ≥ V_{EN,H} all the time. For duration "a", the input voltage starts rising and when VIN is over the UVLO rising threshold, V_{OUT} starts the power-on process, then when V_{out} reaches the target level it is under regulation. During "b", although the power line has a voltage drop, but does not cross UVLO low threshold (falling threshold), the device maintains normal operation, and V_{OUT} is still regulated. At duration "c" V_{IN} drops below the UVLO falling threshold, the control loop is disabled and there is no regulation; meanwhile V_{OUT} drops. For general application, instant power line transient with long power trace at the VIN pin may have V_{IN} level unstable and force a trap as shown in duration "c" which makes V_{OUT} collapse. In this case, adding more input capacitance or improving input trace layout on PCB are effective to improve input power stabilization.

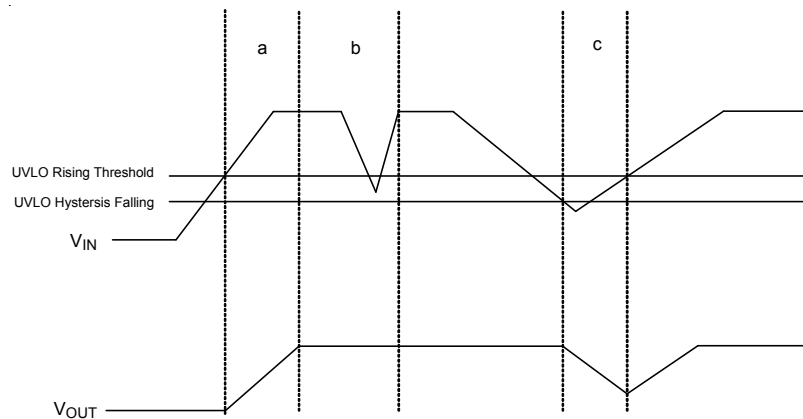


Figure 5. Under-Voltage Lockout Triggering Conditions and Output Variation

Power-Good (PGOOD) Function

The Power-Good function monitors the voltage level at the feedback pin to indicate that the output voltage status is normal or not, this function enables others devices receive the RTQ2533W's Power-Good signal as a logic signal that can be used for the sequence design of the system application. The PGOOD pin is an open-drain structure and an external pull-up resistor connected to an external supply is necessary. The pull-up resistor value between 10kΩ to 100kΩ is recommended for proper operation. The lower limit of 10kΩ results from the maximum pull-down strength of the power-good transistor, and the upper limit of 100kΩ results from the maximum leakage current at the power-good node.

Figure 6 demonstrates some PGOOD scenarios versus

VIN, EN and protection status. During "a", VEN is higher than the VEN_H threshold, and the device is under operation. In this period, VOUT starts rising (the rising time is related to the soft-start capacitor CNR/SS). When VOUT is over the PGOOD hysteresis threshold, the reflected feedback voltage VFB exceeds VPGOOD_HYS threshold, and consequently, the PGOOD pin becomes a high impedance node. The duration "b" indicates some unpredictable operation (ex : OTP, OCP or severe output voltage drop caused by very fast load variation). when VFB is lower than the VIT_PGOOD threshold, VPGOOD is pulled to GND, which indicates that the output voltage is not ready. In duration "c" VOUT has a small drop which is not lower than the PGOOD falling threshold; the PGOOD pin remains in high impedance. After VEN becomes logic "0" VPGOOD is pulled to GND as shown in duration "d".

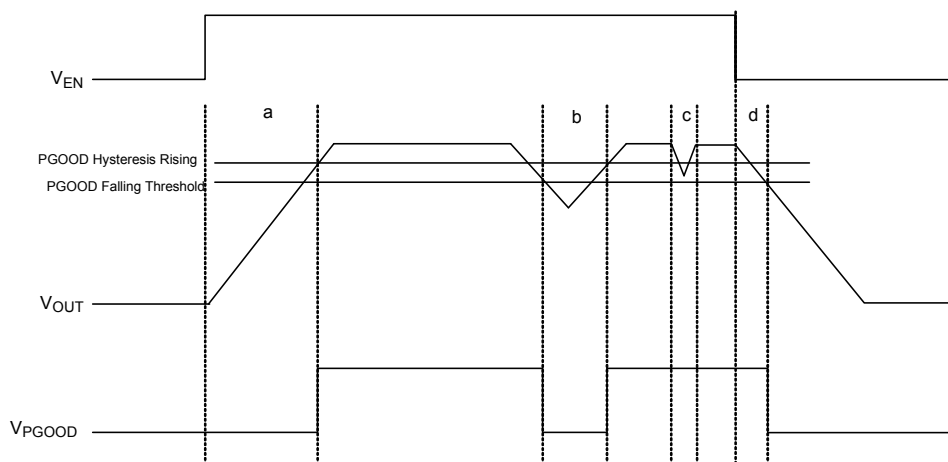


Figure 6. PGOOD Trigger Scenario with Different Operating Status

Reverse Current Protection

Reverse current from V_{OUT} to V_{IN} that flows through the body diode of the pass element instead of the normal conducting channel can happen if the maximum V_{OUT} exceeds $V_{IN} + 0.3V$; in this case, the pass element may be damaged.

For example, if the output is biased above the input supply voltage level or the input supply has an instant drop at light load operation that makes $V_{IN} < V_{OUT}$. As shown in Figure 7, an external Schottky diode could be added to prevent the pass element be damaged from the reverse current.

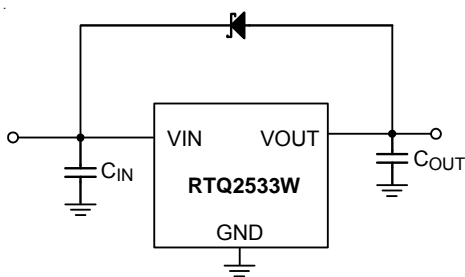


Figure 7. Application Circuit for Reverse Current Protection

Thermal Considerations

Thermal protection limits power dissipation in the RTQ2533W. When power dissipation on the pass element ($P_{DIS} = (V_{IN} - V_{OUT}) \times I_{OUT}$) is too high and raises the junction operation temperature over $160^{\circ}C$, the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass element turns on again after the junction temperature cools down by $20^{\circ}C$.

The output is shorted to ground when there is short circuit at the output. This procedure can reduce the chip temperature and provides maximum safety to end users when output short circuit occurs.

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be

calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is $125^{\circ}C$. The junction-to-ambient thermal resistance, θ_{JA} , is highly package dependent. For a VQFN-20L 3.5x3.5 package, the thermal resistance, θ_{JA} , is $36^{\circ}C/W$ on a high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A = 25^{\circ}C$ can be calculated as below :

$$P_{D(MAX)} = (125^{\circ}C - 25^{\circ}C) / (36^{\circ}C/W) = 2.78W \text{ for a VQFN-20L 3.5x3.5 package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA} . The derating curves in Figure 8 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

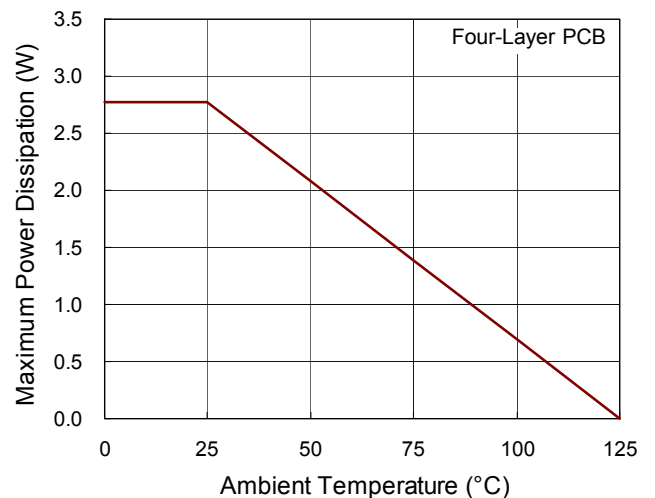


Figure 8. Derating Curve of Maximum Power Dissipation

Layout Considerations

For best performance of the RTQ2533W, the PCB layout suggestions below are highly recommend. All circuit components placed on the same side and as near to the respective LDO pin as possible. Place the ground return path connection to the input and output capacitor. Connect

the ground plane with a wide copper surface for good thermal dissipation. Using vias and long power traces for the input and output capacitors connections is discouraged and has negative effects on performance. Figure 9 shows a layout example that reduce conduction trace loops, helping to minimize inductive parasitics and load transient effects while improving the circuit stability.

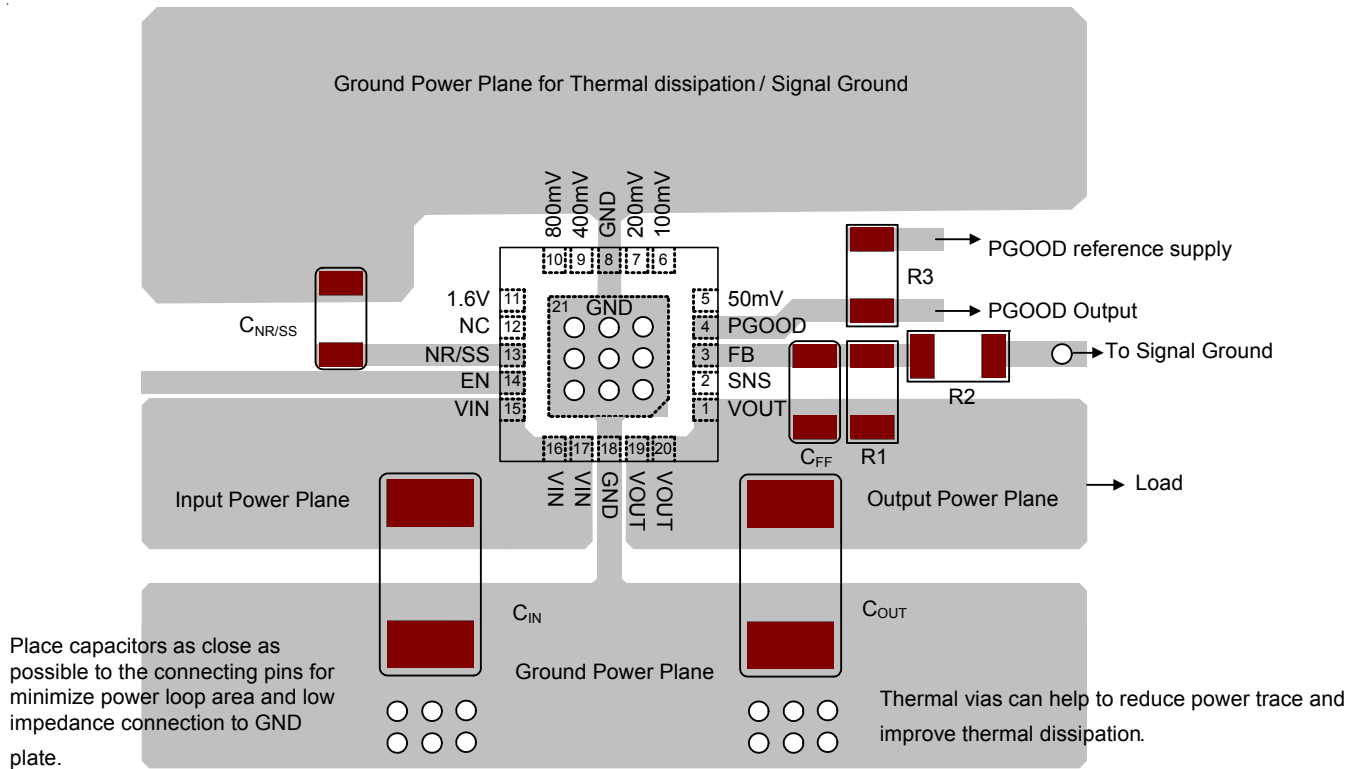
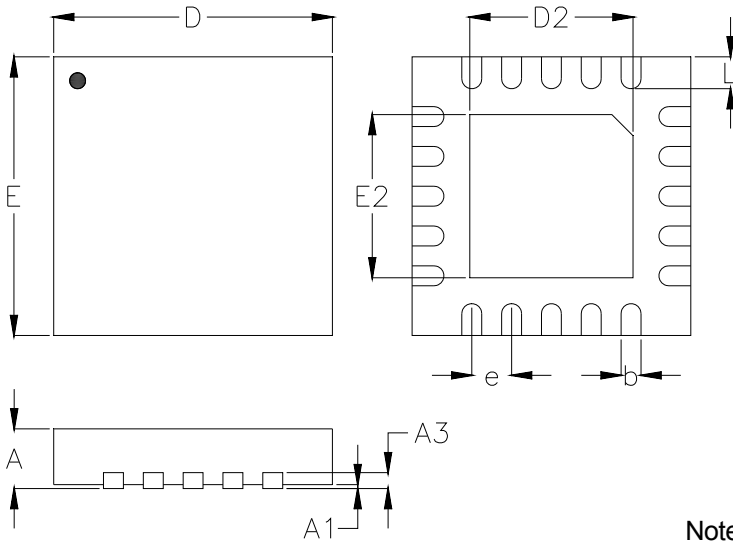


Figure 9. PCB Layout Guide

Outline Dimension



DETAIL A

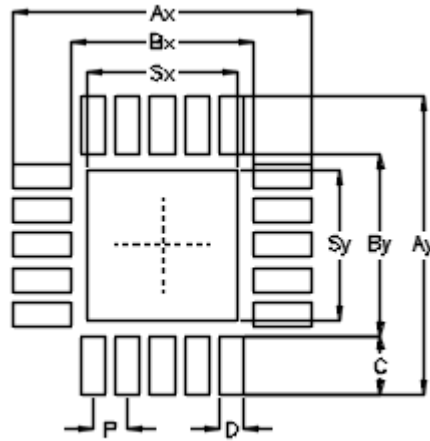
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	3.400	3.600	0.134	0.142
D2	2.000	2.100	0.079	0.083
E	3.400	3.600	0.134	0.142
E2	2.000	2.100	0.079	0.083
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 20L QFN 3.5x3.5 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN3.5*3.5-20	20	0.50	4.30	4.30	2.60	2.60	0.85	0.35	2.15	2.15	±0.05

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City
 Hsinchu, Taiwan, R.O.C.
 Tel: (8863)5526789

Richtek products are sold by description only. Customers should obtain the latest relevant information and data sheets before placing orders and should verify that such information is current and complete. Richtek cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Richtek product. Information furnished by Richtek is believed to be accurate and reliable. However, no responsibility is assumed by Richtek or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Richtek or its subsidiaries.