SE050

Plug & Trust Secure Element

Rev. 1.3 — 7 June 2019 Objective data sheet
504913

1 Introduction

The SE050 is a ready-to-use IoT secure element solution. It provides a root of trust at the IC level and it gives an IoT system state-of-the-art, edge-to-cloud security capability right out of the box.

SE050 allows for securely storing and provisioning credentials and performing cryptographic operations for security critical communication and control functions. SE050 is versatile in IoT security use cases such as secure connection to public/private clouds, device-to-device authentication or protection of sensor data.

SE050 has an independent Common Criteria EAL 6+ security certification up to OS level and supports both RSA & ECC asymmetric cryptographic algorithms with high key length and future proof ECC curves. The latest security measures protect the IC even against sophisticated non-invasive and invasive attack scenarios.

The SE050 is a turnkey solution that comes with Java Card operating system and an applet optimized for IoT security use cases pre-installed. This is complemented by a comprehensive product support package, enabling fast time to market & easy design-in with Plug & Trust middleware for host applications, easy to use development kits, reference designs, and extensive documentation for product evaluation.

The SE050 is a product platform that comes in several pin-to-pin compatible product variants, see [4].

Additional information on the integration can be found in several application notes on www.nxp.com. Also see [3].

1.1 SE050 use cases

- Secure connection to public/private clouds, edge computing platforms, infrastructure
- Device-to-device authentication
- Secure data protection
- Secure commissioning support
- Secure CL/MIFARE/Wi-Fi interactions
- Device ID for blockchain
- Secure key storage
- Secure provisioning of credentials
- Ecosystem protection

1.2 SE050 target applications

- Smart Industry
- Smart Home
- Smart Cities
- Smart Supply Chains

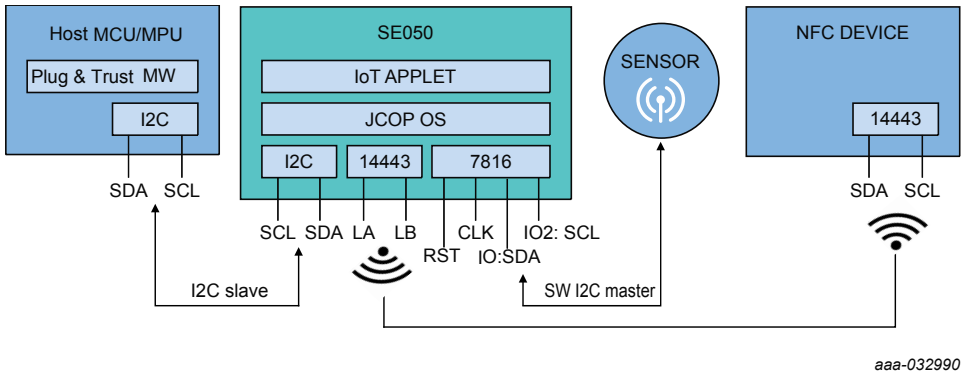

Figure 1. SE050 solution block diagram

Note: *SE050 is designed to be used as a part of an IoT system. It works as an auxiliary security device attached to a host controller. The host controller communicates with SE050 through an I²C interface (with the host controller being the master and the SE050 being the slave). Besides the mandatory connection to the host controller, the SE050 device can optionally be connected to a sensor node or similar element through a separate I²C interface. In this case, the SE050 device is the master and the sensor node the slave. Lastly, SE050 has a connection for a native contactless antenna, providing a wireless interface to an external device like a smartphone.*

1.3 SE050 naming convention

The following table explains the naming conventions of the commercial product name of the SE050 platform. Every SE050 product gets assigned a commercial name, which includes application specific data.

The SE050 commercial names have the following format.

Sx05yagddd/Zrrff

All letters are explained in Table 1 .

Table 1. SE050 commercial name format

Variable	Meaning	Values	Description
x	Interfaces	E	E=I^{2}C Slave, Master,
y	JCOP version	0	
a	Applet Config	A B C	Configuration options with different key provisioning options, see [4]
g	Temperature range	1 2	standard operational ambient temperature 1 = -25 °C - 90 °C , 2 = -40 °C - 105 °C
ddd	Delivery Type	HQ1	HX2QFN20
mrrff		Letters and numbers	NXP internal code to identify individual configurations

2 Features and benefits

2.1 Key benefits

- Plug & Trust for fast and easy design with complete product support package
- Easy integration with different MCU & MPU platforms and OS´ (Linux, RTOS, Windows, Android, etc.)
- Turnkey solution ideal for system-level security without the need to write security code
- Secure credential injection for root of trust at IC level
- Secure, zero-touch connectivity to public & private clouds
- Real end-to-end security, from sensor to cloud
- Ready-to-use example code for each of the key use cases

2.2 Key features

The SE050 is based on NXP's Integral Security Architecture 3.0™ providing a secure and efficient protection against various security threats. The efficiency of the security measures is proven by a Common Criteria EAL6+ certification.

The SE050 operates fully autonomously based on an integrated Javacard operating system and applet. Direct memory access is possible by the fixed functionalities of the applet only. With that, the content from the memory is fully isolated from the host system.

- Built on NXP Integral Security Architecture 3.0 ™
- Uses advanced 40 nm silicon foundry technology
- CC EAL 6+ certified HW and OS as environment to run NXP IoT applications, supporting fully encrypted communications and secured lifecycle management
- Effective protection against advanced attacks, including Power Analysis and Fault Attacks of various kinds
- Multiple logical and physical protection layers, including metal shielding, end-to-end encryption, memory encryption, tamper detection
- Support for RSA and ECC asymmetric cryptography algorithms, future proof curves and high key length, e.g. Brainpool, Edwards and Montgomery curves
- Support for AES and DES symmetric cryptographic algorithms for encryption and decryption
- HMAC, CMAC, SHA-1, SHA-224/256/384/512 operations
- Various options for key derivation functions, including HKDF, MIFARE KDF, PRF (TLS-PSK)
- Optional extended temperature range for industrial applications (-40 °C to +105 °C)
- Small footprint HX2QFN20 package (3x3 mm)
- Standard physical interface I^2C slave (High-speed mode, 3.4 Mbps), I^2C master (Fast mode, 400 kbps). Both can be active at the same time
- Dedicated CL wireless interface for IoT use cases simplifying configuration set-up, maintenance in the field and late stage configuration
- Secured user flash memory up to 50 kB for secure data or key storage
- Support for SCP03 protocol (bus encryption and encrypted credential injection) to securely bind the host with the secure element
- Support for applet level secure messaging channels to allow end-to-end encrypted communication in multi-tenant ecosystems

2.3 Features in detail

Table 2. Feature Overview

Categories	Subcategory	Value
Standards	Security certification	CC EAL6+ (HW+JCOP)
	JavaCard version	3.0.5
	GlobalPlatform specification version	GP 3.0
Cryptography	ECC	ECDSA, ECDH, ECDHE, ECDAA, EDDSA
	Hash	HMAC, secure HMAC, CMAC
	SHA	SHA-1, SHA-224, SHA-256, SHA-384, SHA-512
	Key derivation	HKDF, PBKDF, Wi-Fi KDF,OPC_UA KDF PRF (TLS-PSK)
	AES	AES cipher for de-/encryption
	RSA	RSA cipher for de-/encryption (up to 4096 bit)
Crypto curves	ECC	ECC NIST (192 to 521 bit)
		Brainpool (160 to 512 bit)
		Twisted Edwards Ed25519
		Montgomery Curve25519
		Koblitz (192 to 256 bit)
		Barreto-Naehrig Curve 256 bit
User memory		50 kB
Memory reliability		up to 100 Mio write cycles / 25 years
Interfaces	I^2C Slave	High-speed mode (3.4 Mbps)
	I^2C Master	Fast Mode (400 kbit/s)
	Contactless	ISO14443
Power saving modes	Idle	~1.8 mA
	Power-Down (with state retention)	~430 µA
	Deep Power-Down (no state retention)	<5 µA
Temperature	Standard	-25 - 85 °C
	Extended	-40 - +105 °C
Packaging	Plastic QFN	3x3 mm (HX2QFN20)

3 Functional description

3.1 Functional diagram

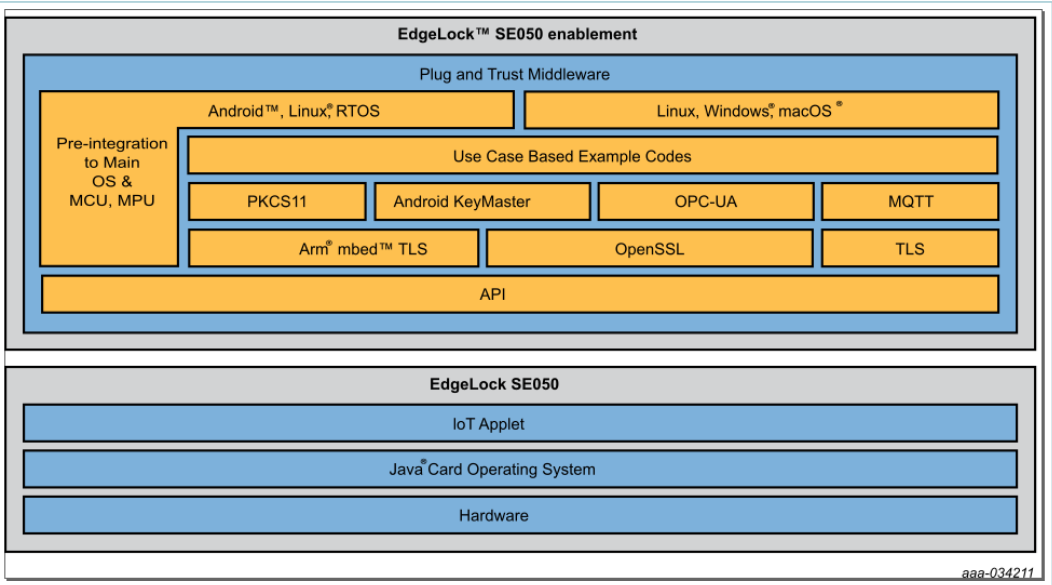

Figure 2. SE050 functional diagram - example Open SSL

The SE050 uses I^2C as communication interface. Section 4 gives more details. The SE050 commands are wrapped using the Smartcard T=1 over I²C (T=1o I^2C) protocol. The detailed documentation of the SE050 commands (see [3]) and T=1 over I^2C protocol encapsulation is available in NXP DocStore.

In order to simplify the product usage a host library which abstracts for SE050 commands and T=1 over I^2C protocol encapsulation is provided. The host library supporting various platforms is available for download including complete source code on the SE050 website.

SE050 IoT applet features a generic file system capable of securely storing secure objects and associated privilege management. All objects can either be stored in persistent memory or in RAM with the capability to securely export and import them to be stored in an externally provided storage. All secure objects feature basic file operations such as write, read, delete and update.

3.1.1 Supported secure object types

A secure object is an entry in the file system of SE050. Each secure object has certain features and capabilities. The following secure object types are available:

- Symmetric Key (AES, DES)
- ECC Key
- RSA Key
- HMAC Key
- Binary File
- User ID
- Counter

- Hash-Extend register

3.1.1.1 Symmetric Key

The Symmetric Key object can securely store symmetric keys of AES 128, 192 and 256 bit and DES keys with single DES, 2K3DES and 3K3DES. The following specific operations are available on symmetric key objects:

- Encrypt
- Decrypt
- Derive
- CMAC
- Secure Import

3.1.1.2 ECC Key

The ECC Key object has the ability to securely store ECC keys of the following curves and key sizes:

- ECC NIST curve: NIST P-192, NIST P-224, NIST P-256, NIST P-384, NIST P-521
- ECC Brainpool curve: 160 bit, 192 bit, 224 bit, 256 bit, 320 bit, 384 bit, 512 bit
- ECC Ed25519 curve: 256 bit
- ECC Montgomery Curve25519: 256 bit
- ECC Koblitz curves: secp160k1, secp192k1, secp224k1, secp256k1
- ECC curves: secp192r1, secp224r1, secp256r1, secp384r1, secp521r1
- ECC Barreto-Naehrig 256 bit curve

The following operations are available on ECC key objects (not all operations are applicable to all curves):

- ECDSA/EDDSA Sign
- ECDSA/EDDSA Verify
- ECDH Generate Shared Secret
- ECDAA Sign
- ECDAA Verify
- Generate Key
- Secure Import

3.1.1.3 RSA Key

The RSA Key object has the ability to securely store RSA Keys up to 4096 bit. The following specific operations are available on RSA key objects:

- RSA Sign
- RSA Verify
- RSA Encrypt
- RSA Decrypt
- Secure Import

3.1.1.4 HMAC Key object

An HMAC key object allows to securely store an HMAC key. The following operations are supported on HMAC Key objects to compute an HMAC:

- Init

- Update
- Finalize

3.1.1.5 Binary file objects

Binary file objects are byte arrays of a generic type. As in a standard file system, the values can be accessed using read/write operations.

3.1.1.6 Counter Objects

Counter objects are special kinds of binary file objects with specific functionality interpreting the content of the file.

The supported operations for counters are:

- Set
- Get
- Increment

3.1.1.7 Hash-Extend register

A hash-extend register secure object stores a hash over all data provided to that secure object. It therefore contains the complete history of values provided to that register since last reboot or since creation and can be used for attestation purposes.

3.1.1.8 User ID secure object

User ID secure objects can be used to create sessions based on the User ID in cases where multi-tenant support without cryptographic credential usage is required.

3.1.2 Access control

Each secure object can be linked to object specific access control policies. An access control policy associates a user identified by an authentication with a set of privileges such as read, write, …

To scale the functionality into a broad range of ecosystems, a set of different authentication options is provided:

- User-ID based authentication
- Symmetric key based authentication with and without secure messaging
- Asymmetric key based authentication with and without secure messaging
  At creation of a secure object, an optional set of policies is associated with that secure object. Each policy assigns a set of allowed operations on that object to an authentication object.

3.1.3 Sessions and multi-threading

The SE050 IoT applet is prepared for ecosystems where multi-threading and multi-tenant use cases are needed on APDU level. To enable that, the applet supports 2 simultaneous sessions that can span full secure messaging sessions, self-authenticated APDUs for tenants not requiring long-lasting sessions and on top one default session for single tenant use cases .

3.1.4 Attestation and trust provisioning

SE050 applet comes with a set of trust provisioned root credentials allowing the owner of the device to securely attest all generated secure keys. Next to that, a customer has the possibility to define own attestation keys.

3.1.5 Application support

For specific ecosystems, SE050 IoT applet has built-in crypto features to simplify the deployment of specific use cases such as

- MIFARE SAM functionality
- Wifi password protection
- ECC-Key and RSA-Key based cloud connectivity
- Secure Sensor readout using I^2C master
- Remote attestation and trust provisioning
- Platform Configuration Registers

3.2 Credential Storage & Memory

Within SE050, all credentials and secure objects are stored inside a dynamic file structure. At creation, a user has to associate a file identifier with the object created. This identifier is then used in subsequent operations to access the object. The number of objects that can be allocated is only limited by the available memory in the system. After usage, objects can be deleted and the associated memory is freed up again.

There is also the possibility to create transient objects. Transient objects have an object descriptor stored in non-volatile memory, but the object content is stored in RAM. Together with the import/export functionality of SE050, transient objects can be used securely store secret keys in a remote memory system.

3.3 Ease of use configuration

All SE050 variants are offered pre-configured for ease of use during development phase.

Therefore customers have all keys pre-injected in SE050 that are required for the main use cases.

4 Communication interfaces

4.1 I^2C Interfaces

The SE050 has one I^2C interface supporting slave and one I^2C interface supporting master mode.

The I^2C slave interface is the main communication interface of the device and is used by the host controller to send arbitrary APDUs to the device. It supports clock frequencies up to 3.4 MHz when operated in High-Speed Mode (HS). The I^2C interface is using the Smartcard T=1 over I^2C protocol.

The default slave address of the SE050 is configured to 0x48.

The I^2C master interface is supposed to be used with slave devices that need to be securely written and read. This interface features a maximum SCL clock rate of 400 kHz.

4.1.1 Supported I²C frequencies

The SE050 I²C slave interface supports the I²C high-speed mode with a maximum SCL clock of up to 3.4 MHz when clock stretching is enabled.

In case clock stretching is disabled the maximum supported SCL clock frequency is 1.7 MHz.

Clock stretching is enabled by default. Clock stretching will occur for frequencies higher than 600 kHz. In case clock stretching is not supported by the I²C master a dedicated configuration with disabled clock stretching has to be used to ensure the above mentioned maximum clock frequency.

The SE050 I²C master interface supports maximum 400 kHz SCL clock frequency.

4.2 ISO7816 and ISO14443 Interface

The SE050 supports in addition to the I²C interface ISO7816 and ISO14443 Smartcard interfaces. For the ISO7816 interface SmartCard protocols T=0 and T=1 are supported. For the ISO14443 interface protocol T=CL is used. The supported resonance input capacitance is 56 pF. In addition one additional GPIO pad IO2 is supported.

The RST_N pin can only be used as external reset source if the ISO7816 interface is enabled. If only the I²C interface is enabled the RST_N pad has no effect. If the SE050 is kept in reset state the current consumption is as defined for idle, see Table 12.

5 Power-saving modes

The device provides two power-saving operation modes. The Power-down mode (with state retention) and the Deep Power-down mode (no state retention). These modes are activated via pad ENA (Deep Power-down mode) or by the SW (Power-down mode).

5.1 Power-down mode

The Power-down mode has the following properties:

- All internal clocks are frozen
- CPU enters power-saving mode with program execution being stopped
- CPU registers keep their contents
- RAM keeps its contents

The SE050 enters into Power-down mode by receiving "End of APDU session request" via the T=1 over I²C protocol. In Power-down mode, all internal clocks are frozen. The IOs hold the logical states they had at the time Power-down mode was activated.

There are two ways to exit from the Power-down mode:

- A reset signal on RST_N (in case the ISO7816 interface is enabled). After wake-up from Power-down mode via RST_N the device is in idle mode (see Table 12)
- An external interrupt edge triggered by a falling edge on I²C_SDA

5.2 Deep Power-down mode

The SE050 provides a special power-saving mode offering maximum power saving. This mode is activated by pulling enable PIN (ENA) to a logic zero level.

While in Deep Power-down mode the internal power is switched off completely and only the I^2C pads stay supplied.

To leave the Deep Power-down mode pad ENA has to be pulled up to to a logic „1" level.

For usage of Deep Power-down mode the SE050 must be supplied via pad V_{in} and pad V_{out}.

6 Ordering information

6.1 Ordering options

Table 3. SE050 Ordering information

12NC	Type number	SE050 Variant	Orderable part number
9353 867 22472	SE050A1HQ1/Z01SG	SE050A1	SE050A1HQ1/Z01SGZ
9353 869 84472	SE050A2HQ1/Z01SH	SE050A2	SE050A2HQ1/Z01SHZ
9353 869 85472	SE050B1HQ1/Z01SE	SE050B1	SE050B1HQ1/Z01SEZ
9353 869 86472	SE050B2HQ1/Z01SF	SE050B2	SE050B2HQ1/Z01SFZ
9353 869 87472	SE050C1HQ1/Z01SC	SE050C1	SE050C1HQ1/Z01SCZ
9353 869 88472	SE050C2HQ1/Z01SD	SE050C2	SE050C2HQ1/Z01SDZ

Table 4. SE050 Ordering information for development kit

12NC	Type number	Description
9353 832 82598	OM-SE050ARD	SE050 Arduino-compatible development kit , SE050C configuration

6.2 Ordering SE050 samples

Samples can be ordered from NXP Semiconductors via nxp.com using the "Buy Direct" button on the product information page for SE050. Note that NXP Semiconductors can provide up to five pieces free of charge. Larger quantities have to be ordered commercially.

6.3 Configuration

Detailed information about the configuration and available variants of the SE050 are available in a separate NXP Application Note, see [4]

7 Pinning information

7.1 Pinning

7.1.1 Pinning HX2QFN20

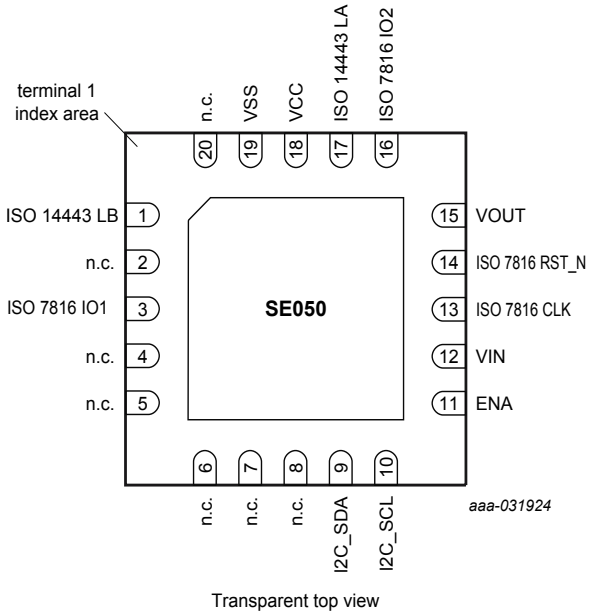

Figure 3. Pin configuration for HX2QFN20 (SOT1969-1)

Table 5. Pin description HX2QFN20

Symbol	Pin	Description
ISO 14443 LB	1	ISO14443 Antenna Connection
n.c.	2	not connected
ISO 7816 IO1	3	ISO 7816 IO or GPIO or I^2C master SDA
n.c.	4	not connected
n.c.	5	not connected
n.c.	6	not connected
n.c.	7	not connected
n.c.	8	not connected
I^2C_SDA	9	I^2C slave data
I^2C_SCL	10	I^2C slave clock
ENA	11	Deep Power-down mode enable
VIN	12	power supply voltage input for I^2C pads and ISO 7816/14443 interface and logic supply in case Deep Power-down mode is used
ISO 7816 CLK	13	ISO 7816 clock input
ISO 7816 RST_N	14	ISO 7816 reset input low active

Symbol	Pin	Description
VOUT	15	supply voltage output to be connected with pad VCC on PCB level, if Deep Power-down mode is used
ISO 7816 IO2	16	ISO7816 IO2 and GPIO pad or I^2C master SCL
ISO 14443 LA	17	ISO14443 antenna connection
VCC	18	logic and ISO7816/ISO1443 interface power supply voltage input, to be connected with pad Vout on PCB level, if Deep Power-down mode to be used
VSS	19	ground
n.c.	20	not connected

The center pad of the IC is not connected, although it is recommended to connect it to ground for thermal reasons.

8 Package

SE050 is offered in HX2QFN20 package. The dimensions are 3 mm x 3 mm x 0,32 mm with a 0,4 mm pitch.

Please refer to the package data sheet [2], SOT1969-1.

9 Marking

Table 6. Marking codes

Type number	Marking code
Sx050...	Line A: S50 Line B: ***** (***** = 5-digit Batch code) Line C: nDyww D: RHF-2006 indicator n: Assembly Center Y: Year WW: Week

10 Packing information

10.1 Reel packing

The SE050 product is available in tape on reel.

Table 7. Reel packing options

Symbol	Parameter	Numbers of units per reel
HX2QFN20	7" tape on reel	3000

11 Electrical and timing characteristics

The electrical interface characteristics of static (DC) and dynamic (AC) parameters for pads and functions used for I^2C are in accordance with the NXP I^2C specification (see [1]).

12 Limiting values

Table 8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to VSS (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			-0.3	+6 [1]	V
V_I	input voltage	any signal pad		-0.3	+6	V
I_I	input current	pad I^2C_SDA, I^2C_SCL		-	10	mA
I_O	output current	pad I^2C_SDA, I^2C_SCL		-	10	mA
I_{lu}	latch-up current	$V_I < 0$ V or $V_I > V_{DD}$		-	100	mA
V_{esd_hbm}	electrostatic discharge voltage (Human Body Model)	pads VCC, VSS, RST_N, I^2C_SDA, I^2C_SCL	[2]		± 2.0	kV
V_{esd_cdm}	electrostatic discharge voltage (Charge Device Model)	pads VCC, VSS, RST_N, I^2C_SDA, I^2C_SCL	[3]		± 500	V
P_{tot}	Total power dissipation		[4]	-	600	mW
T_{stg}	Storage temperature			-55	+125	°C

[1] Maximum supported supply voltage is 6 V. The SE050 is characterized for the specified operating supply voltage range of 1.62 V to 3.6 V.In case of supply voltages above 3.6 V, Deep Power-down mode current <5 µA is not guaranteed.
[2] MIL Standard 883-D method 3015; human body model; C = 100 pF, R = 1.5 kΩ; T_{amb} = -40 °C to +105 °C.
[3] JESD22-C101, JEDEC Standard Field induced charge device model test method.
[4] Depending on appropriate thermal resistance of the package.

13 Recommended operating conditions

The SE050 is characterized by its specified operating supply voltage range of 1.62 V to 3.6 V.

Table 9. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	Nominal supply voltage	1.62	1.8	3.6 [1]	V
V_I	DC input voltage on digital inputs and digital I/O pads	-	-0.3		V_{DD} +0.3	V
H	Field strength	Contactless interface operation	1.5		7.5	A/m
T_{amb}	Operating ambient temperature[2]		-40		+105	°C

[1] Maximum supported supply voltage is 6 V. In case of supply voltages above 3.6 V, Deep Power-down mode current <5 µA is not guaranteed.
[2] All product properties and values specified within this data sheet are only valid within the operating ambient temperature range.

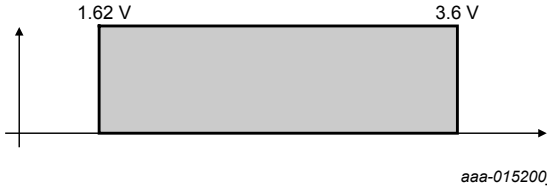

Figure 4. Characteristic supply voltage operating range

[1]

14 Characteristics

14.1 DC characteristics

Measurement conventions

Testing measurements are performed at the contact pads of the device under test. All voltages are defined with respect to the ground contact pad VSS. All currents flowing into the device are considered positive.

14.1.1 General and General Purpose I/O interface

Table 10. Electrical DC characteristics of Input/Output: IO1/IO2. Conditions: V_{DD} = 1.62 V to 3.6 V (see ; V_{SS} = 0 V; T_{amb} = -40 °C to + 105 °C, unless otherwise specified

Maximum supported supply voltage is 6 V. In case of supply voltages above 3.6 V, Deep Power-down mode current <5 µA is not guaranteed.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH level input voltage			0.7 V_{DD}		V_{DD} + 0.3	V
V_{IL}	LOW level input voltage			-0.3		0.25 V_{DD}	V
I_{IH}	HIGH level input current in "weak pull-up" input mode	0.7 V_{DD} ≤ V_I ≤ V_{DD} Test conditions for the maximum absolute value: $I_{IH(max)}$:V_I = 0.7 V_{DD}, V_{DD}=$V_{DD(max)}$				-20	µA
I_{IL}	LOW level input current	0 V ≤ VI ≤ 0.3 V_{DD}; Test conditions for the maximum absolute value: $I_{IL(max)}$:V_I = 0 V, V_{DD} = $V_{DD(max)}$				-50	µA
I_{TL}	HIGH-to-LOW transition input current (only "quasi-bidirectional" mode)	0.3 V_{DD} < V_I ≤ V_{DD}; Test conditions for the maximum absolute value: V_I = 0.5 V_{DD}, V_{DD} = $V_{DD(max)}$	[1]			-250	µA

1 Maximum supported supply voltage is 6 V. In case of supply voltages above 3.6 V, Deep Power-down mode current <5 µA is not guaranteed.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_I	Input current in "weak pull-up" input mode	0 V ≤ V_I ≤ V_{DD}; Test conditions for the maximum absolute value: $I_{I(max)}$:V_I = 0 V, V_{DD} = $V_{DD(max)}$		0		-50	µA
I_{ILIH}	Leakage input current at input voltage beyond V_{DD} in "weak pull-up" input mode	V_{DD} < V_I ≤ V_{DD} + 0.3 V; -40 °C ≤ T_{amb} ≤ +105 °C; Test conditions: V_I = V_{DD} + 0.3 V; V_{DD} = $V_{DD(max)}$$T_{amb}$ = +105 °C				20	µA
I_{ILIL}	Leakage input current at input voltage below V_{SS} in "weak pull-up" input mode	-0.3 V ≤ V_I < 0 V; -40 °C ≤ T_{amb} ≤ +30 °C Test conditions: V_I = -0.3 V; V_{DD}= $V_{DD(max)}$$T_{amb}$ = +30 °C				-50	µA
		-0.3 V ≤ V_I < 0 V;+30 °C ≤ T_{amb} ≤ +105 °C Test conditions: V_I = -0.3 V; V_{DD}= $V_{DD(max)}$$T_{amb}$ = +105 °C				-1000	µA
I_{ILIHQ}	Leakage input current at input voltage beyond V_{DD} (only in "quasi-bidirectional" mode)	V_{DD} < V_I ≤ V_{DD} + 0.3 V; -40 °C ≤ T_{amb}≤ +105 °C Test conditions: V_I = V_{DD} + 0.3 V;V_{DD} = $V_{DD(max)}$; T_{amb} = +105 °C				100	µA
I_{ILILQ}	Leakage input current at input voltage below V_{SS} (only in "quasi-bidirectional" mode)	-0.3 V ≤ V_I < 0 V; -40 °C ≤ T_{amb} ≤ +30 °C Test conditions: V_I = -0.3 V; V_{DD} = $V_{DD(max)}$$T_{amb}$= +30 °C				-120	µA
		-0.3 V ≤ V_I < 0 V;+30 °C ≤ T_{amb} ≤ +105 °C Test conditions: V_I = -0.3 V; V_{DD} = $V_{DD(max)}$$T_{amb}$= +105 °C				-1000	µA
V_{OH}	HIGH level output voltage	I_{OH} = -20 µA;	[2]	0.7 V_{DD}			V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OL}	LOW level output voltage	I_{OL} = 1.0 mA I_{OL} = 0.5 mA				0.3 0.15 V_{DD}	V

[1] IO1/IO2 source a transition current when being externally driven from HIGH to LOW. This transition current (I_{TL}) reaches its maximum value when the input voltage V_I is approximately 0.5 V_{DD}. Current IIL is tested at input voltage V_I= 0.3 V. Figure 6 shows the input characteristic of this quasi-bidirectional port mode.

[2] External pull-up resistor 20 kΩ to V_{DD} assumed. The worst case test condition for parameter V_{OH} is present at minimum V_{DD}.

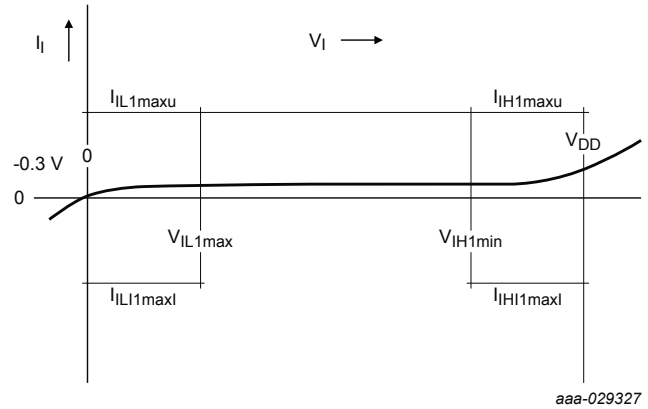

Figure 5. Input characteristic of RST_N

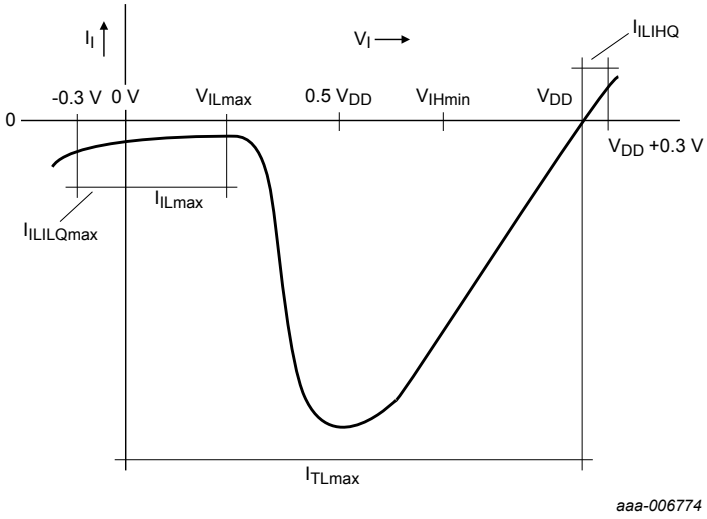

Figure 6. Input characteristic of IO1/IO2 in "quasi-bidirectional" mode

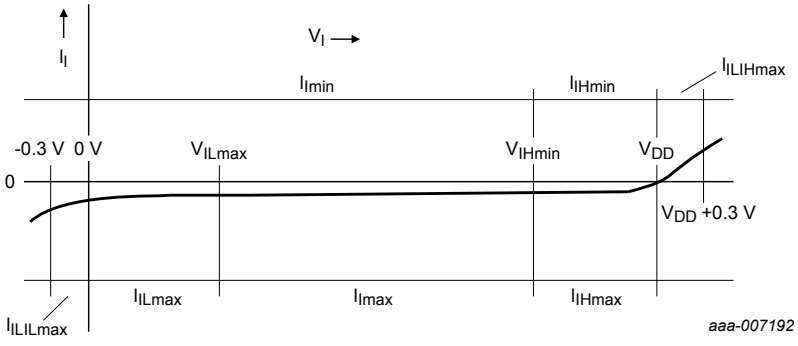

Figure 7. Input characteristic of IO1/IO2 in "weak pull-up" mode

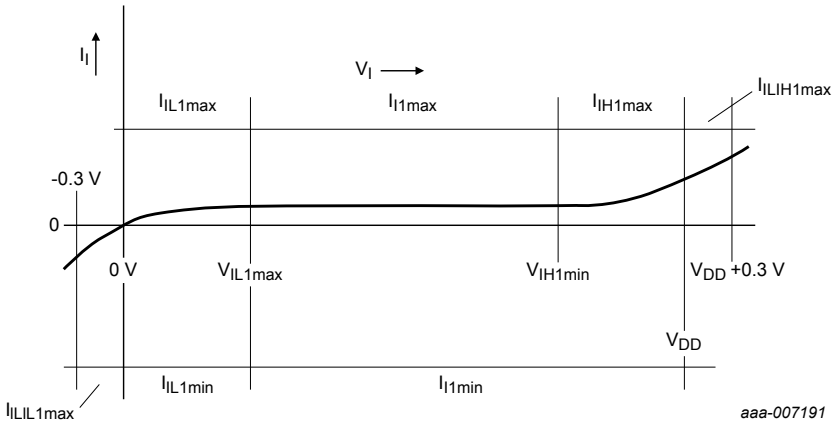

Figure 8. Input characteristic of CLK when the IC is not in reset and of RST_N

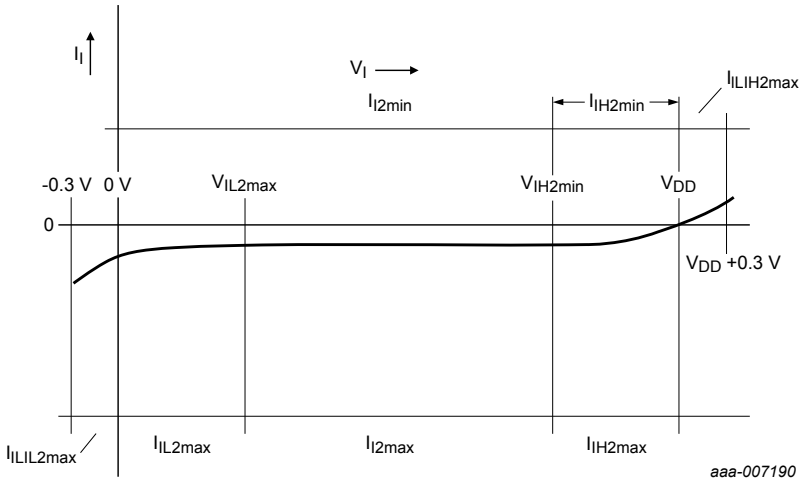

Figure 9. Input characteristic of CLK during IC reset

14.1.2 I^2C Interface

Table 11. Electrical DC characteristics of I^2C pads SDA, SCL. Conditions: V_{DD} = 1.62 V to 3.6 V; V_{SS} = 0 V; T_{amb} = -40 °C to + 105 °C, unless otherwise specified*

Maximum supported supply voltage is 6 V. In case of supply voltages above 3.6 V, Deep Power-down mode current <5 µA is not guaranteed.

SCL, SDA pads either in open-drain or push-pull mode (I^2C Master high-speed mode only).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH level input voltage			0.7 V_{DD}		V_{DD} + 0.3	V
V_{IL}	LOW level input voltage			-0.3		0.25 V_{DD}	V
$V_{OH(PP)}$	HIGH level output voltage (push-pull-mode)	I_{OH} = 3 mA;		0.7 V_{DD}			V
$V_{OL(PP)}$	LOW level output voltage (push-pull mode)	I_{OL} = 3.0 mA				0.3	V
V_{HYS}	Input hysteresis voltage	-		0.081 V			V
$V_{OL(OD)}$	Low level output voltage (open-drain mode)	I_{OL} = 3.0 mA		0		0.4	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{OL(OD)}$	Low level output current (open-drain mode)	V_{OL} = 0.6 V		0.6			mA
I_{WPU}	weak pull-up current	V_{IO} = 0 V		-265	-180	-70	µA
I_{WPD}	weak pull-down current	V_{IO} = VDD		105	200	-300	µA
I_{ILIH}	Leakage input current high level	V_{SDA} = 3.6 V, V_{SCL} = 3.6 V			0.27	15	µA

14.1.3 Power consumption

Table 12. Electrical characteristics of IC supply voltage V_{DD}; V_{SS} = 0 V; T_{amb} = -40 °C to +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DD}	supply voltage range	V_{DD} = 1.62 - 3.6 V	1.62	1.80	3.6	V
	operating mode: Idle mode					
I_{DD}	supply current idle mode	f_{CPU}= 48 MHz, f_{MST} = 96 MHz		1.8	2.9	mA
	operating mode: typical CPU					
	no coprocessor active	f_{CPU}= 48 MHz, f_{MST} = 96 MHz		4.4	5.1	mA
	AES coprocessor active (AES 48 MHz)	CPU in idle mode		6.5	7.5	mA
	FAME coprocessor active (FAME 48 MHz)	CPU in idle mode		14.4	16.1	mA
	DES coprocessor active (DES 96 MHz)	CPU in idle mode		6.5	7.6	mA
$I_{DD(PD)}$	supply current Power-down mode	$V_{DDmin} \leq V_{DD} \leq V_{DDmax}$; Clock to input CLK stopped, T_{amb}= 25 °C		430	480	µA
$I_{DDD\ (DPD)}$	supply current Deep Power-down mode	$V_{DDmin} \leq V_{DD} \leq V_{DDmax}$; Clock to input CLK stopped, T_{amb}= 25 °C		3	5	µA

14.2 AC characteristics

Table 13. Non-volatile memory timing characteristics

Conditions: V_{DD} = 1.62 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{EEP}	FLASH erase + program time		[2]		2.3		ms
t_{EEE}	FLASH erase time				0.9		ms
t_{EEW}	FLASH program time				1.4		ms
t_{EER}	FLASH data retention time	T_{amb} = +55 °C		25			years
N_{EEC}	Intrinsic FLASH endurance[3] (number of programming cycles)			1×10^5	5×10^5		cycles

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
N_{EEC}	FLASH endurance (maximum number of programming cycles applied to the whole memory block performed by NXP static and dynamic wear leveling algorithm)			20×10^6	100×10^6		cycles

[1] Typical values are only referenced for information. They are subject to change without notice.
[2] Given value specifies physical access times of FLASH memory only.
[3] Usage of NXP wear leveling algorithm mandatory.

Table 14. Electrical AC characteristics of I^2C_SDA, I^2C_SCL, and RST_N[1]; V_{DD} = 1.8 V ± 10% or 3 V ± 10% V; V_{SS} = 0 V; T_{amb} = -40 °C to +105 °C°C

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input/Output: I^2C_SDA, I^2C_SCL in open-drain mode							
tr_{IO}	I/O Input rise time	Input/reception mode	[2]			1	µs
tf_{IO}	I/O Input fall time	Input/reception mode	[2]			1	µs
tf_{OIO}	I/O Output fall time	Output/transmission mode; C_L = 30 pF	[2]			0.3	µs
f_{CLK}	External clock frequency in I^2C applications	t_{CLKW}, T_{amb} and V_{DD} in their specified imits		-		400	kHz
t_{CLKW}	Clock pulse width i.r.t. clock period (positive pulse duty cycle of CLK)		[3]	40		60	%
Input/Output: I^2C_SDA, I^2C_SCL in push-pull mode (I^2C master in high-speed mode)							
tr_{IO}	I/O Input rise time	Input/reception mode				0.25	µs
tf_{IO}	I/O Input fall time	Input/reception mode				0.25	µs
tf_{OIO}	I/O Output fall time	Output/transmission mode				0.1	µs
f_{CLK}	External clock frequency in I^2C applications	Input/reception mode		-		3.4	MHz
t_{CLKW}	Clock pulse width i.r.t. clock period (positive pulse duty cycle of CLK)					2.1	%
Inputs: RST_N							
t_{RW}	Reset pulse width (RST_N low) without entering Deep Power-down mode			40		400	µs
t_{RDSLP}	Reset pulse width (RST_N low) to enter Deep Power-down mode			500			µs
t_{WKP}	Wake-up time from Power-down mode	$f_{CLKmin} < f_{CLK} < f_{CLKmax}$		-	8	10	µs
t_{WKPIO}	Pad LOW time for wake-up from Power-down mode	level triggered ext.int.		-	8	10	µs
		edge triggered ext.int.		-	8	10	µs

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{WKPRST}	RST_N LOW time for wake-up from Power-down mode			40		-	µs
t_{WKWT}	Time from Power-down mode wake/up event to I^2C_SDA valid				50	100	ns
C_{PIN}	Pin capacitances RST_N, I^2C_SDA, /I^2C_SCL	Test frequency = 1 MHz; T_{amb} = 25 °C		-		10	pF

[1] All appropriately marked values are typical values and only referenced for information. They are subject to change without notice.
[2] t_r is defined as rise time between 30% and 70% of the signal amplitude.
t_f is defined as fall time between 70% and 30% of the signal amplitude.
[3] During AC testing the inputs RST_N, I^2C_SDA, I^2C_SCL are driven at 0 V to +0.3 V for a LOW input level and at V_{DD} -0.3 V to V_{DD} for a HIGH input level. Clock period and signal pulse (duty cycle) timing is measured at 50% of V_{DD}.

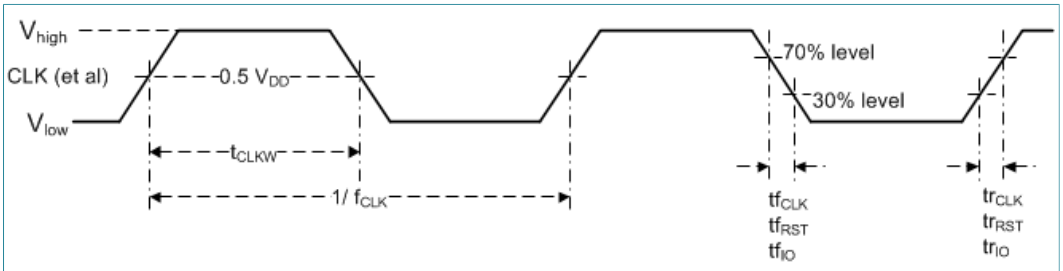

Figure 10. External clock drive and AC test timing reference points of I^2C_SDA, I^2C_SCL, and RST_N (see [2]and [3]) in open-drain mode

Table 15. Electrical AC characteristics of IO1, IO2, CLK and RST_N

Conditions: V_{DD} = 1.8 V ± 10 % or 3 V ± 10 % V; V_{SS} = 0 V; T_{amb} = -40 °C to +105 °C, unless otherwise specified. Typical values are only referenced for information. They are subject to change without notice.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input/Output: IO1/IO2							
tr_{IO}	I/O Input rise time	Input/reception mode	[1] [2]			1	µs
			[3] [2]			0.25 x t_{IOWx_min}	µs
tf_{IO}	I/O Input fall time	Input/reception mode	[1] [2]			1	µs
			[3] [2]			0.25 x t_{IOWx_min}	µs
tr_{OIO}	I/O Output rise time	Output/transmission mode; CL = 30 pF	[2]			0.1	µs
tf_{OIO}	I/O Output fall time	Output/transmission mode; CL = 30 pF	[2]			0.1	µs
Inputs: CLK and RST_N							

2 During AC testing the inputs RST_N, I^2C_SDA, I^2C_SCL are driven at 0 V to +0.3 V for a LOW input level and at V_{DD} -0.3 V to V_{DD} for a HIGH input level. Clock period and signal pulse (duty cycle) timing is measured at 50% of V_{DD}.
3 t_r is defined as rise time between 30% and 70% of the signal amplitude. tf is defined as fall time between 70% and 30% of the signal amplitude.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{CLK}	External clock frequency in ISO/IEC 7816 UART applications	t_{CLKW}, t_{amb} and V_{DD} in their specified limits	[4]	0.85		11.5	MHz
t_{CLKW}	Clock pulse width i.r.t. clock period (positive pulse duty cycle of CLK)			40		60	%
tr_{CLK}	CLK input rise time		[5]			[6]	
tf_{CLK}	CLK input fall time		[2] [6]			[6]	
tr_{RST}	RST_N input rise time		[2]			400	µs
tf_{RST}	RST_N input fall time		[2] [7]			400	µs
t_{RW}	Reset pulse width (RST_N low)			40			µs
t_{WKP}	Wake-up time from Power-Down mode	$f_{CLKmin} \leq f_{CLK} \leq f_{CLKmax}$			17	20	µs
t_{WKPIO}	I/Ox LOW time for wake-up from Power-down mode	level triggered ext.int.			20		µs
		edge triggered ext.int.			20		
t_{WKPRST}	RST_N LOW time for wake-up from Power-down mode						v
Inputs: CLK, RST_N, IO1, IO2							
C_{PIN}	Pin capacitances CLK, RST_N, IO1, IO2	Test frequency = 1 MHz; t_{amb} = 25 °C				20	pF

[1] At minimum IO1 input signal HIGH or LOW level voltage pulse width of 3.2 µs. This timing specification applies to ISO7816 configurations down to a minimum etu duration of 16 CLK cycles at a maximum CLK frequency of 5 MHz (TA1=0x96, (Fi/Di)=(512/32)), for example.
[2] tr is defined as rise time between 10% and 90% of the signal amplitude.
[3] At minimum IO1 input signal HIGH or LOW level voltage pulse width of less than 3.2 µs. This timing specification applies to ISO7816 configurations beyond the conditions listed in note [2], down to a minimum etu duration of 8 CLK cycles at a maximum CLK frequency of 5 MHz (TA1=0x97, (Fi/Di)=(512/64)), for example. An 8 CLKs/etu @ fclk = 5 MHz configuration results in tIOWx_min = 1.6 µs, and in a time of 400 ns for trIO_max and tfIO_max, matching the (Fi/Di)=(512/64) speed enhancement requirements of ETSI TS 102 221.
[4] ISO/IEC 7816 I/O applications have to supply a clock signal to input CLK in the frequency range of 1 MHz to 10 MHz nominal.A ± 15 % tolerance range yields the allowed limits of 0.85 MHz and 11.5 MHz.
[5] During AC testing the inputs CLK, RST_N, and IO1 are driven at 0 V to +0.3 V for a LOW input level and at VDD − 0.3 V to VDD for a HIGH input level. Clock period and signal pulse (duty cycle) timing is measured at 50% of VDD, see Figure 18.
[6] The maximum CLK rise and fall time is 10% of the CLK period 1/fCLK - with the following exception: In the CLK frequency range of 1 MHz to 5 MHz the maximum allowed CLK rise and fall time is 50 ns, if 10% of the CLK period is shorter than 50 ns.
[7] The ETSI TS102 221/GSM 11.1x specifications specify a maximum reset signal (RST_N) rise time and fall time of 400,000 µs, respectively.

Table 16. Electrical AC characteristics of LA, LB; Conditions: T_{amb} = -40 °C to 105 °C, unless otherwise specified

Conditions: T_{amb} = -25 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Typ[1]	Max	Unit
Input/Output: LA, LB						
C_{LALB}[2]	Pin capacitance LA, LB Bare die (SO 28, empty package ground-off)					

Symbol	Parameter	Conditions		Typ[1]	Max	Unit
	Configured for antenna input with 56 pF capacitance Test frequency = 13.56 MHz; T_{amb}= 25 °C	$V_{LA,LB}$ = 2.1 V (rms) $V_{LA,LB}$ = 0.3 V (rms)	[3] [4] [4]	54.3 50.1		pF
R_{LALB}[2]	Pin capacitance LA, LB Bare die (SO 28, empty package ground-off)					
	Configured for antenna input with 56 pF capacitance [5] Test frequency = 13.56 MHz; T_{amb}= 25 °C	$V_{LA,LB}$ = 2.1 V (rms)	[3] [4]	0.913		kΩ
		$V_{LA,LB}$ = 0.3 V (rms)	[4]			
	Wake-up time from Power-Down mode	$f_{CLKmin} \leq f_{CLK} \leq f_{CLKmax}$		17	20	µs
f_{LALB}	Operating frequency LA, LB	level triggered ext.int.		13.56		MHZ

[1] Typical values (± 10%) are only referenced for information. They are subject to change without notice.
[2] The CLALB and RLALB values stated here assume a parallel RC equivalent circuit for the chip.
[3] The value stated here was measured at estimated start of chip operation and is comparable to the values stated in other SmartMX3 family member data sheets.
[4] Measured with sine wave at LA, LB.
[5] 56 pF selection supports all data rates with ID1 antenna (Class 1), however, only 106 kbit/s with 1/2 ID1 antenna (Class 2).

14.3 EMC/EMI

EMC and EMI resistance according to IEC 61967-4.

Note: *tf is defined as fall time between 90% and 10% of the signal amplitude.*

15 Abbreviations

Table 17. Abbreviations

Acronym	Description
AES	Advanced Encryption Standard
APDU	Application Protocol Data Unit
CL	Contactless
CLK	External clock signal input contact pad
CC	Common Criteria
CMAC	Cipher-based MAC
CRC	Cyclic Redundancy Check
CRI	Cryptography Research Incorporated
DES	Digital Encryption Standard
DPA	Differential Power Analysis
DSS	Digital Signature Standard
EAL6	Evaluation Assurance Level
ECC	Elliptic Curve Cryptography
EMC	Electromagnetic compatibility

Acronym	Description
EMI	Electro Magnetic Immunity
FM	Fast-Mode
FM+	Fast-Mode+
GP	Global Platform
GPIO	General-purpose input/output
HS	High-Speed-Mode
HKDF	HMAC-based Extract-and-Expand Key Derivation Function
HMAC	Keyed-Hash Message Authentication Code
HW	Hardware
IC	Integrated Circuit
I^2C	Inter-Integrated Circuit
I/O	Input/Output
IoT	Internet of Things
JCOP	Java Card Open Platform
LA	ISO 14443 Antenna Pad
LB	ISO 14443 Antenna Pad
NFC	Near Field Communication
MAC	Message Authentication Code
MCU	Microcontroller unit
MPU	Microprocessor
MW	Middleware
OS	Operating System
NIST	National Institute for Standards and Technology
PCB	Protocol Control Byte
PKI	Public Key Infrastructure
PRF	Pseudo Random Function
RAM	Random Access Memory
RSA	Rivest-Shamir-Adleman
RST	Reset
SAM	Secure Access Module
SCL	Serial clock
SDA	Serial data
SPA	Simple Power Analysis
SFI	Single Fault Injection
SHA	Secure Hash Algorithm
SW	Software
TLS	Transport Layer Security

Acronym	Description
VCC	Supply Voltage Input
VIN	Voltage Input
VOUT	Voltage Output
VSS	Ground

16 References

[1] NXP SE05x T=1 Over I^2C Specificationl User Manual, Document Number
[2] SOT1969-1; HX2QFN20; Reel packing and package data sheet
[3] SE050 IoT Applet APDU Specification, document number AN 12413
[4] SE050 configurations Application Note, document number AN12436

17 Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
504913	20190607	Objective data sheet		504912
Modifications:	• Changed data sheet status from COMPANY PROPRIETARY to PUBLIC • Updated Table 12 • Updated Section 15			
504912	20190510	Objective data sheet		504911
Modifications:	• Changed structure of document • Updated Section 1 • Updated Section 2.3 • Updated Use Cases and target applications • Updated Section 3.1 • Added Section 3.3 • Updated Section 3.1.2 • Updated Section 3.1.5 • Updated Section 3.2 • Updated chapter Section 4 • Updated and renamed chapter Section 5 • Updated chapter Section 6 • Updated Section 7.1.1 • Updated Section 8 • Updated Section 3.1.3 • Updated Section 3.1.1 • Updated Table 1 • Updated Section 12 • Updated Table 10 • Updated Section 15			
504911	20181122	Objective data sheet		

18 Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Tables

Figures

Contents

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Date of release: 7 June 2019
Document number: 504913