# MOSFET – Power, Single N-Channel 60 V, 15 mΩ, 37 A

#### **Features**

- Small Footprint (5x6 mm) for Compact Design
- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Q<sub>G</sub> and Capacitance to Minimize Driver Losses
- LFPAK4 Package, Industry Standard
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

#### **MAXIMUM RATINGS** (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	60	V
Gate-to-Source Voltage	Gate-to-Source Voltage			±20	V
Continuous Drain Current Raic	Steady State	T <sub>C</sub> = 25°C	I <sub>D</sub>	36	Α
(Notes 1, 2, 3)	State	T <sub>C</sub> = 100°C		21	
Power Dissipation			$P_{D}$	37	W
R <sub>θJC</sub> (Notes 1, 2)		T <sub>C</sub> = 100°C		12	
Continuous Drain Current R <sub>0.IA</sub>	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	12	Α
(Notes 1, 2, 3)	State	T <sub>A</sub> = 100°C	1	8.4	
Power Dissipation		T <sub>A</sub> = 25°C	$P_{D}$	3.8	W
R <sub>θJA</sub> (Notes 1 & 2)		T <sub>A</sub> = 100°C	1	1.9	
Pulsed Drain Current	$T_A = 25^{\circ}C, t_p = 10 \mu s$		I <sub>DM</sub>	185	Α
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>stg</sub>	–55 to + 175	°C
Source Current (Body Diode)			IS	31	Α
Single Pulse Drain-to-Source Avalanche Energy (T <sub>J</sub> = 25°C, I <sub>L(pk)</sub> = 1.6 A)			E <sub>AS</sub>	65	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		TL	260	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	4.1	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	39	

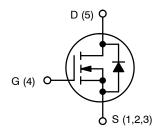
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
- 3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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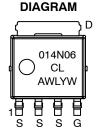
V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX	
60 V	15 mΩ @ 10 V	07.4	
60 V	21.5 m $\Omega$ @ 4.5 V	37 A	



**N-CHANNEL MOSFET** 



LFPAK4 CASE 760AB



**MARKING** 

014N06CL = Specific Device Code A = Assembly Location

WL = Wafer Lot
 Y = Year
 W = Work Week

#### **ORDERING INFORMATION**

See detailed ordering, marking and shipping information on page 5 of this data sheet.

## **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise specified)

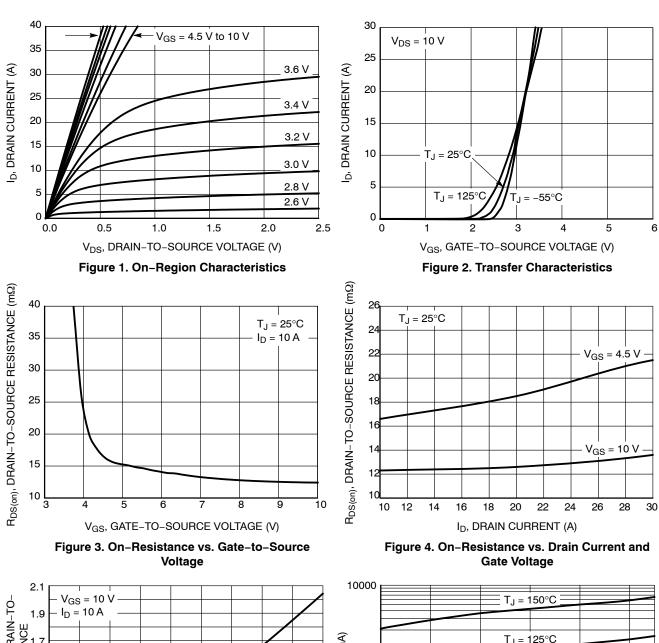
Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> / T <sub>J</sub>				26		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$	T <sub>J</sub> = 25 °C			10	μΑ
		$V_{DS} = 60 \text{ V}$	T <sub>J</sub> = 125°C			250	1
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V				100	nA
ON CHARACTERISTICS (Note 4)					-		
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_D$	= 25 μΑ	1.2		2.0	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>				-5.0		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 10 A		12.5	15	mΩ
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 10 A		17.9	21.5	1
Forward Transconductance	9FS	V <sub>DS</sub> = 15 V, I <sub>D</sub>	= 15 A		43		S
CHARGES, CAPACITANCES & GATE RESIS	TANCE				•	•	
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MH:	z, V <sub>DS</sub> = 25 V		620		pF
Output Capacitance	C <sub>OSS</sub>				340		1
Reverse Transfer Capacitance	C <sub>RSS</sub>				7.0		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 48 V; I <sub>D</sub> = 10 A			4.5		nC
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 48 V; I <sub>D</sub> = 10 A			9.7		1
Threshold Gate Charge	Q <sub>G(TH)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 48 V; I <sub>D</sub> = 10 A			1.3		1
Gate-to-Source Charge	Q <sub>GS</sub>				2.1		
Gate-to-Drain Charge	$Q_{GD}$				1.0		
Plateau Voltage	$V_{GP}$				3.1		V
SWITCHING CHARACTERISTICS (Note 5)					•	•	
Turn-On Delay Time	t <sub>d(ON)</sub>	$V_{GS}$ = 10 V, $V_{DS}$ = 48 V, $I_D$ = 10 A, $R_G$ = 1.0 $\Omega$			7.0		ns
Rise Time	t <sub>r</sub>				13		1
Turn-Off Delay Time	t <sub>d(OFF)</sub>				25		1
Fall Time	t <sub>f</sub>				6.0		1
DRAIN-SOURCE DIODE CHARACTERISTIC	s					•	
Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0 V$ ,	T <sub>J</sub> = 25°C		0.85	1.2	V
		I <sub>S</sub> = 10 A	T <sub>J</sub> = 125°C		0.72		1
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS}$ = 0 V, dIS/dt = 20 A/ $\mu$ s, $I_{S}$ = 10 A			23.8		ns
Charge Time	t <sub>a</sub>				11.9		
Discharge Time	t <sub>b</sub>				11.8		1
Reverse Recovery Charge	Q <sub>RR</sub>				11.6		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

#### **TYPICAL CHARACTERISTICS**



2.1 V<sub>GS</sub> = 10 V 1.9 V<sub>GS</sub> = 10 V 1.9 V<sub>GS</sub> = 10 V 1.9 V<sub>GS</sub> = 10 V V<sub>GS</sub> = 10

Figure 5. On–Resistance Variation with Temperature

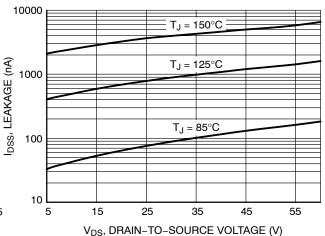


Figure 6. Drain-to-Source Leakage Current vs. Voltage

#### **TYPICAL CHARACTERISTICS**

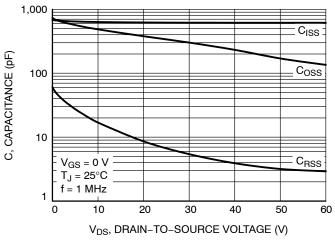


Figure 7. Capacitance Variation

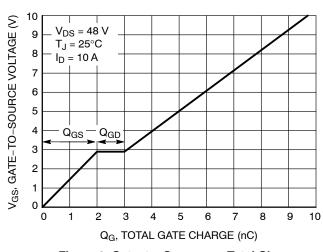


Figure 8. Gate-to-Source vs. Total Charge

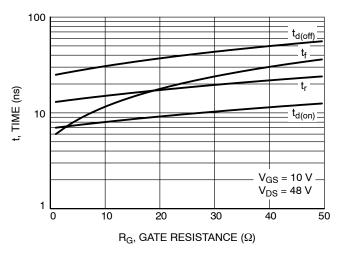


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

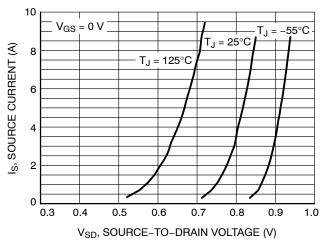


Figure 10. Diode Forward Voltage vs. Current

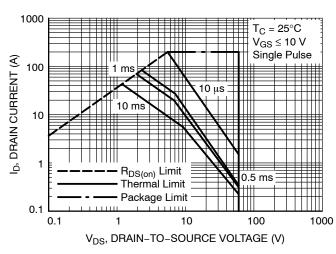


Figure 11. Maximum Rated Forward Biased Safe Operating Area

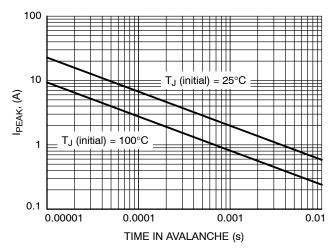


Figure 12. I<sub>PEAK</sub> vs. Time in Avalanche

#### **TYPICAL CHARACTERISTICS**

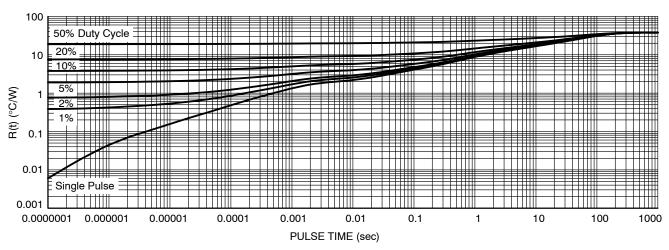


Figure 13. Thermal Characteristics

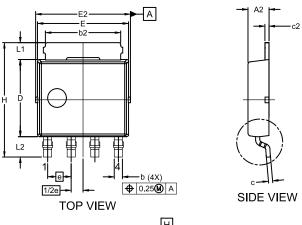
#### **DEVICE ORDERING INFORMATION**

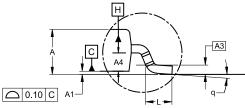
Device	Marking	Package	Shipping <sup>†</sup>
NVMYS014N06CLTWG	014N06CL	LFPAK4 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

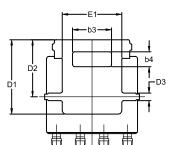
#### PACKAGE DIMENSIONS

#### LFPAK4 5x6 CASE 760AB **ISSUE A**

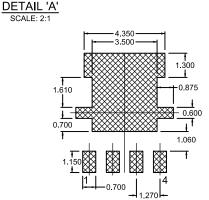




SCALE: 2:1







RECOMMENDED MOUNTING **FOOTPRINT** 

#### NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

UNIT IN MILLIMETER					
DIM	MIN	NOM	MAX		
Α	1.10	1.20	1.30		
Α1	0.00	0.08	0.15		
A2	1.10	1.15	1.20		
А3		0.25			
A4	0.45	0.50	0.55		
b	0.40	0.45	0.50		
b2	3.80	4.10	4.40		
b3	2.00	2.10	2.20		
b4	0.70	0.80	0.90		
ဂ	0.19	0.22	0.25		
c2	0.19	0.22	0.25		
О	4.05	4.15	4.25		
D1	ı	ı	4.20		
D2	3.0	3.10	3.20		
D3	0.30	0.40	0.50		
Ш	4.80	4.90	5.00		
E1	3.10	3.20	3.30		
E2	5.00	5.15	5.30		
е	1.27 BSC				
I	6.00	6.15	6.30		
L	0.40	0.65	0.85		
L1	0.80	0.90	1.00		
L2	0.80	1.05	1.30		
q	0°	4°	8°		

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