Product Change Notification - SYST-15MLFI541

Date:

17 Jun 2019

Product Category:

8-bit Microcontrollers

Affected CPNs:

Notification subject:

ERRATA - PIC16(L)F19195/6/7 Family Silicon Errata and Data Sheet Clarification

Notification text:

SYST-15MLFI541

Microchip has released a new DeviceDoc for the PIC16(L)F19195/6/7 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at PIC16(L)F19195/6/7 Family Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change:

1) Removed Module 7.8 Program Flash Memory (PFM) Endurance (redundant).
2) Data Sheet Clarifications: Removed all modules (Data Sheet updated).

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 17 June 2019

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Attachment(s):

PIC16(L)F19195/6/7 Family Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

PIC16F19195-E/5LX
PIC16F19195-E/MR
PIC16F19195-E/PT
PIC16F19195-I/5LX
PIC16F19195-I/MR
PIC16F19195-I/PT
PIC16F19195T-I/5LX
PIC16F19195T-I/MR
PIC16F19195T-I/PT
PIC16F19196-E/5LX
PIC16F19196-E/MR
PIC16F19196-E/PT
PIC16F19196-I/5LX
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PIC16F19196-I/PT
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PIC16F19196T-I/PT
PIC16F19197-E/5LX
PIC16F19197-E/5LXVAO
PIC16F19197-E/MR
PIC16F19197-E/PT
PIC16F19197-E/PTVAO
PIC16F19197-I/5LX
PIC16F19197-I/5LXVAO
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PIC16(L)F19195/6/7

PIC16(L)F19195/6/7 Family
Silicon Errata and Data Sheet Clarification

The PIC16(L)F19195/6/7 family devices that you have received conform functionally to the current Device Data Sheet (DS40001873**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F19195/6/7 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 8, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F19195/6/7 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		
		A1	A3	A4
PIC16F19195	3084h	2001h	2003h	2004h
PIC16LF19195	3086h	2001h	2003h	2004h
PIC16F19196	3085h	2001h	2003h	2004h
PIC16LF19196	3087h	2001h	2003h	2004h
PIC16F19197	30A2h	2001h	2003h	2004h
PIC16LF19197	30A3h	2001h	2003h	2004h

Note 1: The Device and Revision IDs is located at the respective addresses 8006h and 8005h of configuration memory space.

2: Refer to the *"PIC16(L)F1919X Memory Programming Specification"* (DS40001846) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Summary	Affected Revisions		
				A1	A3	A4
Analog-to-Digital Converter with Computation (ADC^2)	ADC^2 Clock Selection	1.1	Static MSB with FRC selected as ADC clock source.	X		
	ADC^2 with Fixed Voltage Reference (FVR)	1.2	Using the FVR as the ADC positive voltage reference can cause missing codes.	X		
	ADC^2 FRC Clock Sleep Mode	1.3	If in Sleep and ADRC is used, the oscillator continues to run after conversion.	X		
	ADC^2 FRC Clock ADGO Delay	1.4	When using FRC as clock source, there is a delay of 1 instruction cycle.	X		
	ADC^2 Channel Switching	1.5	When switching to FVR, some PMOS gates turn on and feed current back into the networks.	X		
	ADC^2 Conversion	1.6	At the very beginning of the ADC conversion, the input signal may briefly be pulled to ground.	X		
Reset and VBAT	VBAT with ULPBOR	2.1	Higher current with ULPBOR active.	X		
Liquid Crystal Display (LCD) Controller	LP Ladder	3.1	Resistance of LP ladder is different than what is indicated in the data sheet.	X		
	Internal VLCD3 Measurement	3.2	Nonstable readings.	X		
	LCD Charge Pump Low-Power mode	3.3	The LCD Charge Pump Low-Power (Low-Current (LC)) mode is calibrated but not tested.	X		
	1/2 MUX, 1/2 Bias with External Resistor Ladder	3.4	1/2 MUX, 1/2 Bias with External Resistor Ladder is not operational.	X		
Windowed Watchdog Timer (WWDT)	Watchdog Timer Clock Source	4.1	WWDT only operates from the LFINTOSC clock source.	X		
Comparator (CMP)	C2 Low-Power Clocked Comparator	5.1	Unstable output.	X	X	X
Real Time Clock and Calendar (RTCC)	RTCC Alarm	6.1	An alarm will not occur if the lower nibble of ALRMLSEC <3:0> is configured to 0x0.	X	X	X

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Summary	Affected Revisions		
				A1	A3	A4
Electrical Specifications	VBAT current specification.	7.1	Higher typical current.	X		
	SMBus V_{IL} Level	7.2	The maximum V_{IL} level changes when V_{DD} is below 4.0V.	X	X	
	Program Flash Memory (PFM) Endurance	7.3	The PFM endurance is lower than specified.	X		
	Internal Oscillator Frequency Accuracy	7.4	Internal oscillator frequency accuracy may be higher than specified at temperatures between 0 and 60°C.	X	X	X
	Fixed Voltage Reference (FVR) Accuracy	7.5	Fixed Voltage Reference (FVR) output tolerance may be higher than specified at temperatures below -20°C.	X	X	
	Nonvolatile Memory (NVM) for LF Devices	7.6	Performing a row erase through the NVMREG access may not execute as expected when V_{DD} is lowered from >3.3V down to <2.0V between +25°C and -40°C.	X	X	X
	Min. V_{DD} Specification	7.7	V_{DDMIN} specifications are changed for LF devices only.	X	X	X

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A3**).

1. Module: Analog-to-Digital Converter with Computation (ADC^2)

1.1 ADC^2 Clock Selection

The ADC does not function properly if FRC is selected as its clock source resulting in the MSB being stuck as a '0' or a '1'. This also prohibits using the ADC module in Sleep mode.

Work around

None.

Affected Silicon Revisions

A1	A3	A4					
X							

1.2 ADC^2 with Fixed Voltage Reference (FVR)

Using the FVR as the positive voltage reference (V_{REF}+) for the ADC, can cause an increase in missing codes.

Work around

Method 1: Increase the bit conversion time, known as TAD, to 8 µs or higher.

Method 2: Use V_{DD} as the positive voltage reference to the ADC.

Affected Silicon Revisions

A1	A3	A4					
X							

1.3 ADC^2 FRC Clock Sleep Mode

If the part is in Sleep and the ADCRC oscillator is used as the clock source to the ADC, the oscillator continues to run after the conversion is complete. This will increase the current consumption in Sleep mode. The oscillator will stop after the device exits Sleep mode and resumes normal code execution.

Work around

None.

Affected Silicon Revisions

A1	A3	A4					
X							

1.4 ADC^2 FRC Clock ADGO Delay

When using the FRC as the clock source for ADC^2, there is a delay of one instruction cycle between the user setting the ADGO bit and being able to read it. This can lead to a false conversion complete scenario (i.e., ADGO being cleared), depending if the user code has a bit clear test (BTFSC) instruction on the ADGO bit, immediately after setting the ADGO bit. See Code Example below.

```
BSF   ADCON0,ADGO ;Start conversion
BTFSCADCON0,ADGO ;Is conversion
                  done?
GOTO  $-1         ;No, test again
```

The BTFSC will pass the very first time in this situation.

Work around

Add a NOP instruction after setting the ADGO bit and before testing the bit for completion of conversion. See Code Example below:

```
BSF   ADCON0,ADGO ;Start conversion
NOP
BTFSCADCON0,ADGO ;Is conversion
                  done?
GOTO  $-1         ;No, test again
```

Affected Silicon Revisions

A1	A3	A4					
X							

1.5 ADC^2 Channel Switching

When switching to the FVR Input channel on the ADC or ADC^2, from a channel that is of a higher voltage than the FVR, certain PMOS gates will turn on and feed current back into other networks that are also supported by the FVR reference voltage. Until the sample and hold capacitor of the ADC discharges to the new lower voltage level, the PMOS circuits will remain on and the circuits supported by the FVR will experience problems. Some of the affects include; the BOR will trigger at a higher voltage, the internal oscillators will experience frequency changes, and the FVR input to the comparator circuit will be a higher than expected voltage.

Work around

None.

Affected Silicon Revisions

A1	A3	A4					
X	X						

1.6 ADC^2 Conversion

At the very beginning of the ADC conversion, the input signal may briefly be pulled to ground, which in turn may take some charge out of the internal sample and hold capacitor. The problem is more pronounced on inputs with an impedance greater than 1K ohm.

This issue will be seen when sampling the following internal channel inputs: FVR, DAC, and Temperature Indicator and when sampling external sources on an analog pin, including the CVD.

Work around

When sampling the internal channel inputs, FVR, DAC, and Temperature Indicator, increase the minimum TAD time to 4 µS to increase accuracy.

When sampling an external source through an analog pin, keep the input impedance below 1K ohm.

When using the ADC as an internal reference for the CVD module, there is no work around.

Affected Silicon Revisions

A1	A3	A4					
X	X						

2. Module: Reset and VBAT

2.1 VBAT with ULPBOR

In order to avoid high IBAT currents of 10 µA or greater, when utilizing VBAT to provide battery backup the ULPBOR should not be activated. When the part is used in this fashion, VDD should also be either off (0 volts) or >1.5V.

Work around

Do not use VBAT along with ULPBOR.

Affected Silicon Revisions

A1	A3	A4					
X							

3. Module: Liquid Crystal Display (LCD) Controller

3.1 LP Ladder

The resistance of the LP Resistor Ladder is 6.6 M-ohms rather than the 3.3 M-ohms indicated in the data sheet.

Work around

None.

Affected Silicon Revisions

A1	A3	A4					
X							

3.2 Internal VLCD3 Measurement

The ¼ scale tap point provided on the LP Resistor Ladder for use together with the ADC does not provide stable readings to support monitoring of the LCD pump output level.

Work around

Measure the VLCD3 via an external ADC.

Affected Silicon Revisions

A1	A3	A4					
X							

3.3 LCD Charge Pump Low-Power Mode

The LCD Charge Pump Low-Power (Low Current (LC)) mode is calibrated to a nominal value but not tested.

Work around

None.

Affected Silicon Revisions

A1	A3	A4					
X							

3.4 1/2 MUX, 1/2 Bias with External Resistor Ladder

The 1/2 MUX, 1/2 bias with External Resistor Ladder mode of operation is non-functional.

Work around

For 1/2 MUX, 1/2 Bias mode operation use the internal LP, MP or HP ladder.

Affected Silicon Revisions

A1	A3	A4					
X							

4. Module: Windowed Watchdog Timer (WWDT)

4.1 Watchdog Timer Clock Source

When the WDTCS <2:0> bits of the WDTCON1 register are set to either the MFINTOSC (b'001') or the SOSC ('b010') clock source, the WWDT does not operate.

Work around

Use the LFINTOSC (b'000') as the clock source for the WWDT.

Affected Silicon Revisions

A1	A3	A4					
X							

5. Module: Comparator (CMP)

5.1 C2 Low-Power Clocked Comparator

The output of the Low-Power Clocked Comparator (CMP2) is unstable and is not recommended for use.

Work around

None.

Affected Silicon Revisions

A1	A3	A4					
X	X	X					

6. Module: Real Time Clock and Calendar (RTCC)

6.1 Real Time Clock and Calendar (RTCC) Alarm

When using the RTCC alarm function in any mode other than AMASK<3:0> = 0b0000 or AMASK<3:0> = 0b0001, an alarm will not occur if the lower nibble of the ALRMSEC register, ALRMLSEC <3:0>, is configured to 0x0.

Work around

If an alarm is desired when the lower nibble of the SECONDS register = 0x0, configure ALRMLSEC<3:0> = 0xA.

Affected Silicon Revisions

A1	A3	A4					
X	X	X					

7. Module: Electrical Specifications

7.1. V_{BAT} Current Specification

I_{BAT} with V_{BAT}, SOSC and RTCC active (V_{BAT} > V_{DD}) is higher than the 400 nA typical target shown on the data sheet. The typical current observed on rev A1 parts at 25°C will be 1.3 µA at 3.0V V_{DD}.

Work around

None.

Affected Silicon Revisions

A1	A3	A4					
X							

7.2 SMBus V_{IL} Level

When the V_{DD} voltage level supplied to the device is 4.0V and above, the maximum SMBus voltage level for the V_{IL} parameter is 0.8V. When V_{DD} drops below 4.0V, the maximum SMBus voltage level for V_{IL} drops to 0.7V.

Work around

None.

Affected Silicon Revisions

A1	A3	A4					
X	X						

7.3 Program Flash Memory Endurance

The minimum value for the Program Flash Memory (PFM) endurance specification, called out as parameter number MEM30 in the data sheet, is 1K cycles.

Work around

None.

Affected Silicon Revisions

A1	A3	A4					
X							

7.4 Internal Oscillator Frequency Accuracy

HFINTOSC frequency accuracy is greater than shown on the data sheet in Figure 39-6 and listed in Note 1 of the same figure. Over the temperature range of 0 to 60°C, and over V_{DD} range of 2.3V to 5.5V, the internal oscillator frequency accuracy has changed from +/-2% to +/-3%.

Work around

None.

Affected Silicon Revisions

A1	A3	A4					
X	X	X					

7.5 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

Affected Silicon Revisions

A1	A3	A4					
X	X						

7.6 Nonvolatile Memory (NVM) for LF Devices

Performing a row erase through the NVMREG access on LF device may not execute as expected when V_{DD} is lowered from >3.3V down to <2.0V before or during the row erase while also operating between +25°C and -40°C.

Work around

None.

Affected Silicon Revisions

A1	A3	A4					
X	X	X					

7.7 Min V_{DD} Specification for LF Devices

V_{DDMIN} for LF devices is 2.0V.

Work around

None.

Affected Silicon Revisions

A1	A3	A4					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001873**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev F Document (06/2019)

Removed Module 7.8 Program Flash Memory (PFM) Endurance (redundant).

Data Sheet Clarifications: Removed all modules (Data Sheet updated).

Rev E Document (08/2018)

Added A4 silicon rev. Added Module 1.3 ADC^2 FRC Clock Sleep Mode. Added Module 1.4 ADC^2 FRC Clock ADGO Delay. Added Module 1.5 ADC^2 Channel Switching. Added Module 1.6 ADC^2 Conversion. Added Module 6: Real Time Clock and Calendar (RTCC) and 6.1 RTCC Alarm. Added Module 7.8 Program Flash Memory (PFM) Endurance. Updated Table 2.

Rev D Document (05/2018)

Data Sheet Clarifications: Added Module 1: Analog-to-Digital with Computation (ADC^2) and Module 2: Real Time Clock and Calendar (RTCC). Added Module 7.8 Program Flash Memory (PFM) Endurance.

Rev C Document (01/2018)

Added Module 6.7: Min. V_{DD} Specifications. Updated Modules 6.3, 6.4, and 6.5 “Affected Silicon Revisions” Tables.

Rev B Document (10/2017)

Removed Module 6.1: ADC Offset and Gain Error; Added Module 6.4: Internal Oscillator Frequency Accuracy; Added Module 6.6: Nonvolatile Memory (NVM) for LF Devices; Added affected revision A3; Other minor corrections.

Data Sheet Clarifications: Removed Module 1 (Data Sheet updated).

Rev A Document (03/2017)

Initial release of this document; issued for revision A1. Includes silicon issues 1.1 (ADC^2), 1.2 (ADC^2), 2.1 (V_{BAT}), 3.1 (LCD), 3.2 (LCD), 3.3 (LCD), 3.4 (LCD), 4.1 (WWDT), 5.1 (CMP),

Electrical Specifications: 6.1 ADC, 6.2 V_{BAT}, 6.3 SMBus, 6.4 Program Flash Memory, and 6.5 FVR.

Data Sheet Clarifications:

Module 1: LCD

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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