# MAX20343

# Ultra-Low Quiescent Current, Low Noise 3.5W Buck-Boost Regulator

## General Description

The MAX20343 is an ultra-low quiescent current, non-inverting buck-boost converter with 1A current capability at 3.5V intended for applications that require long run times while also demanding bursts of high current. The device employs a unique control algorithm which seamlessly transitions between buck, buck-boost, and boost modes, minimizing discontinuities and subharmonics in the output voltage ripple. The low 1.9V input voltage for startup allows users to power the device from a variety of sources, and the near-zero minimum operating voltage gives the user the ability to extract as much as possible from their energy source. The MAX20343 has also been designed to keep inductance and output capacitance requirements as low as possible for space-constrained applications.

The MAX20343 is ideal for power in optical sensor applications as well as for powering radios in low power, wide area network (LPWAN) applications since in both cases noise must be minimal and efficiency must be high. For instance, the small light-load output voltage ripple allows a photoplethysmography (PPG) system to operate at low LED currents without interference. Additionally, seamless transitions between operating modes enables the use of dynamic voltage scaling (DVS) to minimize headroom on the LED and to save power in such systems. In applications where a low-power-density battery must be buffered by a super-capacitor to provide large LPWAN type bursts of current, the ultra-low operating voltage of the MAX20343 allows the user to extract as much energy as possible from the super capacitor. The low output inductance/capacitance requirement allows a small total solution size. For example in PPG systems, this provides the flexibility to place the MAX20343 on a remote optical module if overcrowding on the main PCB is an issue.

The MAX20343 is available with a highly configurable $I^2C$ serial interface or as a single-pin-enabled fixed-programming version. The device operates over the -40°C to +85°C temperature range, is available in a 16-bump, 1.77mm x 2.01mm, 0.4mm pitch WLP package and a 12-pin, 2.50mm x 2.50mm, 0.5mm pitch FC2QFN package.
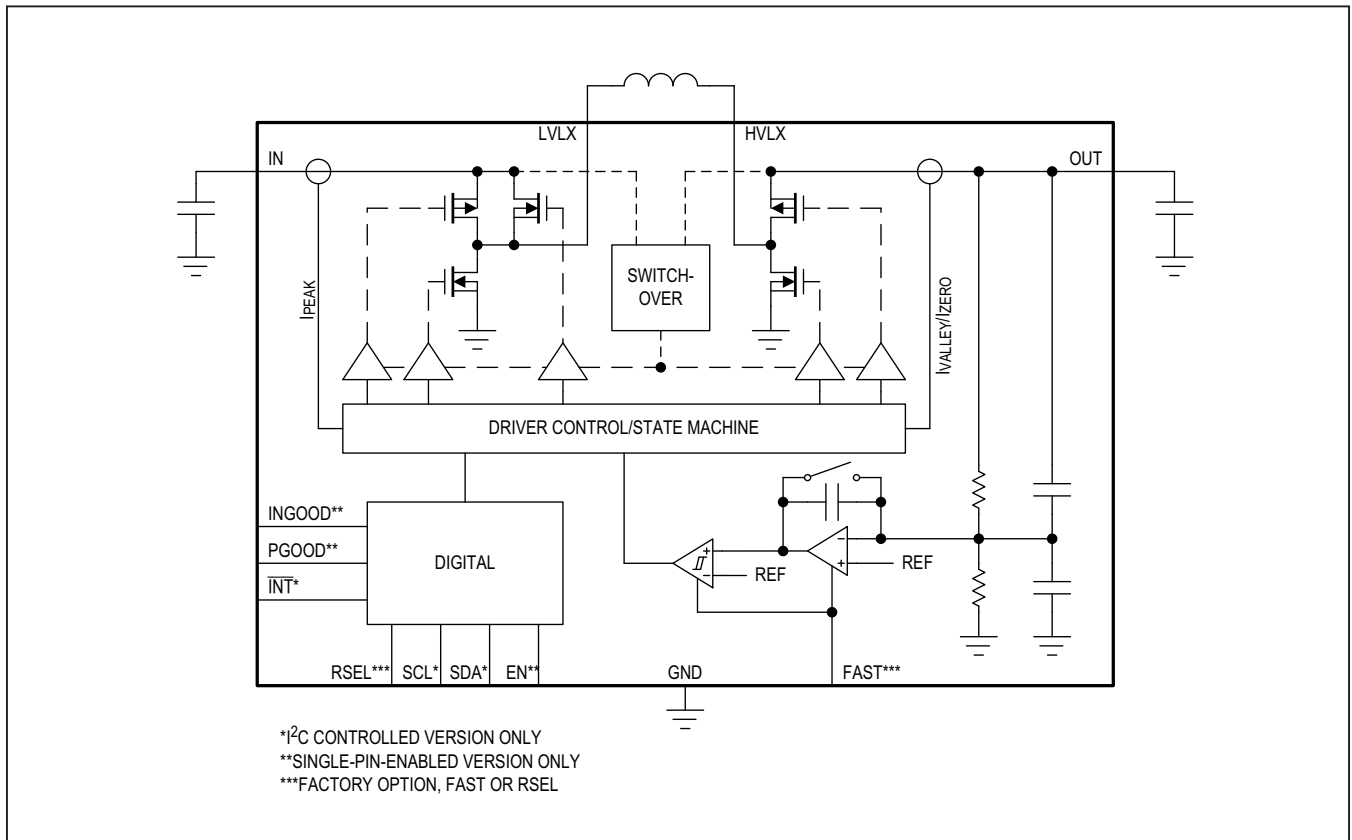
## Benefits and Features

- Extend System Run Time
  - Ultra-Low, 3.5µA (typ) Quiescent Current
  - 250mW Ouptut Power with 500mV Input Voltage
  - Dynamic Voltage Scaling (DVS)
- Low, Continuous Noise Profile
  - Eliminates Discontinuities Across Operating Voltage Range
  - Eliminates Post-Filtering LDO in Noise Sensitive Applications
- Adaptable Load Transient Response
  - Adjustable Peak Current for Optimal Performance in Each Application
  - Fast Load Transient Response Minimizes Settling Time
  - Optional Feedback Integrator
    - Enable for 3.5W Output Power Capabilities
    - Disable for 1.75W Output Power and Faster Load Transient Settling Time
  - FAST Pin Pretriggers Load Response and Offers Improved Load Transient
- Flexible Control Options
  - $I^2C$ Interface with Status Interrupts
  - EN and Status Pins, Single-Resistor $V_{OUT}$ Selection (RSEL)
- Extended Operating Temperature from -40°C to +85°C
- Optimally Sized for Small Applications
  - 16-bump, 1.77mm x 2.01mm, 0.4mm Pitch WLP 12-pin, 2.50mm x 2.50mm, Side-Wettable, 0.5mm Pitch Flip-Chip QFN
  - Inductor/Capacitor Available in 0603/0402 Case Sizes

## Applications

- Biometric Optical Sensing Including PPG
- LPWAN (LTE/NB-IoT, LTE/Cat-M1)
- IoT
- Industrial Sensors

*Ordering Information* **appears at end of data sheet.**

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## Simplified Block Diagram



*I²C CONTROLLED VERSION ONLY
**SINGLE-PIN-ENABLED VERSION ONLY
***FACTORY OPTION, FAST OR RSEL

## Absolute Maximum Ratings

IN, OUT, SDA, SCL, EN, FAST, RSEL,
  PGOOD, INGOOD, $\overline{INT}$, CAP .........................-0.3V to +6.0V
LVLX ...........................................................-0.3V to $V_{IN}$ + 0.3V
HVLX .....................................-0.3V to min($V_{OUT}$ + 0.3V, +6.0V)
Continuous Power Dissipation (Multilayer Board,
  $T_A$ =  +70°C) (4 x 4 Array 16-Ball, 1.77mm x 2.01mm, 0.4mm
  Pitch WLP) (derate 17.26mW/°C above +70°C) ....949.30mW

Continuous Power Dissipation (Multilayer Board,
  $T_A$ = +70°C) (12-Pin, 2.50mm x 2.50mm, 0.5mm Pitch
  FC2QFN) (derate 17.04mW/°C above +70°C).......936.97mW
Operating Temperature Range........................... -40°C to +85°C
Junction Temperature.....................................................+150°C
Storage Temperature Range........................... -40°C to +150°C
Soldering Temperature (reflow)......................................+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Information

| PACKAGE TYPE: 16-BUMP WLP | |
|---|---|
| Package Code | W161C2+1 |
| Outline Number | **21-100328** |
| Land Pattern Number | Refer to **Application Note 1891** |
| THERMAL RESISTANCE, FOUR-LAYER BOARD: | |
| Junction to Ambient ($\theta_{JA}$) | 57.93°C/W |

| PACKAGE TYPE: 12-PIN FC2QFN | |
|---|---|
| Package Code | F122B2F+1 |
| Outline Number | **21-100331** |
| Land Pattern Number | **90-100130** |
| THERMAL RESISTANCE, FOUR-LAYER BOARD: | |
| Junction to Ambient ($\theta_{JA}$) | 58.70°C/W |
| Junction to Case ($\theta_{JC}$) | 23.10°C/W |

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

## Electrical Characteristics

($V_{IN}$ = +1.8V to +5.5V, $C_{IN}$ = 5µF, $C_{OUT}$ = 8µF, $T_J$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C, $V_{IN}$ = +3.7V, L = 1µH, Limits are 100% tested at $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **BUCK-BOOST** | | | | | | | |
| Input Voltage Range | $V_{IN\_START}$ | Input voltage required for startup (Note 2) | | 1.9 | | 5.5 | V |
| Quiescent Supply Current | $I_Q$ | No load, $V_{OUT}$ = 5V, $V_{IN}$ = 3.7V | $V_{CAP}$ forced to $V_{IN}$ | | 3.51 | 5 | µA |
| | $I_{Q\_FAST}$ | | FAST = 1 | | 35 | | µA |
| Shutdown Supply Current | $I_{SHDN}$ | I²C controlled | | | 0.3 | | µA |
| Maximum Output Operative Power (Note 3) | $P_{MAX}$ | Integrator enabled, $V_{IN}$ > 2.7V | BBstFETScale = 0, L = 1µH, $C_{OUT}$ = 8µF | 3.5 | | | W |
| | | | BBstFETScale = 1, L = 2.2µH, $C_{OUT}$ = 4µF | 1.75 | | | |
| | | Integrator disabled, $V_{IN}$ > 3.2V (Note 4) | BBstFETScale = 0, L = 1µH, $C_{OUT}$ = 8µF | 2.8 | | | |
| | | | BBstFETScale = 1, L = 2.2µH, $C_{OUT}$ = 4µF | 1.6 | | | |
| Output Voltage Set Range | $V_{OUT}$ | 50mV step resolution | | 2.5 | | 5.5 | V |
| | | | $V_{IN}$ < 2.1V, CAP forced to $V_{OUT}$ (see Input Operating Voltage section) | 3.3 | | 5.5 | |
| Average Output Voltage Accuracy | ACC_OUT | $I_{OUT}$ = 1mA, $C_{OUT\_EFF}$ = 8µF | | -3 | | +3 | % |
| Line Regulation Error | $V_{LINE\_REG}$ | | | -1 | | +1 | %/V |
| Load Regulation Error | $V_{LOAD\_REG}$ | Integrator enabled, $V_{IN}$ = 2.7V, $V_{OUT}$ = 3.3V, BBstFETScale = 0, $P_{OUT}$ = 3.5W | | | -1 | | % |
| | | Integrator disabled, $V_{IN}$ = 3.7V, $V_{OUT}$ = 5V, $P_{OUT}$ = 1.5W, BBstFETScale = 1, $C_{OUT}$ = 4µF, L = 2.2µH | | | -3.2 | | |
| Line Transient Response | $V_{LINE\_TRAN}$ | $V_{OUT}$ = 3.4V, $V_{IN}$ from 3.4V to 2.9V, 1µs fall time, $I_{LOAD}$ = 750mA, BBstIntegEn = 1, SwoFrcIN = 0 | | | 0 | | mV |
| Load Transient Response | $V_{LOAD\_TRAN}$ | $V_{OUT}$ = 5V, $V_{IN}$ = 3.7V, $I_{LOAD}$ = 10µA to 700mA, BBstIntegEn = 1 | | | -150 | | mV |
| Input Supply Current During Startup | $I_{IN\_STUP}$ | $V_{IN}$ = 3.6V, $V_{OUT}$ = 5V, $I_{LOAD}$ = 0 | | | 1 | | mA/$C_{OUT}$ (µF) |
| Maximum Output Power During Startup | $I_{PWR\_MAX\_STUP}$ | BBstFETScale = 0 | | 330 | 450 | | mW |
| | | BBstFETScale = 1 | | 200 | 280 | | |
| Startup Time | $t_{STARTUP}$ | Time from $V_{OUT}$ = 0V to final value | I²C controlled | | 9.6 | | ms |
| | | | RSEL, BBstRampEn = 0 | | 32 | | |
| PGOOD Threshold | $V_{PGOOD}$ | | | | 84.7 | | %$V_{OUT}$ |
| PGOOD Threshold Hysteresis | $V_{PGOOD\_HYS}$ | | | | 2.25 | | %$V_{OUT}$ |

## Electrical Characteristics (continued)

($V_{IN}$ = +1.8V to +5.5V, $C_{IN}$ = 5µF, $C_{OUT}$ = 8µF, $T_J$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C, $V_{IN}$ = +3.7V, L = 1µH, Limits are 100% tested at $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Input UVLO Rising Threshold | $V_{IN\_UVLO\_R}$ | $V_{IN}$ rising | Soft-start active, CAP forced to $V_{IN}$, or $V_{OUT}$ set below 3.3V | | 1.836 | | V |
| | | | $V_{OUT}$ set higher than 3.3V, soft-start period complete | | 2.185 | | |
| Input UVLO Falling Threshold | $V_{IN\_UVLO\_F}$ | $V_{IN}$ falling | Soft-start active, CAP forced to $V_{IN}$, or $V_{OUT}$ set below 3.3V | | 1.782 | | V |
| | | | $V_{OUT}$ set higher than 3.3V, soft-start period complete | | 2.101 | | |
| Output UVLO Falling Threshold | $V_{OUT\_UVLO\_F}$ | $V_{OUT}$ falling | | | 1.873 | | V |
| Output UVLO Rising Threshold | $V_{OUT\_UVLO\_R}$ | $V_{OUT}$ rising | | | 1.963 | | V |
| **DIGITAL** | | | | | | | |
| SDA, EN, SCL, $\overline{INT}$, PGOOD, INGOOD FAST, RSEL Input Leakage Current | $I_{LK\_IO}$ | $T_J$ = +25°C | | -1 | | +1 | µA |
| SDA, EN, SCL, FAST Input Logic High | $V_{IO\_IH}$ | | | 1.4 | | | V |
| SDA, EN, SCL, FAST Input Logic Low | $V_{IO\_IL}$ | | | | | 0.4 | V |
| SDA, $\overline{INT}$, PGOOD, INGOOD Output Logic Low | $V_{IO\_OL}$ | $I_{OL}$ = 4mA | | | | 0.4 | V |
| SCL Clock Frequency | $f_{SCL}$ | | | 400 | | 680 | kHz |
| Bus Free Time Between STOP and START Condition | $t_{BUF}$ | | | 0.75 | | | µs |
| START Condition (Repeated) Hold Time | $t_{HD\_STA}$ | (Note 5) | | 0.35 | | | µs |
| Low Period of SCL Clock | $t_{LOW}$ | | | 0.75 | | 1.25 | µs |
| High Period of SCL Clock | $t_{HIGH}$ | | | 0.35 | | | µs |
| Setup Time for a Repeated START Condition | $t_{SU\_STA}$ | | | 0.35 | | | µs |

## Electrical Characteristics (continued)

($V_{IN}$ = +1.8V to +5.5V, $C_{IN}$ = 5µF, $C_{OUT}$ = 8µF, $T_J$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C, $V_{IN}$ = +3.7V, L = 1µH, Limits are 100% tested at $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Data Hold Time | $t_{HD\_DAT}$ | (Note 6) | 0 | | 0.53 | µs |
| Data Setup Time | $t_{SU\_DAT}$ | | 100 | | | ns |
| Setup Time for STOP Condition | $t_{SU\_STO}$ | | 0.35 | | | µs |
| Spike Pulse Widths Suppressed by Input Filter | $t_{SP}$ | | 50 | | | ns |

**Note 1:** All devices are 100% production tested at $T_A$ = +25°C. Limits over the operating temperature range are guaranteed by design.
**Note 2:** Output power across the input operating voltage range is limited by input current. Refer to TOC03 for details on how the power limit changes with $V_{IN}$.
**Note 3:** The parameter is not production tested and values are generated through characterization only.
**Note 4:** Operation down to 2.7V is supported with the integrator disabled, but stability is only guaranteed up to 1.75W output power. Beyond 1.75W, oscillations could occur unless output capacitance is increased.
**Note 5:** $f_{SCL}$ must meet the minimum clock low time plus the rise/fall times.
**Note 6:** The maximum $t_{HD\_DAT}$ has to be met only if the device does not stretch the low period ($t_{LOW}$) of the SCL signal.
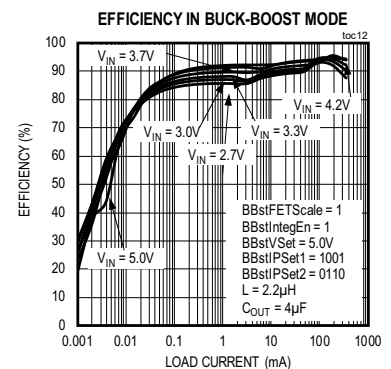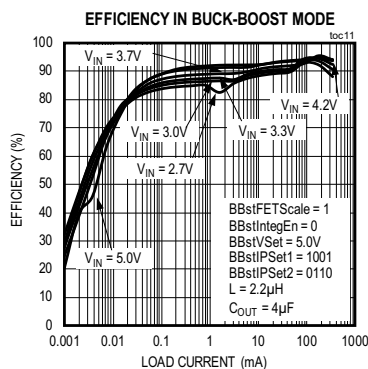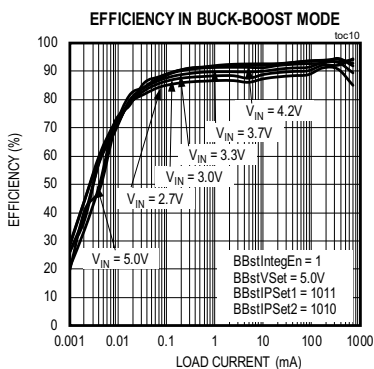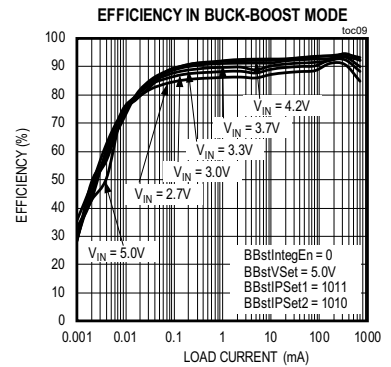
## Typical Operating Characteristics

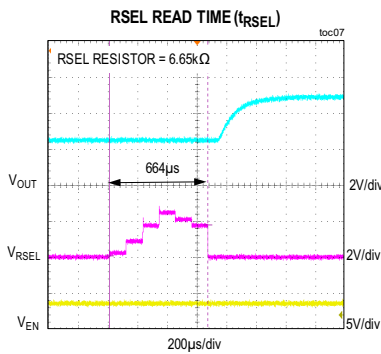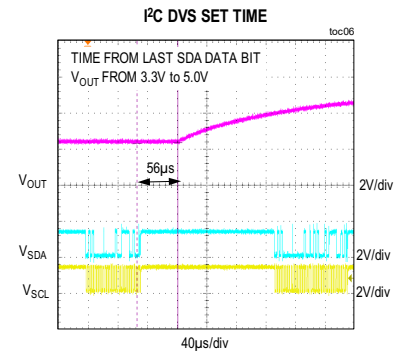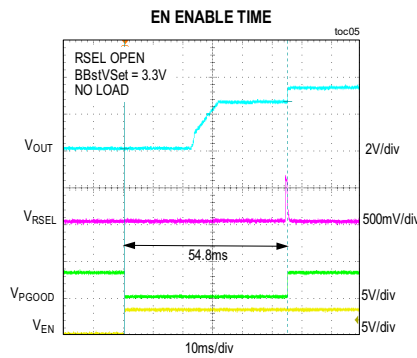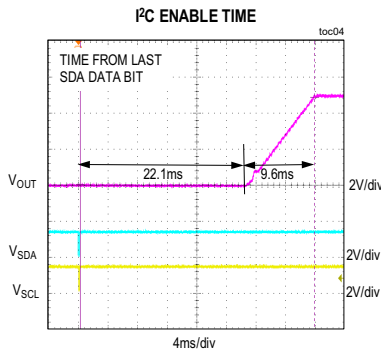($V_{IN}$ = +3.7V, $C_{IN}$ = GRM155R60J226ME11, refer to Figure 9 single capacitor derating, $C_{OUT}$ = 2x GRM155R60J226ME11, L = 1µH, BBstZCCmpDis = 0, BBstLowEMI = 0, BBstMode = 0, SwoFrcIN = 1, BBstIPAdptDis = 0, BBstFETScale = 0, $T_A$ = +25°C, unless otherwise noted.)

## Typical Operating Characteristics (continued)

($V_{IN}$ = +3.7V, $C_{IN}$ = GRM155R60J226ME11, refer to Figure 9 single capacitor derating, $C_{OUT}$ = 2x GRM155R60J226ME11, L = 1µH, BBstZCCmpDis = 0, BBstLowEMI = 0, BBstMode = 0, SwoFrcIN = 1, BBstIPAdptDis = 0, BBstFETScale = 0, $T_A$ = +25°C, unless otherwise noted.)



I²C ENABLE TIME



EN ENABLE TIME



I²C DVS SET TIME



RSEL READ TIME ($t_{RSEL}$)



$V_{OUT}$ TRANSITION TIME RAMP DISABLED



EFFICIENCY IN BUCK-BOOST MODE



EFFICIENCY IN BUCK-BOOST MODE



EFFICIENCY IN BUCK-BOOST MODE



EFFICIENCY IN BUCK-BOOST MODE

## Typical Operating Characteristics (continued)

($V_{IN}$ = +3.7V, $C_{IN}$ = GRM155R60J226ME11, refer to Figure 9 single capacitor derating, $C_{OUT}$ = 2x GRM155R60J226ME11, L = 1µH, BBstZCCmpDis = 0, BBstLowEMI = 0, BBstMode = 0, SwoFrcIN = 1, BBstIPAdptDis = 0, BBstFETScale = 0, $T_A$ = +25°C, unless otherwise noted.)



EFFICIENCY IN BUCK-ONLY MODE
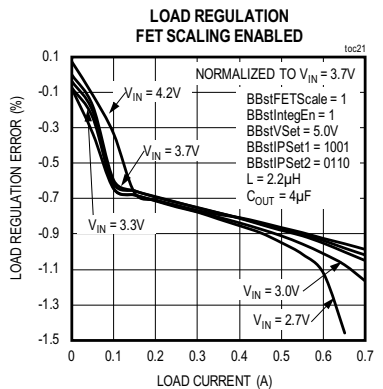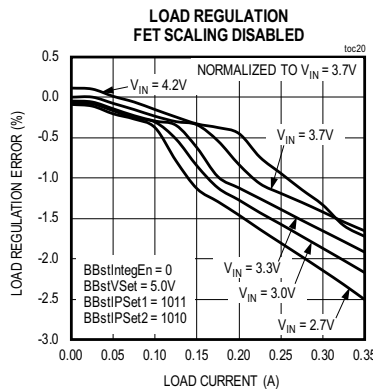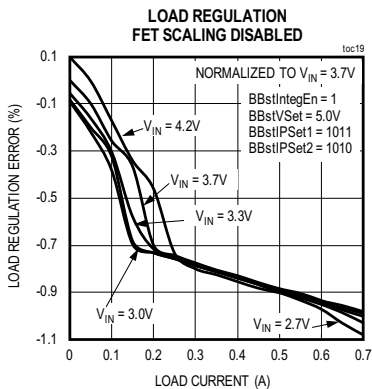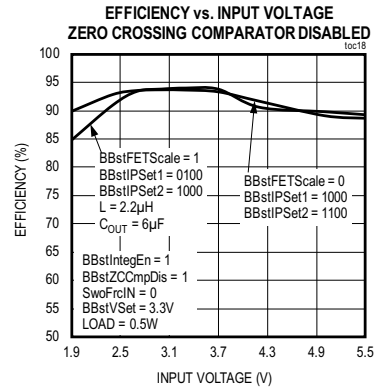
toc13

BBstMode = 1
BBstIntegEn = 0
SwoFrcIN = 0
BBstVSet = 3.3V
BBstIPSet1 = 1110
BBstIPSet2 = 1111



EFFICIENCY IN BUCK-ONLY MODE

toc14

BBstMode = 1
BBstIntegEn = 1
SwoFrcIN = 0
BBstVSet = 3.3V
BBstIPSet1 = 1110
BBstIPSet2 = 1111



EFFICIENCY IN BUCK-ONLY MODE

toc15

BBstMode = 1
BBstFETScale = 1
BBstIntegEn = 0
SwoFrcIN = 0
BBstVSet = 3.3V
BBstIPSet1 = 1110
BBstIPSet2 = 1111
L = 2.2µH
$C_{OUT}$ = 6µF



EFFICIENCY IN BUCK-ONLY MODE

toc16

BBstMode = 1
BBstFETScale = 1
BBstIntegEn = 1
SwoFrcIN = 0
BBstVSet = 3.3V
BBstIPSet1 = 1110
BBstIPSet2 = 1111
L = 2.2µH
$C_{OUT}$ = 6µF



EFFICIENCY vs. INPUT VOLTAGE
ZERO CROSSING COMPARATOR ENABLED

toc17

BBstFETScale = 0
BBstIPSet1 = 1000
BBstIPSet2 = 1100

BBstFETScale = 1
BBstIPSet2 = 1000
L = 2.2µH
$C_{OUT}$ = 6µF

BBstIntegEn = 1
BBstZCCmpDis = 0
SwoFrcIN = 0
BBstVSet = 3.3V
LOAD = 0.5W



EFFICIENCY vs. INPUT VOLTAGE
ZERO CROSSING COMPARATOR DISABLED

toc18

BBstFETScale = 1
BBstIPSet1 = 0100
BBstIPSet2 = 1000
L = 2.2µH
$C_{OUT}$ = 6µF

BBstFETScale = 0
BBstIPSet1 = 1000
BBstIPSet2 = 1100

BBstIntegEn = 1
BBstZCCmpDis = 1
SwoFrcIN = 0
BBstVSet = 3.3V
LOAD = 0.5W



LOAD REGULATION
FET SCALING DISABLED

toc19

NORMALIZED TO $V_{IN}$ = 3.7V

BBstIntegEn = 1
BBstVSet = 5.0V
BBstIPSet1 = 1011
BBstIPSet2 = 1010



LOAD REGULATION
FET SCALING DISABLED

toc20

NORMALIZED TO $V_{IN}$ = 3.7V

BBstIntegEn = 0
BBstVSet = 5.0V
BBstIPSet1 = 1011
BBstIPSet2 = 1010



LOAD REGULATION
FET SCALING ENABLED

toc21

NORMALIZED TO $V_{IN}$ = 3.7V

BBstFETScale = 1
BBstIntegEn = 1
BBstVSet = 5.0V
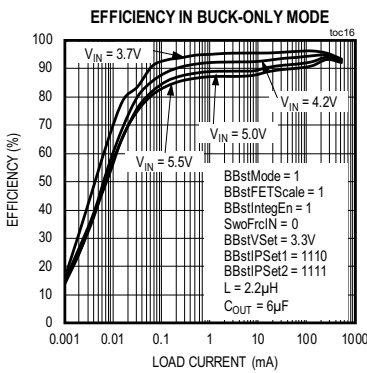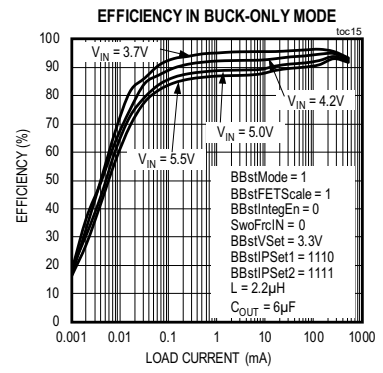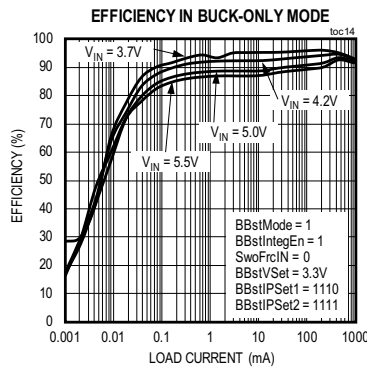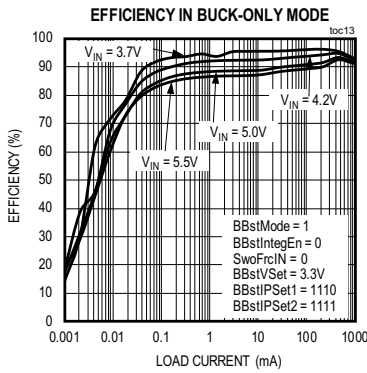BBstIPSet1 = 1001
BBstIPSet2 = 0110
L = 2.2µH
$C_{OUT}$ = 4µF

## Typical Operating Characteristics (continued)

($V_{IN}$ = +3.7V, $C_{IN}$ = GRM155R60J226ME11, refer to Figure 9 single capacitor derating, $C_{OUT}$ = 2x GRM155R60J226ME11, L = 1µH, BBstZCCmpDis = 0, BBstLowEMI = 0, BBstMode = 0, SwoFrcIN = 1, BBstIPAdptDis = 0, BBstFETScale = 0, $T_A$ = +25°C, unless otherwise noted.)
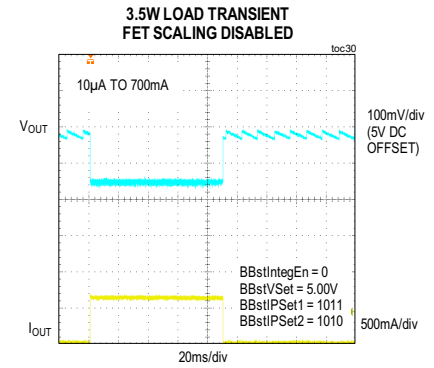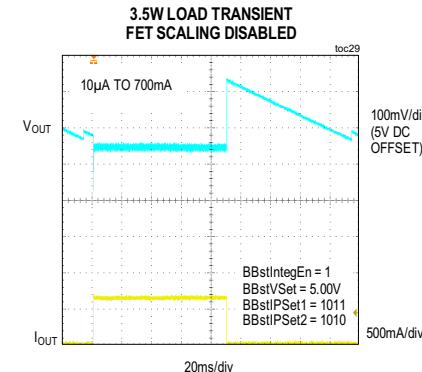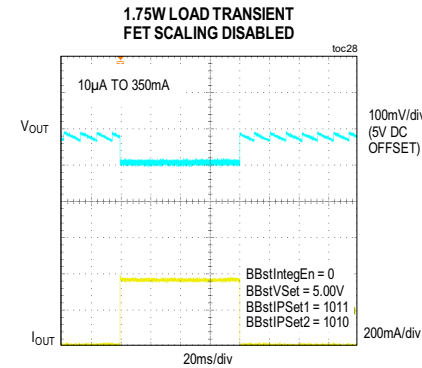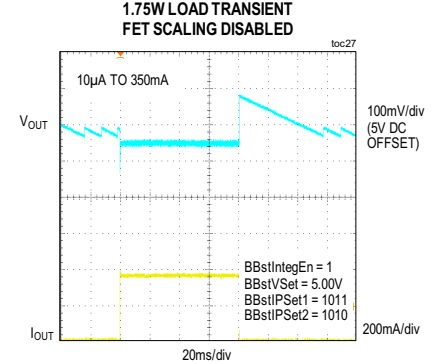
## Typical Operating Characteristics (continued)

($V_{IN}$ = +3.7V, $C_{IN}$ = GRM155R60J226ME11, refer to Figure 9 single capacitor derating, $C_{OUT}$ = 2x GRM155R60J226ME11, L = 1µH, BBstZCCmpDis = 0, BBstLowEMI = 0, BBstMode = 0, SwoFrcIN = 1, BBstIPAdptDis = 0, BBstFETScale = 0, $T_A$ = +25°C, unless otherwise noted.)



0.875W LOAD TRANSIENT
FET SCALING ENABLED
toc31
10µA TO 175mA
$V_{OUT}$
100mV/div
(5V DC
OFFSET)
BBstFETScale = 1
BBstIntegEn = 1
BBstVSet = 5.00V
BBstIPSet1 = 1001
BBstIPSet2 = 0110
$I_{OUT}$
100mA/div
20ms/div



0.875W LOAD TRANSIENT
FET SCALING ENABLED
toc32
10µA TO 175mA
$V_{OUT}$
100mV/div
(5V DC
OFFSET)
BBstFETScale = 1
BBstIntegEn = 0
BBstVSet = 5.00V
BBstIPSet1 = 1001
BBstIPSet2 = 0110
$I_{OUT}$
100mA/div
20ms/div



1.75W LOAD TRANSIENT
FET SCALING ENABLED
toc33
10µA TO 350mA
$V_{OUT}$
100mV/div
(5V DC
OFFSET)
BBstFETScale = 1
BBstIntegEn = 1
BBstVSet = 5.00V
BBstIPSet1 = 1001
BBstIPSet2 = 0110
$I_{OUT}$
200mA/div
20ms/div



1.75W LOAD TRANSIENT
FET SCALING ENABLED
toc34
10µA TO 350mA
$V_{OUT}$
100mV/div
(5V DC
OFFSET)
BBstFETScale = 1
BBstIntegEn = 0
BBstVSet = 5.00V
BBstIPSet1 = 1001
BBstIPSet2 = 0110
$I_{OUT}$
200mA/div
20ms/div



LOAD TRANSIENT WITHOUT FAST MODE
toc35
10µA TO 700mA
BBstIntegEn = 0
BBstFast = 0
BBstVSet = 5.00V
BBstIPSet1 = 1011
BBstIPSet2 = 1010
$V_{OUT}$
100mV/div
(5V DC
OFFSET)
$I_{OUT}$
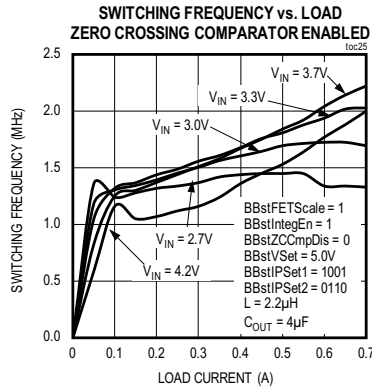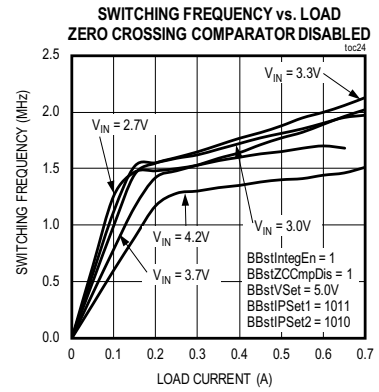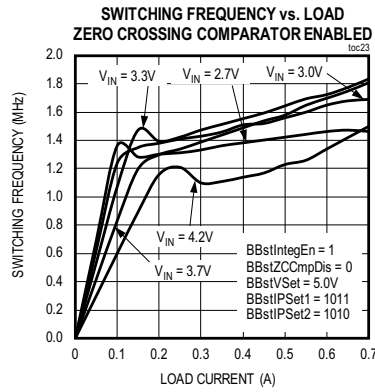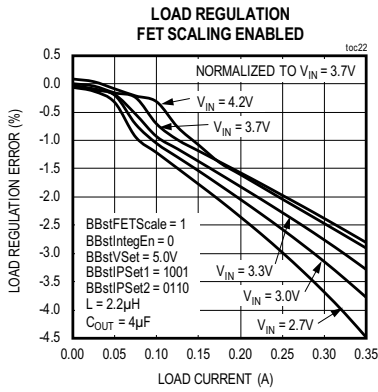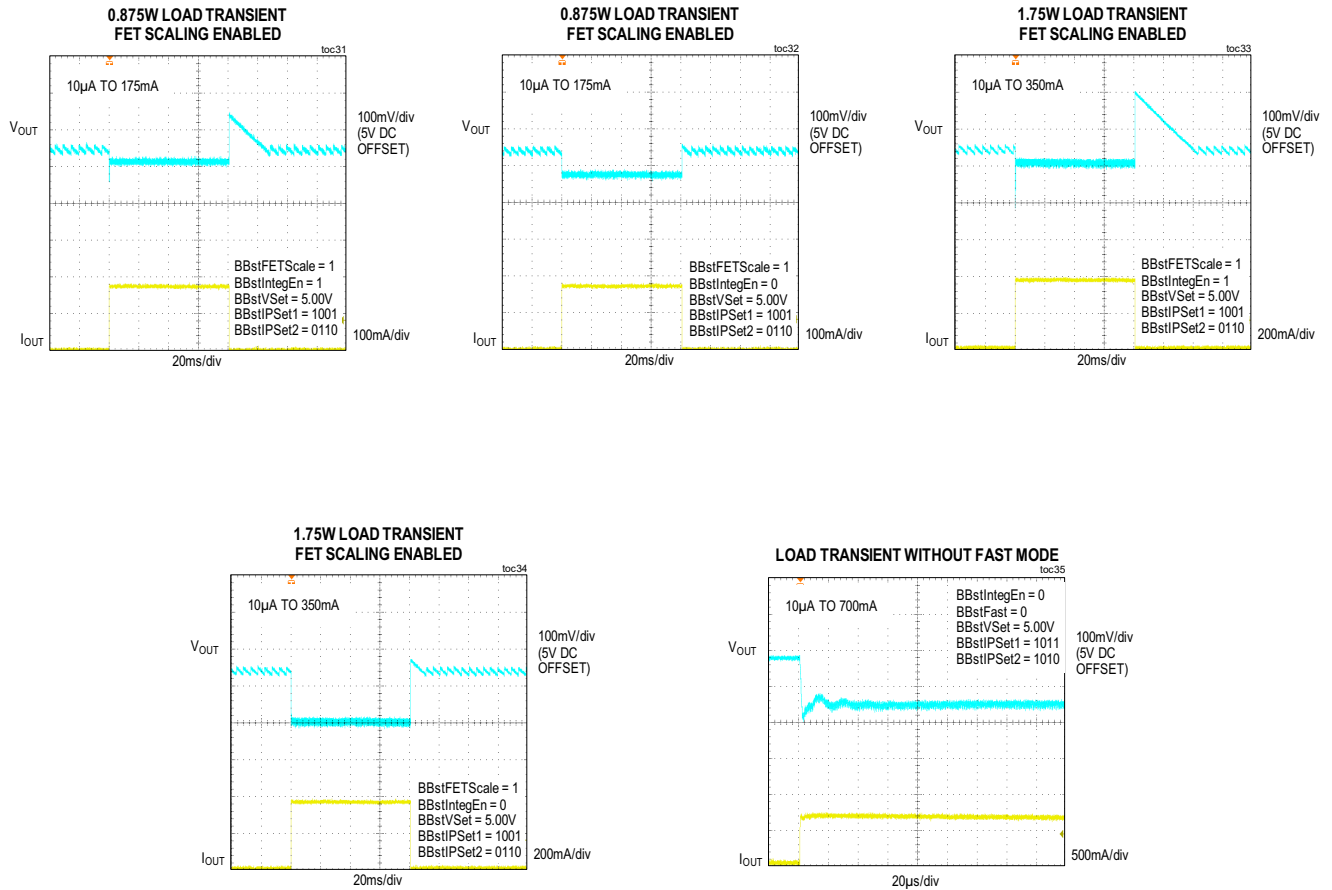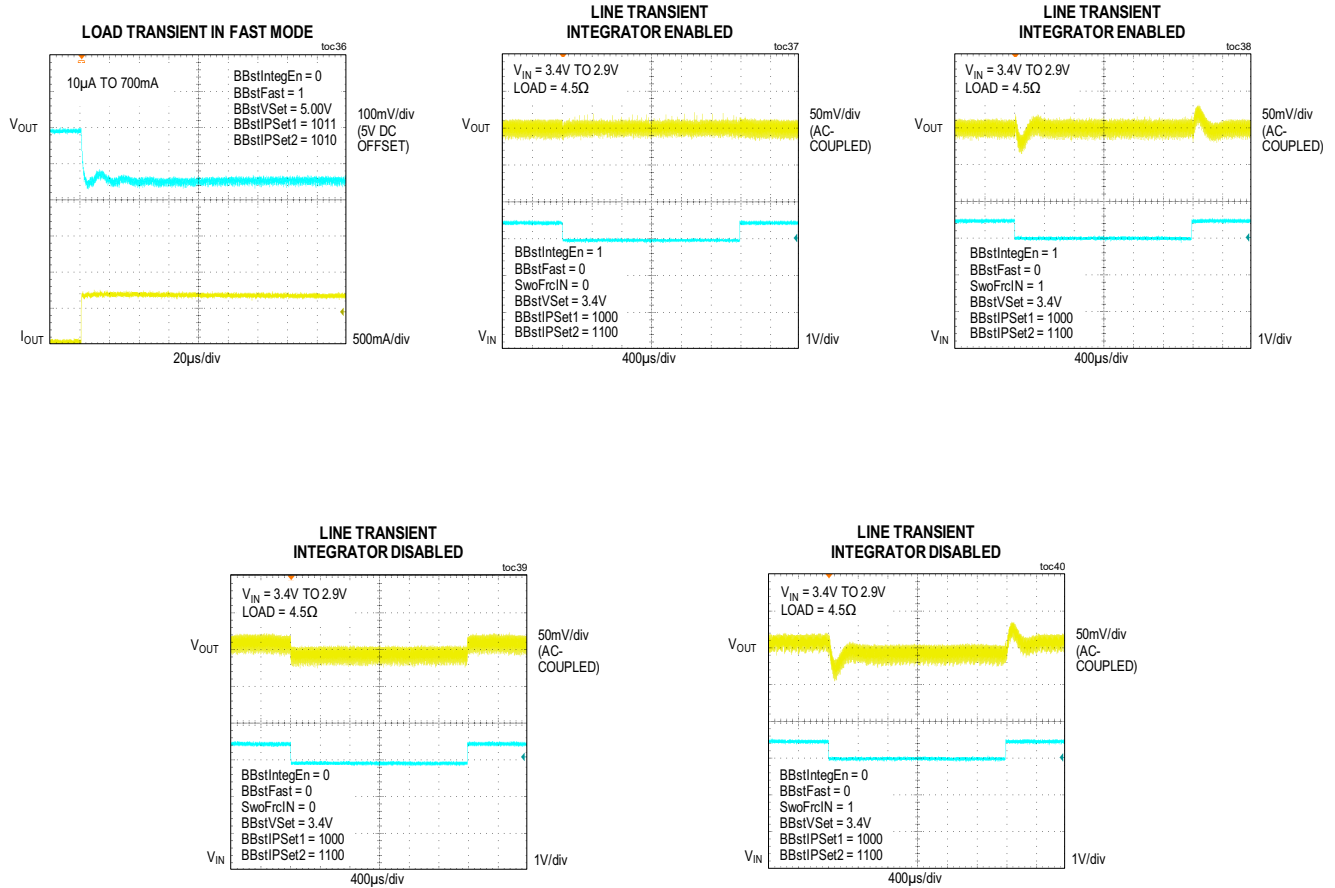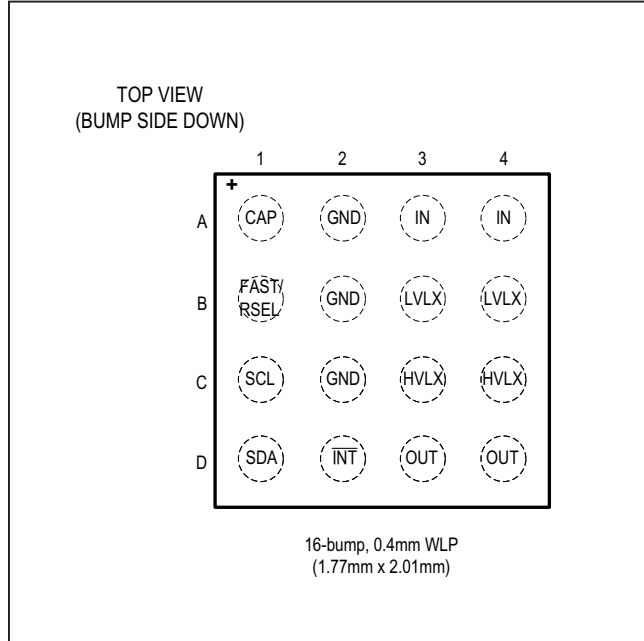500mA/div
20µs/div

## Typical Operating Characteristics (continued)

($V_{IN}$ = +3.7V, $C_{IN}$ = GRM155R60J226ME11, refer to Figure 9 single capacitor derating, $C_{OUT}$ = 2x GRM155R60J226ME11, L = 1µH, BBstZCCmpDis = 0, BBstLowEMI = 0, BBstMode = 0, SwoFrcIN = 1, BBstIPAdptDis = 0, BBstFETScale = 0, $T_A$ = +25°C, unless otherwise noted.)

**LOAD TRANSIENT IN FAST MODE**
toc36

10µA TO 700mA

BBstIntegEn = 0
BBstFast = 1
BBstVSet = 5.00V
BBstIPSet1 = 1011
BBstIPSet2 = 1010

$V_{OUT}$

100mV/div
(5V DC
OFFSET)

$I_{OUT}$

500mA/div

20µs/div

**LINE TRANSIENT
INTEGRATOR ENABLED**
toc37

$V_{IN}$ = 3.4V TO 2.9V
LOAD = 4.5Ω

$V_{OUT}$

50mV/div
(AC-
COUPLED)

BBstIntegEn = 1
BBstFast = 0
SwoFrcIN = 0
BBstVSet = 3.4V
BBstIPSet1 = 1000
BBstIPSet2 = 1100

$V_{IN}$

1V/div

400µs/div

**LINE TRANSIENT
INTEGRATOR ENABLED**
toc38

$V_{IN}$ = 3.4V TO 2.9V
LOAD = 4.5Ω

$V_{OUT}$

50mV/div
(AC-
COUPLED)

BBstIntegEn = 1
BBstFast = 0
SwoFrcIN = 1
BBstVSet = 3.4V
BBstIPSet1 = 1000
BBstIPSet2 = 1100

$V_{IN}$

1V/div

400µs/div

**LINE TRANSIENT
INTEGRATOR DISABLED**
toc39

$V_{IN}$ = 3.4V TO 2.9V
LOAD = 4.5Ω

$V_{OUT}$

50mV/div
(AC-
COUPLED)

BBstIntegEn = 0
BBstFast = 0
SwoFrcIN = 0
BBstVSet = 3.4V
BBstIPSet1 = 1000
BBstIPSet2 = 1100

$V_{IN}$

1V/div

400µs/div

**LINE TRANSIENT
INTEGRATOR DISABLED**
toc40

$V_{IN}$ = 3.4V TO 2.9V
LOAD = 4.5Ω

$V_{OUT}$

50mV/div
(AC-
COUPLED)

BBstIntegEn = 0
BBstFast = 0
SwoFrcIN = 1
BBstVSet = 3.4V
BBstIPSet1 = 1000
BBstIPSet2 = 1100

$V_{IN}$

1V/div

400µs/div

## Pin Configuration

### I²C-Controlled WLP

TOP VIEW
(BUMP SIDE DOWN)

|  | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| A | CAP | GND | IN | IN |
| B | FAST/RSEL | GND | LVLX | LVLX |
| C | SCL | GND | HVLX | HVLX |
| D | SDA | INT | OUT | OUT |

16-bump, 0.4mm WLP
(1.77mm x 2.01mm)

### Single-Pin-Enabled WLP

TOP VIEW
(BUMP SIDE DOWN)

|  | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| A | CAP | GND | IN | IN |
| B | FAST/RSEL | GND | LVLX | LVLX |
| C | INGOOD | GND | HVLX | HVLX |
| D | EN | PGOOD | OUT | OUT |

16-bump, 0.4mm WLP
(1.77mm x 2.01mm)

### I²C-Controlled FC2QFN

TOP VIEW
(PAD SIDE DOWN)

| Pin | Name |
|---|---|
| 1 | CAP |
| 2 | FAST/RSEL |
| 3 | SCL |
| 4 | SDA |
| 5 | INT |
| 6 | OUT |
| 7 | OUT |
| 8 | HVLX |
| 9 | LVLX |
| 10 | IN |
| 11 | IN |
| 12 | GND |

12-PIN, 0.5mm FC2QFN
(2.50mm x 2.50mm)

### Single-Pin-Enabled FC2QFN

TOP VIEW
(PAD SIDE DOWN)

| Pin | Name |
|---|---|
| 1 | CAP |
| 2 | FAST/RSEL |
| 3 | INGOOD |
| 4 | EN |
| 5 | PGOOD |
| 6 | OUT |
| 7 | OUT |
| 8 | HVLX |
| 9 | LVLX |
| 10 | IN |
| 11 | IN |
| 12 | GND |

12-PIN, 0.5mm FC2QFN
(2.50mm x 2.50mm)

## Pin Description

| PIN | | | | NAME | FUNCTION |
|---|---|---|---|---|---|
| I²C-Controlled WLP | Single-Pin-Enabled WLP | I²C-Controlled FC2QFN | Single-Pin-Enabled FC2QFN | | |
| A1 | A1 | 1 | 1 | CAP | Bypass Capacitor Connection for Internal Supply. Connect through 470nF of capacitance to GND. |
| A2, B2, C2 | A2, B2, C2 | 12 | 12 | GND | Ground |
| A3, A4 | A3, A4 | 10, 11 | 10, 11 | IN | Input Supply. Bypass to GND with effective capacitance equal to the minimum of 5µF and the value of the derating curve (Figure 9) for a bias voltage $V_{IN}$ placed as close to the device as possible. |
| B1 | B1 | 2 | 2 | FAST* | Fast Transient Response. When FAST is high, the quiescent current of MAX20343 increases in order to improve response time to a load step. When FAST is low, the quiescent current is decreased to save power. |
| B1 | B1 | 2 | 2 | RSEL* | Output Voltage Select. Connect a resistor from RSEL to GND based on the desired output voltage. See Figure 8. |
| B3, B4 | B3, B4 | 9 | 9 | LVLX | Switching Node. Connect to HVLX through a 1µH inductor if BBstFETScale = 0 or a 2.2µH inductor if BBstFETScale = 1. |
| C1 | — | 3 | — | SCL | I²C Serial Clock Input |
| — | C1 | — | 3 | INGOOD | Input Power Good. LOW indicates that the CAP pin voltage is forced to $V_{OUT}$ and the input voltage is below $V_{IN\_UVLO\_F}$ when $V_{OUT} \geq 3.3V$ and the soft-start period is complete. Power capabilities might be limited. If CAP is forced to $V_{IN}$, INGOOD does not function when $V_{IN} < V_{IN\_UVLO\_F}$. It is an open drain output and should be connected to an external logic supply using a pullup resistor. |
| C3, C4 | C3, C4 | 8 | 8 | HVLX | Switching Node. Connect to LVLX through a 1µH inductor if BBstFETScale = 0 or a 2.2µH inductor if BBstFETScale = 1. |
| D1 | — | 4 | — | SDA | I²C Serial Data Input/Open-Drain Output |
| — | D1 | — | 4 | EN | Enable. Active high. |
| D2 | — | 5 | — | $\overline{INT}$ | Interrupt Output. Open-drain, connect through pullup resistor to system logic supply. |
| — | D2 | — | 5 | PGOOD | Power Good Output. Indicates when output is ready for use. It is an open drain output and should be connected to an external logic supply using a pullup resistor. |
| D3, D4 | D3, D4 | 6, 7 | 6, 7 | OUT | Buck-Boost Output. If BBstFETScale = 0, bypass to GND with effective capacitance equal to twice the value of the derating curve (Figure 9) for a bias voltage $V_{OUT}$, placed as close to the device as possible. If BBstFETScale = 1, bypass to GND with effective capacitance equal to the value of the derating curve (Figure 9) for a bias voltage $V_{OUT}$, placed as close to the device as possible. |

*The function of B1 is determined by the factory configuration of the device. See Table 2 for the specific configuration of each device.*

## Functional Diagram



*I²C CONTROLLED VERSION ONLY
**SINGLE-PIN-ENABLED VERSION ONLY
***FACTORY OPTION, FAST OR RSEL
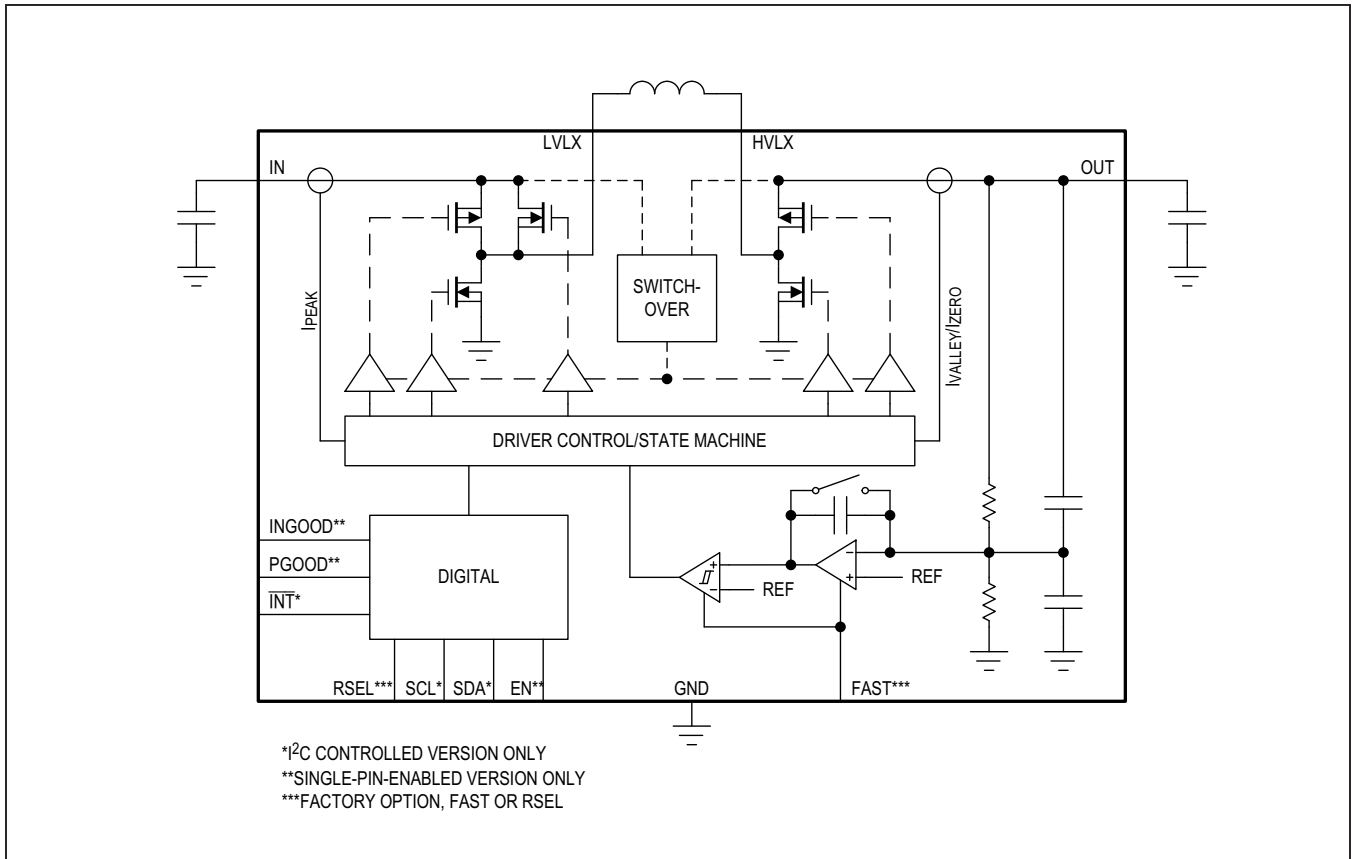
## Detailed Description

The MAX20343 is an ultra-low quiescent current, non-inverting buck-boost converter with 1A current capability at 3.5V intended for applications that require long run times while also demanding bursts of high current. A peak/valley current-controlled hysteretic architecture yields a fast transient response time with minimal settling time that allows the device to handle large load transients in high peak-power applications. The device has a unique control algorithm that seamlessly transitions between buck, buck-boost, and boost operation to minimize discontinuities and sub-harmonic noise in the output ripple.

The low, 1.9V startup voltage is compatible with a variety of power sources, and the near-zero minimum operating voltage extracts as much energy as possible from the source. Low inductance and capacitance requirements allow for a small total-solution size and make the MAX20343 well-suited for space-constrained applications. The device has a high efficiency and low noise that also makes it suitable for wireless and noise-sensitive applications such as LPWAN and optical sensor systems. It has an ultra-low, 3.5µA (typ) quiescent current and discontinuous conduction mode (DCM) to operate at low loads and extend run time in low average-power, battery-powered applications

### Startup Voltage

The MAX20343 is guaranteed to start up with a minimum input voltage of 1.9V. After device startup, an internal bootstrapping function allows the device to operate down to a 0.5V input. See the "Input Operating Voltage" section for more details.

## Architectural Description

The MAX20343 buck-boost comprises a typical non-inverting buck-boost topology. Figure 1 illustrates the basic structure of the regulator with arrows depicting the inductor current flow in each switching phase.

The buck-boost features a frequency comparator to monitor its switching frequency. Switching frequency increases as the load current increases. Under low loads, the buck-boost optimizes its feedback loop for low quiescent current. When load requirements increase the switching frequency to the $f_{HIGH}$ threshold, the low-quiescent current mode is disabled to improve response time. The $f_{HIGH}$ threshold is set by BBFHighSH[1:0] in the BBstCfg1 register. Hysteresis prevents the buck-boost regulator from resuming the low-quiescent current mode until the switch frequency decreases to $f_{HIGH}$ / 4.

### Switching Phases

Depending on the buck-boost configurations, the topology enters different sequences of phases to generate the desired output voltage. Only two switches are on in each phase.

- Phase 1: MP1 on, MP2 on. Inductor charges.
- Phase 2: MP1 on, MN2 on. Inductor charges.
- Phase 3: MN1 on, MP2 on. Inductor discharges.
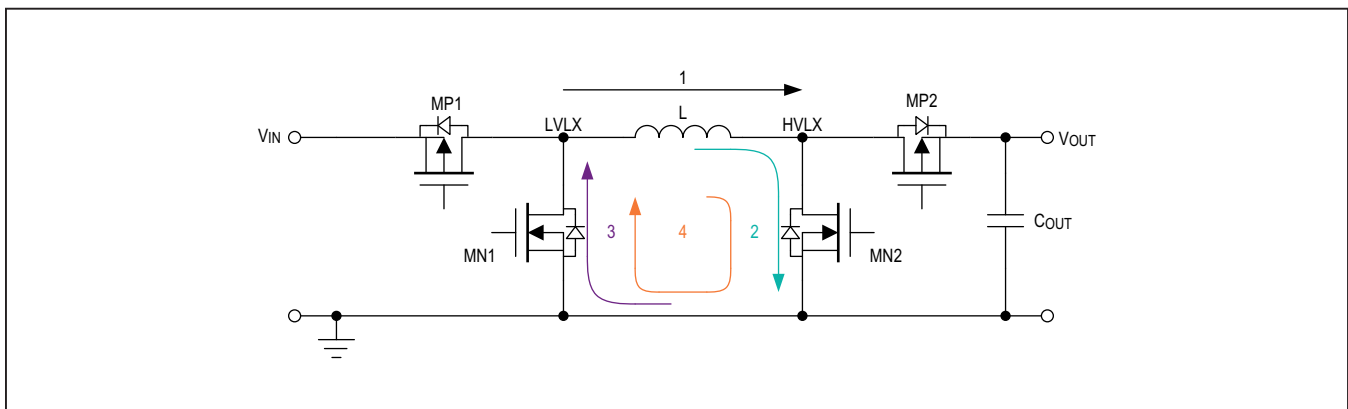- Phase 4: MN1 on, MN2 on. Freewheeling.



Figure 1. The Buck-Boost Regulator and Switching Phases

## Buck-Boost Mode

When BBstMode = 0 (register 0x01[2]), the regulator operates in buck-boost mode. The inductor charges in Phase 2 up to BBstIPSet1 (register 0x03[3:0]). This minimizes noise when $V_{IN}$ is close to $V_{OUT}$. The buck-boost then transitions to Phase 1. If $V_{IN} > V_{OUT}$, the inductor continues charging until either the current reaches BBstIPSet1 + BBstIPSet2 (register 0x03[7:4]) or after a 500ns delay. If $V_{IN} \leq V_{OUT}$, the buck-boost waits for the 500ns timeout to elapse or until the current drops to the valley limit. Next, the regulator enters Phase 3 to discharge the inductor current to the valley limit. When the inductor current reaches the valley-current crossing threshold or falls below 0, the regulator freewheels in Phase 4 until the next charge phase. When operating in continuous conduction mode (CCM), the buck-boost enters Phase 4 for approximately 30ns if BBstZCCmpDis = 1 (register 0x01[4]). The buck-boost skips Phase 4 when operating in CCM and BBstZCCmpDis = 0. The valley behavior is determined by BBstZCCmpDis. Figure 2 shows the inductor current in buck-boost mode.

## Buck-Only Mode

To maximize efficiency when $V_{IN} > V_{OUT}$, the buck-boost regulator has a buck-only mode. When BBstMode = 1, the regulator behaves as a synchronously rectified buck regulator. If the device is set to buck-only mode, the regulator never enters Phase 2. Instead, the inductor is always charged in Phase 1. The inductor charges until the inductor current reaches BBstIPSet1 or the 500ns timeout elapses. The regulator then transitions to Phase 3 to provide a path to deliver the inductor current to the output. Figure 3 shows the inductor current in buck-only mode.

Buck-only mode reduces switching losses present in buck-boost mode. Buck-only mode should be used when $V_{OUT}$ is always less than $V_{IN}$ to maximize efficiency.

## Inductor Peak and Valley Current Limits

The buck-boost regulator monitors the maximum and minimum values of the inductor current to control output noise and reduce switching losses. If BBstAdptDis = 1 (register 0x04[1]), the peak currents are fixed to the values in BBstISet (register 0x03) and the valley current is fixed to 0mA. If BBstAdptDis = 0, the peak and valley currents are allowed to change based on load requirements.

Peak currents are set in the BBstISet register. BBstIPSet1 controls the peak current when $V_{IN} < V_{OUT}$ and begins the timeout period for Phase 1. BBstIPSet2 sets a secondary current limit in buck-boost mode when $V_{IN} > V_{OUT}$. The total inductor current limit when $V_{IN} > V_{OUT}$ is BBstIPSet1 + BBstIPSet2. The buck-boost

regulator transitions to Phase 3 if the inductor current reaches BBstIPSet1 + BBstIPSet2 before the 500ns timeout has elapsed. Minimizing the difference between BBstIPSet1 and BBstIPSet2 reduces the output ripple, but decreases efficiency. Care must be taken to optimize the peak current settings to keep a low output ripple while maximizing efficiency. Figure 4 and Figure 5 present the safe operating area of BBstIPSet2 with respect to BBstIPSet1. Selecting values different than those of Figure 4 and Figure 5 for a given BBstIPSet1 value can reduce efficiency and increase output ripple. Figure 6 and Figure 7 are graphical guides to selecting combinations of BBstPSet1 and BBstIPSet2 to maximize efficiency for specific BBstVSet values.

For cases where the startup current requirement is different than the nominal operating current, two bits, BBstIP1SS and BBstIP2SS, override BBstIPSet1 and BBstIPSet2, respectively, during soft-start. See BBstIP1SS and BBstIP2SS (Table 2) for device-specific values.
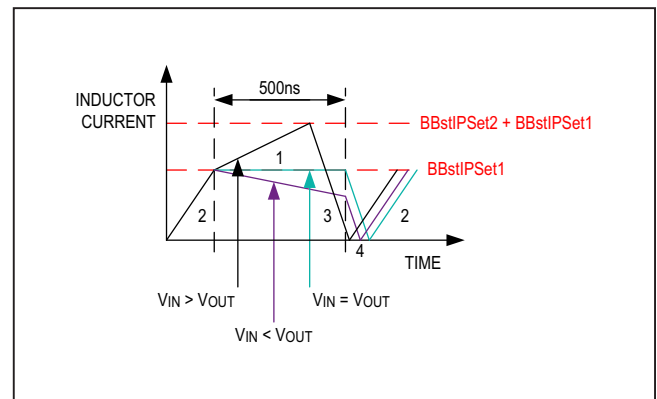


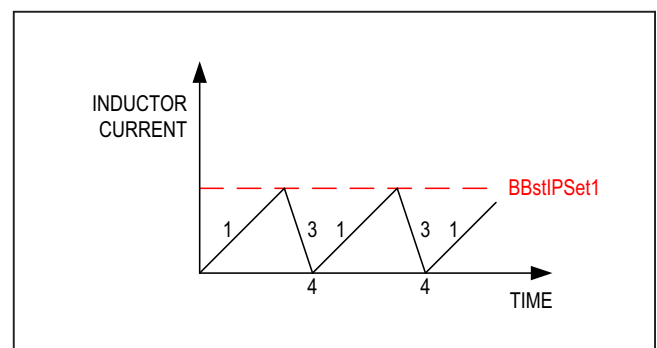Figure 2. Buck-Boost Inductor Current in Buck-Boost Mode



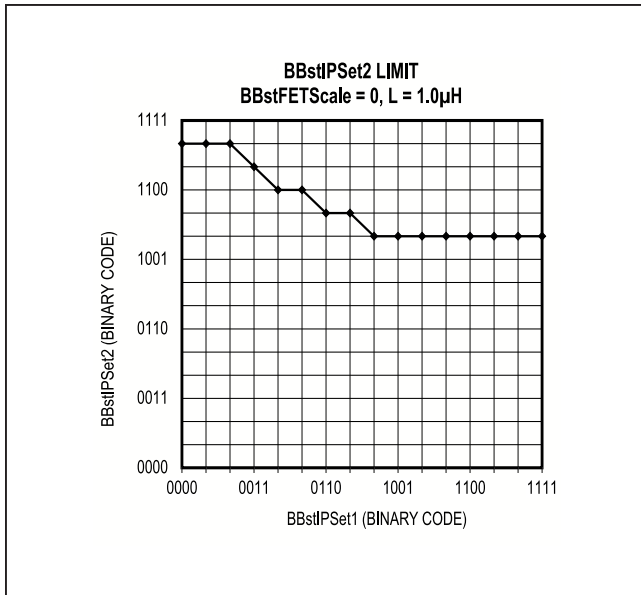Figure 3. Buck-Boost Inductor Current in Buck-Only Mode

Figure 4. Minimum BBstIPSet2 Limit for a Given BBstIPSet1 Setting for BBstFETScale = 0
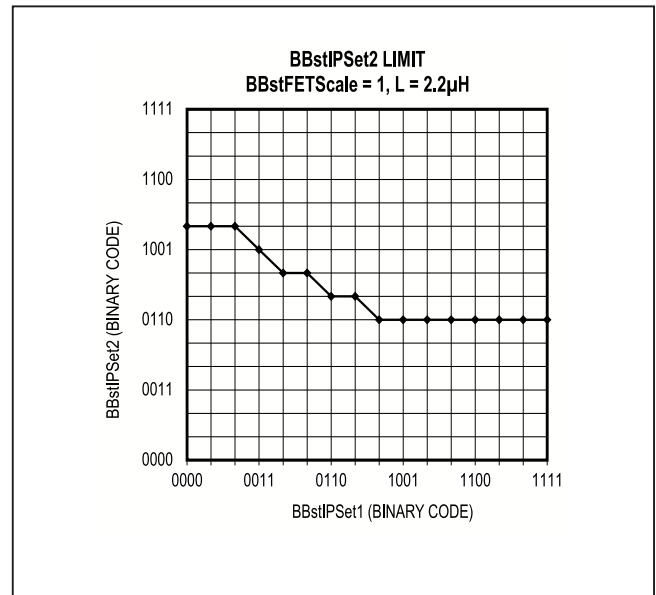


Figure 5. Minimum BBstIPSet2 Limit for a Given BBstIPSet1 Setting for BBstFETScale = 1
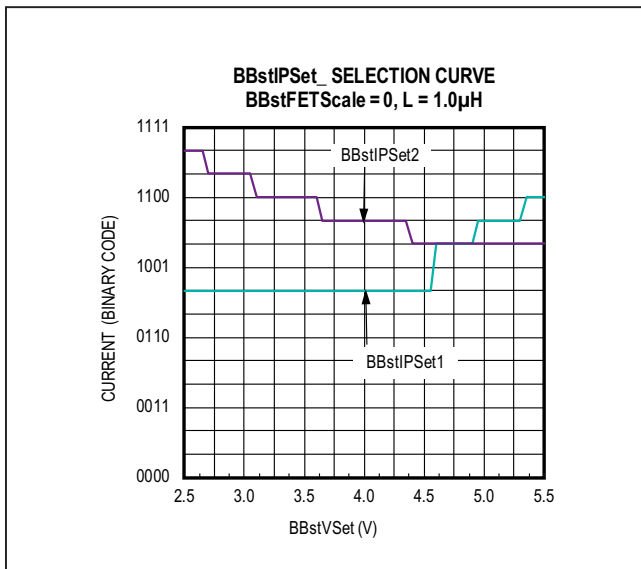


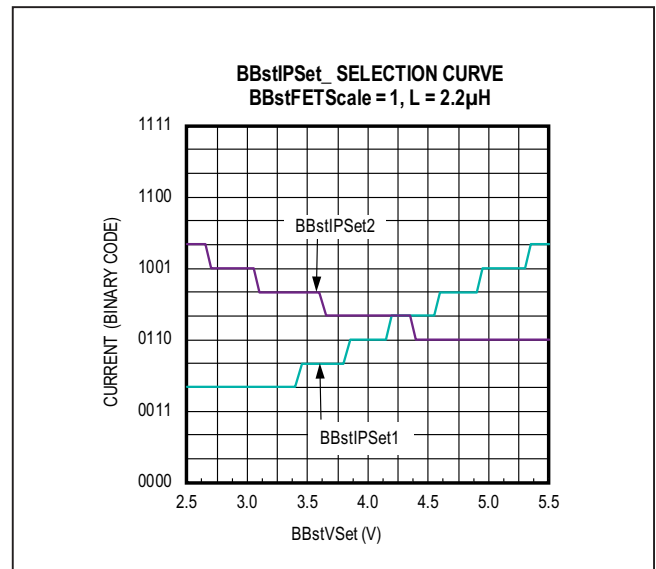Figure 6. Recommended BBstIPSet1 and BBstIPSet2 Settings for BBstFETScale = 0



Figure 7. Recommended BBstIPSet1 and BBstIPSet2 Settings for BBstFETScale = 1

The MAX20343 behavior when BBstIPAdptDis = 0 can be further defined with a zero current comparator. The device transitions to Phase 4 when its control loop detects a zero current crossing.

When BBstZCCmpDis = 1 (register 0x01[4]), the zero crossing comparator is disabled and the buck-boost operates with only peak and valley current limits. In this configuration, the valley current limit acts as the zero crossing limit. In DCM, the valley limit is 0mA and is a true zero current crossing. In CCM, the peak and valley limits are automatically adjusted by the adaptive current control, so the effective zero current point might be larger than 0mA. This causes the MAX20343 to briefly enter Phase 4 each time the inductor current reaches the valley current threshold before transitioning to an inductor-charging phase. Setting BBstZCCmpDis = 0 enables the zero current comparator and the buck-boost operates with peak, valley, and zero crossing current limits. While the adaptive current loop adjusts the peak and valley currents, the zero crossing limit is fixed at 0mA. In DCM, the regulator functions similarly to when BBstZCCmpDis = 1. However, in CCM, the valley current is greater than the zero crossing current, so the regulator bypasses Phase 4 and directly enters an inductor-charging phase when the inductor current reaches the valley current threshold.

Disabling the zero current crossing comparator reduces the buck-boost output ripple. Enabling the comparator improves efficiency in CCM by removing the Phase 4 stage in CCM that is otherwise present when BBstZCCmpDis = 1.

### Integrator Control Loop Disable

The MAX20343 contains an integrator in its control loop for normal operation. This integrator improves the load regulation for larger loads, but increases the transient response time. For applications where the output must quickly settle to a final regulation value to prevent noise injection during sensitive measurements (such as in PPG measurements), the integrator can be disabled so the regulator operates with a proportional-only control loop. The BBstIntegEn bit (register 0x04[2]) enables and disables the integrator to speed response time on load transients (integrator off) or to increase the load capacity (integrator on). Note that when the integrator is disabled output stability is only guaranteed up to the maximum output power for input voltages down to 2.5V. To operate at lower input voltages, the output capacitance must be increased.

### Input Operating Voltage

Operating at low input voltages enables a system to extract as much energy as possible from its energy source before shutting down. The MAX20343 can operate with input voltages as low as 0.5V after initialization to maximize this energy use. This allows a system to run the MAX20343 well below the minimum startup voltage, albeit at a reduced power capability.

When the input voltage is low, the $R_{ON}$ of the input p-channel MOSFET increases. To offset the inherent increase in resistance, an n-channel MOSFET is present in parallel with the input MOSFET. The n-channel MOSFET is only enabled when the input voltage falls below $V_{IN\_UVLO\_F}$ to reduce switching losses at higher input voltages. In order to provide sufficient overdrive for the n-channel device, it is necessary to keep $V_{OUT} \geq 3.3V$. Therefore, high power operation below $V_{IN\_UVLO\_F}$ is only guaranteed if the output voltage is set to 3.3V or above.

The internal supply can be forced to $V_{IN}$ to reduce quiescent current when $V_{IN} > V_{IN\_UVLO\_F}$ to minimize quiescent draw from $V_{OUT}$ (see SwoFrcIN: register 0x04[3]). The MAX20343 input voltage becomes limited only by the amount of power it is able to pull from the source and deliver to the output. As long as the output voltage is maintained, the part remains active.

### Device Control

#### I2C-Controlled

The I2C-controlled versions of MAX20343 enable system flexibility by providing an interface between the device and a host microcontroller. Different parameters of the regulator, such as output voltage the inductor peak current levels, FET scaling, etc., can be optimized in real time for any application. While default values are programmed by the factory, new values can be set in the I2C registers. In versions of the MAX20343 with an I2C interface and an RSEL voltage selection pin, the default voltage selected by the RSEL resistor can be overwritten over I2C after the OutGood (register 0x05[1]) status goes high.

The full configuration settings and status information provided through this interface are detailed in the register descriptions. I2C-controlled versions of MAX20343 have the seven-bit slave address 0b0101000 (0x28). The write address is 0x50 and the read address is 0x51.

**Single-Pin-Enable**

In the single-pin-enabled, fixed-programming versions of MAX20343, all configuration settings excluding the output voltage are programmed by the factory and cannot be modified in an application. Setting EN high turns on the regulator. Two status pins, INGOOD and PGOOD, signal that the input and output voltages are ready to support the full system power requirements, respectively.

When the FAST/RSEL pin of a single-pin-enabled MAX20343 is configured to RSEL, the output voltage is set by the the RSEL resistor at startup. When the FAST/RSEL pin is configured to FAST, the output voltage is set by the factory.

**Dynamic Voltage Scaling (DVS)**

The output voltage of I$^2$C-controlled MAX20343 devices can be changed at any point while the device is enabled without restarting the device. This feature is known as dynamic voltage scaling. DVS enables systems to operate at different voltage rails when the voltage or power requirements of the system change in different operating modes. By decreasing the voltage to the minimum value required by an operating mode, the overall system efficiency increases. The output voltage is set in BBstVSet[5:0] (register 0x02[5:0]).

**RSEL Voltage Setting**

RSEL is a unique, single-resistor output voltage selection method that minimizes quiescent current. Once power is applied at $V_{IN}$ and the enable pin is brought high, the MAX20343 starts up and regulates to the minimum programmable voltage (2.5V). Once an internal PGOOD signal indicates that the voltage has reached an acceptable level, the device begins drawing up to 200µA from $V_{IN}$ in order to read the resistor value on RSEL. This current is only present during the RSEL resistor detection time, typically 750µs. After the detection and output voltage programming period, the output increases to the set value. The output rise time is determined by the BBstRampEn setting Figure 8 illustrates this startup sequence.

RSEL has many benefits, including lower cost and smaller size. Only one resistor is needed versus the two resistors required in typical feedback connections. Another benefit of RSEL is that one regulator can be used in multiple projects with different output voltages just by changing a single standard 1% resistor. Lastly, RSEL eliminates wasting current continuously through feedback resistors for ultra-low power, battery-operated products. Select the RSEL resistor value by choosing the desired output voltage in Table 1. Leaving RSEL open sets the output to the default voltage of the device (see Table 2 for device configurations).
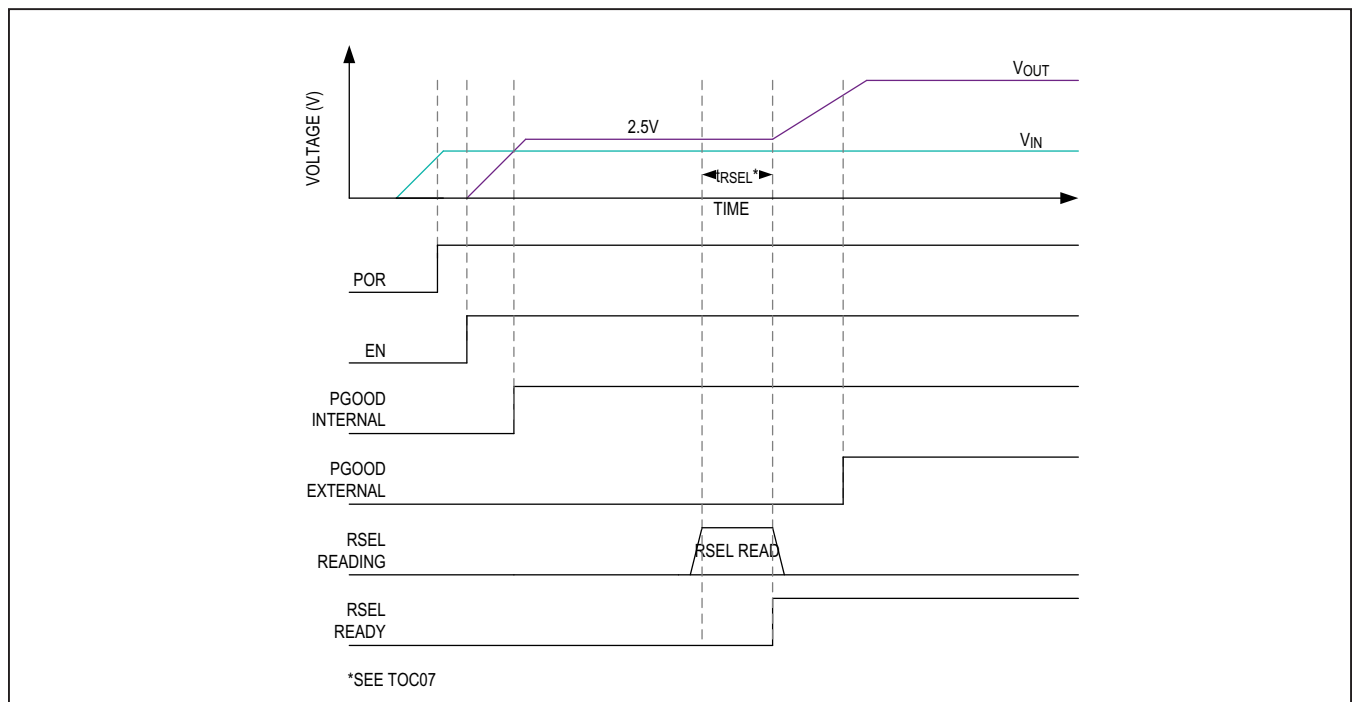


Figure 8. MAX20343 RSEL Startup Sequence

## Table 1. RSEL Selection Table

| OUTPUT VOLTAGE (V) | STD RES 1% (kΩ) |
|---|---|
| Default | OPEN |
| 2.5 | 604 |
| 2.7 | 422 |
| 3.0 | 348 |
| 3.2 | 210 |
| 3.3 | 150 |
| 3.4 | 105 |
| 3.5 | 75 |
| 3.6 | 52.3 |
| 3.7 | 37.4 |
| 3.8 | 26.7 |
| 4.0 | 18.7 |
| 4.2 | 13.3 |
| 4.5 | 9.31 |
| 5.0 | 6.65 |
| 5.5 | SHORT |

## Register Map

### MAX20343

| AD-DRESS | NAME | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|
| **USER** | | | | | | | | | |
| 0x00 | ChipID[7:0] | | | | ChipID[7:0] | | | | |
| 0x01 | BBstCfg0[7:0] | BBstEn | BBstRampEn | BBstFast | BBstZC-CmpDis | BBst-LowEMI | BBst-Mode | BBstActDsc | BBstPsvDsc |
| 0x02 | BBstVSet[7:0] | BBFHighSh[1:0] | | | BBstVSet[5:0] | | | | |
| 0x03 | BBstISet[7:0] | BBstIPSet2[3:0] | | | | BBstIPSet1[3:0] | | | |
| 0x04 | BBstCfg1[7:0] | FstCmpEn | PasThr-Mode | SwoFrcIN | – | – | BBstInt-egEn | BBstI-PAdptDis | BBstFETScale |
| 0x05 | Status[7:0] | – | – | – | – | – | – | OutGood | InUVLO |
| 0x06 | Int[7:0] | – | – | – | – | – | – | Out-GoodInt | InUV-LOInt |
| 0x07 | Mask[7:0] | – | – | – | – | – | – | OutGood-IntM | InUV-LOIntM |
| 0x50 | LockMsk[7:0] | – | – | – | – | – | – | – | BBLck |
| 0x51 | LockUnlock[7:0] | | | | PASSWD[7:0] | | | | |

## Register Details

### ChipID (0x00)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | ChipID[7:0] | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| ChipID | 7:0 | ChipID[7:0] indicates the version of the device in use. |

### BBstCfg0 (0x01)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | BBstEn | BBstRampEn | BBstFast | BBstZCC-mpDis | BBstLowE-MI | BBstMode | BBstActDsc | BBstPsvDsc |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| BBstEn | 7 | Buck-Boost Enable<br>0 = Buck-boost disabled<br>1 = Buck-boost enabled |
| BBstRampEn | 6 | Buck-Boost Ramp Enable<br>0 = Output voltage setting transition is performed without intermediate steps<br>1 = Output voltage setting increases are performed with a digital ramp of 50mV every 50µs |
| BBstFast | 5 | Buck-Boost Pretrigger Mode Setting<br>Increases the quiescent current of the buck-boost to improve output regulation during load transients.<br>0 = Normal, low quiescent current operation<br>1 = Fast response mode enabled. Quiescent current increased to 35µA (typ). |
| BBstZCCmpDis | 4 | Buck-Boost Zero-Crossing Comparator Disable. Latched internally, it can only be changed when BBstEn = 0<br>0 = Enabled<br>1 = Disabled |
| BBstLowEMI | 3 | Buck-Boost Low EMI Mode<br>Increases the rise/fall time of HVLX/LVLX to reduce EMI, at the cost of efficiency.<br>0 = Normal operation<br>1 = Increase rise/fall time on HVLX/LVLX by 3x |
| BBstMode | 2 | Buck-Boost Operating Mode<br>Configures the regulator to operate in buck-boost or buck-only mode. Latched internally, can only be changed while BBstEn = 0.<br>0 = Buck-boost mode<br>1 = Buck-only mode |
| BBstActDsc | 1 | Buck-Boost Active Discharge Control<br>0 = Buck-boost not actively discharged<br>1 = Buck-boost actively discharged on shutdown |
| BBstPsvDsc | 0 | Buck-Boost Passive Discharge Control<br>0 = Buck-boost not passively discharged<br>1 = Buck-boost passively discharged on shutdown |

## BBstVSet (0x02)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | BBFHighSh[1:0] | | BBstVSet[5:0] | | | | | |
| Access Type | Write, Read | | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| BBFHighSh | 7:6 | Buck-Boost $f_{HIGH}$ Thresholds<br>Selects the switching frequency threshold $f_{HIGH}$. If the buck-boost switching frequency exceeds the $f_{HIGH}$ rising threshold, all the blocks are kept ON ($I_Q$ is higher) until the frequency reaches the $f_{HIGH}$ falling threshold. A small glitch on $V_{OUT}$ can be present at the $f_{HIGH}$ crossover.<br>00 = 25kHz rising / 6.125kHz falling<br>01 = 35kHz rising / 8.25kHz falling<br>10 = 50kHz rising / 12.5kHz falling<br>11 = 100kHz rising / 25kHz falling |
| BBstVSet | 5:0 | Buck-Boost Output Voltage Setting<br>2.5V to 5.5V, Linear Scale, 50mV increments<br>000000 = 2.5V<br>000001 = 2.55V<br>...<br>≥111100 = 5.5V |

## BBstISet (0x03)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | | BBstIPSet2[3:0] | | | | BBstIPSet1[3:0] | | |
| Access Type | | Write, Read | | | | Write, Read | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| BBstIPSet2 | 7:4 | Buck-Boost Nominal Maximum Peak Current Setting<br>See buck-boost operation section for a description of the peak current settings. 0mA (minimum $t_{ON}$) to 618.75mA, linear scale, 41.25mA increments for BBstFETScale = 0. 0mA (minimum $t_{ON}$) to 375mA, linear scale, 25mA increments for BBstFETScale = 1.<br><br>BBstFETScale = 0:<br>0000 = 0mA (minimum $t_{ON}$)<br>0001 = 41.25mA<br>...<br>1111 = 618.75mA<br><br>Recommended settings<br>$V_{OUT}$ ≤ 2.65V: 577.50mA<br>2.65V < $V_{OUT}$ ≤ 3.05V: 536.25mA<br>3.05V < $V_{OUT}$ ≤ 3.60V: 495mA<br>3.60V < $V_{OUT}$ ≤ 4.35V: 453.75mA<br>$V_{OUT}$ > 4.35V: 412.50mA<br><br>BBstFETScale = 1:<br>0000 = 0mA (minimum $t_{ON}$)<br>0001 = 25mA<br>...<br>1111 = 375mA<br><br>Recommended settings<br>$V_{OUT}$ ≤ 2.65V: 250mA<br>2.65V < $V_{OUT}$ ≤ 3.05V: 225mA<br>3.05V < $V_{OUT}$ ≤ 3.60V: 200mA<br>3.60V < $V_{OUT}$ ≤ 4.35V: 175mA<br>$V_{OUT}$ > 4.35V: 150mA |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|-------------|
| BBstIPSet1 | 3:0 | Buck-boost nominal peak current setting 1<br>Nominal peak current when charging inductor between $V_{IN}$ and GND. See buck-boost operation section for a description of the peak current settings. 0mA (minimum $t_{ON}$) to 618.75mA, linear scale, 41.25mA increments for BBstFETScale = 0. 0mA (minimum $t_{ON}$) to 375mA, linear scale, 25mA increments for BBstFETScale = 1.<br><br>BBstFETScale = 0:<br>0000 = 0mA (minimum $t_{ON}$)<br>0001 = 41.25mA<br>...<br>1111 = 618.75mA<br><br>Recommended settings<br>$V_{OUT} \leq 4.55V$: 330mA<br>$4.55V < V_{OUT} \leq 4.90V$: 412.50mA<br>$4.90V < V_{OUT} \leq 5.30V$: 453.75mA<br>$V_{OUT} > 5.3V$: 495mA<br><br>BBstFETScale = 1:<br>0000 = 0mA (minimum $t_{ON}$)<br>0001 = 25mA<br>...<br>1111 = 375mA<br><br>Recommended settings<br>$V_{OUT} \leq 3.40V$: 100mA<br>$3.40V < V_{OUT} \leq 3.80V$: 125mA<br>$3.80V < V_{OUT} \leq 4.15V$: 150mA<br>$4.20V < V_{OUT} \leq 4.55V$: 175mA<br>$4.60V < V_{OUT} \leq 4.90V$: 200mA<br>$4.95V < V_{OUT} \leq 5.30V$: 225mA<br>$V_{OUT} > 5.30V$: 250mA |

## BBstCfg1 (0x04)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | FstCmpEn | PasThr-Mode | SwoFrcIN | – | – | BBstIntegEn | BBstIPAdpt-Dis | BBst-FETScale |
| **Access Type** | Write, Read | Write, Read | Write, Read | – | – | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| FstCmpEn | 7 | FAST Comparator Enable<br>The FAST mode comparator is enabled by the logical AND of the FAST pin and FstCmpEn.<br>0 = FAST pin does not control FAST mode<br>1= FAST pin can set the device into FAST mode |
| PasThrMode | 6 | Pass Through Mode<br>Bypasses the regulator to connect $V_{OUT}$ to $V_{IN}$. This can only be enabled when BBstEn = 0 (register 0x01).<br>0 = Pass Through Mode disabled<br>1 = Pass Through Mode enabled. Enable only when BBstEn = 0. |
| SwoFrcIN | 5 | Force Switch-Over<br>Controls how the device powers the internal circuitry.<br>0 = Switch-over supply forced to $V_{OUT}$ when $V_{OUT} > V_{OUT\_UVLO\_R}$.<br>1 = Switch-over supply forced to $V_{IN}$. |
| BBstIntegEn | 2 | Buck-Boost Integrator Enable<br>The Integrator can be disabled to improve settling time on load transients at the cost of load regulation error. Latched internally, it can only be changed when BBstEn = 0.<br>0 = Integrator disabled<br>1 = Integrator enabled |
| BBstIPAdptDis | 1 | Adaptive Peak/Valley Current Adjustment Disable<br>0 = Enabled<br>1 = Disabled, peak current fixed to the values set by BBstIPSet1 and BBstIPSet2. Valley current is fixed to 0mA. |
| BBstFETScale | 0 | FET Scale<br>Reduces FET sizes by a factor of 2. This setting can be used to optimize efficiency for lighter loads if it is acceptable to support lower maximum output power. If BBst-FETScale = 0, the part supports 3.5W and requires a 1µH inductor and at least twice the derated capacitance in Figure 9. If BBstFETScale = 1, the part supports 1.75W requires a 2.2µH inductor and at least the derated capacitance in Figure 9. Latched internally, it can only be changed when BBstEn = 0.<br>0 = FET scaling disabled<br>1 = FET scaling enabled |

## Status (0x05)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | – | – | – | – | – | – | OutGood | InUVLO |
| Access Type | – | – | – | – | – | – | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| OutGood | 1 | Status of Output Voltage<br>0 = Output has not reached full power capability<br>1 = Output voltage is high enough to support full power capability |
| InUVLO | 0 | Status register showing whether input voltage is low enough to enable parallel input NMOS.<br>0 = $V_{IN}$ high enough for full power operation<br>1 = Power may be limited due to low $V_{IN}$ |

## Int (0x06)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | – | – | – | – | – | – | OutGoodInt | InUVLOInt |
| Access Type | – | – | – | – | – | – | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| OutGoodInt | 1 | Change in OutGood caused an interrupt |
| InUVLOInt | 0 | Change in InUVLO caused an interrupt |

## Mask (0x07)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | – | – | – | – | – | – | OutGood-IntM | InUVLOIntM |
| Access Type | – | – | – | – | – | – | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| OutGoodIntM | 1 | OutGoodIntM masks the OutGoodInt interrupt.<br>0 = Not masked<br>1 = Masked |
| InUVLOIntM | 0 | InUVLOIntM masks the InUVLOInt interrupt.<br>0 = Not masked<br>1 = Masked |

## LockMsk (0x50)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | – | – | – | – | – | – | – | BBLck |
| Access Type | – | – | – | – | – | – | – | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| BBLck | 0 | Lock Mask for Buck-Boost Registers<br>0 = Buck-Boost Registers not masked from locking/unlocking<br>1 = Buck-Boost Registers masked from locking/unlocking |

## LockUnlock (0x51)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | PASSWD[7:0] | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| PASSWD | 7:0 | Lock/Unlock Password<br>Write 0xAA with BBLck unmasked to lock the BBstVSet[5:0] field<br>Write 0x55 with BBLck unmasked to unlock the BBstVSet[5:0] field |

## Applications Information

### Input and Output Capacitance

The MAX20343 is designed to be compatible with small case-size ceramic capacitors. As such, the device has low-input and low-output capacitance requirements to accommodate the steep voltage derating of 0603 and 0402 (imperial) capacitors. The sample derating curve in Figure 9 presents the minimum capacitance required at IN and OUT. To ensure stability and low noise, the capacitance on IN should be the minimum of 5µF and the value of Figure 9 at the lowest expected $V_{IN}$. The capacitance on OUT should be equal to the value of Figure 9 at the lowest expected $V_{OUT}$ for BBstFETScale = 1 and twice that value for BBstFETScale = 0.

### I²C Interface

The MAX20343 contains an I²C-compatible interface for data communication with a host controller (SCL and SDA). The interface requires a minimum 140kHz clock frequency and supports a frequencies of up to 400kHz. SCL and SDA require pullup resistors that are connected to a positive supply.

### Slave Address

The MAX20343 slave address is 0b0101000 (0x28) plus the Read/$\overline{Write}$ bit. Set the Read/$\overline{Write}$ bit high to configure the MAX20343 to read mode (0x51). Set the Read/$\overline{Write}$ bit low to configure the MAX20343 to write mode (0x50). The address is the first byte of information sent to the MAX20343 after the START condition.
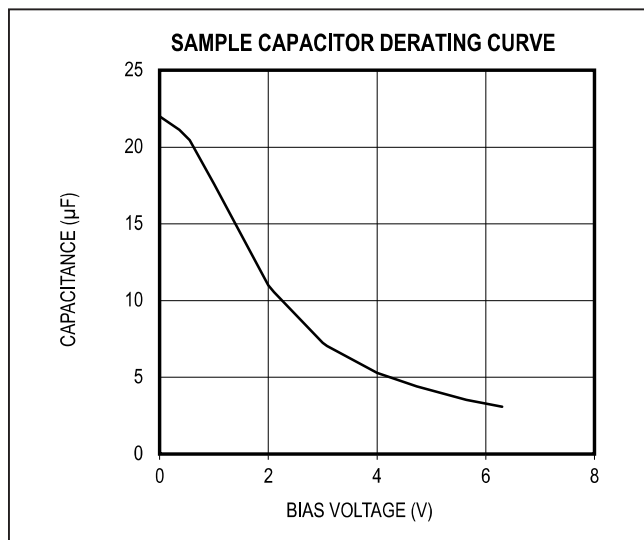
### Start, Stop, and Repeated Start Conditions

When writing to the MAX20343 using I²C, the master sends a START condition (S) followed by the MAX20343 I²C write address. After the address, the master sends the register address of the register that is to be programmed. The master then ends communication by issuing a STOP condition (P) to relinquish control of the bus, or a REPEATED START condition (Sr) to communicate to another I²C slave. See Figure 10.

### Bit Transfer

One data bit is transferred on the rising edge of each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the *Start, Stop, and Repeated Start Conditions* section). Both SDA and SCL remain high when the bus is not active.

### Single-Byte Write

In this operation, the master sends an address and two data bytes to the slave device (Figure 11). The following procedure describes the single byte write operation:

- The master sends a START condition.
- The master sends the 7-bit slave address plus a write bit (low).
- The addressed slave asserts an ACK on the data line.
- The master sends the 8-bit register address.
- The slave asserts an ACK on the data line only if the address is valid (NACK if not).
- The master sends 8 data bits.
- The slave asserts an ACK on the data line.
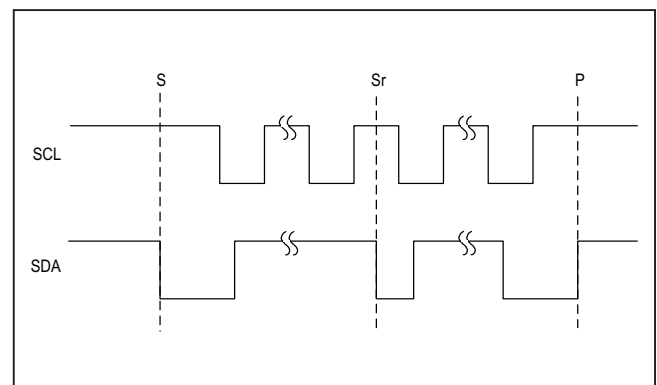- The master generates a STOP condition.



Figure 9. Capacitor Derating for Input and Output Capacitance



Figure 10. I²C START, STOP, and REPEATED START Conditions

**Burst Write**

In this operation, the master sends an address and multiple data bytes to the slave device (Figure 12). The slave device automatically increments the register address after each data byte is sent, unless the register being accessed is 0x00, in which case the register address remains the same. The following procedure describes the burst write operation:

● The master sends a START condition.

● The master sends the 7-bit slave address plus a write bit (low).

● The addressed slave asserts an ACK on the data line.

● The master sends the 8-bit register address.

● The slave asserts an ACK on the data line only if the address is valid (NACK if not).

● The master sends 8 data bits.

● The slave asserts an ACK on the data line.

● Repeat 6 and 7 N-1 times.

● The master generates a STOP condition.
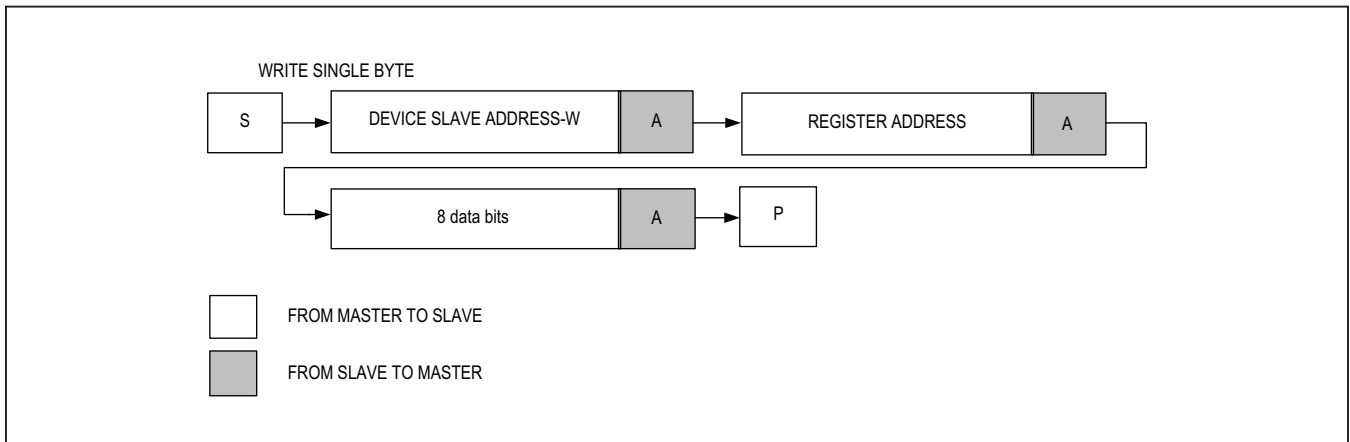
Figure 11. Write Byte Sequence
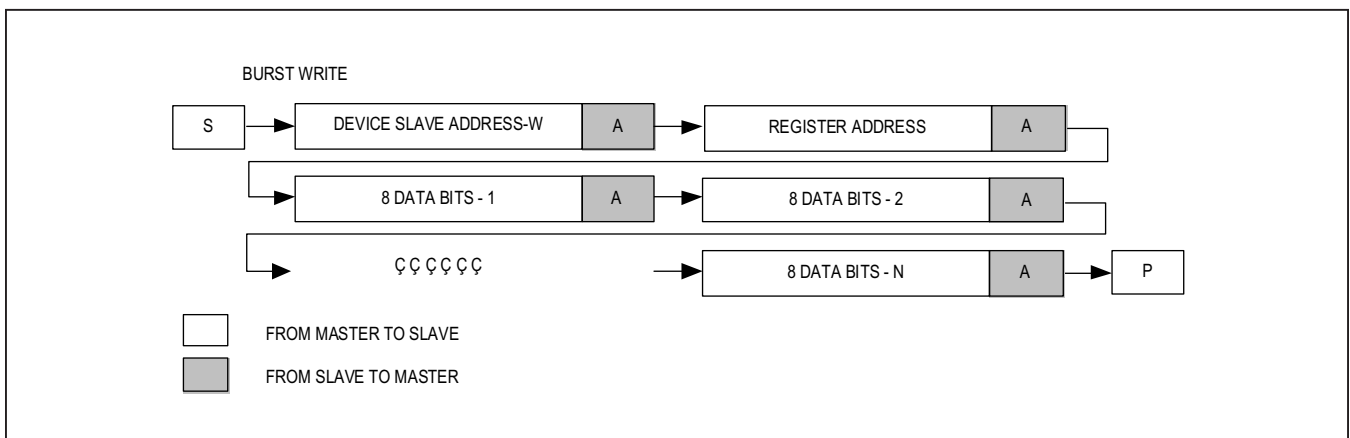
Figure 12. Burst Write Sequence

## Single Byte Read

In this operation, the master sends an address plus two data bytes and receives one data byte from the slave device (Figure 13). The following procedure describes the single byte read operation:

● The master sends a START condition.

● The master sends the 7-bit slave address plus a write bit (low).

● The addressed slave asserts an ACK on the data line.

● The master sends the 8-bit register address.

● The slave asserts an ACK on the data line only if the address is valid (NACK if not).

● The master sends a REPEATED START condition.

● The master sends the 7-bit slave address plus a read bit (high).

● The addressed slave asserts an ACK on the data line.

● The slave sends 8 data bits.

● The master asserts a NACK on the data line.

● The master generates a STOP condition.

## Burst Read

In this operation, the master sends an address plus two data bytes and receives multiple data bytes from the slave device (Figure 14). The following procedure describes the burst byte read operation:

● The master sends a START condition.

● The master sends the 7-bit slave address plus a write bit (low).

● The addressed slave asserts an ACK on the data line.

● The master sends the 8-bit register address.

● The slave asserts an ACK on the data line only if the address is valid (NACK if not).

● The master sends a REPEATED START condition.

● The master sends the 7-bit slave address plus a read bit (high).

● The slave asserts an ACK on the data line.

● The slave sends 8 data bits.

● The master asserts an ACK on the data line.

● Repeat 9 and 10 N-2 times.

● The slave sends the last 8 data bits.

● The master asserts a NACK on the data line.
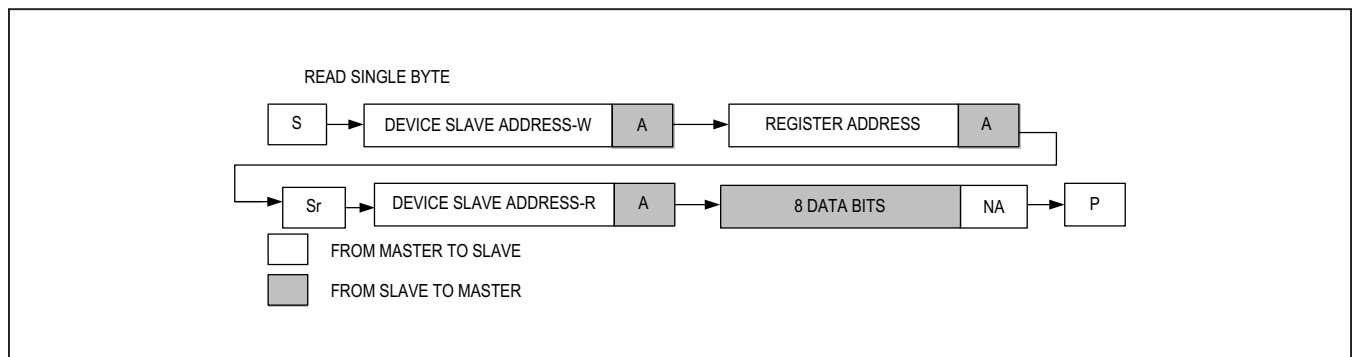
● The master generates a STOP condition.



Figure 13. Read Byte Sequence

## Acknowledge Bits

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX20343 generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and hold it low during the high period of the ninth clock pulse (Figure 15). To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits allows for detection of unsuccessful data transfers.
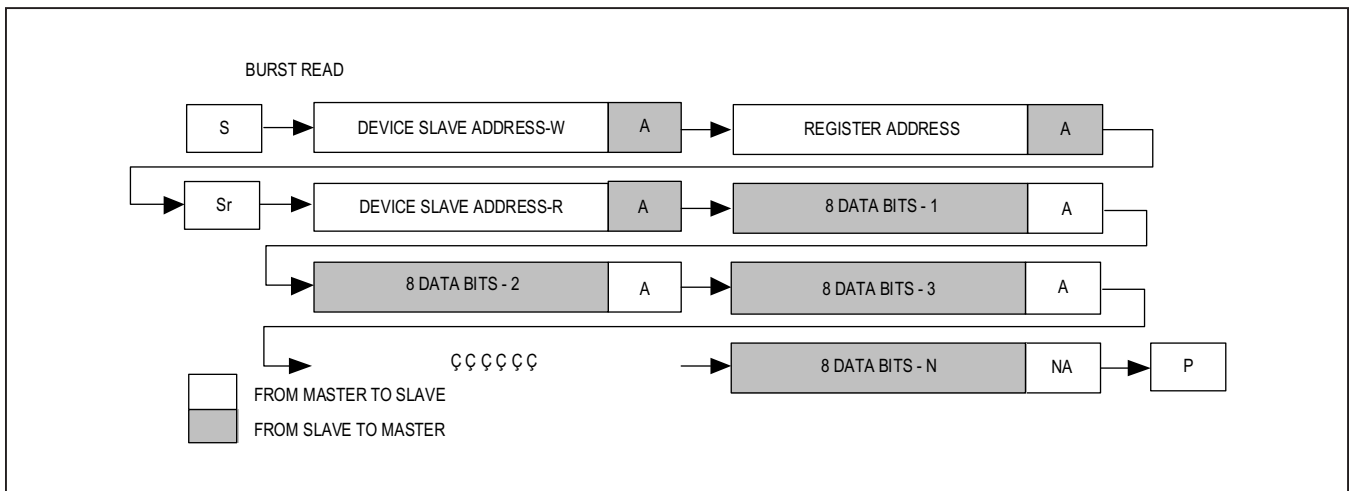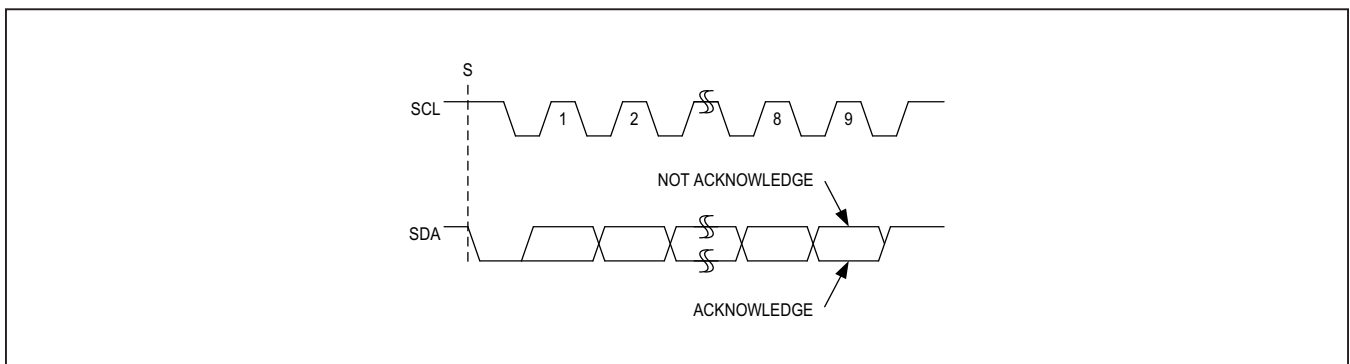


Figure 14. Burst Read Sequence



Figure 15. Acknowledge Bits

## Table 2. Register Bit Default Values

| REGISTER BITS | DEVICE | |
| --- | --- | --- |
| | MAX20343B | MAX20343E |
| BBstEn | Disabled | Disabled |
| BBstRampEn | Single Step | Single Step |
| BBstFast | Low $I_Q$ Mode | Low $I_Q$ Mode |
| BBstZCCmpDis | ZCC Disabled | ZCC Disabled |
| BBstLowEMI | High Efficiency | High Efficiency |
| BBstMode | Buck-Boost | Buck-Boost |
| BBstActDsc | Active Discharge on Shutdown (50ms) | Active Discharge on Shutdown (50ms) |
| BBstPsvDsc | Passive Discharge in Shutdown | Passive Discharge in Shutdown |
| BBstFHighSh[1:0] | 100kHz/25kHz | 100kHz/25kHz |
| SwoFrcIN | Switch-Over Forced to $V_{OUT}$ when OutGood = 1 | Switch-Over Forced to $V_{IN}$ |
| BBstLowVinEn | Shutdown when SwoFrcIN = 0 and $V_{OUT}$ < $V_{OUT\_}$ UVLO_F | Shutdown when SwoFrcIN = 0 and $V_{IN}$ < $V_{IN\_}$ UVLO_F |
| BBstVSet[5:0] | 3.20V | 5.00V |
| BBstIntegEn | Disable Integrator | Disable Integrator |
| BBstIPAdptDis | Adaptive Peak Current Enabled | Adaptive Peak Current Enabled |
| BBstFETScale | FET Scaling Enabled | FET Scaling Enabled |
| FastRSELMode | FAST | FAST |
| EnI2CMode | I$^2$C Control | I$^2$C Control |
| BBstIPSet1[3:0] | 100mA | 225mA |
| BBstIPSet2[3:0] | BBstIPSet1 + 200mA | BBstIPSet1 + 150mA |
| BBstIP1SS[3:0] | 375mA | 375mA |
| BBstIP2SS[3:0] | BBstIPSet1 + 75mA | BBstIPSet1 + 75mA |

## Table 3. Register Default Values

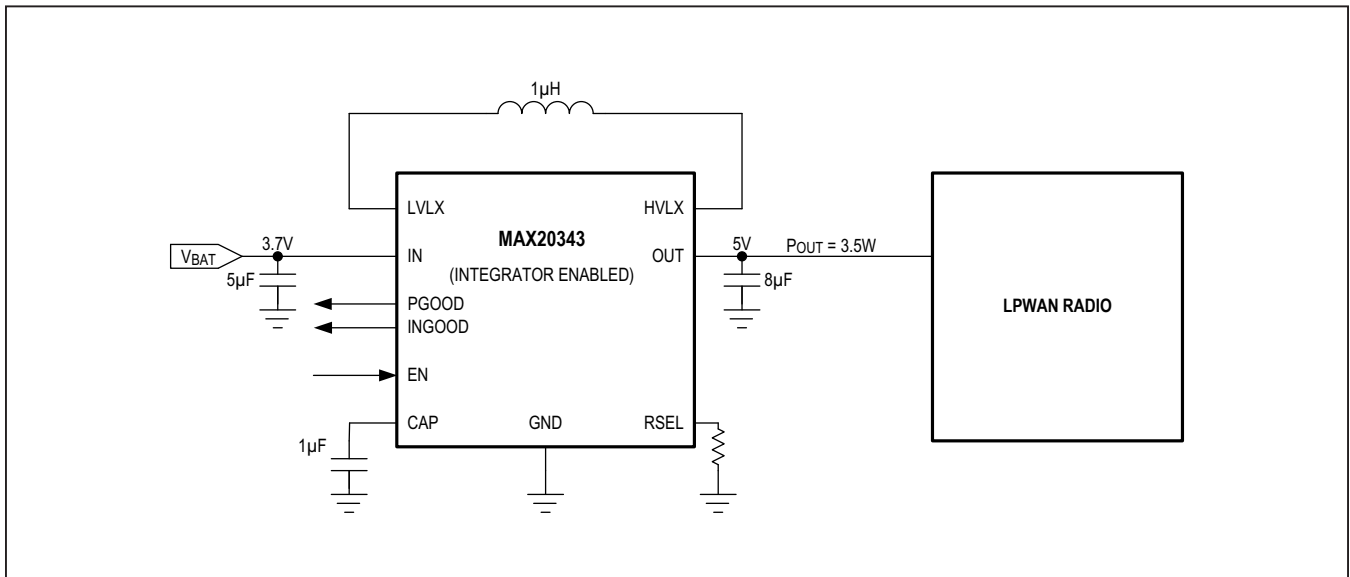| REGISTER | NAME | DEVICE | |
| --- | --- | --- | --- |
| | | MAX20343B | MAX20343E |
| 0x00 | ChipID | 0x01 | 0x01 |
| 0x01 | BBstCfg0 | 0x13 | 0x13 |
| 0x02 | BBstVSet | 0xCE | 0xF2 |
| 0x03 | BBstISet | 0x84 | 0x69 |
| 0x04 | BBstCfg1 | 0x01 | 0xA1 |
| 0x05 | Status | 0x00 | 0x00 |
| 0x06 | Int | 0x00 | 0x00 |
| 0x07 | Mask | 0x03 | 0x03 |
| 0x50 | LockMsk | 0x01 | 0x01 |
| 0x51 | LockUnlock | 0xFF | 0xFF |

## Typical Application Circuits

### Optical Heart Rate LED Supply
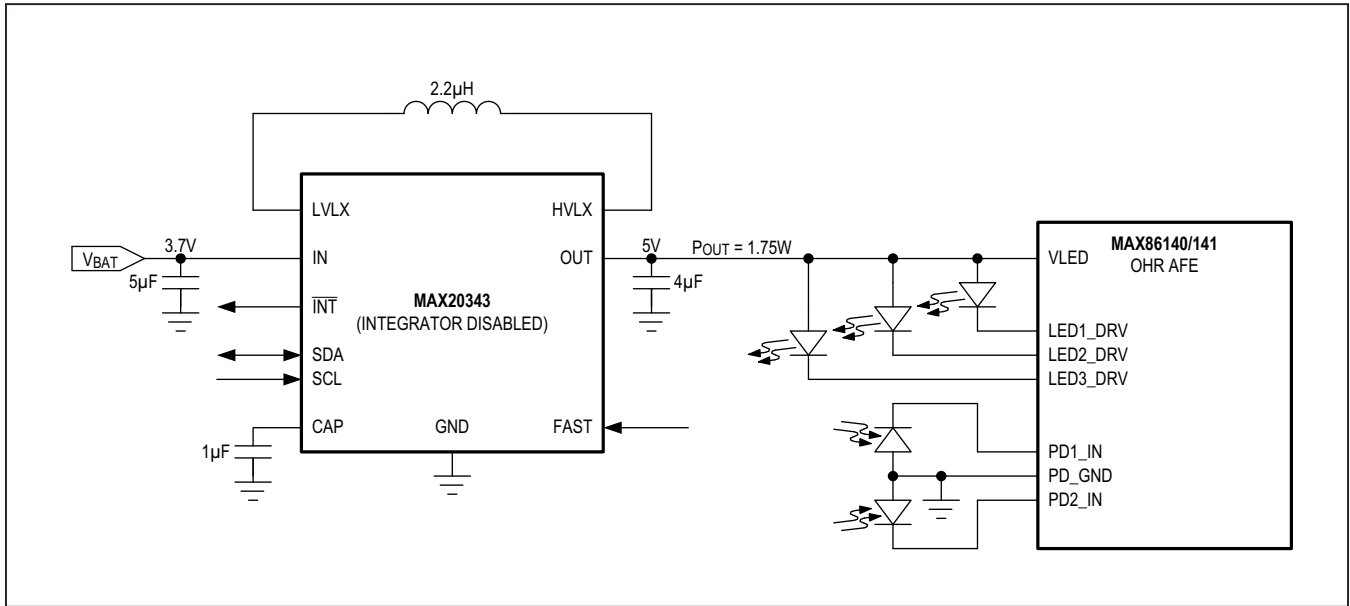


### LPWAN Radio Supply

## Ordering Information

| PART NUMBER | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX20343BEFC+* | -40°C to +85°C | 12 FC2QFN |
| MAX20343BEFC+T* | -40°C to +85°C | 12 FC2QFN |
| MAX20343BEWE+ | -40°C to +85°C | 16 WLP |
| MAX20343BEWE+T | -40°C to +85°C | 16 WLP |
| MAX20343EEWE+ | -40°C to +85°C | 16 WLP |
| MAX20343EEWE+T | -40°C to +85°C | 16 WLP |

+ Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape-and-reel.
*Future product—contact factory for availability.

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 3/19 | Initial release | — |
| 1 | 3/19 | Corrected typos; updated BBstFETScale Bit Description (and corrected typo), and added future product designation to MAX20343EEWE+ and MAX20343EEWE+T | 19, 21, 25, 34 |
| 2 | 4/19 | Updated the *General Description, Benefits and Features, Absolute Maximum Ratings, Package Information, Pin Configuration, Pin Description, Buck-Boost Mode* and *Inductor Peak and Valley Current Limits* sections, and Register Map and BBstCfg0 (0x01) tables; added MAX20343BEFC+ and MAX20343BEFC+T as future parts to the *Ordering Information* table | 1, 3, 12–13 16, 18, 20–21, 34 |
| 3 | 6/19 | Removed future part designation from MAX20343EEWE+ and MAX20343EEWE+T in the *Ordering Information* table | 34 |