

# **Product Change Notification - SYST-24CPOY499**

Date:

25 Jul 2019

**Product Category:** 

**Current And Power Measurement ICs** 

**Affected CPNs:** 

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**Notification subject:** 

ERRATA - PAC1932/3/4 Family Silicon Errata and Data Sheet Clarification

**Notification text:** 

**Notification Status:** Final

# **Description of Change:**

1.) of this document

2) Issued for silicon revision B1

Impacts to Data Sheet: None

**Reason for Change:** To Improve Productivity

**Change Implementation Status:** Complete

Estimated First Ship Date: 25 Jul 2019

NOTE: Please be advised that after the estimated first ship date customers may receive pre and post change parts.

Markings to Distinguish Revised from Unrevised Devices: Traceability Code

# Attachment(s):

PAC1932/3/4 Family Silicon Errata and Data Sheet Clarification

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# SYST-24CPOY499 - ERRATA - PAC1932/3/4 Family Silicon Errata and Data Sheet Clarification

Affected Catalog Part Numbers (CPN)

PAC1932T-I/J6CX

PAC1932T-I/JQ

PAC1933T-I/J6CX

PAC1933T-I/JQ

PAC1934T-I/J6CX

PAC1934T-I/JQ

Date: Wednesday, July 24, 2019



# PAC1932/3/4

# PAC1932/3/4 Family Silicon Errata and Data Sheet Clarification

The PAC1932/3/4 family devices that you have received conform functionally to the current Device Data Sheet (DS20005850**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

Any future revision of the PAC1932/3/4 silicon will address this issue.

Data Sheet clarifications and corrections start on page 2, following the discussion of silicon issues.

To identify the silicon revision, read the Revision ID Register (Address 0xFF) and refer to Table 1.

TABLE 1: SILICON REVISION VALUES

Part Number	Device ID	Revision ID	Silicon Revision
PAC1934	0x5B	0x03	B1
PAC1933	0x5A	0x03	B1
PAC1932	0x59	0x03	B1

**Note 1:** The Device ID and Revision ID are located near the end of the register map at locations 0xFD and 0xFF respectively, as specified in the data sheet DS20005850D.

# TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Jaqua Summany	Affected Revisions		
Wodule	reature	item Number	Issue Summary	B1		
REFRESH	REFRESH	1	In certain cases, the internal clock remains enabled during the SLEEP state which increases power consumption	Х		

Table 3 shows typical power supply currents for a PAC1934 at different sampling rates, with and without a Workaround being used. Both Workarounds deliver the same power supply current result.

## TABLE 3: POWER SUPPLY CURRENT WITH AND WITHOUT WORKAROUND

Supply current vs sample rate (sps)	8 sps	64 sps	256 sps	1024 sps
No Workaround	308 μΑ	329 µA	410 µA	604 µA
With Workaround	12 µA	75 μA	278 μΑ	578 μA

#### Silicon Errata Issues

## 1. Module: REFRESH

When a REFRESH command (SEND Byte) is followed directly by another REFRESH command (SEND Byte), the internal clock is not properly disabled during SLEEP modes. This causes an increase in supply current for sampling rates below 1kSps but does not otherwise affect performance.

There are two possible workarounds, one or the other may be preferred for certain applications. For a given application, use the same workaround throughout the application, do not mix and match Workaround 1 and Workaround 2 in the same application.

The workarounds have been implemented in the drivers and software tools associated with the PAC193X devices. Read the release notes associated with the software for more details.

#### Work around 1

One workaround for the anomaly is to WRITE to any R/W register before and after each REFRESH command. This causes the clock to stop between sampling cycles as it should. This workaround produces no side effects except for the burden of the extra WRITE commands.

#### Work around 2

A second workaround is to change the SEND byte for REFRESH to a WRITE byte, with a dummy data payload (normally the SEND byte for REFRESH does not have data, only the address for the REFRESH command). This is a simpler workaround but has the side effect that the device generates a NACK instead of an ACK since it is not expecting a payload. For Linux applications, these NACKs show up as entries in the kernel log which is probably undesirable.

# Affected Silicon Revisions

B1				
Χ				

## **Data Sheet Clarifications**

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS20005850**D**):

None.

# APPENDIX A: DOCUMENT REVISION HISTORY

# Rev A Document (5/2019) Silicon revision B1

Initial release of this document; issued for silicon revision B1.

PA	C <sub>1</sub>	9	32	13	14
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NOTES:

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