Product Change Notification - SYST-07FJOF556

Date:

08 Aug 2019

Product Category:

32-bit Microcontrollers

Affected CPNs:

Notification subject:

ERRATA - SAM D09 Series Family Silicon Errata and Data Sheet Clarifications

Notification text:

SYST-07FJOF556

Microchip has released a new DeviceDoc for the SAM D09 Series Family Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at SAM D09 Series Family Silicon Errata and Data Sheet Clarifications .

Notification Status: Final

Description of Change:

1) This is the initial released version of this document.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 08 Aug 2019

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

SAM D09 Series Family Silicon Errata and Data Sheet Clarifications

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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If you wish to change your PCN profile, including opt out, please go to the PCN home page select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Affected Catalog Part Numbers (CPN)

ATSAMD09C13A-SSUT
ATSAMD09D14A-MUT

SAM D09 Series Family
Silicon Errata and Data Sheet Clarification

The SAM D09 Series family of devices that you have received conform functionally to the current Device Data Sheet (Atmel-42414G-SAM-D09-Datasheet_09/2016), except for the anomalies described in this document.

New Silicon Errata Issues

Note:	This document provides information on new errata issues for the SAM D09 Series of devices. Please refer to the current device data sheet for all pre-existing silicon errata issues.

1. Module: BOD12

On External Reset, the BOD12 reset cause can also be triggered.

Work around

Ignore BOD12 reset cause if External reset cause is set.

Affected Silicon Revisions

A	B						
X							

Data Sheet Clarifications

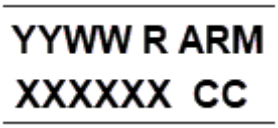
The following typographic corrections and clarifications are to be noted for the latest version of the Device Data Sheet (Atmel-42414G-SAM-D09-Datasheet_09/2016).

Note: Corrections in tables and paragraphs are shown in **bold.** Where possible, the original bold text formatting has been removed for clarity.

1. Module: Package Marking Information

In the current device data sheet, the SAM D09 Package Marking Information is missing. The information is as follows:

All devices are marked with the Atmel logo, a shortened ordering code and additional marking (the two last lines).



Where:

- "Y" or "YY": Manufacturing Year (last OR two last digit(s))
- "WW": Manufacturing Week
- "R": Revision
- "XXXXXX": Lot number
- "CC": Internal Code

2. Module: XOSC32 EN1K bit

The EN1K bit is referenced several times in the device data sheet. The EN1K bit is not implemented for this device.

3. Module: OSCULP32K Characteristics

The value for the minimum output frequency is incorrect. The corrected information is shown in bold below.

TABLE 30-39: ULTRA-LOW POWER INTERNAL 32 kHz RC OSCILLATOR CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{OUT}	Output frequency	Calibrated against a 32.768 kHz reference at 25°C, over [-40, +85]C, over [1.62, 3.63]V	27.8	32.768	37.8	kHz
		Calibrated against a 32.768 kHz reference at 25°C, at V_{DD}=3.3V	**32.5**	32.768	32.8	
		Calibrated against a 32.768 kHz reference at 25°C, over [1.62, 3.63]V	31.9	32.768	33.1	
Duty	Duty Cycle			50		%

4. Module: Brown-out Detectors (BOD) Characteristics

Figure 30-3 and Figure 30-4 have an incorrect reset Polarity value. The corrected figures are as shown below:

FIGURE 30-3: BOD33 HYSTERESIS OFF

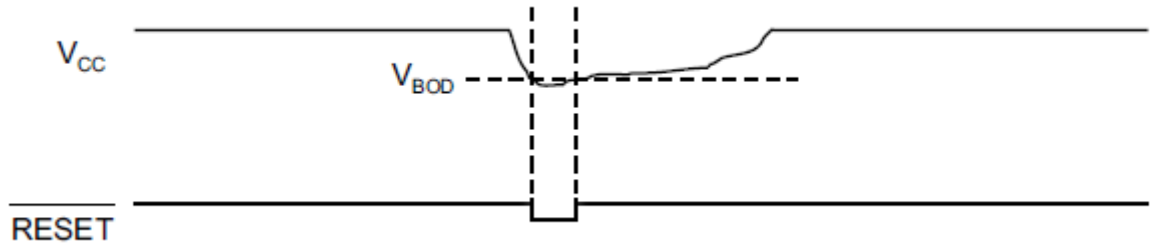
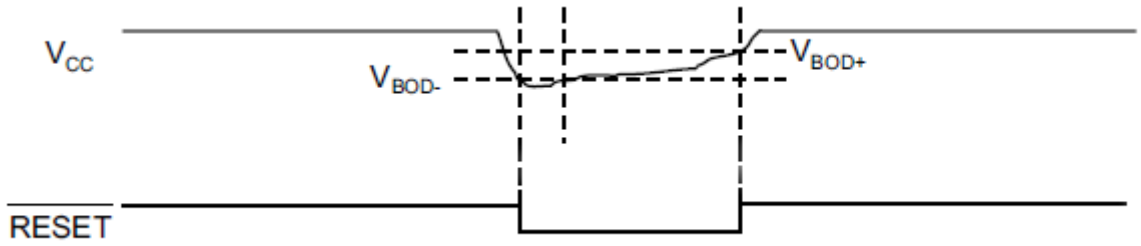


FIGURE 30-4: BOD33 LEVEL VALUE



5. Module: ADC Power Management

A new information has been added to the Section 29.5.2, and is shown in bold.

The ADC will continue to operate in any sleep modes where the selected source clock is running. The ADC's interrupts can be used to wake up the device from sleep modes (**Except the OVERRUN interrupt)**. The events can trigger other operations in the system without exiting the sleep modes. Refer to "PM – Power Manager" on page 107 for details on the different sleep modes.

6. Module: EVSYS Register Summary

The USER register is displayed incorrectly in the Register Summary. The correct USER register summary section is displayed as follows:

0x0120	USER0	7:0					CHANNEL[3:0]				
...											
0x0136	USER22	7:0					CHANNEL [3:0]				

7. Module: EVSYS Principle of Operation

Section 23.6.1 has some incorrect information in the second part, the corrected information is shown in bold.

The EVSYS allows for communication between peripherals via events. Peripherals that respond to events (event users) are connected to multiplexers which have all event channels as input. **Each peripheral emitting events (Event Generator) can be connected to one or multiple event users, using one or multiple channels of the Event System.**

8. Module: NVMCTRL - CTRLA Register

Table 21-6 for the Command bit displays Write Lockbits as a feature. Write lockbits are not supported on this device.

9. Module: NVMCTRL - NVM User Configuration

Table 21-2 and Table 21-3 show incorrect values on the last two rows of each table. These values are not possible per the device memory density.

10. Module: RTC - Overview

The overview section for the RTC has had a new verbiage, which has been highlighted in bold.

The Real-Time Counter (RTC) is a 32-bit counter with a 10-bit programmable prescaler that typically runs continuously to keep track of time. The RTC can wake up the device from sleep modes using the alarm/compare wake up, periodic wake up or overflow wake up mechanisms.

The RTC is clocked by any clock sources selectable through the Generic Clock module (GCLK), providing the signal GCLK_RTC.

The RTC can generate periodic peripheral events from outputs of the prescaler, as well as alarm/compare interrupts and peripheral events, which can trigger at any counter value. Additionally, the timer can trigger an overflow interrupt and peripheral event, and be reset on the occurrence of an alarm/compare match. This allows periodic interrupts and peripheral events at very long and accurate intervals.

The 10-bit programmable prescaler can scale down the clock source, and so a wide range of resolutions and time-out periods can be configured. With a 32.768 kHz clock source, the minimum counter tick interval is 30.5 µs, and time-out periods can range up to 36 hours. With the counter tick interval configured to 1s, the maximum time-out period is more than 136 years.

11. Module: 32 kHz Internal Oscillator (OSC32K) Operation

The data sheet erroneously lists a 1.024 kHz output and the EN1K bit in section 16.6.4. These are not available for this device.

12. Module: 32 kHz External Crystal Oscillator (XOSC32K) Operation

The data sheet erroneously lists a 1.024 kHz output and the EN1K bit in the Section 16.6.3. These are not available for this device.

13. Module: SYSCTRL - XOSC Register

The register description for the GAIN bit has been updated, and the newly added text is shown in bold.

These bits select the gain for the oscillator. The listed maximum frequencies are recommendations, and might vary based on capacitive load and crystal characteristics. **Those bits must be properly configured even when the Automatic Amplitude Gain Control is active.**

14. Module: SYSCTRL - XOSC Register

The AMPGC bit has been updated with a new note, as shown in bold.

Note: The configuration of the oscillator gain is mandatory even if AMPGC feature is enabled at startup.

15. Module: 32kHz Ultra-Low Power Internal Oscillator (OSCULP32K) Operation

The data sheet erroneously lists a 1.024 kHz output in Section 16.6.5. The corrected text is shown in bold.

The OSCULP32K provides a tunable, low-speed and ultra-low power clock source. The OSCULP32K is factory calibrated under typical voltage and temperature conditions. The OSCULP32K should be preferred to the OSC32K whenever the power requirements are prevalent over frequency stability and accuracy.

The OSCULP32K can be used as a source for the generic clock generators, as described in the “GCLK – Generic Clock Controller” on page 85.

The OSCULP32K is enabled by default after a Power-on Reset (POR) and will always run except during POR. **The OSCULP32K has a 32.768 kHz output that is always running.**

16. Module: 32 kHz Internal Oscillator (OSC32K) Operation

The data sheet erroneously lists a 1.024 kHz output and the EN1K bit in section 16.6.4. These are not available for this device.

17. Module: 32 kHz External Crystal Oscillator (XOSC32K) Operation

The data sheet erroneously lists a 1.024 kHz output and the EN1K bit in section 16.6.3. These are not available for this device.

18. Module: Debug Operation - DCFGn Register

The register is erroneously listed as Read-Write. This register is Read Only.

APPENDIX A: REVISION HISTORY

Revision A Document (07/2019)

This is the initial released version of this document.

Note the following details of the code protection feature on Microchip devices:

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