

# LMH2180

## 75 MHz Dual Clock Buffer

### General Description

The LMH2180 is a high speed dual clock buffer designed for portable communications and applications requiring multiple accurate multi-clock systems. The LMH2180 integrates two 75 MHz low noise buffers with independent shutdown pins into a small package. The LMH2180 ensures superb system operation between the baseband and the oscillator signal path by eliminating crosstalk between the multiple clock signals.

Unique technology and design provides the LMH2180 with the ability to accurately drive both large capacitive and resistive loads. Low supply current combined with shutdown pins for each channel means the LMH2180 is ideal for battery powered applications. The LMH2180's rapid recovery after disable optimizes performance and current consumption. This part does not use an internal ground reference, thus providing additional system flexibility. The LMH2180 operates both with single and split supplies.

The flexible buffers provide system designers the capacity to manage complex clock signals in the latest wireless applications. Each buffer delivers 106 V/ $\mu$ s internal slew rate with independent shutdown and duty cycle precision. The patented analog circuit of each buffer drives capacitive loads greater than 20 pF. Each input is internally biased to 1V, removing the need for external resistors. Both channels have rail-to-rail inputs and outputs, a gain of one, and are AC coupled with the use of one capacitor.

Replacing a discrete buffer solution with the LMH2180 provides many benefits: simplified board layout, minimized parasitic components, simplified BOM, design durability across multiple applications, simplification of clock paths, and the ability to reduce the number of clock signal generators in the system. The LMH2180 is produced in the tiny 8-pin LLP solder bump and no pullback packages minimizing the required PCB space. National's advanced packaging offers direct PCB-IC evaluation via pin access.

### Features

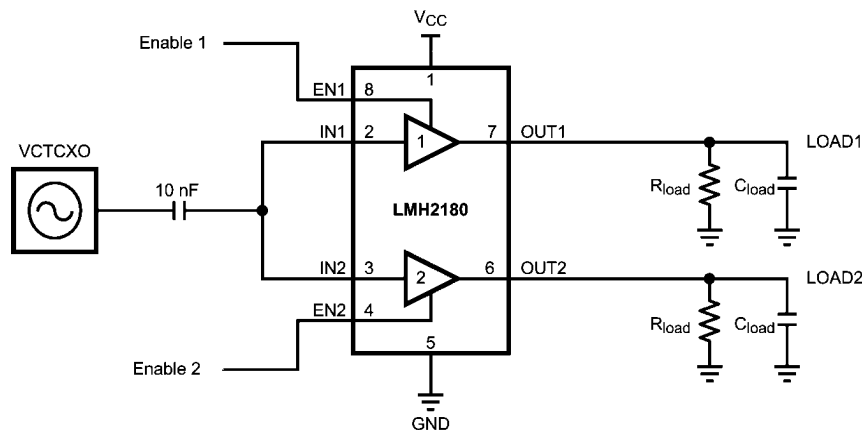
(Typical values are:  $V_{SUPPLY} = 2.7V$  and  $C_L = 10$  pF, unless otherwise specified.)

|  |                |
|--|----------------|
| ■ Small signal bandwidth   | 78 MHz         |
| ■ Supply voltage range   | 2.4V to 5V     |
| ■ Phase noise ( $V_{IN} = 1 V_{PP}$ ,<br>$f_C = 38.4$ MHz, $\Delta f = 1$ kHz) | -123dBc/Hz     |
| ■ Slew rate  | 106 V/ $\mu$ s |
| ■ Total supply current   | 2.3 mA         |
| ■ Shutdown current   | 30 $\mu$ A     |
| ■ Rail-to-rail input and output  |                |
| ■ Individual buffer enable pins  |                |
| ■ Rapid $T_{on}$ technology  |                |
| ■ Crosstalk rejection circuitry  |                |
| ■ 8-pin LLP, pin access packaging  |                |
| ■ Temperature range  | -40°C to 85°C  |

### Applications

- 3G mobile applications
- WLAN-WiMAX modules
- TD\_SCDMA multi-mode MP3 and camera
- GSM modules
- Oscillator modules

### Typical Application



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**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

|                           |                 |
|---------------------------|-----------------|
| Supply Voltages (V+– V–)  | 5.5V            |
| ESD Tolerance             |                 |
| Human Body (Note 4)       | 2000V           |
| Machine Model (Note 5)    | 200V            |
| Charged Device Model      | 1000V           |
| Storage Temperature Range | –65°C to +150°C |

|                                  |        |
|----------------------------------|--------|
| Junction Temperature (Note 3)    | +150°C |
| Soldering Information            |        |
| Infrared or Convection (35 sec.) | 235°C  |

**Operating Ratings** (Note 1)

|   |                |
|---|----------------|
| Supply Voltage (V+ – V–)                | 2.4V to 5.0V   |
| Temperature Range (Notes 2, 3)          | –40°C to +85°C |
| Package Thermal Resistance (Notes 2, 3) |                |
| LLP-8 ( $\theta_{JA}$ )                 | 217°C/W        |

**2.7V Electrical Characteristics**

Unless otherwise specified, all limits are guaranteed for  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 2.7\text{V}$ ,  $V_{SS} = 0\text{V}$ ,  $V_{CM} = 1\text{V}$ ,  $\text{Enable}_{1,2} = V_{DD}$ ,  $C_L = 10\text{pF}$ ,  $R_L = 30\text{k}\Omega$ , Load is connected to  $V_{SS}$ ,  $C_{COUPLING} = 10\text{nF}$ . **Boldface** limits apply at temperature range extremes of operating condition. See (Note 2)

| Symbol                                  | Parameter  | Conditions   | Min<br>(Note 7) | Typ<br>(Note 6) | Max<br>(Note 7)   | Units                        |
|---|--|--|-----------------|-----------------|-------------------|------------------------------|
| <b>Frequency Domain Response</b>        |  |  |                 |                 |                   |                              |
| SSBW                                    | Small Signal Bandwidth                                 | $V_{IN} = 100\text{mV}_{PP}$ ; –3 dB   |                 | 78              |                   | MHz                          |
| LSBW                                    | Large Signal Bandwidth                                 | $V_{IN} = 1.0\text{V}_{PP}$ ; –3 dB  |                 | 60              |                   | MHz                          |
| GfN                                     | Gain Flatness < 0.1 dB                                 | $f > 100\text{kHz}$  |                 | 4.9             |                   | MHz                          |
| <b>Distortion and Noise Performance</b> |  |  |                 |                 |                   |                              |
| $\phi_n$                                | Phase Noise  | $V_{IN} = 1\text{V}_{PP}$ , $f_C = 38.4\text{MHz}$ , $\Delta f = 1\text{kHz}$  |                 | –123            |                   | dBc/Hz                       |
|   |  | $V_{IN} = 1\text{V}_{PP}$ , $f_C = 38.4\text{MHz}$ , $\Delta f = 10\text{kHz}$ |                 | –132            |                   | dBc/Hz                       |
| $e_n$                                   | Input-Referred Voltage Noise                           | $f = 1\text{MHz}$ , $R_{SOURCE} = 50\Omega$                                    |                 | 13              |                   | $\text{nV}/\sqrt{\text{Hz}}$ |
| $I_{SOLUTION}$                          | Output to Input  | $f = 1\text{MHz}$ , $R_{SOURCE} = 50\Omega$                                    |                 | 84              |                   | dB                           |
| CT                                      | Crosstalk Rejection                                    | $f = 38.4\text{MHz}$ , $V_{IN} = 1\text{V}_{PP}$                               |                 | 41              |                   | dB                           |
| <b>Time Domain Response</b>             |  |  |                 |                 |                   |                              |
| $t_r$                                   | Rise Time  | 0.1 $V_{PP}$ Step (10-90%)   |                 | 6               |                   | ns                           |
| $t_f$                                   | Fall Time  |  |                 | 5               |                   | ns                           |
| $t_s$                                   | Settling Time to 0.1%                                  | 1 $V_{PP}$ Step  |                 | 120             |                   | ns                           |
| OS                                      | Overshoot  | 0.1 $V_{PP}$ Step  |                 | 37              |                   | %                            |
| SR                                      | Slew Rate (Note 8)                                     | $V_{IN} = 2\text{V}_{PP}$  |                 | 106             |                   | $\text{V}/\mu\text{s}$       |
| <b>Static DC Performance</b>            |  |  |                 |                 |                   |                              |
| $I_S$                                   | Supply Current   | Enable <sub>1,2</sub> = $V_{DD}$ ; No Load                                     |                 | 2.3             | 2.7<br><b>2.9</b> | mA                           |
|   |  | Enable <sub>1</sub> = $V_{DD}$ , Enable <sub>2</sub> = $V_{SS}$ , No Load      |                 | 1.3             | 1.5<br><b>1.6</b> | mA                           |
|   |  | Enable <sub>1,2</sub> = $V_{SS}$ ; No Load                                     |                 | 30              | 41<br><b>46</b>   | $\mu\text{A}$                |
| PSRR                                    | Power Supply Rejection Ratio                           | DC (3.0V to 5.0V)  | 65<br><b>64</b> | 68              |                   | dB                           |
| $A_{CL}$                                | Small Signal Voltage Gain                              | $V_{IN} = 0.2\text{V}_{PP}$  | <b>0.95</b>     | 1.0             | <b>1.05</b>       | V/V                          |
| $V_{OS}$                                | Output Offset Voltage                                  |  |                 | –0.5            | 17<br><b>18</b>   | mV                           |
| TC $V_{OS}$                             | Temperature Coefficient Output Offset Voltage (Note 9) |  |                 | 2.8             |                   | $\mu\text{V}/^\circ\text{C}$ |
| $R_{OUT}$                               | Output Resistance                                      | $f = 100\text{kHz}$  |                 | 0.6             |                   | $\Omega$                     |
|   |  | $f = 38.4\text{MHz}$   |                 | 166             |                   |                              |

| Symbol                           | Parameter                                      | Conditions                                       | Min<br>(Note 7)     | Typ<br>(Note 6) | Max<br>(Note 7) | Units      |
|----------------------------------|--|--|---------------------|-----------------|-----------------|------------|
| <b>Miscellaneous Performance</b> |  |  |                     |                 |                 |            |
| $R_{IN}$                         | Input Resistance per Buffer                    | Enable = $V_{DD}$                                |                     | 137             |                 | k $\Omega$ |
|                                  |  | Enable = $V_{SS}$                                |                     | 137             |                 |            |
| $C_{IN}$                         | Input Capacitance per Buffer                   | Enable = $V_{DD}$                                |                     | 1.3             |                 | pF         |
|                                  |  | Enable = $V_{SS}$                                |                     | 1.3             |                 |            |
| $Z_{IN}$                         | Input Impedance                                | $f = 38.4$ MHz, Enable = $V_{DD}$                |                     | 4.5             |                 | k $\Omega$ |
|                                  |  | $f = 38.4$ MHz, Enable = $V_{SS}$                |                     | 4.2             |                 |            |
| $V_O$                            | Output Swing Positive                          | $V_{IN} = V_{DD}$                                | 2.66<br><b>2.65</b> | 2.69            |                 | V          |
|                                  | Output Swing Negative                          | $V_{IN} = V_{SS}$                                |                     | 19              | 35<br><b>37</b> | mV         |
| $I_{SC}$                         | Output Short-Circuit Current<br>(Notes 10, 11) | Sourcing, $V_{IN} = V_{DD}$ , $V_{OUT} = V_{SS}$ | -21<br><b>-18</b>   | -25             |                 | mA         |
|                                  |  | Sinking, $V_{IN} = V_{SS}$ , $V_{OUT} = V_{DD}$  | 23<br><b>15</b>     | 25              |                 |            |
| $V_{en\_hmin}$                   | Enable High Active Minimum Voltage             |  |                     | 1.2             |                 | V          |
| $V_{en\_lmax}$                   | Enable Low Inactive Maximum Voltage            |  |                     | 0.6             |                 |            |

## 5V Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ ,  $V_{SS} = 0\text{V}$ ,  $V_{CM} = 1\text{V}$ ,  $\text{Enable}_{1,2} = V_{DD}$ ,  $C_L = 10$  pF,  $R_L = 30$  k $\Omega$ , Load is connected to  $V_{SS}$ ,  $C_{COUPLING} = 10$  nF. **Boldface** limits apply at temperature range extremes of operating condition. See (Note 2)

| Symbol                                  | Parameter                    | Conditions  | Min<br>(Note 7) | Typ<br>(Note 6) | Max<br>(Note 7)   | Units                  |
|---|------------------------------|---|-----------------|-----------------|-------------------|------------------------|
| <b>Frequency Domain Response</b>        |                              |   |                 |                 |                   |                        |
| SSBW                                    | Small Signal Bandwidth       | $V_{IN} = 100$ mV <sub>PP</sub> ; -3 dB                                   |                 | 87              |                   | MHz                    |
| LSBW                                    | Large Signal Bandwidth       | $V_{IN} = 1.0$ V <sub>PP</sub> ; -3 dB                                    |                 | 68              |                   | MHz                    |
| GFN                                     | Gain Flatness < 0.1 dB       | $f > 100$ kHz   |                 | 25              |                   | MHz                    |
| <b>Distortion and Noise Performance</b> |                              |   |                 |                 |                   |                        |
| $\phi_n$                                | Phase Noise                  | $V_{IN} = 1$ V <sub>PP</sub> , $f_C = 38.4$ MHz, $\Delta f = 1$ kHz       |                 | -123            |                   | dBc/Hz                 |
|   |                              | $V_{IN} = 1$ V <sub>PP</sub> , $f_C = 38.4$ MHz, $\Delta f = 10$ kHz      |                 | -132            |                   | dBc/Hz                 |
| $e_n$                                   | Input-Referred Voltage Noise | $f = 1$ MHz, $R_{SOURCE} = 50\Omega$                                      |                 | 12              |                   | nV/ $\sqrt{\text{Hz}}$ |
| $I_{SOLUTION}$                          | Output to Input              | $f = 1$ MHz, $R_{SOURCE} = 50\Omega$                                      |                 | 84              |                   | dB                     |
| CT                                      | Crosstalk Rejection          | $f = 38.4$ MHz, $P_{IN} = 0$ dBm  |                 | 59              |                   | dB                     |
| <b>Time Domain Response</b>             |                              |   |                 |                 |                   |                        |
| $t_r$                                   | Rise Time                    | 0.1 V <sub>PP</sub> Step (10-90%)   |                 | 6               |                   | ns                     |
| $t_f$                                   | Fall Time                    |   |                 | 6               |                   | ns                     |
| $t_s$                                   | Settling Time to 0.1%        | 1 V <sub>PP</sub> Step  |                 | 70              |                   | ns                     |
| OS                                      | Overshoot                    | 0.1V <sub>PP</sub> Step   |                 | 13              |                   | %                      |
| SR                                      | Slew Rate (Note 8)           | $V_{IN} = 2$ V <sub>PP</sub>  |                 | 124             |                   | V/ $\mu\text{s}$       |
| <b>Static DC Performance</b>            |                              |   |                 |                 |                   |                        |
| $I_S$                                   | Supply Current               | Enable <sub>1,2</sub> = $V_{DD}$ ; No Load                                |                 | 3.4             | 4.0<br><b>4.1</b> | mA                     |
|   |                              | Enable <sub>1</sub> = $V_{DD}$ , Enable <sub>2</sub> = $V_{SS}$ ; No Load |                 | 1.8             | 2.2<br><b>2.3</b> |                        |
|   |                              | Enable <sub>1,2</sub> = $V_{SS}$ ; No Load                                |                 | 32              | 43<br><b>49</b>   | $\mu\text{A}$          |

| Symbol                           | Parameter  | Conditions   | Min<br>(Note 7)     | Typ<br>(Note 6) | Max<br>(Note 7) | Units |
|----------------------------------|--|--|---------------------|-----------------|-----------------|-------|
| PSRR                             | Power Supply Rejection Ratio                           | DC (3.0V to 5.0V)  | 65<br><b>64</b>     | 68              |                 | dB    |
| A <sub>CL</sub>                  | Small Signal Voltage Gain                              | V <sub>IN</sub> = 0.2 V <sub>PP</sub>  | <b>0.95</b>         | 1.0             | <b>1.05</b>     | V/V   |
| V <sub>OS</sub>                  | Output Offset Voltage                                  |  |                     | -1.4            | 21<br><b>22</b> | mV    |
| TC V <sub>OS</sub>               | Temperature Coefficient Output Offset Voltage (Note 9) |  |                     | 2.4             |                 | μV/°C |
| R <sub>OUT</sub>                 | Output Resistance                                      | f = 100 kHz  |                     | 0.5             |                 | Ω     |
|                                  |  | f = 38.4 MHz   |                     | 126             |                 |       |
| <b>Miscellaneous Performance</b> |  |  |                     |                 |                 |       |
| R <sub>IN</sub>                  | Input Resistance per Buffer                            | Enable = V <sub>DD</sub>   |                     | 138             |                 | kΩ    |
|                                  |  | Enable = V <sub>SS</sub>   |                     | 138             |                 |       |
| C <sub>IN</sub>                  | Input Capacitance per Buffer                           | Enable = V <sub>DD</sub>   |                     | 1.3             |                 | pF    |
|                                  |  | Enable = V <sub>SS</sub>   |                     | 1.3             |                 |       |
| Z <sub>IN</sub>                  | Input Impedance  | f = 38.4 MHz, Enable = V <sub>DD</sub>   |                     | 4.3             |                 | kΩ    |
|                                  |  | f = 38.4 MHz, Enable = V <sub>SS</sub>   |                     | 4.2             |                 |       |
| V <sub>O</sub>                   | Output Swing Positive                                  | V <sub>IN</sub> = V <sub>DD</sub>  | 4.96<br><b>4.95</b> | 4.99            |                 | V     |
|                                  | Output Swing Negative                                  | V <sub>IN</sub> = V <sub>SS</sub>  |                     | 10              | 35<br><b>50</b> | mV    |
| I <sub>SC</sub>                  | Output Short-Circuit Current<br>(Notes 10, 11)         | Sourcing, V <sub>IN</sub> = V <sub>DD</sub> , V <sub>OUT</sub> = V <sub>SS</sub> | -80<br><b>-62</b>   | -90             |                 | mA    |
|                                  |  | Sinking, V <sub>IN</sub> = V <sub>SS</sub> , V <sub>OUT</sub> = V <sub>DD</sub>  | 60<br><b>43</b>     | 65              |                 |       |
| V <sub>en_hmin</sub>             | Enable High Active Minimum Voltage                     |  |                     | 1.2             |                 | V     |
| V <sub>en_lmax</sub>             | Enable Low Inactive Maximum Voltage                    |  |                     | 0.6             |                 |       |

**Note 1:** "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of the device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

**Note 2:** The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

**Note 3:** The maximum power dissipation must be derated at elevated temperatures and is dictated by  $T_{J(MAX)}$ ,  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable power dissipation is  $P_{DMAX} = (T_{J(MAX)} - T_A) / \theta_{JA}$  or the number given in the *Absolute Maximum Ratings*, whichever is lower.

**Note 4:** Human body model, applicable std. JESD22-A114C.

**Note 5:** Machine model, applicable std. JESD22-A115-A.

**Note 6:** Typical values represent the most likely parametric norms at  $T_A = +25^\circ\text{C}$ , and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

**Note 7:** Datasheet min/max specification limits are guaranteed by test or statistical analysis.

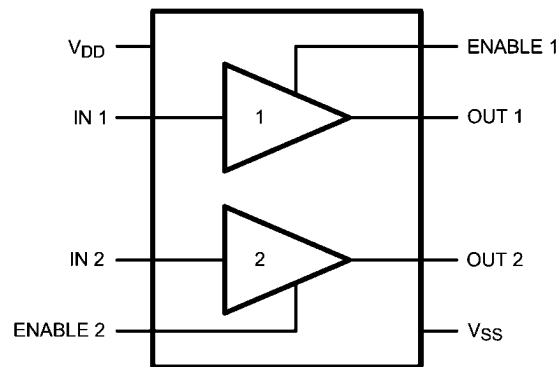
**Note 8:** Slew rate is the average of the rising and falling slew rates.

**Note 9:** Average Temperature Coefficient is determined by dividing the changing in a parameter at temperature extremes by the total temperature change.

**Note 10:** Short-Circuit test is a momentary test. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of  $150^\circ\text{C}$ .

**Note 11:** Positive current corresponds to current flowing into the device.

## Block Diagram

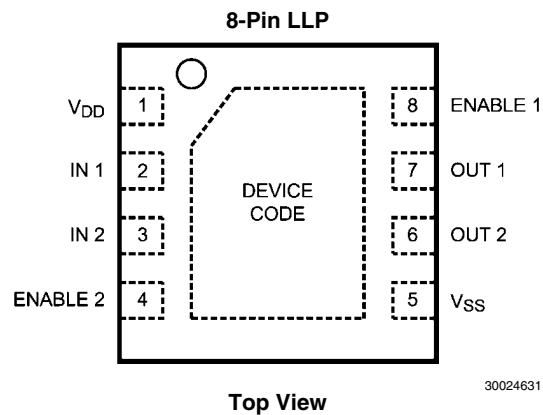


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## Pin Descriptions

| Pin No. | Pin Name        | Description               |
|---------|-----------------|---------------------------|
| 1       | V <sub>DD</sub> | Voltage supply connection |
| 2       | IN 1            | Input 1                   |
| 3       | IN 2            | Input 2                   |
| 4       | ENABLE 2        | Enable buffer 2           |
| 5       | V <sub>SS</sub> | Ground connection         |
| 6       | OUT 2           | Output 2                  |
| 7       | OUT 1           | Output 1                  |
| 8       | ENABLE 1        | Enable buffer 1           |

## Connection Diagram



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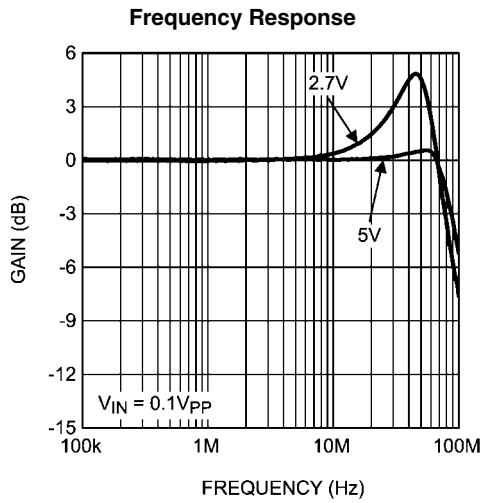
## Ordering Information

| Package                  | Part Number | Package Marking | Transport Media          | NSC Drawing |
|--------------------------|-------------|-----------------|--------------------------|-------------|
| 8-Pin LLP<br>Solder Bump | LMH2180YD   | LMH2180YD       | 1k Units Tape and Reel   | YDA08A      |
|                          | LMH2180YDX  |                 | 4.5k Units Tape and Reel |             |
| 8-Pin LLP<br>No Pullback | LMH2180SD   | LMH2180SD       | 1k Units Tape and Reel   | SDA08A      |
|                          | LMH2180SDX  |                 | 4.5 Units Tape and Reel  |             |

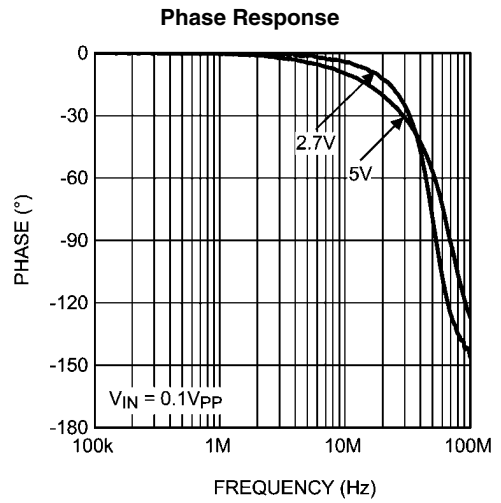
### Typical Performance Characteristics

$R_L = 30k\Omega$  and  $C_{COUPLING} = 10nF$ , unless otherwise specified.

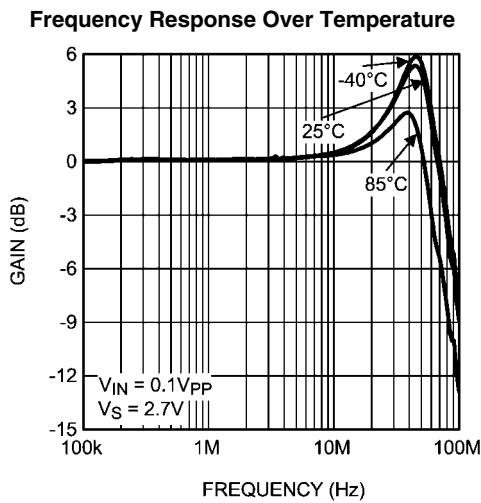
$T_J = 25^\circ C$ ,  $V_{DD} = 2.7V$ ,  $V_{SS} = 0V$ ,  $Enable_{1,2} = V_{DD}$ ,  $C_L = 10 pF$ ,



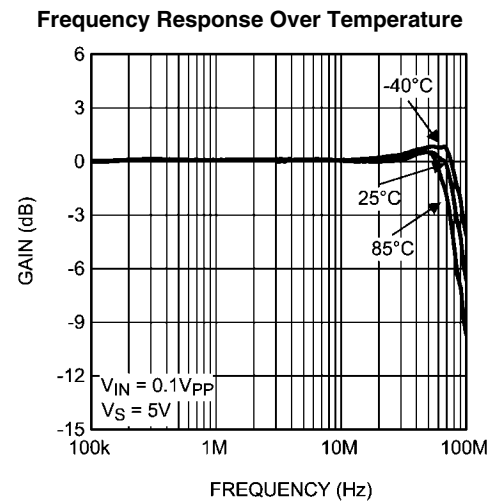
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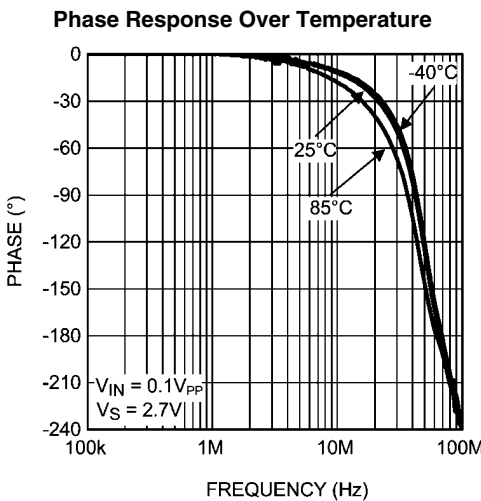
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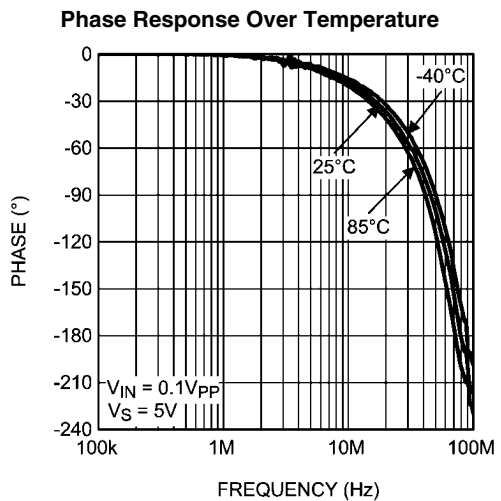
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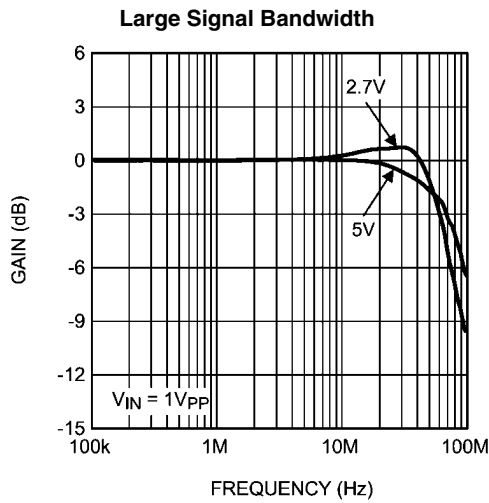
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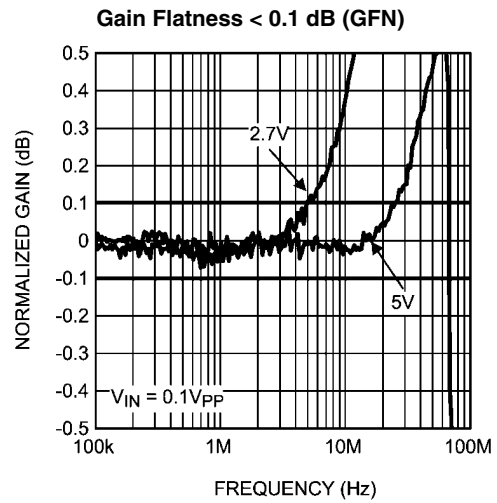
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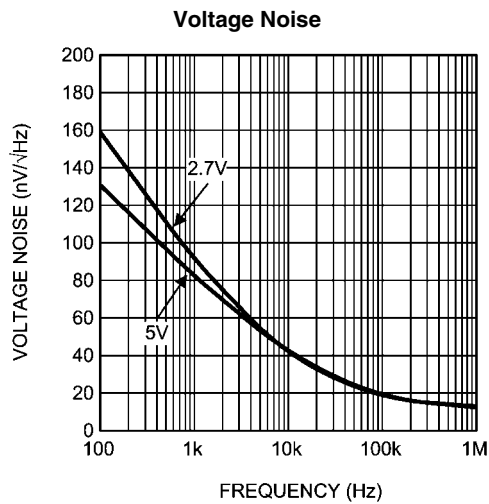
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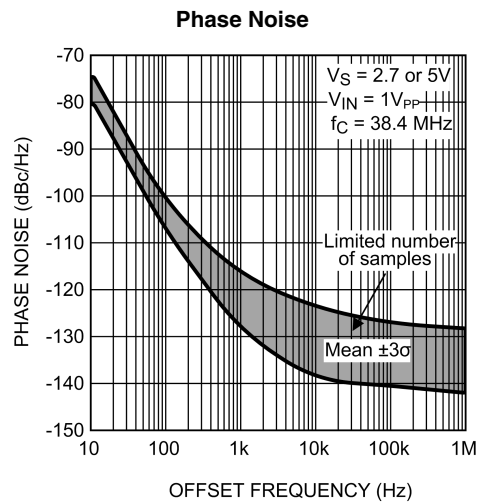
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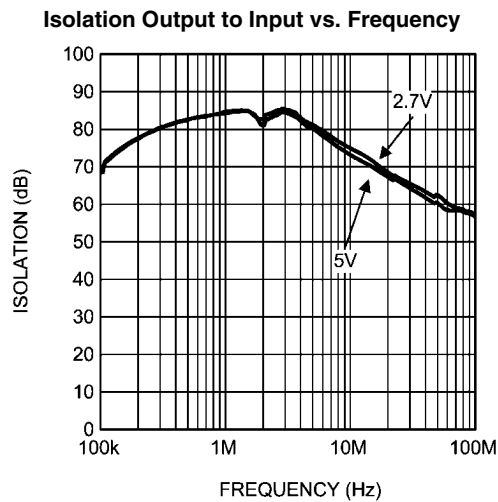
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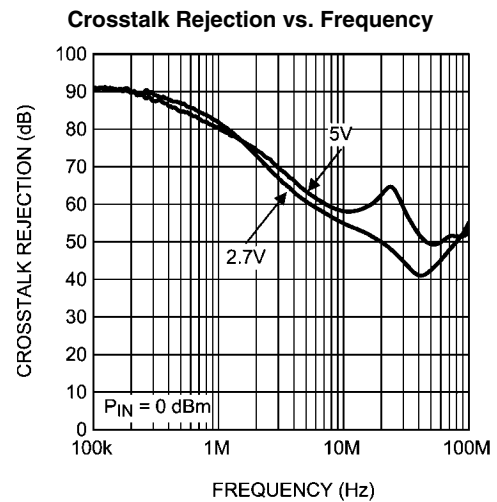
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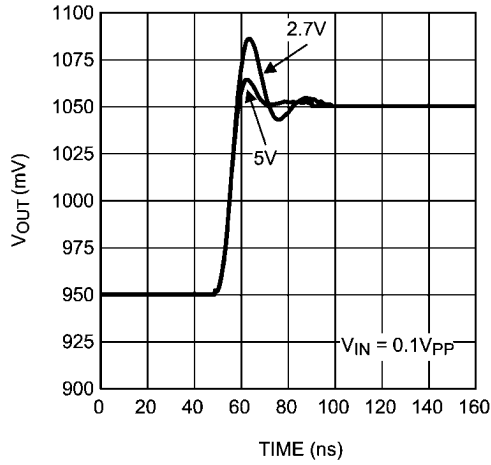


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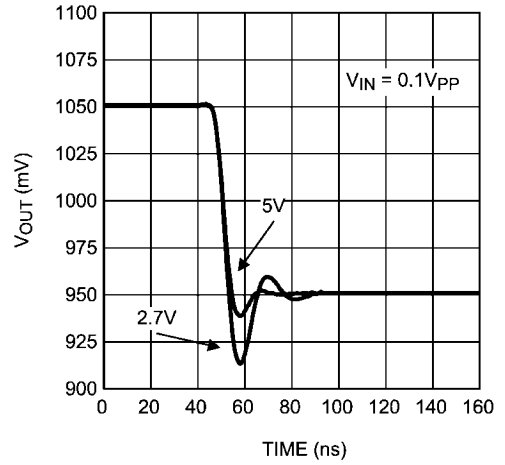
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**Transient Response Positive**



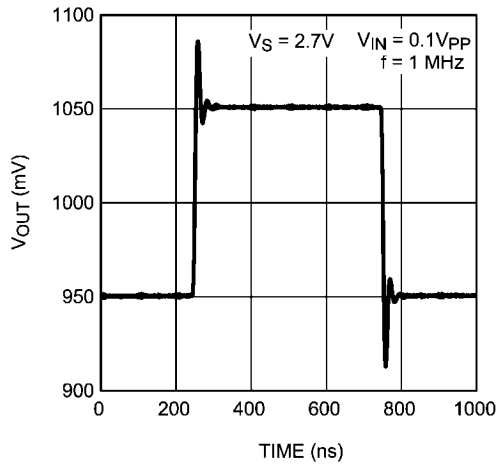
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**Transient Response Negative**



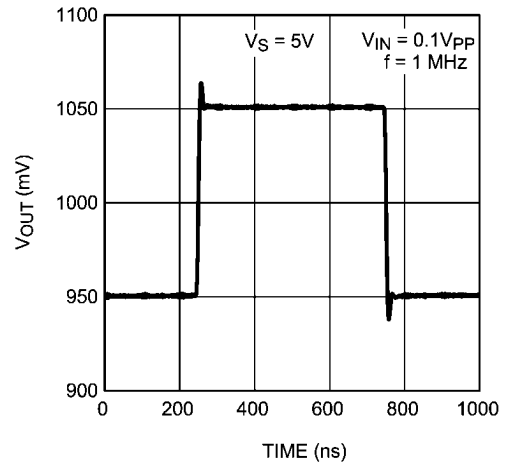
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**Small Signal Pulse Response**



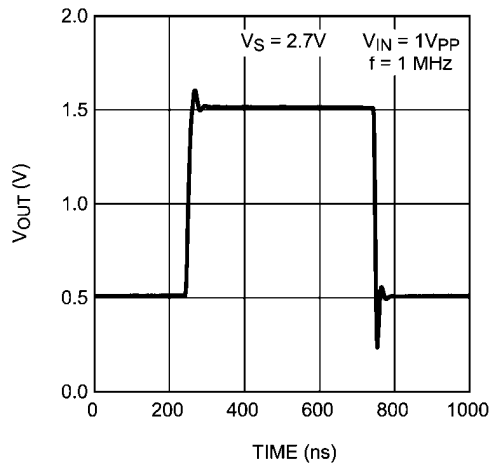
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**Small Signal Pulse Response**



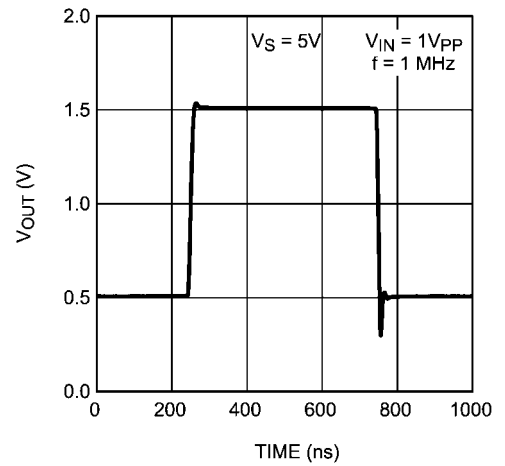
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**Large Signal Response**



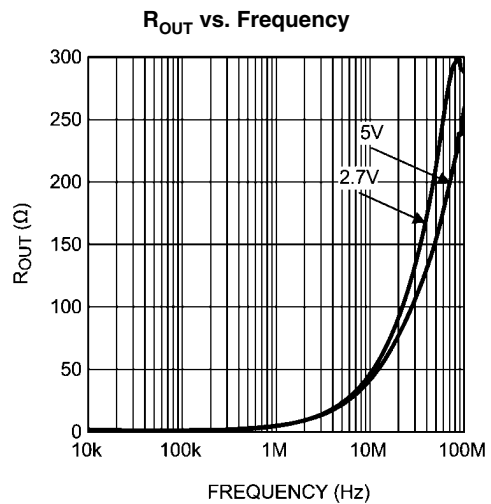
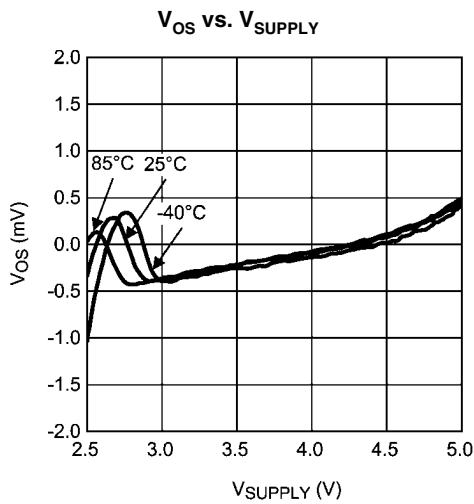
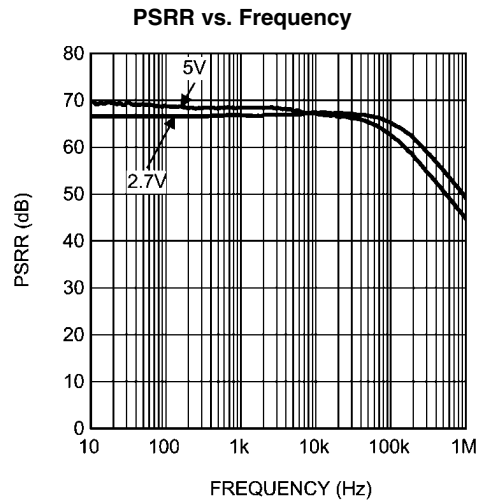
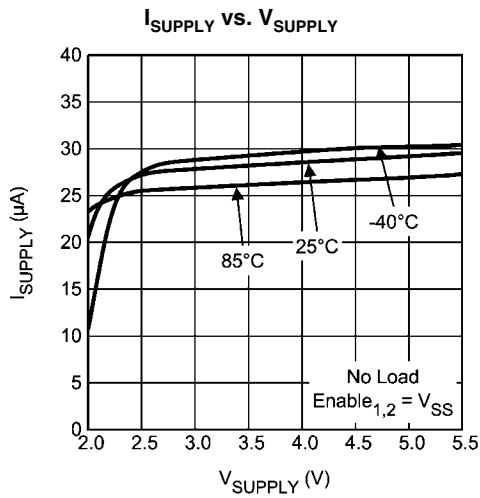
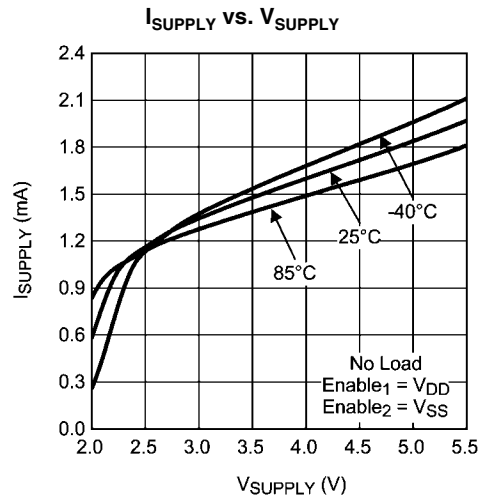
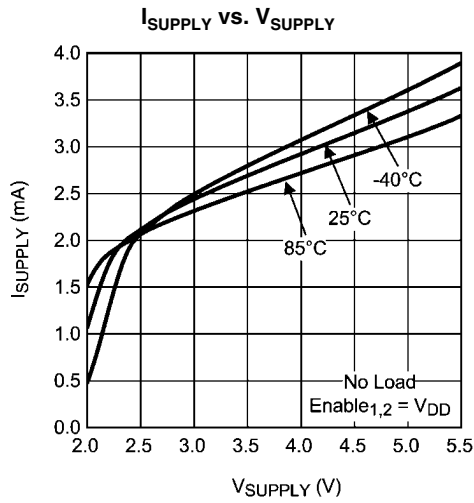
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**Large Signal Response**

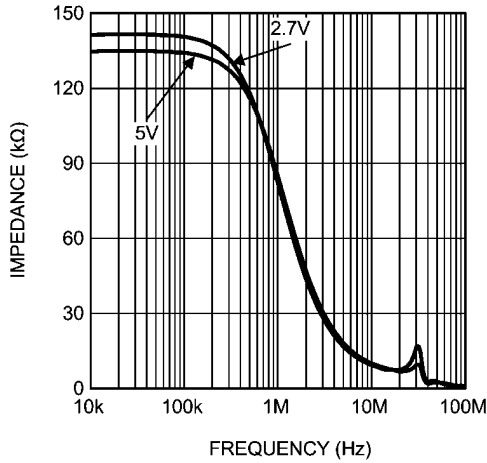


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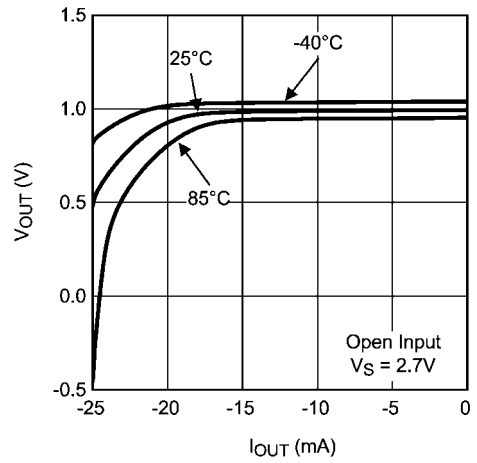


Input Impedance vs. Frequency



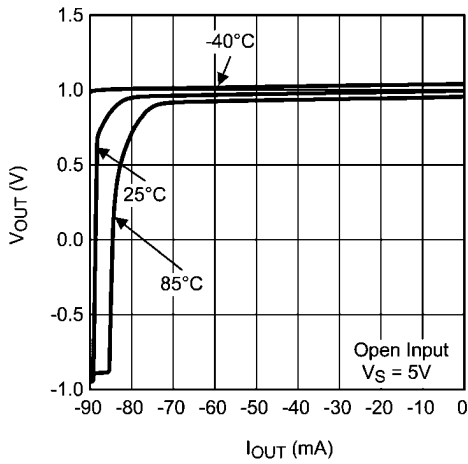
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V<sub>OUT</sub> vs. I<sub>OUT</sub> (Sourcing)



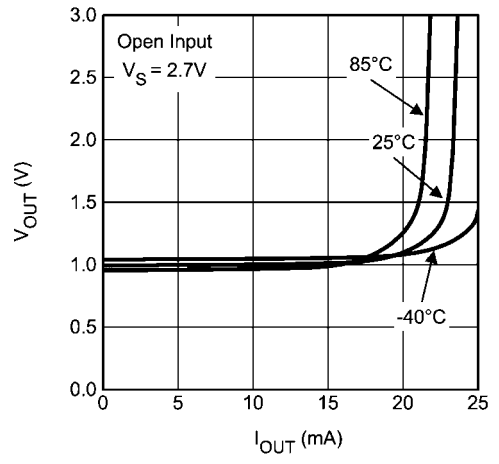
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V<sub>OUT</sub> vs. I<sub>OUT</sub> (Sourcing)



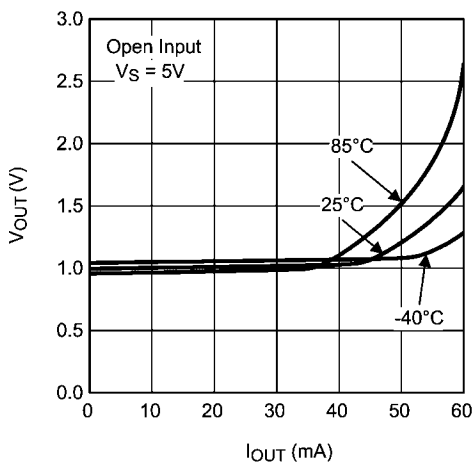
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V<sub>OUT</sub> vs. I<sub>OUT</sub> (Sinking)



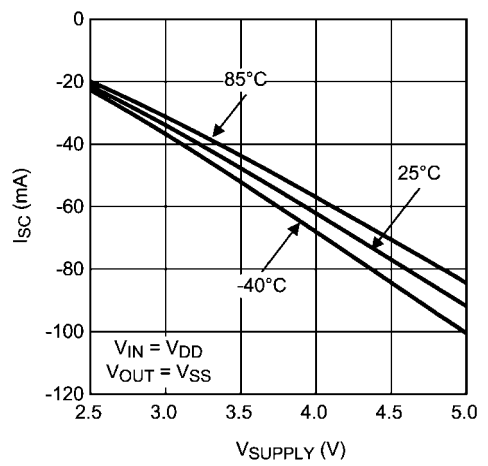
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V<sub>OUT</sub> vs. I<sub>OUT</sub> (Sinking)



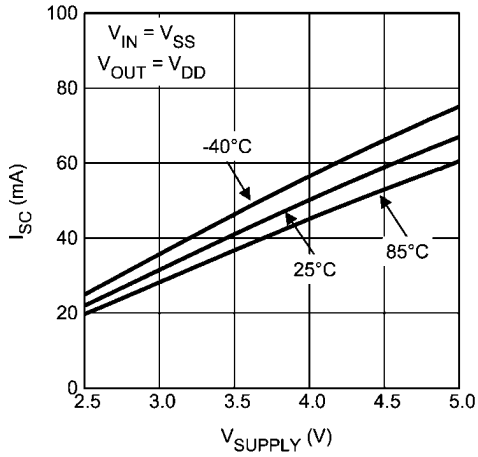
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I<sub>SC</sub> Sourcing vs. V<sub>SUPPLY</sub> Over Temperature



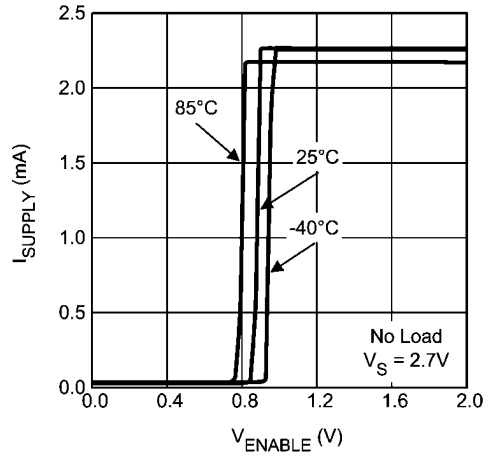
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**$I_{SC}$  Sinking vs.  $V_{SUPPLY}$  Over Temperature**



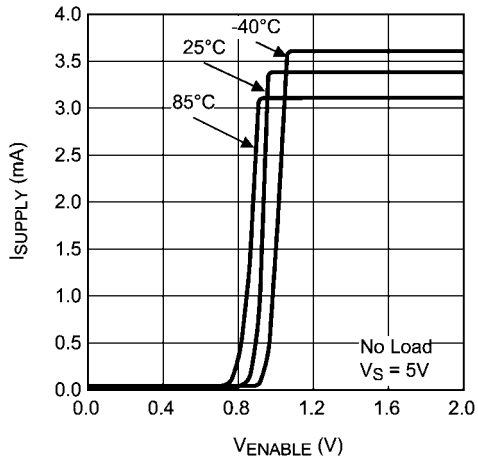
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**$I_{SUPPLY}$  vs.  $V_{ENABLE}$**



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**$I_{SUPPLY}$  vs.  $V_{ENABLE}$**



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# Application Information

## GENERAL

The LMH2180 is designed to minimize the effects of spurious signals from the base chip to the oscillator. Also the influence of varying load resistance and capacitance to the oscillator is minimized, while the drive capability is increased.

The inputs of the LMH2180 are internally biased at 1V, making AC coupling possible without external bias resistors.

To optimize current consumption, a buffer that is not in use can be disabled by connecting its enable pin to  $V_{SS}$ .

The LMH2180 has no internal ground reference; therefore, either single or split supply configurations can be used.

The LMH2180 is an easy replacement for discrete circuitry. It simplifies board layout and minimizes the effect of layout related parasitic components.

## INPUT CONFIGURATION

The internal 1V input biasing allows AC coupling of the input signal. This biasing avoids the use of external resistors, as depicted in *Figure 1*. The biasing prevents a large DC load at the oscillators output that creates a load impedance and may affect its oscillating frequency. As a result of this biasing, the maximum amplitude of the AC signal is  $2V_{pp}$ .

The coupling capacitance C1 should be large enough to let the AC signal pass. This is a unity gain buffer with rail-to-rail inputs and outputs.

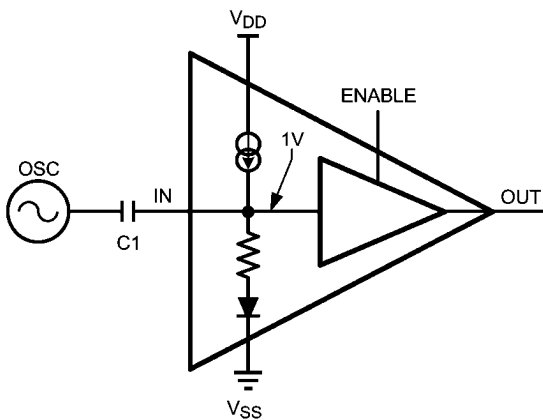


FIGURE 1. Input Configuration

## FREQUENCY PULLING

Frequency pulling is the frequency variation of an oscillator caused by a varying load. In the typical application, the load of the oscillator is a fixed capacitor (C1) in series with the input impedance of the buffer.

To keep the input impedance as constant as possible, the input is biased at 1V, even when the part is disabled. A simplified schematic of the input configuration is shown in *Figure 1*.

## ISOLATION AND CROSSTALK

Output to input isolation prevents the clock signal of the oscillator from being affected by spurious signals generated by the digital blocks behind the output buffer. See the charac-

teristic graphic entitled Isolation Output to Input vs. Frequency.

A block diagram of the isolation is shown in *Figure 2*. Crosstalk rejection between buffers prevents signals from affecting each other. *Figure 2* shows a Baseband IC and a Bluetooth module as an example. See the characteristic graphic labeled Crosstalk Rejection vs. Frequency for more information.

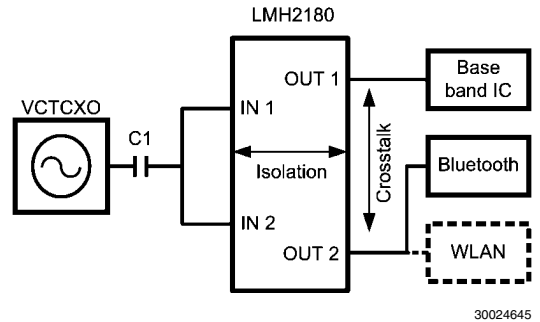


FIGURE 2. Isolation Block Diagram

## DRIVING CAPACITIVE LOADS

Each buffer can drive a capacitive load. Be aware that every capacitor directly connected to the output becomes part of the loop of the buffer. In most applications the load consists of the capacitance of copper tracks and the input capacitance of the application blocks. Capacitance reduces the gain/phase margin and decreases the stability. This leads to peaking in the frequency response and in extreme situations oscillations can occur. To drive a large capacitive load it is recommended to include a series resistor between the buffer and the load capacitor. The best value for this isolation resistance can be found by experimentation.

The LMH2180 datasheet reflects measurements with capacitive loads of 10 pF at the output of the buffers. Most common applications will probably use a lower capacitive load, which will result in lower peaking and significantly greater bandwidth, see *Figure 3*.

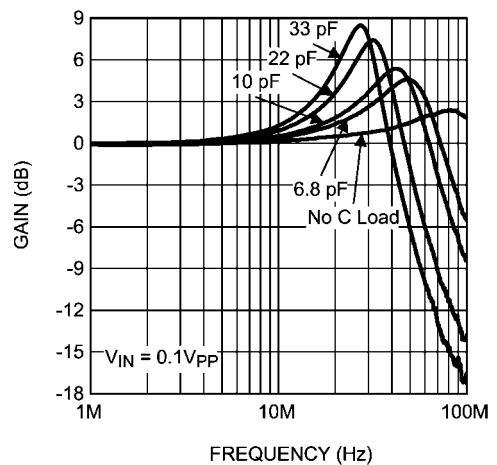
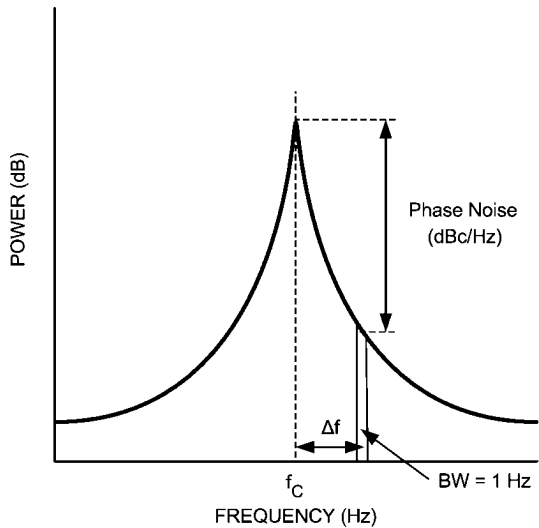


FIGURE 3. Bandwidth and Peaking

**PHASE NOISE**

A clock buffer adds noise to the clock signal. This noise causes uncertainty in the phase of the clock signal. This uncertainty is described by jitter (time domain) or phase noise (frequency domain). Communication systems, such as Wireless LAN, require a low jitter / phase noise clock signal to obtain a low Bit Error Rate. *Figure 4* shows the frequency domain representation of a clock signal with frequency  $f_c$ . Without Phase Noise the entire signal power would only be located at the frequency  $f_c$ . Phase Noise spreads some of the power to adjacent frequencies. Phase Noise is usually specified in dBc/Hz at a given frequency offset  $\Delta f$  from the carrier, where dBc is the power level in dB relative to the carrier. The noise power is measured within a 1Hz bandwidth.



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**FIGURE 4. Phase Noise**

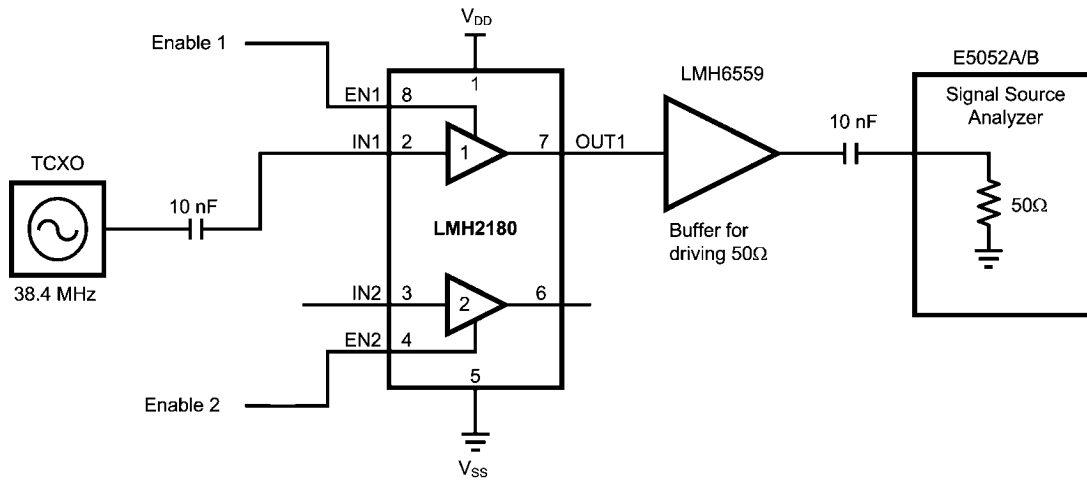
*Figure 5* shows the setup used to measure the LMH2180 phase noise. The clock driving the LMH2180 is a state of the art 38.4MHz TCXO. Both the TCXO phase noise and the phase noise at the LMH2180 output were measured. At offset frequencies of 1kHz and higher from the carrier, the TCXO phase noise is sufficiently low to accurately calculate the LMH2180 contribution to the phase noise at the output. The LMH6559, whose phase noise contribution can be neglected, is used to drive the 50Ω input impedance of the Signal Source Analyzer.

**LAYOUT DESIGN RECOMMENDATION**

Careful consideration during circuit design and PCB layout will eliminate problems and will optimize the performance of the LMH2180. It is best to have the same ground plane on the PCB for all decoupling and other ground connections.

To ensure a clean supply voltage it is best to place decoupling capacitors close to the LMH2180, between  $V_{DD}$  and  $V_{SS}$ .

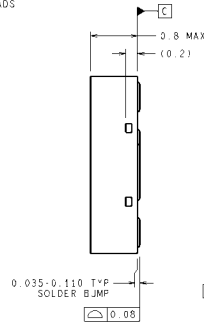
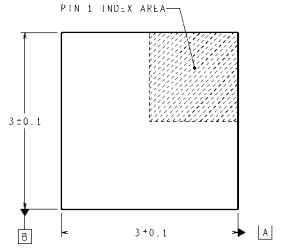
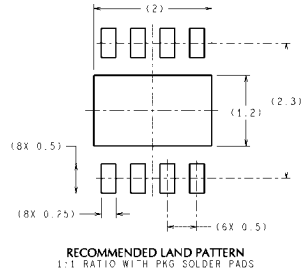
Another important issue is the value of the components, because this also determines the sensitivity to disturbances. Resistor values have to be low enough to avoid a significant noise contribution and large enough to avoid a significant increase in power consumption while loading inputs or outputs to heavily.



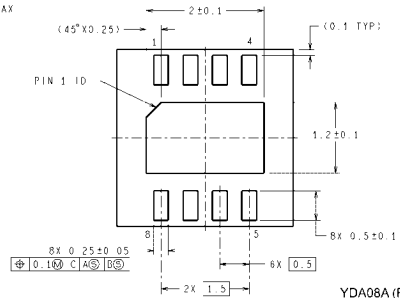
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**FIGURE 5. Measurement Setup**

**Physical Dimensions** inches (millimeters) unless otherwise noted

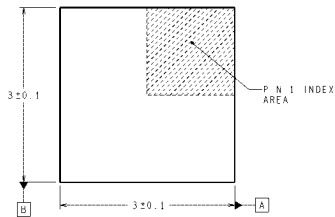
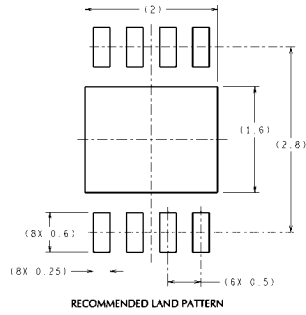


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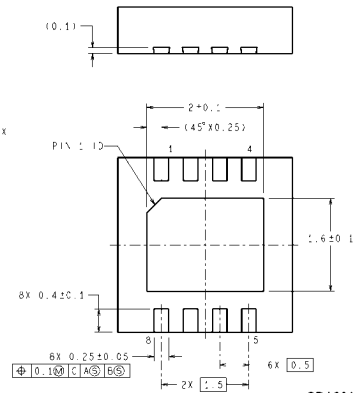
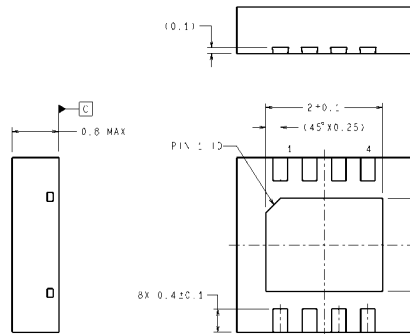


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# Notes

LMH2180

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