



Customer Information Notification

201908004I

Issue Date: 10-Sep-2019

Effective Date: 11-Sep-2019

Dear *Emma Tempest*,

Here's your personalized quality information concerning products Premier Farnell PLC purchased from NXP.

For detailed information we invite you to [view this notification online](#)

This notice is NXP Company Proprietary.



Change Category

- | | | | | |
|--|---|--|---|---|
| <input type="checkbox"/> Wafer Fab Process | <input type="checkbox"/> Assembly Process | <input type="checkbox"/> Product Marking | <input type="checkbox"/> Test Location | <input type="checkbox"/> Design |
| <input type="checkbox"/> Wafer Fab Materials | <input type="checkbox"/> Assembly Materials | <input type="checkbox"/> Mechanical Specification | <input type="checkbox"/> Test Process | <input checked="" type="checkbox"/> Errata |
| <input type="checkbox"/> Wafer Fab Location | <input type="checkbox"/> Assembly Location | <input type="checkbox"/> Packing/Shipping/Labeling | <input type="checkbox"/> Test Equipment | <input type="checkbox"/> Electrical spec./Test coverage |
| <input type="checkbox"/> Firmware | <input type="checkbox"/> Other | | | |

i.MXRT1060 &
i.MXRT1064 Errata
Rev1 Updates

Description

NXP Semiconductors announces errata update for the i.MXRT1060 & i.MXRT1064 to revision 1. The revision history included in the updated documents provides a detailed description of the changes. Changes are summarized below.

Added following 5 errata:

- * ERR011572: Cortex-M7: Write-Trough stores and loads may return incorrect data
- * ERR050130: PIT: Temporary incorrect value reported in LMTR64H register in lifetimer mode
- * ERR050144: SAI: Setting FCONT = 1 when TMR > 0 may not function correctly
- * ERR050101: USB: Endpoint conflict issue in device mode
- * ERR050194: QTMR: overflow flag and interrupt can't be generated while configured as counter up mode

The i.MXRT1060 & i.MXRT1064 errata revision 1 is attached to this notice, and can be found at:

<https://www.nxp.com/docs/en/nxp/errata/IMXRT1060CE.pdf>

<https://www.nxp.com/docs/en/errata/IMXRT1064CE.pdf>

Reason

The errata were added for additional technical clarification on some device features.

Identification of Affected Products

Product identification does not change

Anticipated Impact on Form, Fit, Function, Reliability or Quality

No impact on form, fit, function, reliability or quality.

Additional information

Affected products and sales history information: see attached file

Additional documents: [view online](#)



Contact and Support

For all inquiries regarding the ePCN tool application or access issues, please [contact NXP "Global Quality Support Team"](#).

For all Quality Notification content inquiries, please contact your local NXP Sales Support team.

For specific questions on this notice or the products affected please contact our specialist directly:

Name Daniel Cheng

Position Product Engineer

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At NXP Semiconductors we are constantly striving to improve our product and processes to ensure they reach the highest possible Quality Standards.

Customer Focus, Passion to Win.

NXP Quality Management Team.

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