Product Change Notification - SYST-16VOLC851

Date:

17 Sep 2019

Product Category:

8-bit Microcontrollers

Affected CPNs:

Notification subject:

Data Sheet - PIC18F26/45/46Q10 28/40-Pin, Low-Power, High-Performance Microcontrollers

Notification text:

SYST-16VOLC851

Microchip has released a new Product Documents for the PIC18F26/45/46Q10 28/40-Pin, Low-Power, High-Performance Microcontrollers of devices. If you are using one of these devices please read the document located at PIC18F26/45/46Q10 28/40-Pin, Low-Power, High-Performance Microcontrollers.

Notification Status: Final

Description of Change: 1) Updated AC/DC Graphs; Tables 39-3, 39-8, 39-14; Figure 39-2; Section 40

Impacts to Data Sheet: None

Reason for Change: To Improve Manufacturability

Change Implementation Status: Complete

Date Document Changes Effective: 17 Sep 2019

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

PIC18F26/45/46Q10 28/40-Pin, Low-Power, High-Performance Microcontrollers

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

PIC18F24Q10-I/ML
PIC18F24Q10-I/SO
PIC18F24Q10-I/SP
PIC18F24Q10-I/SS
PIC18F24Q10-I/STX
PIC18F24Q10T-I/ML
PIC18F24Q10T-I/SO
PIC18F24Q10T-I/SS
PIC18F24Q10T-I/STX
PIC18F25Q10-I/ML
PIC18F25Q10-I/SO
PIC18F25Q10-I/SP
PIC18F25Q10-I/SS
PIC18F25Q10-I/STX
PIC18F25Q10T-I/ML
PIC18F25Q10T-I/SO
PIC18F25Q10T-I/SS
PIC18F25Q10T-I/STX
PIC18F26Q10-E/ML
PIC18F26Q10-E/SO
PIC18F26Q10-E/SP
PIC18F26Q10-E/SS
PIC18F26Q10-E/STX
PIC18F26Q10-I/ML
PIC18F26Q10-I/SO
PIC18F26Q10-I/SP
PIC18F26Q10-I/SS
PIC18F26Q10-I/STX
PIC18F26Q10T-I/ML
PIC18F26Q10T-I/SO
PIC18F26Q10T-I/SS
PIC18F26Q10T-I/STX
PIC18F27Q10-E/ML
PIC18F27Q10-I/ML
PIC18F27Q10-I/SO
PIC18F27Q10-I/SP
PIC18F27Q10-I/SS
PIC18F27Q10-I/STX
PIC18F27Q10T-I/ML
PIC18F27Q10T-I/SO
PIC18F27Q10T-I/SS
PIC18F27Q10T-I/STX
PIC18F45Q10-E/MP
PIC18F45Q10-E/P
PIC18F45Q10-E/PT
PIC18F45Q10-I/MP

PIC18F45Q10-I/P
PIC18F45Q10-I/PT
PIC18F45Q10T-I/MP
PIC18F45Q10T-I/PT
PIC18F46Q10-E/MP
PIC18F46Q10-E/P
PIC18F46Q10-E/PT
PIC18F46Q10-I/MP
PIC18F46Q10-I/P
PIC18F46Q10-I/PT
PIC18F46Q10T-I/MP
PIC18F46Q10T-I/PT
PIC18F47Q10-I/MP
PIC18F47Q10-I/P
PIC18F47Q10-I/PT
PIC18F47Q10T-I/MP
PIC18F47Q10T-I/PT

PIC18F26/45/46Q10

28/40/44-Pin, Low-Power, High-Performance Microcontrollers

Description

PIC18F26/45/46Q10 microcontrollers feature analog, core independent, and communication peripherals for a wide range of general purpose and low-power applications. These 28/40/44-pin devices are equipped with a 10-bit ADC with Computation (ADC^2) automating Capacitive Voltage Divider (CVD) techniques for advanced touch sensing, averaging, filtering, oversampling and performing automatic threshold comparisons. They also offer a set of core independent peripherals such as Complementary Waveform Generator (CWG), Windowed Watchdog Timer (WWDT), Cyclic Redundancy Check (CRC)/Memory Scan, Zero-Cross Detect (ZCD), Configurable Logic Cell (CLC), and Peripheral Pin Select (PPS), providing increased design flexibility and lower system cost.

Core Features

- C Compiler Optimized RISC Architecture
- Operating Speed:
  - DC – 64 MHz clock input over the full V_{DD} range
  - 62.5 ns minimum instruction cycle
- Programmable 2-Level Interrupt Priority
- 31-Level Deep Hardware Stack
- Three 8-Bit Timers (TMR2/4/6) with Hardware Limit Timer (HLT)
- Four 16-Bit Timers (TMR0/1/3/5)
- Low-Current Power-on Reset (POR)
- Power-up Timer (PWRT)
- Brown-out Reset (BOR)
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
  - Watchdog Reset on too long or too short interval between watchdog clear events
  - Variable prescaler selection
  - Variable window size selection
  - All sources configurable in hardware or software

Memory

- Up to 64K Bytes Program Flash Memory
- Up to 3615 Bytes Data SRAM Memory
- Up to 1024 Bytes Data EEPROM
- Programmable Code Protection
- Direct, Indirect and Relative Addressing modes

Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 5.5V
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Power-Saving Operation Modes

- Doze: CPU and Peripherals Running at Different Cycle Rates (typically CPU is lower)
- Idle: CPU Halted While Peripherals Operate
- Sleep: Lowest Power Consumption
- Peripheral Module Disable (PMD):
  - Ability to selectively disable hardware module to minimize active power consumption of unused peripherals
- Extreme Low-Power mode (XLP)
  - Sleep: 500 nA typical @ 1.8V
  - Sleep and Watchdog Timer: 900 nA typical @ 1.8V

Digital Peripherals

- Configurable Logic Cell (CLC):
  - Integrated combinational and sequential logic
- Complementary Waveform Generator (CWG):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
- Capture/Compare/PWM (CCP) modules:
  - Two CCPs
  - 16-bit resolution for Capture/Compare modes
  - 10-bit resolution for PWM mode
- 10-Bit Pulse-Width Modulators (PWM):
  - Two 10-bit PWMs
- Serial Communications:
  - Two Enhanced USART (EUSART) with Auto-Baud Detect, Auto-wake-up on Start, RS-232, RS-485, LIN compatible
  - SPI
  - I^2C, SMBus and PMBus™ compatible
- Up to 35 I/O Pins and One Input Pin:
  - Individually programmable pull-ups
  - Slew rate control
  - Interrupt-on-change on all pins
  - Input level selection control
- Programmable CRC with Memory Scan:
  - Reliable data/program memory monitoring for Fail-Safe operation (e.g., Class B)
  - Calculate CRC over any portion of Flash or EEPROM
  - High-speed or background operation
- Hardware Limit Timer (TMR2/4/6+HLT):
  - Hardware monitoring and Fault detection

- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O
- Data Signal Modulator (DSM)

Analog Peripherals

- 10-Bit Analog-to-Digital Converter with Computation (ADC^2):
  - 35 external channels
  - Conversion available during Sleep
  - Four internal analog channels
  - Internal and external trigger options
  - Automated math functions on input signals:
    - Averaging, filter calculations, oversampling and threshold comparison
  - 8-bit hardware acquisition timer
- Hardware Capacitive Voltage Divider (CVD) Support:
  - 8-bit precharge timer
  - Adjustable Sample-and-Hold capacitor array
  - Guard ring digital output drive
- Zero-Cross Detect (ZCD):
  - Detect when AC signal on pin crosses ground
- 5-Bit Digital-to-Analog Converter (DAC):
  - Output available externally
  - Programmable 5-bit voltage (% of V_{DD},[V_{REF+} - V_{REF-}], FVR)
  - Internal connections to comparators and ADC
- Two Comparators (CMP):
  - Four external inputs
  - External output via PPS
- Fixed Voltage Reference (FVR) Module:
  - 1.024V, 2.048V and 4.096V output levels
  - Two buffered outputs: One for DAC/CMP and one for ADC

Clocking Structure

- High-Precision Internal Oscillator Block (HFINTOSC):
  - Selectable frequencies up to 64 MHz
  - ±1% at calibration
- 32 kHz Low-Power Internal Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOSC)
- External High-frequency Oscillator Block:
  - Three crystal/resonator modes
  - Digital Clock Input mode
  - 4x PLL with external sources
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if external clock stops
- Oscillator Start-up Timer (OST)

Programming/Debug Features

- In-Circuit Serial Programming™ (ICSP™) via Two Pins

- In-Circuit Debug (ICD) with Three Breakpoints via Two Pins
- Debug Integrated On-Chip

PIC18F26/45/46Q10 Family Types

Table 1. Devices included in this data sheet

Device	Program Memory Flash (bytes)	Data SRAM (bytes)(2)	Data EEPROM (bytes)	I/O Pins	16-bit Timers	Comparators	10-bit ADC2 with Computation (ch)	5-bit DAC	Zero-Cross Detect	CCP/10-bit PWM	CWG	CLC	Low Voltage Detect (LVD)	8-bit TMR with HLT	Windowed Watchdog Timer	CRC with Memory Scan	EUSART	I2C/SPI	PPS	Peripheral Module Disable	Temperature Indicator	Debug(1)
PIC18F26Q10	64k	3615	1024	25	4	2	24	1	1	2/2	1	8	1	3	Y	Y	2	2	Y	Y	Y	I
PIC18F45Q10	32k	2304	256	36	4	2	35	1	1	2/2	1	8	1	3	Y	Y	2	2	Y	Y	Y	I
PIC18F46Q10	64k	3615	1024	36	4	2	35	1	1	2/2	1	8	1	3	Y	Y	2	2	Y	Y	Y	I

Note:

1. Debugging Methods: (I) – Integrated on-chip.
2. SRAM includes 256 bytes of SECTOR space which is not included in the data size displayed by MPLAB X.

Table 2. Devices not included in this data sheet

Device	Program Memory Flash (bytes)	Data SRAM (bytes)(2)	Data EEPROM (bytes)	I/O Pins	16-bit Timers	Comparators	10-bit ADC2 with Computation (ch)	5-bit DAC	Zero-Cross Detect	CCP/10-bit PWM	CWG	CLC	Low Voltage Detect (LVD)	8-bit TMR with HLT	Windowed Watchdog Timer	CRC with Memory Scan	EUSART	I2C/SPI	PPS	Peripheral Module Disable	Temperature Indicator	Debug(1)
PIC18F24Q10	16k	1280	256	25	4	2	24	1	1	2/2	1	0	1	3	Y	Y	1	1	Y	Y	Y	I
PIC18F25Q10	32k	2304	256	25	4	2	24	1	1	2/2	1	0	1	3	Y	Y	1	1	Y	Y	Y	I
PIC18F27Q10	128k	3615	1024	25	4	2	24	1	1	2/2	1	8	1	3	Y	Y	2	2	Y	Y	Y	I
PIC18F47Q10	128k	3615	1024	36	4	2	35	1	1	2/2	1	8	1	3	Y	Y	2	2	Y	Y	Y	I

Note:

1. Debugging Methods: (I) – Integrated on-chip.
2. SRAM includes 256 bytes of SECTOR space which is not included in the data size displayed by MPLAB X.

Data Sheet Index:

1. DS40001945 Data Sheet, 28-Pin, 8-bit Flash Microcontrollers
2. DS40002043 Data Sheet, 28/40-Pin, 8-bit Flash Microcontrollers

Packages

Important: For other small form-factor package availability and marking information, visit http://www.microchip.com/packaging or contact your local Microchip sales office.

Packages	SPDIP (SP)	SOIC (SO)	SSOP (SS)	QFN (ML) (6x6x0.9)	VQFN (STX) (4x4x1)	TQFP (PT)	PDIP (P)	QFN (MP) (5x5x0.9)
PIC18F26Q10	•	•	•	•	•			
PIC18F45Q10						•	•	•
PIC18F46Q10						•	•	•

Important: Pin details are subject to change.

Pin Diagrams

Figure 1. 28-pin SPDIP, SSOP, SOIC

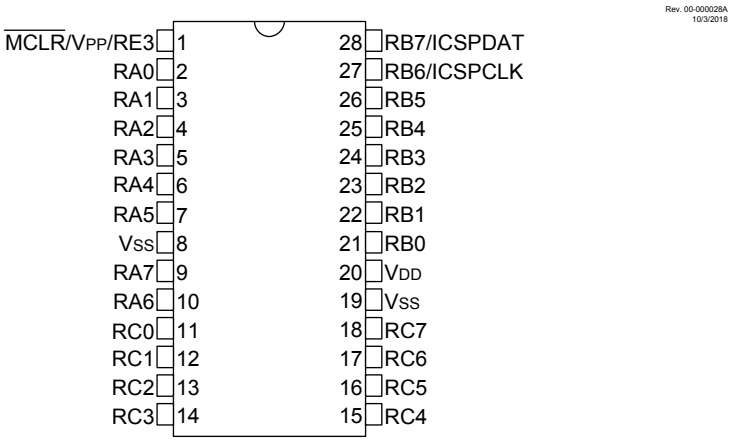
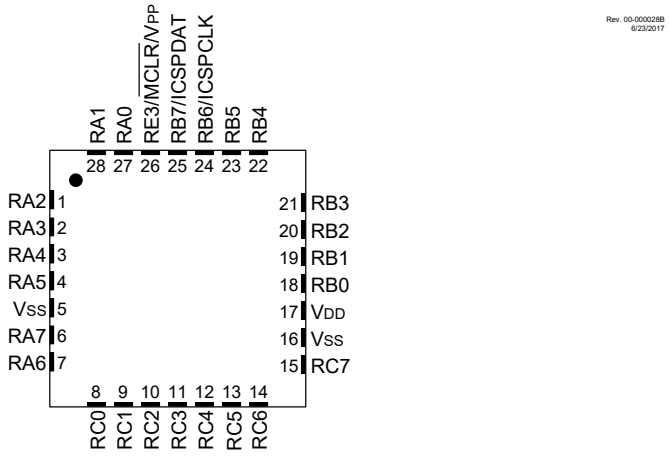


Figure 2. 28-pin QFN VQFN



Note: It is recommended that the exposed bottom pad be connected to V_{SS}, however it must not be the only V_{SS} connection to the device.

Figure 3. 40-pin PDIP

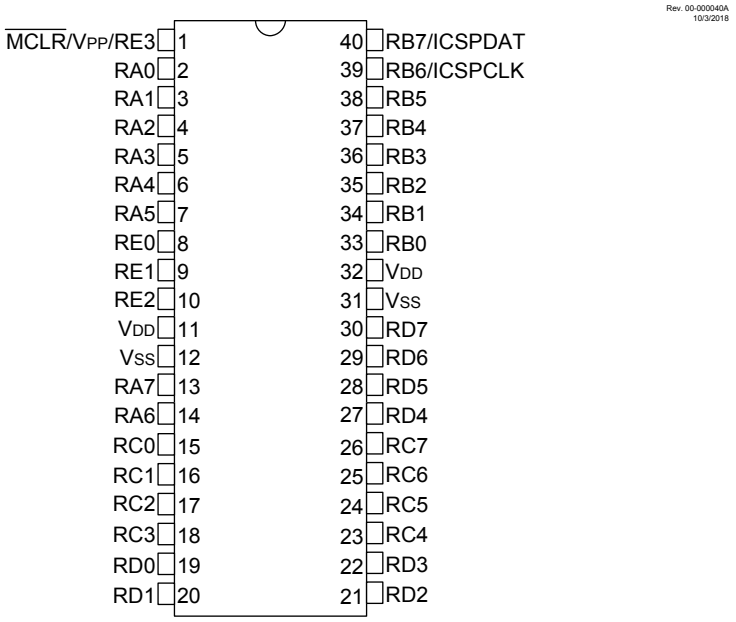
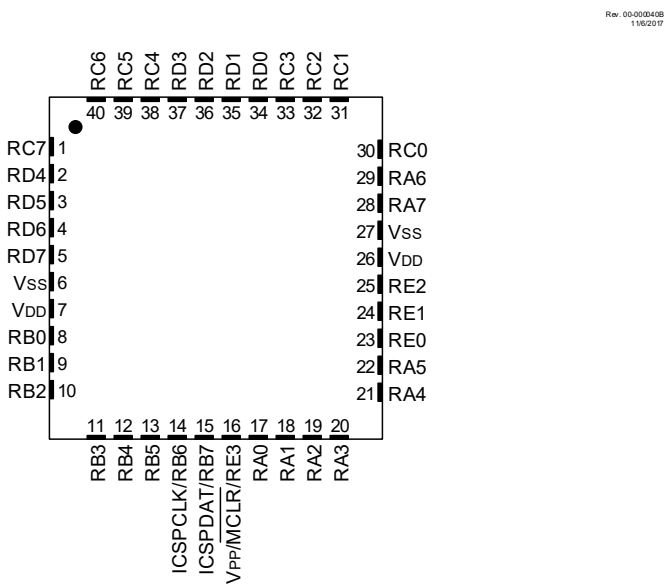
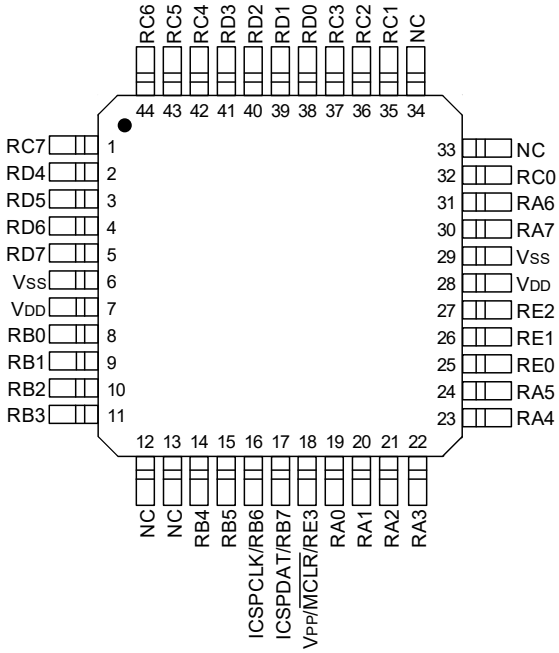


Figure 4. 40-pin QFN



Note: It is recommended that the exposed bottom pad be connected to V_{SS}, however it must not be the only V_{SS} connection to the device.

Figure 5. 44-pin TQFP



Pin Allocation Tables

Table 3. 28-Pin Allocation Table

I/O(2)	28-Pin SPDIP, SOIC, SSOP	28-Pin (V)QFN	A/D	Reference	Comparator	Timers	CCP	CWG	ZCD	Interrupt	EUSART	DSM	MSSP	Pull-up	Basic
RA0	2	27	ANA0	—	C1IN0- C2IN0-	—	—	—	—	IOCA0	—	—	—	Y	—
RA1	3	28	ANA1	—	C1IN1- C2IN1-	—	—	—	—	IOCA1	—	—	—	Y	—
RA2	4	1	ANA2	DAC1OUT1 V_{REF-} (DAC) V_{REF-} (ADC)	C1IN0+ C2IN0+	—	—	—	—	IOCA2	—	—	—	Y	—
RA3	5	2	ANA3	V_{REF+} (DAC) V_{REF+} (ADC)	C1IN1+	—	—	—	—	IOCA3	—	MDCARL(1)	—	Y	—
RA4	6	3	ANA4	—	—	T0CKI(1)	—	—	—	IOCA4	—	MDCARH(1)	—	Y	—
RA5	7	4	ANA5	—	—	—	—	—	—	IOCA5	—	MDSRC(1)	$\overline{SS1}$(1)	Y	—
RA6	10	7	ANA6	—	—	—	—	—	—	IOCA6	—	—	—	Y	CLKOUT OSC2
RA7	9	6	ANA7	—	—	—	—	—	—	IOCA7	—	—	—	Y	OSC1 CLKIN
RB0	21	18	ANB0	—	C2IN1+	—	—	CWG1(1)	ZCDIN	IOCB0 INT0(1)	—	—	—	Y	—
RB1	22	19	ANB1	—	C1IN3- C2IN3-	—	—	—	—	IOCB1 INT1(1)	—	—	—	Y	—
RB2	23	20	ANB2	—	—	—	—	—	—	IOCB2 INT2(1)	—	—	—	Y	—

.....continued

I/O(2)	28-Pin SPDIP, SOIC, SSOP	28-Pin (V)QFN	A/D	Reference	Comparator	Timers	CCP	CWG	ZCD	Interrupt	EUSART	DSM	MSSP	Pull-up	Basic
RB3	24	21	ANB3	—	C1IN2- C2IN2-	—	—	—	—	IOCB3	—	—	—	Y	—
RB4	25	22	ANB4	—	—	T5G(1)	—	—	—	IOCB4	—	—	—	Y	—
RB5	26	23	ANB5	—	—	T1G(1)	—	—	—	IOCB5	—	—	—	Y	—
RB6	27	24	ANB6	—	—	—	—	—	—	IOCB6	—	—	—	Y	ICSPCLK
RB7	28	25	ANB7	DAC1OUT2	—	T6IN(1)	—	—	—	IOCB7	—	—	—	Y	ICSPDAT
RC0	11	8	ANC0	—	—	T1CKI(1) T3CKI(1) T3G(1)	—	—	—	IOCC0	—	—	—	Y	SOSCO
RC1	12	9	ANC1	—	—	—	CCP2(1)	—	—	IOCC1	—	—	—	Y	SOSCIN SOSCI
RC2	13	10	ANC2	—	—	T5CKI(1)	CCP1(1)	—	—	IOCC2	—	—	—	Y	—
RC3	14	11	ANC3	—	—	T2IN(1)	—	—	—	IOCC3	—	—	SCK1(1) SCL1(3,4)	Y	—
RC4	15	12	ANC4	—	—	—	—	—	—	IOCC4	—	—	SDI1(1) SDA1(3,4)	Y	—
RC5	16	13	ANC5	—	—	T4IN(1)	—	—	—	IOCC5	—	—	—	Y	—
RC6	17	14	ANC6	—	—	—	—	—	—	IOCC6	CK1(1,3)	—	—	Y	—
RC7	18	15	ANC7	—	—	—	—	—	—	IOCC7	RX1/DT1(1,3)	—	—	Y	—
RE3	1	26	—	—	—	—	—	—	—	IOCE3	—	—	—	Y	Vpp/$\overline{MCLR}$
V_{SS}	19	16	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
V_{DD}(5)	20	17	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	8	5	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
OUT(2)	—	—	ADGRDA ADGRDB	—	C1OUT C2OUT	TMR0	CCP1 CCP2 PWM3 PWM4	CWG1A CWG1B CWG1C CWG1D	—	—	TX1/CK1(3) DT1(3)	DSM	SDO1 SCK1	—	—

Note:

1. This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to the peripheral input selection table for details on which port pins may be used for this signal.
2. All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in the peripheral output selection table.
3. This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4. These pins are configured for I^2C logic levels; The SCLx/SDAx signals may be assigned to any of these pins. PPS assignments to the other pins (e.g., RB1) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.
5. A 0.1 uF bypass capacitor to V_{SS} is required on the V_{DD} pin.

Table 4. 40/44-Pin Allocation Table

I/O(2)	40-Pin PDIP	40-Pin QFN	44-Pin QFN	44-Pin TQFP	A/D	Reference	Comparator	Timers	CCP	CWG	ZCD	Interrupt	EUSART	DSM	MSSP	Pull-up	Basic
RA0	2	17	19	19	ANA0	—	C1INO- C2IN0-	—	—	—	—	IOCA0	—	—	—	Y	—
RA1	3	18	20	20	ANA1	—	C1IN1- C2IN1-	—	—	—	—	IOCA1	—	—	—	Y	—
RA2	4	19	21	21	ANA2	DAC1OUT1 V_{REF-} (DAC5) V_{REF-} (ADC)	C1IN0+ C2IN0+	—	—	—	—	IOCA2	—	—	—	Y	—
RA3	5	20	22	22	ANA3	V_{REF+} (DAC5) V_{REF+} (ADC)	C1IN1+	—	—	—	—	IOCA3	—	MDCARL(1)	—	Y	—
RA4	6	21	23	23	ANA4	—	—	T0CKI(1)	—	—	—	IOCA4	—	MDCARH(1)	—	Y	—

.....continued

I/O(2)	40-Pin PDIP	40-Pin QFN	44-Pin QFN	44-Pin TQFP	A/D	Reference	Comparator	Timers	CCP	CWG	ZCD	Interrupt	EUSART	DSM	MSSP	Pull-up	Basic
RA5	7	22	24	24	ANA5	—	—	—	—	—	—	IOCA5	—	MDSRC(1)	$\overline{SS1}$(1)	Y	—
RA6	14	29	33	31	ANA6	—	—	—	—	—	—	IOCA6	—	—	—	Y	CLKOUT OSC2
RA7	13	28	32	30	ANA7	—	—	—	—	—	—	IOCA7	—	—	—	Y	OSC1 CLKIN
RB0	33	8	9	8	ANB0	—	C2IN1+	—	—	CWG1(1)	ZCDIN	IOCB0 INT0(1)	—	—	$\overline{SS2}$(1)	Y	—
RB1	34	9	10	9	ANB1	—	C1IN3- C2IN3-	—	—	—	—	IOCB1 INT1(1)	—	—	SCK2(1) SCL2(3,4)	Y	—
RB2	35	10	11	10	ANB2	—	—	—	—	—	—	IOCB2 INT2(1)	—	—	SDI2(1) SDA2(3,4)	Y	—
RB3	36	11	12	11	ANB3	—	C1IN2- C2IN2-	—	—	—	—	IOCB3	—	—	—	Y	—
RB4	37	12	14	14	ANB4	—	—	T5G(1)	—	—	—	IOCB4	—	—	—	Y	—
RB5	38	13	15	15	ANB5	—	—	T1G(1)	—	—	—	IOCB5	—	—	—	Y	—
RB6	39	14	16	16	ANB6	—	—	—	—	—	—	IOCB6	CK2(1,3)	—	—	Y	ICSPCLK
RB7	40	15	17	17	ANB7	DAC1OUT2	—	T6IN(1)	—	—	—	IOCB7	RX2/ DT2(1,3)	—	—	Y	ICSPDAT
RC0	15	30	34	32	ANC0	—	—	T1CKI(1) T3CKI(1) T3G(1)	—	—	—	IOCC0	—	—	—	Y	SOSCO
RC1	16	31	35	35	ANC1	—	—	—	CCP2(1)	—	—	IOCC1	—	—	—	Y	SOSCIN SOSCI
RC2	17	32	36	36	ANC2	—	—	T5CKI(1)	CCP1(1)	—	—	IOCC2	—	—	—	Y	—
RC3	18	33	37	37	ANC3	—	—	T2IN(1)	—	—	—	IOCC3	—	—	SCK1(1) SCL1(3,4)	Y	—
RC4	23	38	42	42	ANC4	—	—	—	—	—	—	IOCC4	—	—	SDI1(1) SDA1(3,4)	—	—
RC5	24	39	43	43	ANC5	—	—	T4IN(1)	—	—	—	IOCC5	—	—	—	Y	—
RC6	25	40	44	44	ANC6	—	—	—	—	—	—	IOCC6	CK1(1,3)	—	—	Y	—
RC7	26	1	1	1	ANC7	—	—	—	—	—	—	IOCC7	RX1/ DT1(1,3)	—	—	Y	—
RD0	19	34	38	38	AND0	—	—	—	—	—	—	—	—	—	—	Y	—
RD1	20	35	39	39	AND1	—	—	—	—	—	—	—	—	—	—	Y	—
RD2	21	36	40	40	AND2	—	—	—	—	—	—	—	—	—	—	Y	—
RD3	22	37	41	41	AND3	—	—	—	—	—	—	—	—	—	—	Y	—
RD4	27	2	2	2	AND4	—	—	—	—	—	—	—	—	—	—	Y	—
RD5	28	3	3	3	AND5	—	—	—	—	—	—	—	—	—	—	Y	—
RD6	29	4	4	4	AND6	—	—	—	—	—	—	—	—	—	—	Y	—
RD7	30	5	5	5	AND7	—	—	—	—	—	—	—	—	—	—	Y	—
RE0	8	23	25	25	ANE0	—	—	—	—	—	—	—	—	—	—	Y	—
RE1	9	24	26	26	ANE1	—	—	—	—	—	—	—	—	—	—	Y	—
RE2	10	25	27	27	ANE2	—	—	—	—	—	—	—	—	—	—	Y	—
RE3	1	16	18	18	—	—	—	—	—	—	—	IOCE3	—	—	—	Y	Vpp/$\overline{MCLR}$

.....continued

I/O(2)	40-Pin PDIP	40-Pin QFN	44-Pin QFN	44-Pin TQFP	A/D	Reference	Comparator	Timers	CCP	CWG	ZCD	Interrupt	EUSART	DSM	MSSP	Pull-up	Basic
V_{SS}	12	6	6	6	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
V_{DD}(5)	11	7	7	7	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
V_{DD}(5)	32	26	28	28	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
V_{SS}	31	27	30	29	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
OUT(2)	—	—	—	—	ADGRDA ADGRDB	—	C1OUT C2OUT	TMR0	CCP1 CCP2 PWM3 PWM4	CWG1A CWG1B CWG1C CWG1D	—	—	TX1/CK1(3) DT1(3) TX2/CK2(3) DT2(3)	DSM	SDO1 SCK1 SDO2 SCK2	—	—

Note:

1. This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to the peripheral input selection table for details on which port pins may be used for this signal.
2. All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in the peripheral output selection table.
3. This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4. These pins are configured for I^2C logic levels; The SCLx/SDAx signals may be assigned to any of these pins. PPS assignments to the other pins (e.g., RB1) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.
5. A 0.1 uF bypass capacitor to V_{SS} is required on all V_{DD} pins.