Ultra Large band Silicon Capacitor
ULSC424.610 (100nF / 0402 / BV=11V)

Rev 1.5 TD

General description

Market: ULSC Capacitor targets Optical communication system such as ROSA/TOSA, SONET and all optoelectronics as well as High speed data system or products.
The ULSC is suitable for DC blocking, feedback, coupling and bypassing applications in all broadband optoelectronics and High-speed data system.
The unique technology of integrated passive device in silicon, developed by Murata(*), offers unique performances with low insertion loss, low reflection and phase stability from 16 KHz to 20 GHz.
These capacitors in ultra-deep trenches in silicon have been developed in a semiconductor process, in order to integrate trench MOS capacitor providing high capacitance value of 100 nF in a SMT 0402.
The ULSC capacitor provides very high stability of the capacitance over temperature, voltage variation as well as a very high reliability.
ULSC capacitors have an extended operating temperature ranging from -55 to 150°C, with very low capacitance change over temperature (60ppm/°C).

Assembly: Flip chip or embedded applications through existing laminated packages (LGA, BGA) or rigid PCB, FR4 or flex platforms.

Copper pads optional for embedding.

Key features

- **Ultra Large band performance to 20 GHz**
- **Resonance free**
- **Phase stability**
- **Insertion low < 0.4dB Typ. up to 20 GHz**
- **Ultra-high stability of capacitance value:**
  - Temperature 60ppm/°C (-55 °C to +150 °C)
  - Voltage <0.1%/Volts
  - Negligible capacitance loss through ageing
- **Low profile:** 400µm, 100 µm on request
- **Break down voltage > 11V**
- **Low leakage current < 100pA**
- **High reliability**
- **High operating temperature** (up to 150 °C)
- **Compatible with high temperature cycling during manufacturing operations** (exceeding 300 °C)
- **Compatible with almost EIA 0402 footprint**

Key applications

- **ROSA/TOSA**
- **SONET**
- **High speed digital logic**
- **Microwave/millimeter system**
- **Volume limited applications**
- **Broadband test equipment**

(*) Murata Integrated Passive Solutions

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Functional diagram

The next figure provides implementation set-up of the capacitor (2 connections).

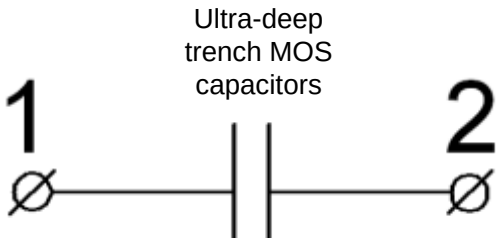


Fig.1: 100nF capacitor block diagram

Electrical performances

Performances summary

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value		-	100	-	nF
ΔC_P	Capacitance tolerance (*)		-15	-	+15	%
T_{OP}	Operating temperature		-55	20	150	°C
T_{STG}	Storage temperature (**)		-70	-	165	°C
ΔC_T	Capacitance temperature variation	-55 °C to 150 °C	-	60	-	ppm/°C
BV	Break down voltage		11	-	-	V
RV_{DC}	Rated voltage		-	-	3.8(***) 3.4(****)	V_{DC}
ΔC_{RVDC}	Capacitance voltage variation	From 0 V to RV_{DC}	-	-	0.1	$\%/V_{DC}$
IR	Insulation resistor		-	10	-	GΩ
ESR	Equivalent Serial Resistance		-	250	400	mΩ
ESL	Equivalent Serial Inductance	@ 1GHz	-	180	-	pH
Fc-3db	Cut-off frequency at 3dB		-	-	16	kHz
IL	Insertion loss	@ 20 GHz	-	-	0.4	dB
RL	Return loss	Up to 20 GHz	14	-	-	dB

Table1: 100nF capacitor performances

(*) Other capacitance tolerances upon request.

(**) only valid for components without packing

(***): 10 years of intrinsic life time predictions at 100°C

(****): 10 years of intrinsic life time predictions at 150°C

Module S-parameters of 100nF ULSC in transmission mode

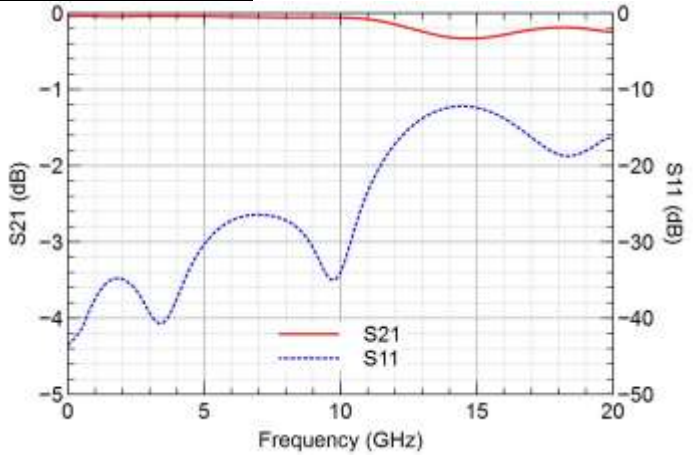


Fig.2 100nF ULSC measurement results (module of S-parameters)

Schematic of 100nF ULSC in transmission mode

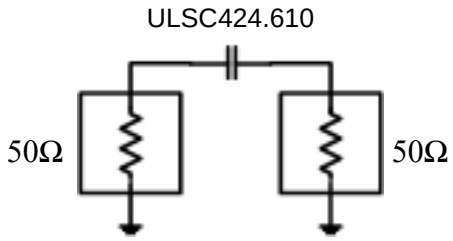


Fig.3 100nF ULSC measurement schematic

Capacitance variation versus DC biasing

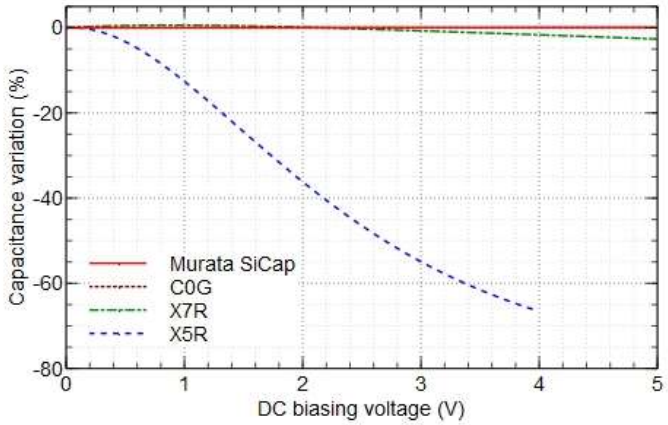


Fig. 4 Capacitance variation versus DC biasing (in function of ULSC and MLCC technology)

Capacitance variation versus operating temperature

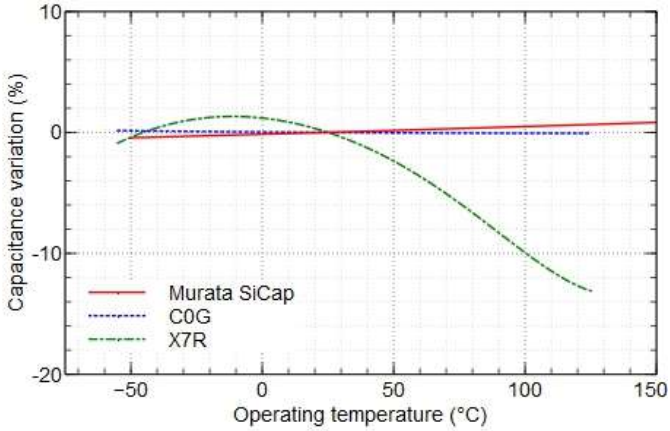


Fig.5 Capacitance variation versus operating temperature (in function of ULSC and MLCC technology)

Failure Predictions

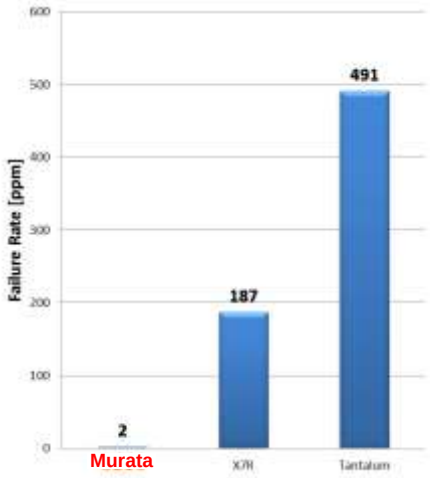
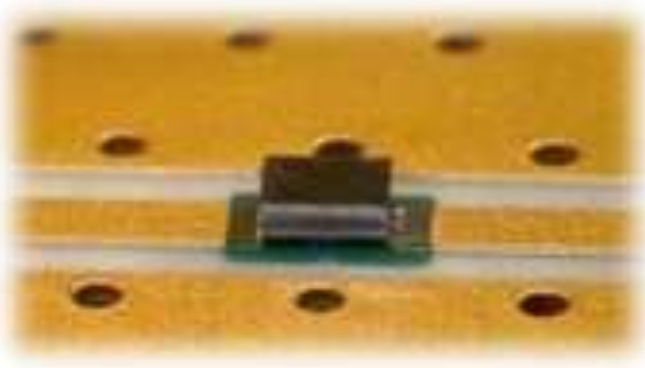


Fig. 6 Projected capacitor Failure Rate in 10 Years at 85°C and 50% of the Rating voltage (in function of ULSC, tantalum and MLCC technology)

Test bench



10-mils Rogers 4350B.
Nominal Pad dimensions –
pad length = 0.476 mm, pad width and line width = 0.551mm, pad gap = 0.246 mm.

Fig. 7 test bench picture used for 100nF ULSC characterization

Pinning definition

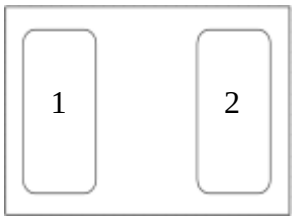


Fig.8 100nF Capacitor pin configurations

pin #	Symbol	Description
1	Signal1	Signal
2	Signal2	Signal

Table 2: Pin description

Ordering information

Type number	Package		
	ProductName	Die name	Description
935 155 424 610	ULSC424.610	-	100nF/0402/BV>11V – 2 pads – 1.2 x 0.7 x 0.40 mm
935 156 424 610	ULSC424.610	-	100nF/0402/BV>11V – 2 pads – 1.2 x 0.7 x 0.10 mm

Table 3: Die information

(*): Capacitor die dimension: 1.26 x 0.76 mm (without scribe line)

Capacitor die size after sawing : 1.2 x 0.7 mm

Scribe line = 100µm (saw lane currently used = 60µm)

Type number	Package			
	Packing	Finishing	Description	Version
935 155 424 610-F1N	6” film frame carrier(***)	ENIG(**)	0402 - 100nF – 2 pads – 1.20mm x 0.70mm x 0.40mm	1
935 155 424 610-T3N	T&R 1 000units	ENIG(**)	0402 - 100nF – 2 pads – 1.20mm x 0.70mm x 0.40mm	1
935 155 424 610-T4N	T&R 10 000units	ENIG(**)	0402 - 100nF – 2 pads – 1.20mm x 0.70mm x 0.40mm	1
935 156 424 610-F1N	6” film frame carrier(***)	ENIG(**)	0402 - 100nF – 2 pads – 1.20mm x 0.70mm x 0.10mm	1
935 156 424 610-T3N	T&R 1 000units	ENIG(**)	0402 - 100nF – 2 pads – 1.20mm x 0.70mm x 0.10mm	1
935 156 424 610-T4N	T&R 10 000units	ENIG(**)	0402 - 100nF – 2 pads – 1.20mm x 0.70mm x 0.10mm	1

Table 4: Packing ordering information

(**) ENIG : Min 0.1µm Au / 5µm Ni

(***) Other film frame carrier are possible on request

Test and Quality inspection

The Murata manufacturing center is certified:

- ISO-9001
- ISO-14001
- ISO-13485
- ISO-TS16949
- OHSAS-18001

Murata is RoHS compliant.

Mounting conditions

The ULSC Capacitor is compatible with standard reflow technology.
It is recommended to design mirror pads on the PCB.
For further information, please see our mounting application note.

Pad Metallization

The ULSC Capacitor is delivered as standard with NiAu finishing [ENIG].
Other Metallization, such as Copper, Thick Gold or Aluminum pads are possible on request.
ULSC series is compatible with standard reflow technology.
It is recommended to design mirror pads on the PCB.
For further information, please see our mounting application note.

Package outline

The ULSC Capacitor is delivered as a naked, with opening for contacts.

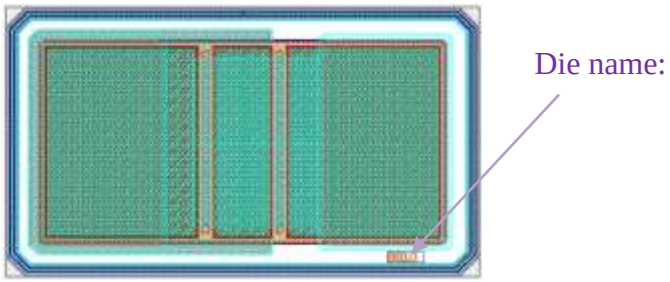
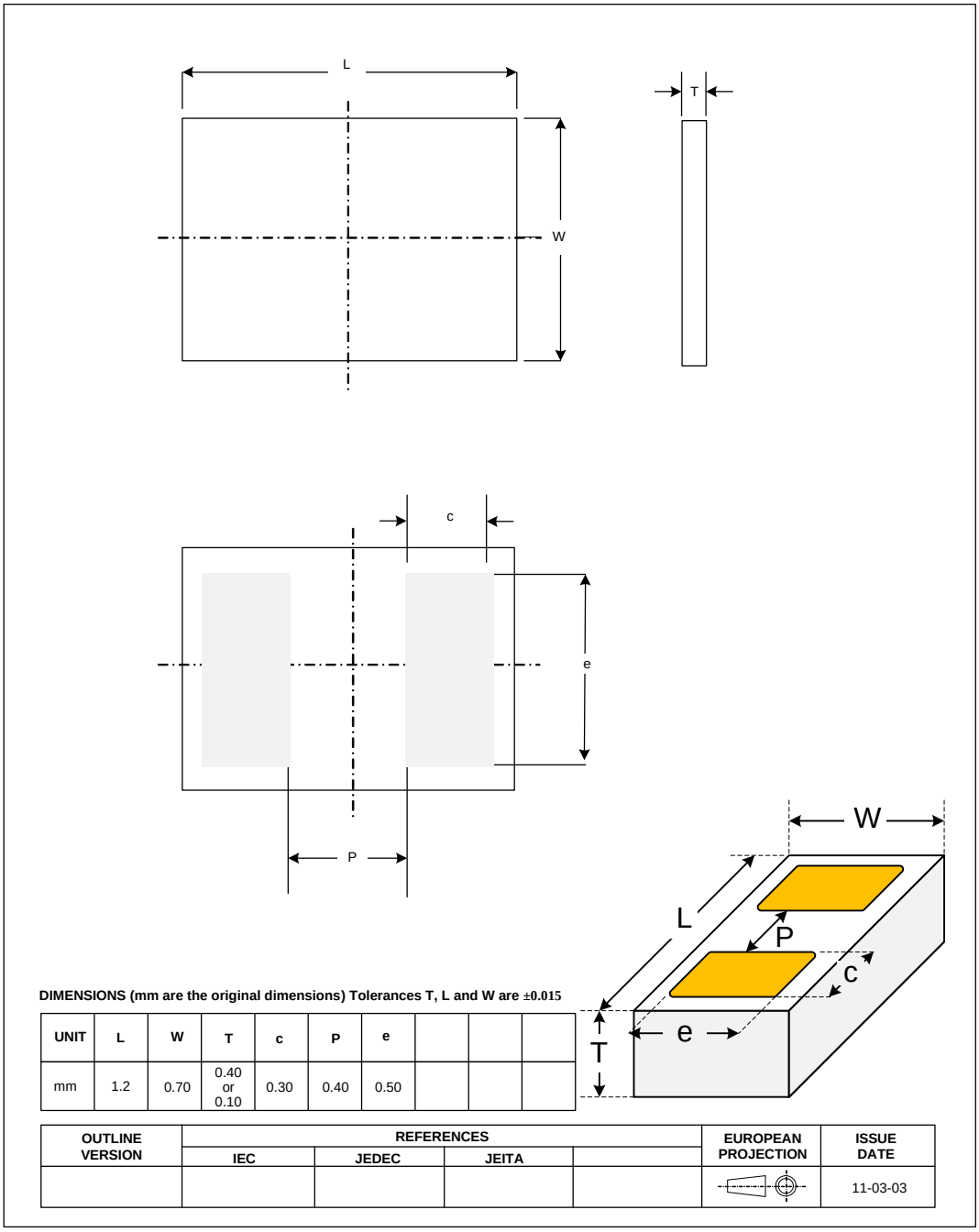


Fig.9: Micro photography of a 100 nF Capacitor



DIMENSIONS (mm are the original dimensions) Tolerances T, L and W are ±0.015

UNIT	L	W	T	c	P	e			
mm	1.2	0.70	0.40 or 0.10	0.30	0.40	0.50			

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
						11-03-03

Fig.10: Package outline 100nF Capacitor

Assembly consideration

The attachment techniques recommended by Murata for the UBSC/BBSC/ULSC capacitors silicon capacitors on the customers substrates are fully detailed in specific documents available on our website. **To assure the correct use and proper functioning of Murata capacitors please download the assembly instructions on www.ipdia.com/assembly and read them carefully.**

For UBSC/BBSC/ULSC assembly instructions @ 100 & 400 µm, please go to www.ipdia.com/assembly and download the pdf file called **'IPDiA UBSC, BBSC, ULSC-100&400µm - NiAu finishing - Assembly by Soldering'.**

Packing format

Tape and Reel format definition:

Tape Ref	Cavity dimensions			Carrier Tape width	Carrier Tape pitch	Reel size	Qty per reel
	Ao	Bo	Ko				
LO-691	0.92mm	1.31mm	0.56mm	8 mm	4mm	7”	1 000

Table 5: Tape & Reel references

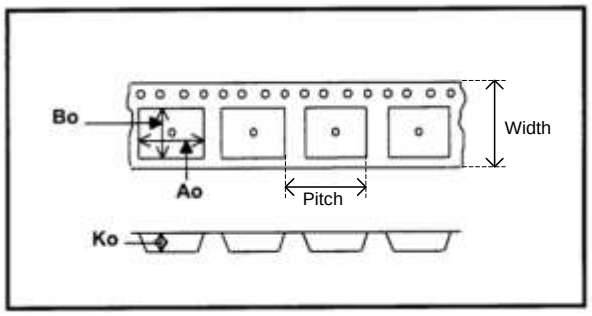


Fig. 12: Tape & Reel dimensions

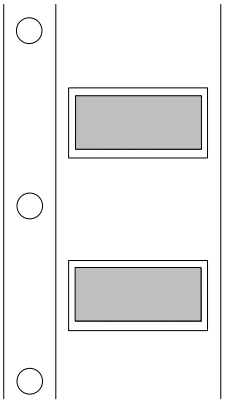


Fig. 13: Die orientation (flip) within the carrier (Pocket) related to tape and reel orientation

Tape Width	A Diameter	C	D (min)	N Hub	W1	W2 (max)
8mm	178 mm +/- 1.0	13.5 mm ± 0.5	20.2 mm	60 mm + 0.1 -0.0	93mm ± 0.5	11.5

Table 6 : Reel references used for tape width 8mm

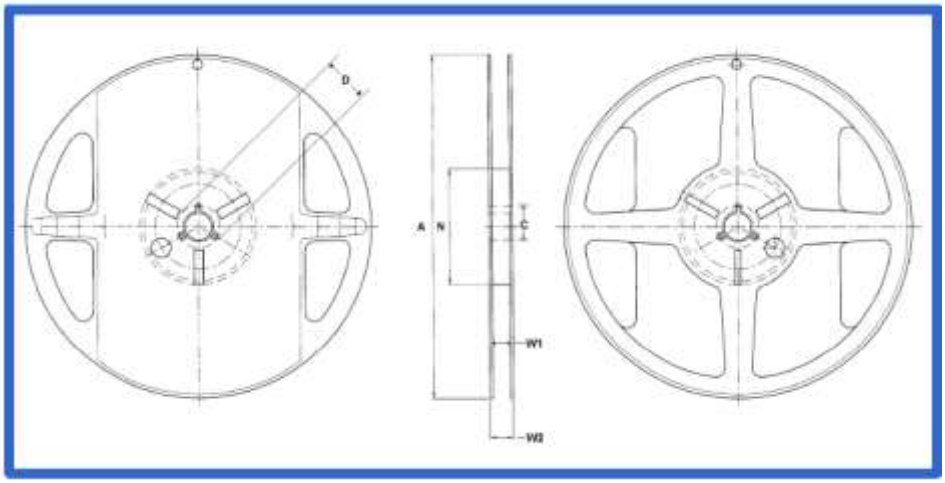


Fig. 14 : Reel references and dimensions used for tape width 8mm

Film frame carrier format definition: Ref: FF070 (Perfection products)

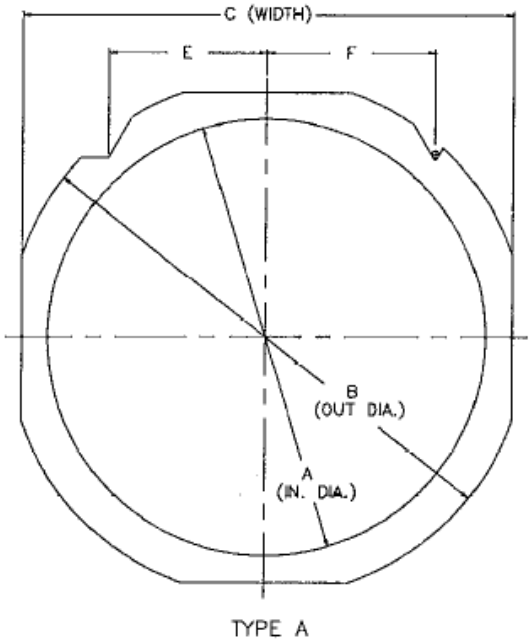


Fig.15: Dimension of film frame carrier

Wafer diameter (***)	Frame type	Inside diameter (A)	Outside diameter (B)	Width (C)	Thickness (D)	Pin location (E)	Pin location (F)	Frame style	Weight(lbs) (stainless)
6.0” (150mm)	Type A	7.639”	8.976”	8.346”	0.048	2.370”	2.500”	DTF-2-6-1	0.21

(***) other size and type on request.

Table 7: Details of film frame carrier

Waffle pack format definition: Ref: H20-052040-66C02 (Entegris) for 250µm thick

Designation	Part number	Material / Standard
Waffle pack	H20-052040-66C02	ChipSentry® (Black Conductive Polycarbonate) Pocket Dimensions: 1.32mm x 1.02mm x 0.51mm Capacity: 20x20 (400)
Pair of Waffle pack clip	H20-04-61C02	STAT-PRO 100 (Polypropylene with carbon powder)
Standard cover	H20-02-66C02	ChipSentry® (Black Conductive Polycarbonate)
Visual inspection criteria	Condition B	Standard MIL-STD-883J

Die orientation (flip) within the pocket related to waffle pack orientation

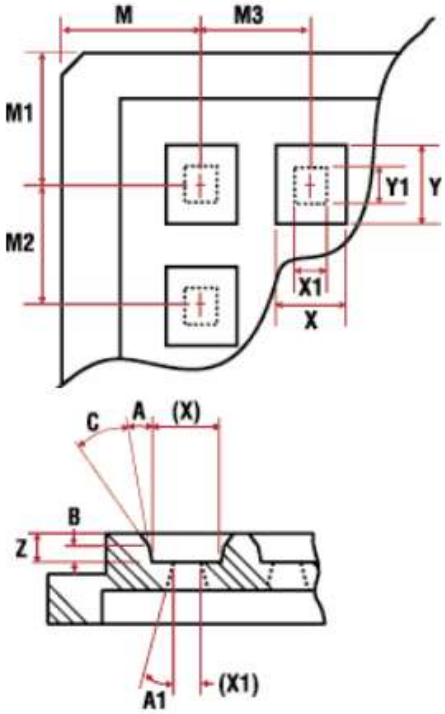


Fig.6: Dimensions of waffle pack

POCKET LOCATIONS	
M	= 4.22mm ±0.08mm
M1	= 4.22mm ±0.08mm
M2	= 2.24mm ±0.05mm
M3	= 2.24mm ±0.05mm
Array	= 20x20 (400)
POCKET DETAILS	
X	= 1.32mm ±0.05mm *pocket size*
Y	= 1.02mm ±0.05mm *pocket size*
Z	= 0.51mm ±0.05mm *pocket depth*
A	= 7° ±1/2° *pocket draft angle*
	No Cross Slots
OVERALL TRAY SIZE	
Size	= 50.80mm ±0.10mm
Height	= 3.96mm +0.05mm -0.08mm
Flatness	= 0.10mm

Table 6: Details of waffle pack

Definitions

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Revision history

Revision	Date	Description	Author
Release 1.0	**2014 February 18th**	**Objective specification**	**LDU**
Release 1.1	**2014 April 4th**	**Update**	**LDU/OGA**
Release 1.2	**2014 April 17th**	**Update of die thickness**	**LDU/OGA**
Release 1.3	**2014 May 22th**	**Packing update**	**OGA**
Release 1.4	**2014 June 17th**	**Packing update**	**OGA**
Release 1.5	**2017 July 3rd**	**Murata version**	**OGA**

Life Support Applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Murata customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Murata for any damages resulting from such improper use or sale.