Broadband Silicon Capacitor
BBSC722.410 (1nF / 0201M / BV30V)

Rev 1.5 TD

General description

BBSC Capacitor targets Optical communication system such as ROSA/TOSA, SONET and all optoelectronics as well as High speed data system or products.
The BBSC is suitable for DC blocking, feedback, coupling and bypassing applications in all broadband optoelectronics and High-speed data system.
The unique technology of integrated passive device in silicon, developed by Murata(*), offers unique performances with low insertion loss, low reflection and phase stability from 1.60 MHz to 40 GHz.
These Broadband MOS Silicon Capacitors (BBSC) in silicon have been developed in a semiconductor process, in order to combine ultra-deep trench MOS capacitors for high capacitance value of 1 nF (for kHz–MHz range) and MIM capacitors for low capacitance value for GHz range), both in a SMT 0201M (0.6 x 0.3mm).
The BBSC capacitor provides very high stability of the capacitance over temperature, voltage variation as well as a very high reliability.
BBSC capacitors have an extended operating temperature ranging from -55 to 150°C, with very low capacitance change over temperature (60ppm/°C)

Assembly: flip chip applications through existing laminated packages or rigid PCB, ceramic substrate, FR4 or flex platforms suitable.

Please refer to our assembly application note for further recommendations.

Bump finishing: SAC305 type 6

Key features

- **Broadband performance to 40GHz**
- **Resonance free**
- **Phase stability**
- **Insertion low < 0.3dB Typ.**
- **Ultra-high stability of capacitance value:**
  - Temperature 60ppm/°C (-55 °C to +150 °C)
  - Voltage <0.1%/Volts
  - Negligible capacitance loss through ageing
- **Low profile:** 140 µm including bump height
- **Break down voltage > 30V**
- **Low leakage current**
- **High reliability**
- **High operating temperature** (up to 150 °C)
- **Compatible with high temperature cycling during manufacturing operations** (exceeding 300 °C)
- **Compatible with EIA 0201 footprint**
- **SAC305 40µm bumps after reflow**

Key applications

- **ROSA/TOSA**
- **SONET**
- **High speed digital logic**
- **Microwave/millimeter system**
- **Volume limited applications**
- **Broadband test equipment**

(*) Murata Integrated Passive Solutions

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Functional diagram

The next figure provides implementation set-up of the capacitor (2 connections).

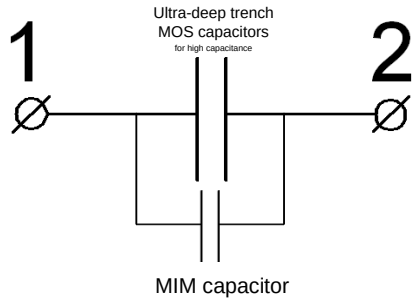


Fig. 1: 1nF/0201M BBSC capacitor block diagram

Electrical performances

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@ 25°C	-	1	-	nF
ΔC_P	Capacitance tolerance		-15	-	+15(*)	%
T_{OP}	Operating temperature		-55	20	150	°C
T_{STG}	Storage temperature(**)		-70	-	165	°C
ΔC_T	Capacitance temperature variation	-55 °C to 150 °C	-	60	-	ppm/°C
BV	Break down voltage	@ 25°C	30	-	-	V
RV_{DC}	Rated voltage		-	10	16(***) 13.6(****)	V_{DC}
ΔC_{RVDC}	Capacitance voltage variation	From 0 V to RV_{DC}	-	-	0.1	$\%/V_{DC}$
IR	Insulation resistor	@ 25°C & RV_{DC}	-	10	-	GΩ
Fc-3db	Cut-off frequency at 3dB		-	-	1.6	MHz
IL	Insertion loss	@ 20 GHz	-	0.2	-	dB
		@ 40GHz	-	0.3	-	dB
RL	Return loss	Up to 40 GHz	22	-	-	dB

Table 1: 1nF/0201M BBSC capacitor performances

(*) Other capacitance tolerances upon request.

(**) component without packing.

(***) 10 years of intrinsic life time predictions at 100°C

(****) 10 years of intrinsic life time predictions at 150°C

Module S-parameters of 1nF BBSC in transmission mode

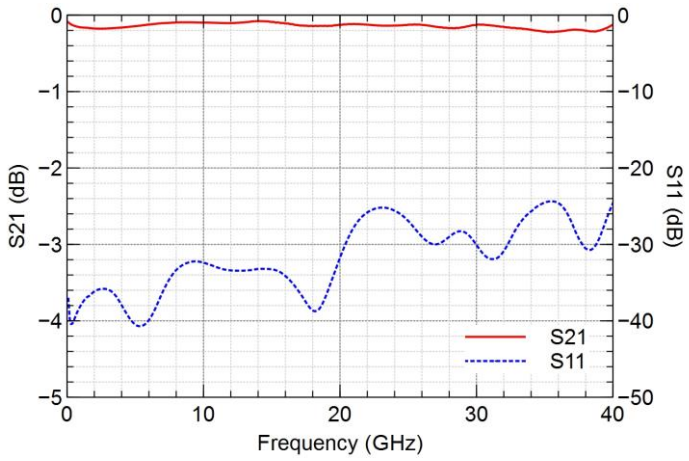
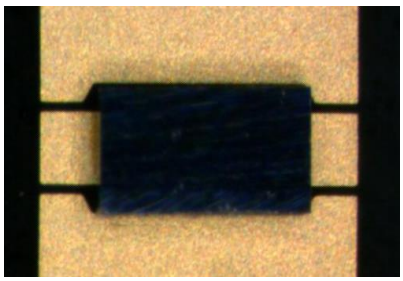
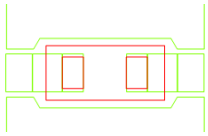


Fig. 2 1nF BBSC measurement results (module of S-parameters)

Test bench board





Red: Part outline
Green: Fixture outline

10-mil thick Quartz substrate using coplanar waveguide (CPW) environment. The CPW test fixture was designed with a 200um gap between the mounting pads and a 180um wide center trace matched to the capacitor's termination width with access line of 50 Ohm characteristic impedance

Fig. 3 test bench picture used for 1nF BBSC characterization

Capacitance variation versus DC biasing

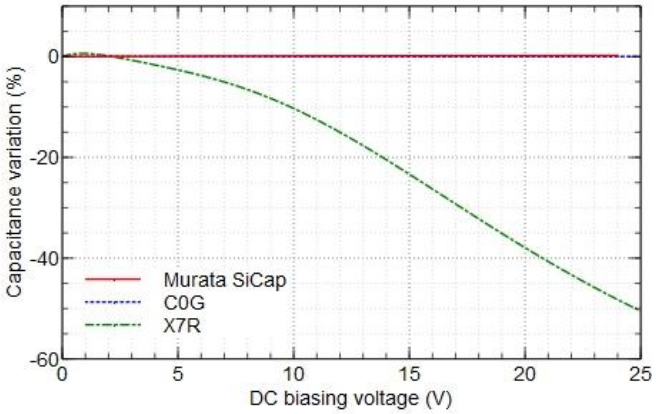


Fig. 4 Capacitance variation versus DC biasing (in function of BBSC and MLCC technology)

Capacitance variation versus operating temperature

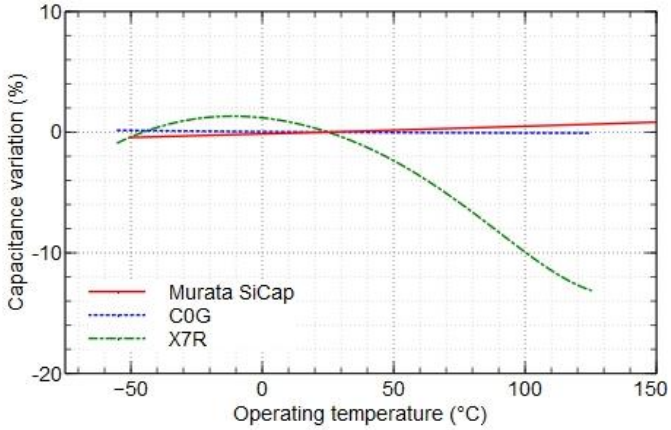


Fig.5 Capacitance variation versus operating temperature (in function of BBSC and MLCC technology)

Failure Predictions

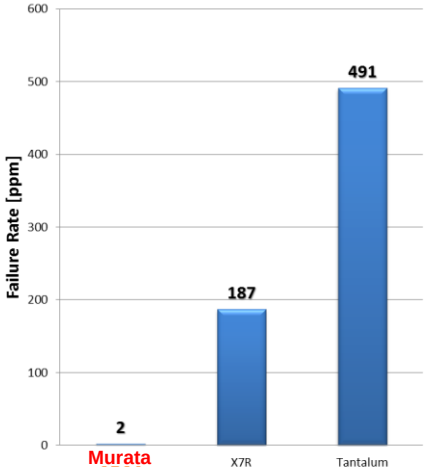


Fig. 6 Projected capacitor Failure Rate in 10 Years at 85°C and 50% of the Rating voltage (in function of BBSC, tantalum and MLCC technology)

Schematic of 1nF BBSC in transmission mode

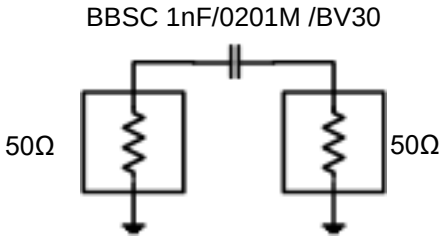


Fig.7 1nF BBSC measurement schematic

Pinning definition

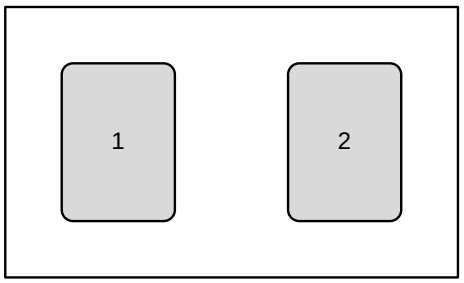


Fig. 8: 1nF Capacitor pin configurations

pin #	Symbol	Description
1	Signal1	Signal
2	Signal2	Signal

Table 2: Pin description

Ordering information

Type number	Package		
	P/N	Die name	Description
939 114 722 410	BBSC722.410	-	1nF / 0201M / BV>30V – 2 pads – 0.6 x 0.3 x 0.14 mm(*)

Table 3: Die information

(*): Capacitor die dimension: 0.56 x 0.26 mm (without scribe line)

Capacitor die size after sawing: 0.6 x 0.3 mm

Scribe line = 80µm (saw lane currently used = 40µm)

Type number	Package		
	Packing	Finishing	Description
939 114 722 410-F1S	6” film frame carrier	SAC(**)	0201M - 1nF – 2 pads – 0.6 x 0.3 mm x 0.14mm

Table 4: Packing ordering information

(**) ENIG+ SAC305 type 6

Test and Quality inspection

The Murata manufacturing center is certified:

- ISO-9001
- ISO-14001
- ISO-13485
- ISO-TS16949
- OHSAS-18001

Murata is RoHS compliant.

Mounting conditions

The BBSC Capacitor is compatible with standard reflow technology.
It is recommended to design mirror pads on the PCB.
For further information, please see our mounting application note.

Pad Metallization

The BBSC Capacitor is delivered as standard with SAC305 bumping.
Other Metallization, such as ENIG, Copper, Thick Gold or Aluminum pads are possible on request.
BBSC series is compatible with standard reflow technology.

Package outline

The BBSC Capacitor is delivered as a naked die, with bumps.

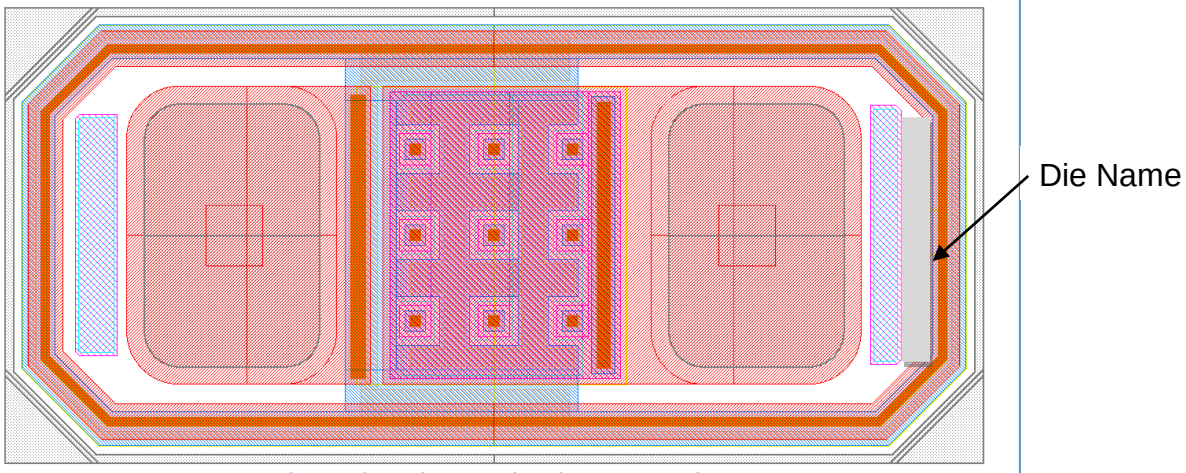
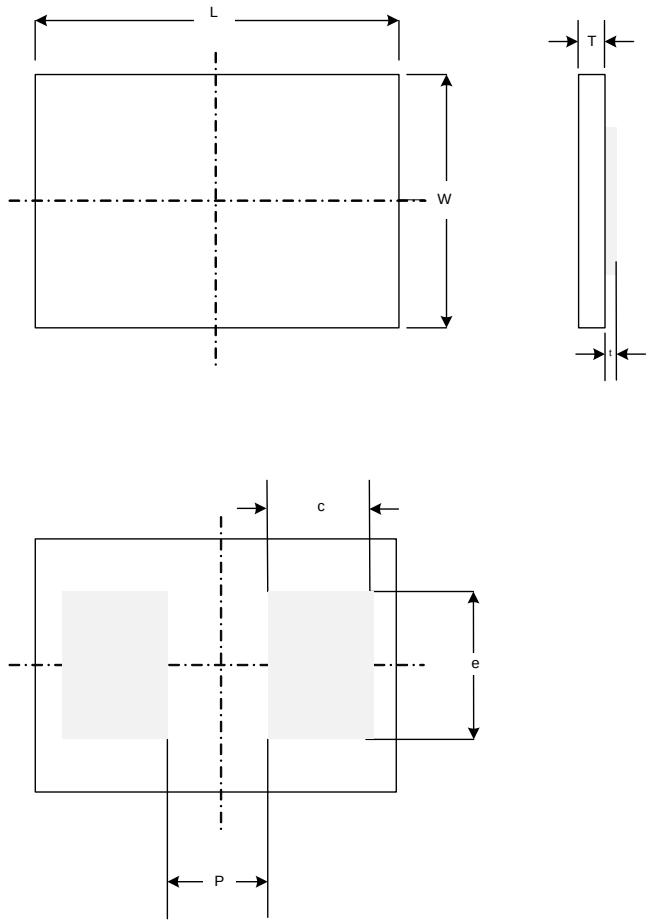


Fig. 9: Micro photography of a 1nF Capacitor



(*): solder joint height after reflow on board.
Tolerances L and W are ±0.015mm.
Tolerance T is ±0.01mm

DIMENSIONS (mm are the original dimensions).

UNIT	L	W	T	c	P	e	t		
mm	0.60	0.30	0.10	0.1	0.20	0.15	0.04(*)		

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			14-06-24

Fig. 10: Package outline 1nF Capacitor

Assembly consideration

The attachment techniques recommended by Murata for the 1/BBSC/ULSC capacitors silicon capacitors on the customers substrates are fully detailed in specific documents available on our website. **To assure the correct use and proper functioning of Murata capacitors please download the assembly instructions on www.ipdia.com/assembly and read them carefully.**

For UBSC/BBSC/ULSC assembly instructions @ 100 & 400 µm, please go to www.ipdia.com/assembly and download the pdf file called **‘‘Murata UBSC, BBSC, ULSC- 100&400µm - NiAu finishing - Assembly by Soldering’.**

Packing format

Film frame carrier format definition: Ref: FF070 (Perfection products)

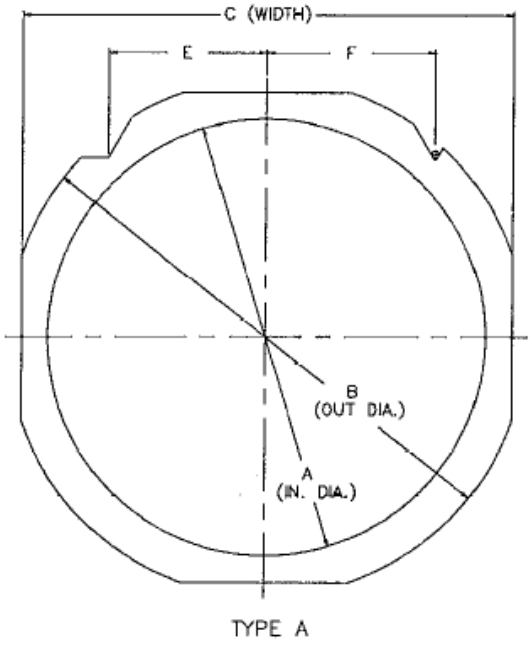


Fig. 11: Dimension of film frame carrier

Wafer diameter (***)	Frame type	Inside diameter (A)	Outside diameter (B)	Width (C)	Thickness (D)	Pin location (E)	Pin location (F)	Frame style	Weight(lbs) (stainless)
6.0” (150mm)	Type A	7.639”	8.976”	8.346”	0.048	2.370”	2.500”	DTF-2-6-1	0.21

(***) other size and type on request.

Table 5: Details of film frame carrier

Definitions

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Revision history

Revision	Date	Description	Author
Release 1.0	**2016 June 28th**	**Objective specification**	**OGA**
Release 1.1	**2016 Sept 22nd**	**Preliminary specification**	**LLR/NNO**
Release 1.2	**2016 Sept 29th**	**Packing update**	**OGA**
Release 1.3	**2017 March 27th**	**Packing update**	**OGA**
Release 1.4	**2017 April 4th**	**Murata version**	**OGA**
Release 1.5	**2017 June 9th**	**Rated voltage update**	**OGA**

Life Support Applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Murata customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Murata for any damages resulting from such improper use or sale.

For more information, please visit: http://www.murata.com
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