

**GENERAL DESCRIPTION**

The MYRGP-W/MYRGP-B series is a synchronous step-down micro DC/DC converter which integrates an inductor and a control IC in one tiny package (2.0mm×2.5mm, h=1.0mm). An internal coil simplifies the circuit and enables minimization of noise and other operational trouble due to the circuit wiring. A wide operating voltage range of 2.5V to 5.5V enables support for applications that require an internally fixed output voltage (0.8V to 3.6V). The MYRGP-W/MYRGP-B series use synchronous rectification at an operating frequency of 3.0MHz. The MYRGP-W/MYRGP-B series use High Speed Transient Response -COT synchronous rectification.



PWM control (MYRGP-W) or PWM/PFM switching control (MYRGP-B) automatic can be selected.

The series have a high speed soft-start as fast as 0.3ms in typical for quick turn-on. With the built-in UVLO (Under Voltage Lock Out) function, the internal P-channel driver transistor is forced OFF when input voltage becomes 2.0V or lower. When CE=Low, the integrated C<sub>L</sub> discharge function which enables the electric charge at the output capacitor C<sub>L</sub> to be discharged via the internal discharge switch located between the L<sub>x</sub> and V<sub>SS</sub> pins. The power consumption will be less than 1.0μA.

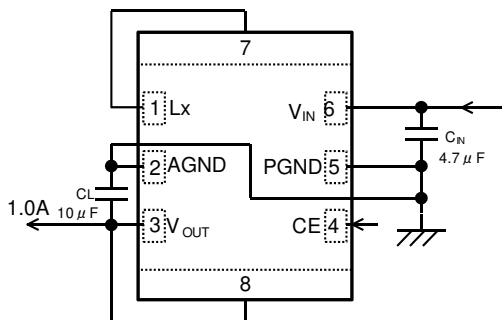
**APPLICATIONS**

- Note Book PC
- Tablet PC
- SSD(Solid State Drive)
- Mobile phone
- Digital still camera
- Portable game machine

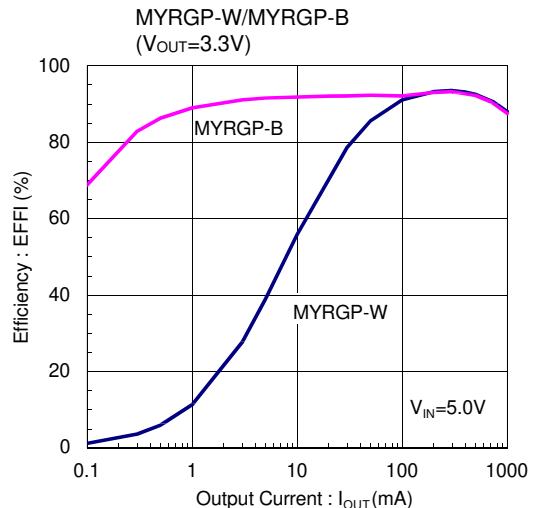
**FEATURES**

Input Voltage	: 2.5V~5.5V
Output Voltage	: 0.8V~3.6V(±2.0%)
Switching Frequency	: 3.0MHz
Output Current	: 1.0A
Efficiency	: 93% (V <sub>IN</sub> =5.0V, V <sub>OUT</sub> =3.3V/300mA)
Control Methods	: High Speed Transient Response -COT 100% Duty Cycle PWM (MYRGP-W) PWM/PFM (MYRGP-B)
Circuit Protection	: Thermal Shut Down Current Limit Circuit (Drop) Short Circuit Protection (Latch)
Functions	: Soft-start Circuit Built-in UVLO C <sub>L</sub> Discharge
Output Capacitor	: Low ESR Ceramic Capacitor
Operating Ambient Temperature	: -40°C~+105°C
Environmentally Friendly	: EU RoHS Compliant, Pb Free Halogen Free

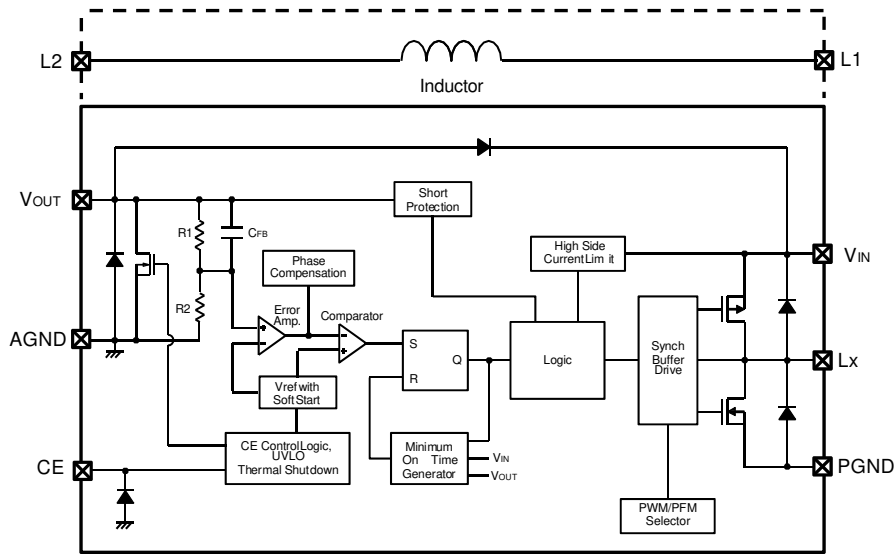
**TYPICAL APPLICATION CIRCUIT**



**TYPICAL PERFORMANCE CHARACTERISTICS**

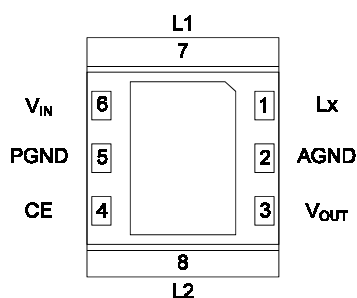


■ BLOCK DIAGRAM



\* The MYRGP-W offers a fixed PWM control, a Control Logic of PWM/PFM Selector is fixed at “PWM” internally.  
The MYRGP-B control scheme is a fixed PWM/PFM automatic switching, a Control Logic of PWM/PFM Selector is fixed at “PWM/PFM automatic switching” internally.  
Diodes inside the circuit are an ESD protection diode and a parasitic diode.

### ■ PIN CONFIGURATION



BOTTOM VIEW

- \* It should be connected the pin No.2 and 5 to the GND pin.
- \* If the dissipation pad needs to be connected to other pins, it should be connected to the GND pin.
- \* Please refer to pattern layout page for the connecting to PCB.

### ■ PIN ASSIGNMENT

PIN NUMBER	PIN NAME	FUNCTIONS
1	Lx	Switching Output
2	AGND	Analog Ground
3	V <sub>OUT</sub>	Fixed Output Voltage PIN
4	CE	Chip Enable
5	PGND	Power Ground
6	V <sub>IN</sub>	Power Input
7	L1	Inductor Electrodes
8	L2	Inductor Electrodes

### ■ FUNCTION TABLE

CE PIN Function

PIN NAME	SIGNAL	STATUS
CE	Low	Stand-by
	High	Active

\* Please do not leave the CE pin open.

### ■ ABSOLUTE MAXIMUM RATINGS

Ta=25°C			
PARAMETER	SYMBOL	RATINGS	UNITS
V <sub>IN</sub> Pin Voltage	V <sub>IN</sub>	-0.3 ~ +6.2	V
Lx Pin Voltage	V <sub>Lx</sub>	- 0.3 ~ V <sub>IN</sub> + 0.3 or + 6.2 <sup>(1)</sup>	V
V <sub>OUT</sub> Pin Voltage	V <sub>out</sub>	- 0.3 ~ V <sub>IN</sub> + 0.3 or + 4.0 <sup>(2)</sup>	V
CE Pin Voltage	V <sub>CE</sub>	- 0.3 ~ +6.2	V
Power Dissipation	P <sub>d</sub>	1000 <sup>(3)</sup>	mW
Operating Ambient Temperature	T <sub>opr</sub>	- 40 ~ + 105	°C
Storage Temperature	T <sub>stg</sub>	- 55 ~ + 125	°C

All voltages are described based on the GND (AGND and PGND) pin.

<sup>(1)</sup> The maximum value should be either V<sub>IN</sub>+0.3 or +6.2 in the lowest voltage

<sup>(2)</sup> The maximum value should be either V<sub>IN</sub>+0.3 or +4.0 in the lowest voltage

<sup>(3)</sup> The power dissipation figure shown is PCB mounted (40mm×40mm, t=1.6mm, Glass Epoxy FR-4).

Please refer to page 11 for details.

### ■ ELECTRICAL CHARACTERISTICS

#### ● MYRGP-W/MYRGP-B

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Output Voltage	V <sub>OUT</sub>	When connected to external components, I <sub>OUT</sub> =30mA	<E-1>	<E-2>	<E-3>	V	①
Operating Voltage Range	V <sub>IN</sub>		2.5	-	5.5	V	①
Maximum Output Current	I <sub>OUTMAX</sub>	When connected to external components, V <sub>IN</sub> =<C-1>	1000	-	-	mA	①
UVLO Voltage <sup>(2)</sup>	V <sub>UVLO</sub>	V <sub>OUT</sub> =0.6V, Voltage which Lx pin holding "L" level <sup>(6)</sup>	1.35	2	2.48	V	③
Quiescent Current (MYRGP-B)	I <sub>q</sub>	V <sub>OUT</sub> =V <sub>OUT(E)</sub> × 1.1V	-	25	40	μA	②
Quiescent Current (MYRGP-W)	I <sub>q</sub>	V <sub>OUT</sub> =V <sub>OUT(E)</sub> × 1.1V	-	400	825	μA	②
Stand-by Current	I <sub>STB</sub>	V <sub>CE</sub> =0V	-	0	1	μA	②
Minimum ON time <sup>(2)</sup>	t <sub>ONmin</sub>	When connected to external components, V <sub>IN</sub> =V <sub>CE</sub> =<C-1>, I <sub>OUT</sub> =1mA	<E-5>	<E-6>	<E-7>	ns	①
Thermal Shutdown	T <sub>TSD</sub>		-	150	-	°C	①
Thermal shutdown Hysteresis	T <sub>HYS</sub>		-	30	-	°C	①
LxSW "H" ON Resistance	R <sub>LXH</sub>	V <sub>OUT</sub> =0.6V, I <sub>LX</sub> =100mA <sup>(3)</sup>	-	0.24	0.37	Ω	④
LxSW "L" ON Resistance <sup>(4)</sup>	R <sub>LXL</sub>	V <sub>OUT</sub> =V <sub>OUT(T)</sub> × 1.1V, I <sub>LX</sub> =100mA <sup>(3)</sup>	-	0.16	0.3	Ω	④
LxSW "H" Leakage Current	I <sub>LeakH</sub>	V <sub>IN</sub> =5.5V, V <sub>CE</sub> =0V, V <sub>OUT</sub> =0V, V <sub>LX</sub> =5.5V	-	0	30	μA	⑤
LxSW "L" Leakage Current	I <sub>LeakL</sub>	V <sub>IN</sub> =5.5V, V <sub>CE</sub> =0V, V <sub>OUT</sub> =0V, V <sub>LX</sub> =0V	-	0	1	μA	⑤
Current Limit <sup>(5)</sup>	I <sub>LIMH</sub>	V <sub>OUT</sub> =0.6V, I <sub>LX</sub> until Lx pin oscillates	1.3	1.5	2.5	A	⑥
Output Voltage Temperature Characteristics	ΔV <sub>OUT</sub> / (V <sub>OUT</sub> · Δtopr)	I <sub>OUT</sub> =30mA, -40°C ≤ T <sub>opr</sub> ≤ 85°C	-	±100	-	ppm/°C	①
CE"H" Voltage	V <sub>CEH</sub>	V <sub>OUT</sub> =0.6V, Applied voltage to V <sub>CE</sub> , Voltage changes Lx to "H" level <sup>(6)</sup>	1.4	-	5.5	V	③
CE"L" Voltage	V <sub>CEL</sub>	V <sub>FB</sub> =0.6V, Applied voltage to V <sub>CE</sub> , Voltage changes Lx to "L" level <sup>(6)</sup>	AGND	-	0.3	V	③
CE"H" Current	I <sub>CEH</sub>	V <sub>IN</sub> =5.5V, V <sub>CE</sub> =5.5V, V <sub>OUT</sub> =0V	-0.1	-	0.1	μA	⑤
CE"L" Current	I <sub>CEL</sub>	V <sub>IN</sub> =5.5V, V <sub>CE</sub> =0V, V <sub>OUT</sub> =0V	-0.1	-	0.1	μA	⑤
Soft-start Time	t <sub>SS</sub>	After "H" is fed to CE, the time by which clocks are generated at Lx pin.	0.1	0.3	0.5	ms	③
Short Protection Threshold Voltage	V <sub>SHORT</sub>	Sweeping V <sub>OUT</sub> , V <sub>OUT</sub> voltage which Lx becomes "L" level <sup>(6)</sup>	0.17	0.27	0.37	V	③
C <sub>L</sub> Discharge	R <sub>DCHG</sub>	V <sub>CE</sub> =0V, V <sub>OUT</sub> =4.0V	50	210	300	Ω	⑦
Inductance	L	Test Freq.=1MHz	-	1	-	μH	-
Inductor Rated Current	I <sub>DC</sub>	ΔT=+40deg	-	1.3	-	A	-

Unless otherwise stated, V<sub>IN</sub>=5.0V, V<sub>CE</sub>=5.0V, V<sub>OUT(T)</sub>=Nominal Voltage  
NOTE:

<sup>(1)</sup> When the difference between the input and the output is small, 100% duty might come up and internal control circuits keep P-ch driver turning on even though the output current is not so large.

If current is further pulled from this state, output voltage will decrease because of P-ch driver ON resistance.

<sup>(2)</sup> Including UVLO detect voltage, hysteresis operating voltage range for UVLO release voltage.

<sup>(3)</sup> R<sub>LXH</sub>=(V<sub>IN</sub> - Lx pin measurement voltage) / 100mA, R<sub>LXL</sub>=Lx pin measurement voltage / 100mA <sup>(4)</sup> Design value for the MYRGP-B series

<sup>(5)</sup> Current limit denotes the level of detection at peak of coil current.

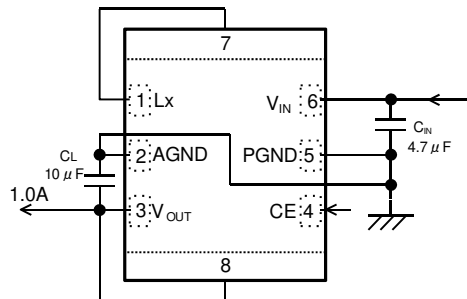
<sup>(6)</sup> "H"=V<sub>IN</sub> - V<sub>IN</sub> - 1.2V, "L"=- 0.1V ~ + 0.1V

**■ ELECTRICAL CHARACTERISTICS**

●SPEC Table (V<sub>OUT</sub>, t<sub>ONmin</sub>)

NOMINAL OUTPUT VOLTAGE	V <sub>OUT</sub>			t <sub>ONmin</sub> f <sub>osc</sub> =3.0MHz				NOMINAL OUTPUT VOLTAGE	V <sub>OUT</sub>			t <sub>ONmin</sub> f <sub>osc</sub> =3.0MHz			
	<E-1>	<E-2>	<E-3>	<C-1>	<E-5>	<E-6>	<E-7>		<E-1>	<E-2>	<E-3>	<C-1>	<E-5>	<E-6>	<E-7>
	V <sub>OUT(T)</sub>	MIN.	TYP.	MAX.	V <sub>IN</sub>	MIN.	TYP.		MAX.	V <sub>OUT(T)</sub>	MIN.	TYP.	MAX.	V <sub>IN</sub>	MIN.
0.80	0.784	0.800	0.816	2.70	71	119	166	2.25	2.205	2.250	2.295	3.75	140	200	260
0.85	0.833	0.850	0.867	2.70	72	121	169	2.30	2.254	2.300	2.346	3.83	140	200	260
0.90	0.882	0.900	0.918	2.70	73	122	171	2.35	2.303	2.350	2.397	3.92	140	200	260
0.95	0.931	0.950	0.969	2.70	74	123	172	2.40	2.352	2.400	2.448	4.00	140	200	260
1.00	0.980	1.000	1.020	2.70	86	123	160	2.45	2.401	2.450	2.499	4.08	140	200	260
1.05	1.029	1.050	1.071	2.70	91	130	169	2.50	2.450	2.500	2.550	4.17	140	200	260
1.10	1.078	1.100	1.122	2.70	95	136	177	2.55	2.499	2.550	2.601	4.25	140	200	260
1.15	1.127	1.150	1.173	2.70	99	142	185	2.60	2.548	2.600	2.652	4.33	140	200	260
1.20	1.176	1.200	1.224	2.70	104	148	193	2.65	2.597	2.650	2.703	4.42	140	200	260
1.25	1.225	1.250	1.275	2.70	108	154	201	2.70	2.646	2.700	2.754	4.50	140	200	260
1.30	1.274	1.300	1.326	2.70	112	160	209	2.75	2.695	2.750	2.805	4.58	140	200	260
1.35	1.323	1.350	1.377	2.70	117	167	217	2.80	2.744	2.800	2.856	4.67	140	200	260
1.40	1.372	1.400	1.428	2.70	121	173	225	2.85	2.793	2.850	2.907	4.75	140	200	260
1.45	1.421	1.450	1.479	2.70	125	179	233	2.90	2.842	2.900	2.958	4.83	140	200	260
1.50	1.470	1.500	1.530	2.70	130	185	241	2.95	2.891	2.950	3.009	4.92	140	200	260
1.55	1.519	1.550	1.581	2.70	134	191	249	3.00	2.940	3.000	3.060	5.00	140	200	260
1.60	1.568	1.600	1.632	2.70	138	198	257	3.05	2.989	3.050	3.111	5.08	140	200	260
1.65	1.617	1.650	1.683	2.75	140	200	260	3.10	3.038	3.100	3.162	5.17	140	200	260
1.70	1.666	1.700	1.734	2.83	140	200	260	3.15	3.087	3.150	3.213	5.25	140	200	260
1.75	1.715	1.750	1.785	2.92	140	200	260	3.20	3.136	3.200	3.264	5.33	140	200	260
1.80	1.764	1.800	1.836	3.00	140	200	260	3.25	3.185	3.250	3.315	5.42	140	200	260
1.85	1.813	1.850	1.887	3.08	140	200	260	3.30	3.234	3.300	3.366	5.50	140	200	260
1.90	1.862	1.900	1.938	3.17	140	200	260	3.35	3.283	3.350	3.417	5.50	142	203	264
1.95	1.911	1.950	1.989	3.25	140	200	260	3.40	3.332	3.400	3.468	5.50	144	206	268
2.00	1.960	2.000	2.040	3.33	140	200	260	3.45	3.381	3.450	3.519	5.50	146	209	272
2.05	2.009	2.050	2.091	3.42	140	200	260	3.50	3.430	3.500	3.570	5.50	148	212	276
2.10	2.058	2.100	2.142	3.50	140	200	260	3.55	3.479	3.550	3.621	5.50	151	215	280
2.15	2.107	2.150	2.193	3.58	140	200	260	3.60	3.528	3.600	3.672	5.50	153	218	284
2.20	2.156	2.200	2.244	3.67	140	200	260								

**■ TYPICAL CIRCUIT**



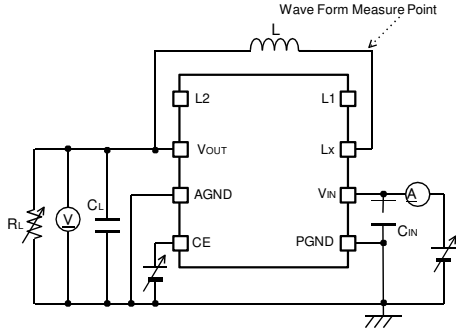
PARAMETER	VALUE
C <sub>IN</sub>	10V/4.7µF
C <sub>L</sub>	10V/10µF

**NOTE:**

The integrated Inductor can be used only for this DC/DC converter. Please do not use this inductor for other reasons.

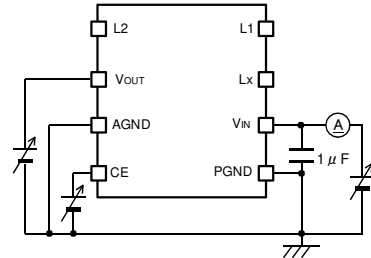
■ TEST CIRCUITS

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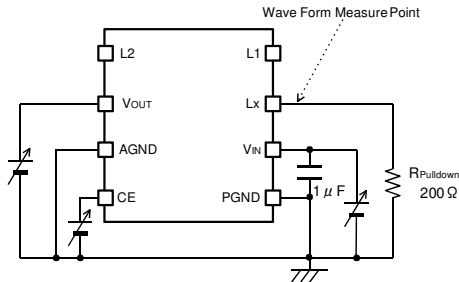


※External Components L :  
1.0  $\mu$  H (Selected goods)  
CIN : 4.7  $\mu$  F (Ceramic)  
CL : 10  $\mu$  F (Ceramic)

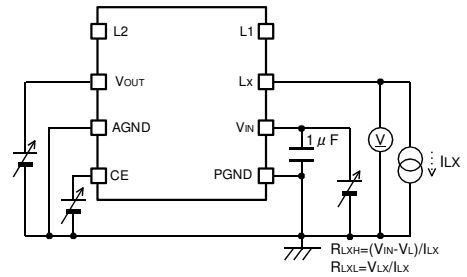
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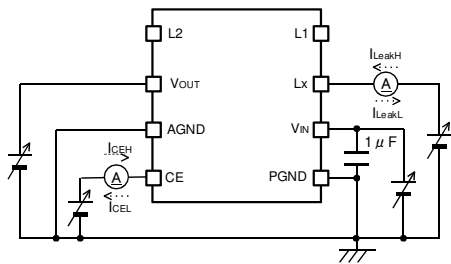
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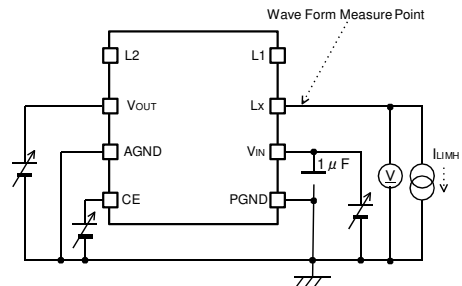
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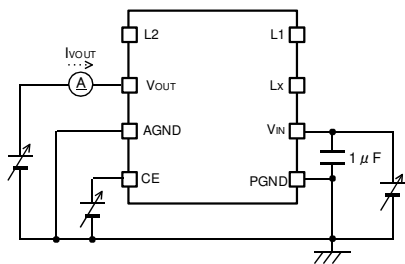
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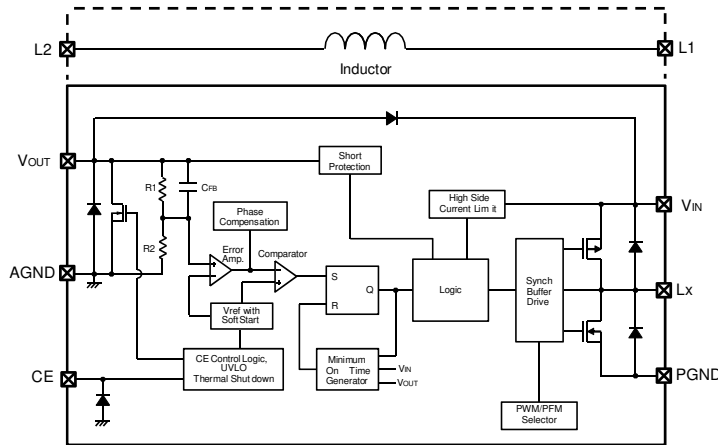


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**OPERATIONAL EXPLANATION**

The MYRGP-W/MYRGP-B series consists of a reference voltage source, error amplifier, comparator, phase compensation, minimum on time generation circuit, output voltage adjustment resistors, P-channel MOS driver transistor, N-channel MOS switching transistor for the synchronous switch, current limiter circuit, UVLO circuit, thermal shutdown circuit, short protection circuit, PWM/PFM selection circuit and others. (See the BLOCK DIAGRAM below.)



<BLOCK DIAGRAM>

The method is High Speed circuit Architecture for Transient with Constant On Time control, which features on time control method and a fast transient response that also achieves low output voltage ripple. The on time ( $t_{on}$ ) is determined by the input voltage and output voltage, and turns on the Pch MOS driver Tr. for a fixed time. During the off time ( $t_{off}$ ), the voltage that is fed back through R1 and R2 is compared to the reference voltage by the error amp, and the error amp output is phase compensated and sent to the comparator. The comparator compares this signal to the reference voltage, and if the signal is lower than the reference voltage, sets the SR latch. On time then resumes. By doing this, PWM operation takes place with the off time controlled to the optimum duty ratio and the output voltage is stabilized. The phase compensation circuit optimizes the frequency characteristics of the error amp, and generates a ramp wave similar to the ripple voltage that occurs in the output to modulate the output signal of the error amp. This enables a stable feedback system to be obtained even when a low ESR capacitor such as a ceramic capacitor is used, and a fast transient response and stabilization of the output voltage are achieved.

<Minimum on time generation circuit>

Generates an on time that depends on the input voltage and output voltage ( $t_{on}$ ). The on time is set as given by the equations below.

$$t_{on} (ns) = V_{OUT}/V_{IN} \times 333$$

<Switching frequency>

The switching frequency can be obtained from the on time ( $t_{on}$ ), which is determined by the input voltage and output voltage, as given by the equation below.

$$f_{osc} (MHz) = V_{OUT}(V) / (V_{IN}(V) \times t_{on}(ns))$$

<100% duty cycle mode>

When the load current is heavy and the voltage difference between input voltage and output voltage is small, 100% duty cycle mode is activated and it keeps the Pch MOS driver Tr. turning on. 100% duty cycle mode attains a high output voltage stability and a high-speed response under all load conditions, from light to heavy, even in conditions where the dropout voltage is low.

<Error amp>

The error amp monitors the output voltage. The voltage divided by the internal R1 and R2 resistors is a feedback voltage for Error Amp. and compared to the reference voltage. The output voltage of the error amp becomes higher when the feedback voltage is higher than the reference voltage. The frequency characteristics of the error amp are optimized internally.

## ■ OPERATIONAL EXPLANATION (Continued)

### <Current Limit>

The current limiter circuit of the MYRGP-W/MYRGP-B series monitors the current flowing through the P-channel MOS driver transistor connected to the Lx pin. When the driver current is greater than a specific level, the current limit function operates to turn off the pulses from the Lx pin at any given timing. When the over current state is eliminated, the IC resumes its normal operation.

### <Reference voltage source, soft-start function>

The reference voltage forms a reference that is used to stabilize the output voltage of the IC. After chip enable of the IC, the reference voltage connected to the error amp increases linearly during the soft-start interval.

This allows the voltage divided by the internal R1 and R2 resistors and the reference voltage to be controlled in a balanced manner, and the output voltage rises in proportion to the rise in the reference voltage. This operation prevents rush input current and enables the output voltage to rise smoothly.

If the output voltage does not reach the set output voltage within the soft start time, such as when the load is heavy or a large capacity output capacitor is connected, the balancing of the voltage divided by the internal resistors R1 and R2 and the reference voltage is lost, however, the current restriction function activates to prevent an excessive increase of input current, enabling a smooth rise of the output voltage.

### <PWM/PFM selection circuit>

PWM control is a continuous conduction mode, and operates at a stable switching frequency by means of an on time ( $t_{on}$ ) that is determined by the input voltage and output voltage regardless of the load.

PWM/PFM auto switching control is a discontinuous conduction mode at light loads, and lowers the switching frequency to reduce switching loss and improve efficiency.

The MYRGP-W series is internally fixed to PWM control.

The MYRGP-B series is internally fixed to PWM/PFM auto switching control.

### <CE function>

Operation starts when “H” voltage is input into the CE pin. The IC can be put in the shutdown state by inputting “L” voltage into the CE pin. In the shutdown state, the supply current of the IC is  $0\mu\text{A}$  (TYP.), and the Pch MOS driver Tr. and Nch MOS switch Tr. for synchronous rectification turn off. The CE pin is a CMOS input and the sink current is  $0\mu\text{A}$ .

### <UVLO>

When the  $V_{IN}$  voltage becomes  $2.00\text{V}$  (TYP.) or lower, the P-ch MOS driver transistor output driver transistor is forced OFF to prevent false pulse output caused by unstable operation of the internal circuitry. When the  $V_{IN}$  pin voltage becomes  $2.10\text{V}$  (TYP.) or higher, switching operation takes place. By releasing the UVLO function, the IC performs the soft start function to initiate output startup operation. The UVLO circuit does not cause a complete shutdown of the IC, but causes pulse output to be suspended; therefore, the internal circuitry remains in operation.

### <Thermal Shutdown>

For protection against heat damage of the ICs, thermal shutdown function monitors chip temperature. The thermal shutdown circuit starts operating and the P-ch MOS driver and N-ch MOS driver transistor will be turned off when the chip's temperature reaches  $150^\circ\text{C}$ . When the temperature drops to  $120^\circ\text{C}$  (TYP.) or less after shutting of the current flow, the IC performs the soft-start function to initiate output startup operation.

### <Short-circuit protection function>

The short-circuit protection circuit protects the device that is connected to this product and to the input/output in situations such as when the output is accidentally shorted to GND. The short-circuit protection circuit monitors the output voltage, and when the output voltage falls below the short-circuit protection threshold voltage, it turns off the Pch MOS driver Tr and latches it. Once in the latched state, operation is resumed by turning off the IC from the CE pin and then restarting, or by re-input into the  $V_{IN}$  pin.



■ OPERATIONAL EXPLANATION (Continued)

<CL High Speed Discharge>

The product can quickly discharge the electric charge at the output capacitor (CL) when a low signal to the CE pin which enables a whole IC circuit put into OFF state, is inputted via the N-ch MOS switch transistor located between the VOUT pin and the GND pin. When the IC is disabled, electric charge at the output capacitor (CL) is quickly discharged so that it may avoid application malfunction.

$$V = V_{OUT(T)} \times e^{-t / \tau}$$

$$t = \tau \ln (V_{OUT(T)} / V)$$

V : Output voltage after discharge

V<sub>OUT(T)</sub> : Output voltage

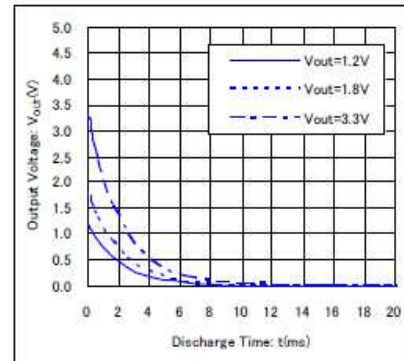
t : Discharge time

$\tau$  : CL × RDCHG

CL : Capacitance of Output capacitor

RDCHG : CL auto-discharge resistance,  
but it depends on supply voltage.

Output Voltage Discharge characteristics  
RDCHG=210Ω (TYP.) CL=10μF

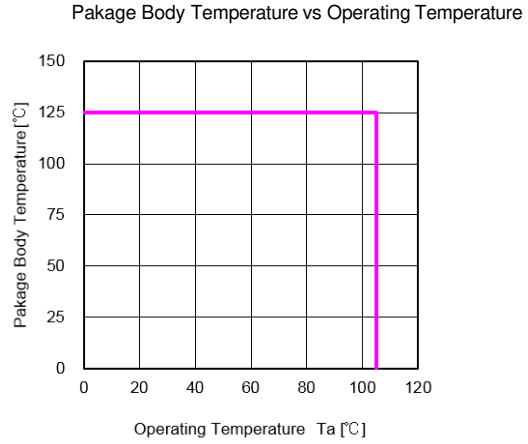
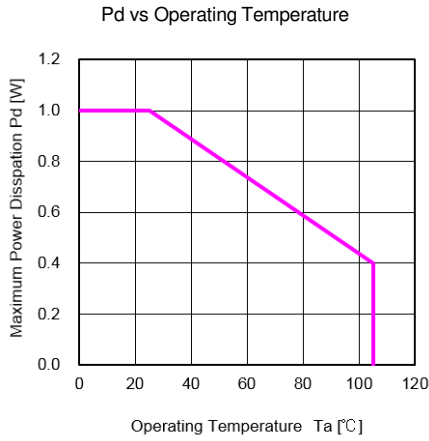


■ NOTE ON USE

1. For the phenomenon of temporal and transitional voltage decrease or voltage increase, the IC may be damaged or deteriorated if IC is used beyond the absolute MAX. specifications.
2. Spike noise and ripple voltage arise in a switching regulator as with a DC/DC converter. These are greatly influenced by external component selection, such as the coil inductance, capacitance values, and board layout of external components. Once the design has been completed, verification with actual components should be done.
3. The DC/DC converter characteristics depend greatly on the externally connected components as well as on the characteristics of this IC, so refer to the specifications and standard circuit examples of each component when carefully considering which components to select. Be especially careful of the capacitor characteristics and use B characteristics (JIS standard) or X7R, X5R (EIA standard) ceramic capacitors.
4. Sufficiently reinforce the ground wiring. In particular, reinforce near the PGND and AGND pin as fluctuations of the ground phase due to the ground current during switching may cause the operation of the IC to become unstable.
5. Mount external components as close as possible to the IC. Keep the wiring short and thick to lower the wiring impedance.
6. A feature of High Speed Transient Response -COT control is that it controls the off time in order to control the duty, which varies due to the effects of power loss between the input ( $V_{IN}$  pin) and output ( $V_{OUT}$  pin) due to the load, and thus the switching frequency fluctuates. In addition, changes in the on time due to 100% duty cycle mode are allowed. For this reason, caution must be exercised as the characteristics of the switching frequency will vary depending on the external component characteristics, board layout, input voltage, output voltage, load current and other parameters.
7. Due to propagation delay inside the product, the on time generated by the minimum on time generation circuit may not be the same as the on time that is the ratio of the input voltage to the output voltage.
8. With regard to the current limiting value, the actual coil current may at times exceed the electrical characteristics due to propagation delay inside the product.
9. The CE pin is a CMOS input pin. Do not use with the pin open. If connecting to the input or ground, use a resistor up to 1M $\Omega$ . To prevent malfunctioning of the device connected to this product or the input/output due to short circuiting between pins, it is recommended that a resistor be connected.
10. If the output voltage drops below the short circuit protection threshold voltage at the end of the soft start interval, operation will stop.
11. PWM/PFM auto switching control is a discontinuous conduction mode when the load is light, and in cases where the voltage difference between input and output is low or the coil inductance is higher than the value indicated in the standard circuit example, the coil current may reverse when the load is light, and thus pulse skipping will not be possible and light load efficiency will worsen.
12. When the input voltage is close to the minimum input voltage, the current limit circuit might not be able to work.
13. When the voltage difference between input voltage and output voltage is low, the load stability feature may deteriorate.
14. If the capacitance value is not sufficient by degrading CL due to the low temp. condition and DC bias feature, 100% duty cycle might come up for the load transient condition. Add capacitance value for CL if necessary.
15. If the capacitance value is not sufficient by degrading CL due to the low temp. condition and DC bias feature, the duty cycle might not be stable. Add capacitance value for CL if necessary.
16. MURATA places an importance on improving our products and their reliability. We request that users incorporate fail-safe designs and post-aging protection treatment when using MURATA products in their systems.

■ NOTE ON USE (Continued)

17. Please use within the power dissipation range below. Please also note that the power dissipation may be changed by test conditions, the power dissipation figure shown is PCB mounted.



the power loss of mini DC/DC according to the following formula:

$$power\ loss = V_{out} \times I_{out} \times ((100/EFFI) - 1) \quad (W)$$

$V_{out}$  : Output Voltage (V)

$I_{out}$  : Output Current (A)

EFFI : Conversion Efficiency (%)

Measurement Condition (Reference data)

Condition: Mount on a board

Ambient: Natural convection

Soldering: Lead (Pb) free

Board: Dimensions 40 x 40 mm (1600 mm<sup>2</sup> in one side)

Copper (Cu) traces occupy 50% of the board area

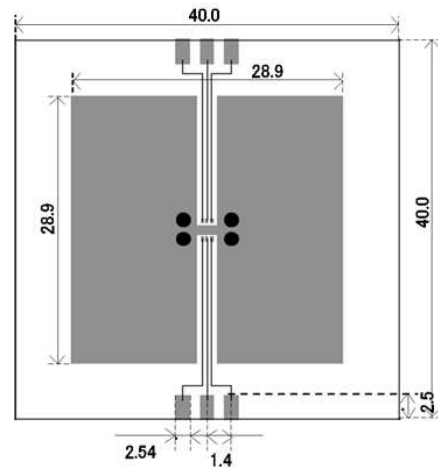
In top and back faces

Package heat-sink is tied to the copper traces

Material: Glass Epoxy (FR-4)

Thickness: 1.6mm

Through-hole: 4 x 0.8 Diameter



Evaluation Board (unit: mm)

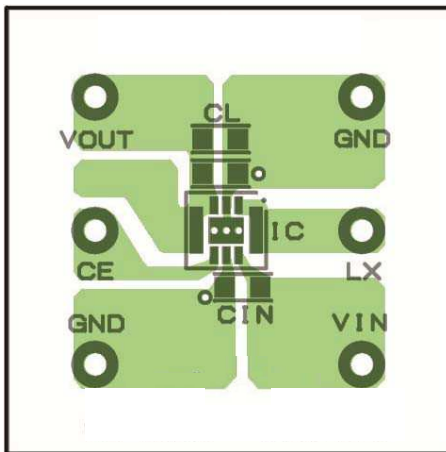
■ NOTE ON USE (Continued)

18. Instructions of pattern layouts

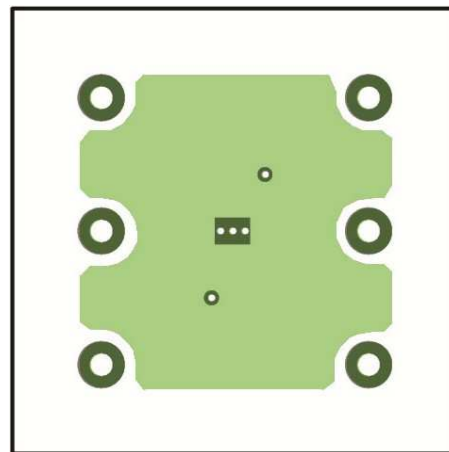
The operation may become unstable due to noise and/or phase lag from the output current when the wire impedance is high, please place the input capacitor( $C_{IN}$ ) and the output capacitor ( $C_L$ ) as close to the IC as possible.

- (1) In order to stabilize VIN voltage level, we recommend that a by-pass capacitor ( $C_{IN}$ ) be connected as close as possible to the VIN pin, PGND pin.
- (2) Please mount each external component as close to the IC as possible.
- (3) Wire external components as close to the IC as possible and use thick, short connecting traces to reduce the circuit impedance.
- (4) Make sure that the GND traces are as thick as possible, as variations in ground potential caused by high ground currents at the time of switching may result in instability of the IC.
- (5) This series' internal driver transistors bring on heat because of the output current and ON resistance of P-channel and N- channel MOS driver transistors. Please consider the countermeasures against heat if necessary.

<Reference pattern layout>



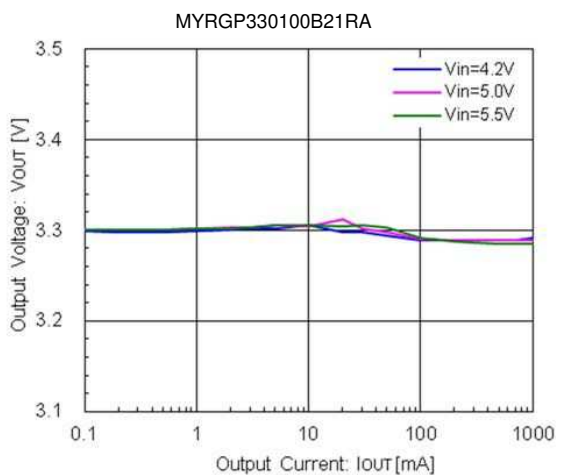
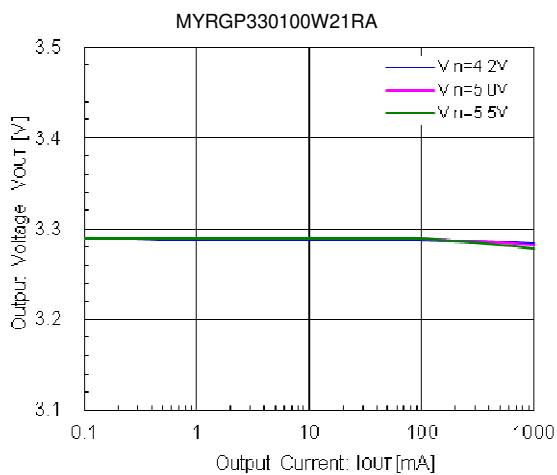
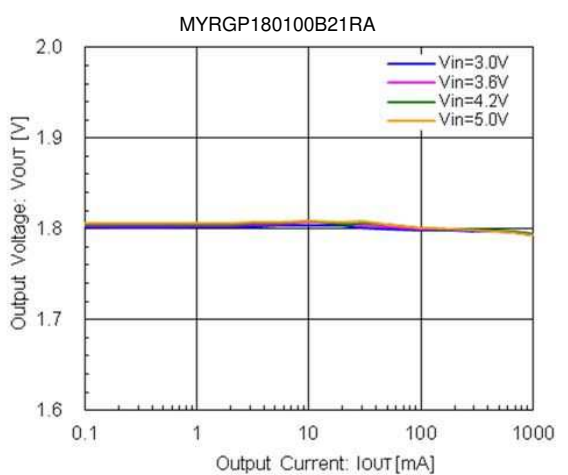
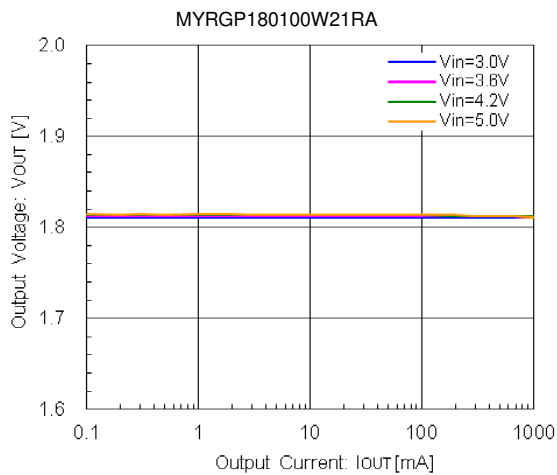
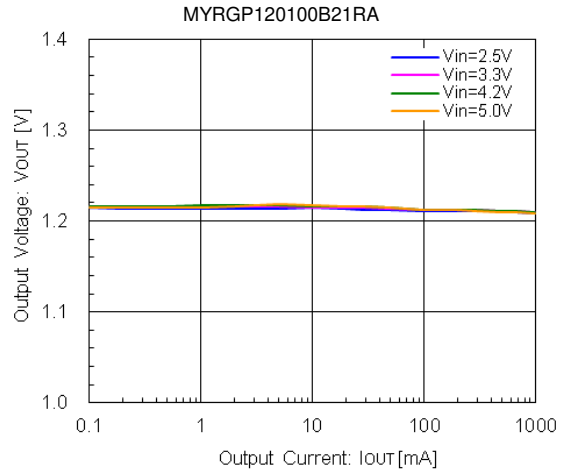
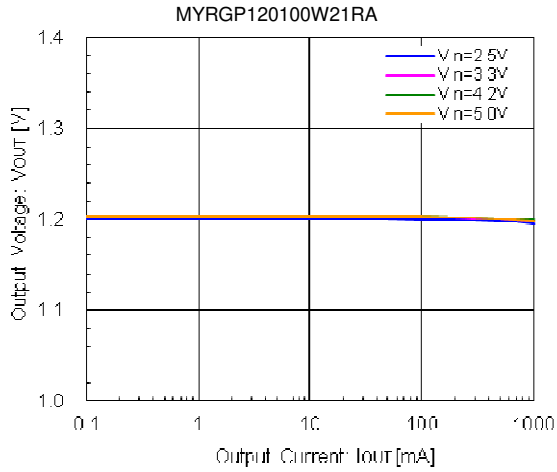
<TOP VIEW>



<BACK SIDE TOP VIEW>

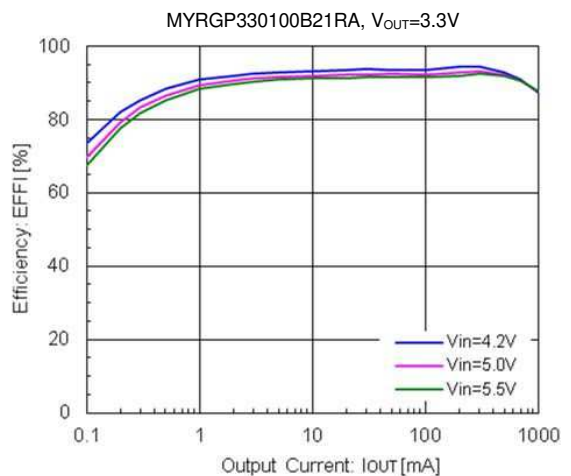
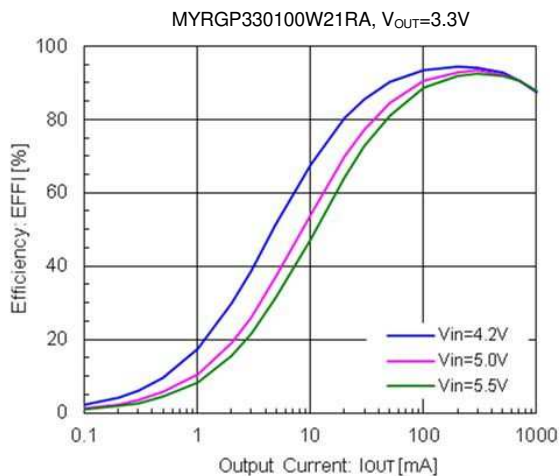
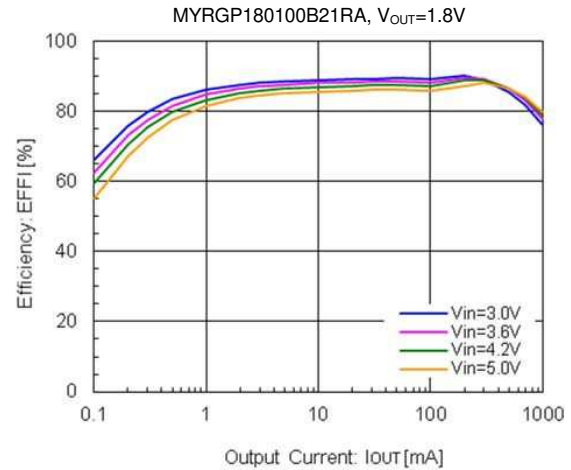
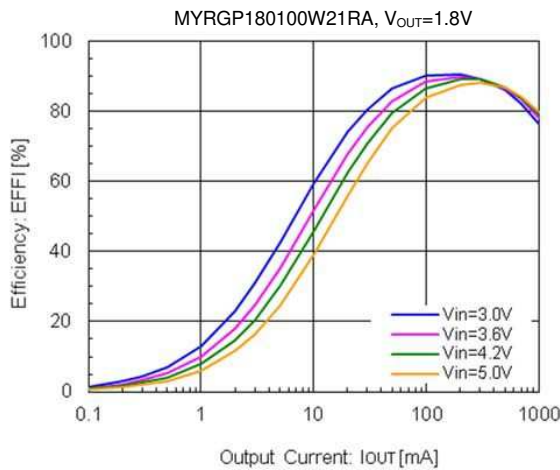
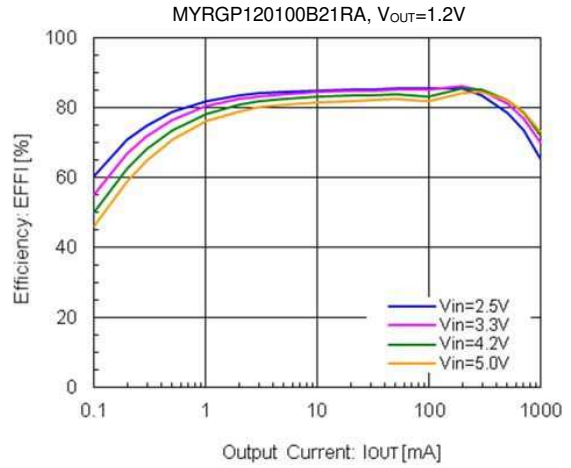
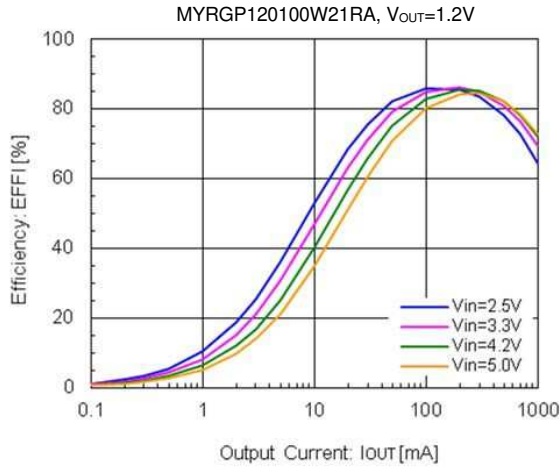
**TYPICAL PERFORMANCE CHARACTERISTICS**

(1) Output Voltage vs. Output Current



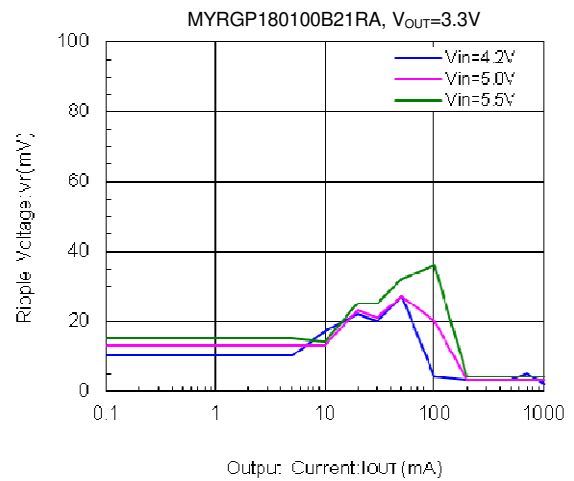
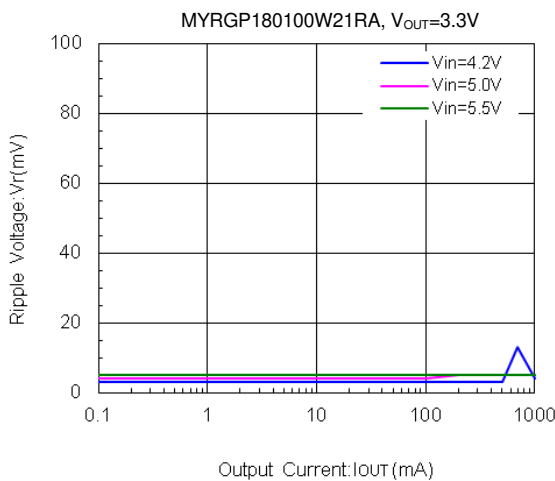
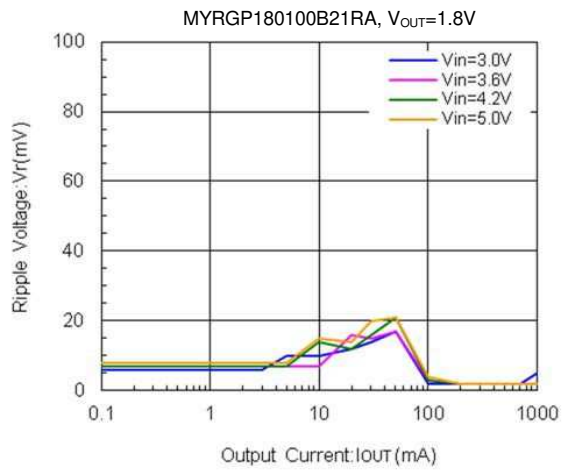
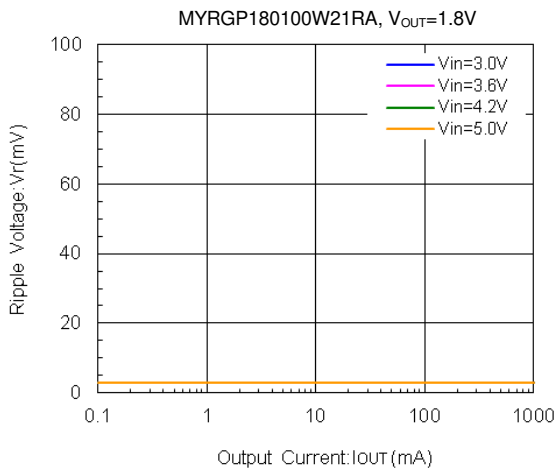
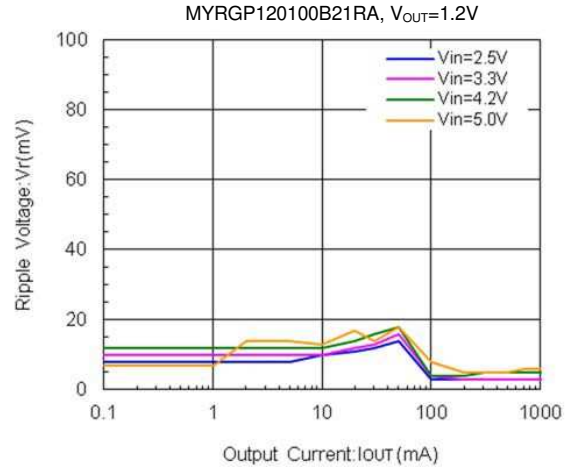
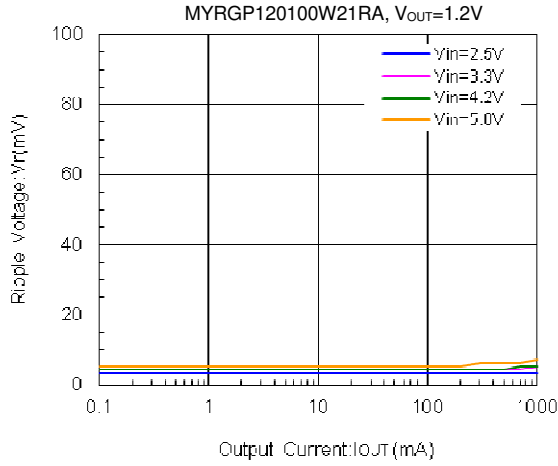
■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(2) Efficiency vs. Output Current



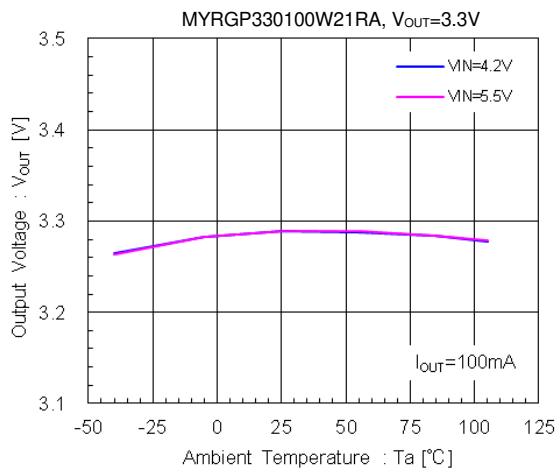
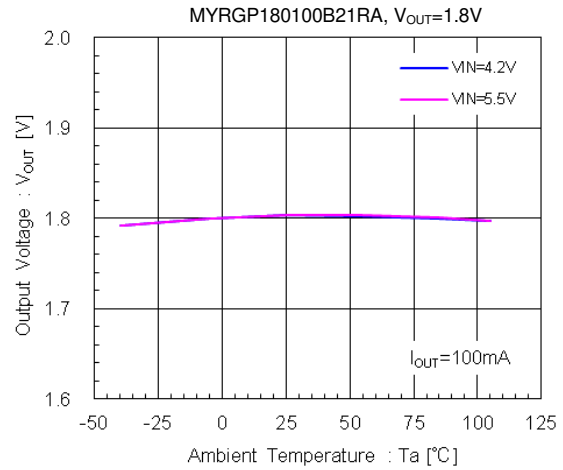
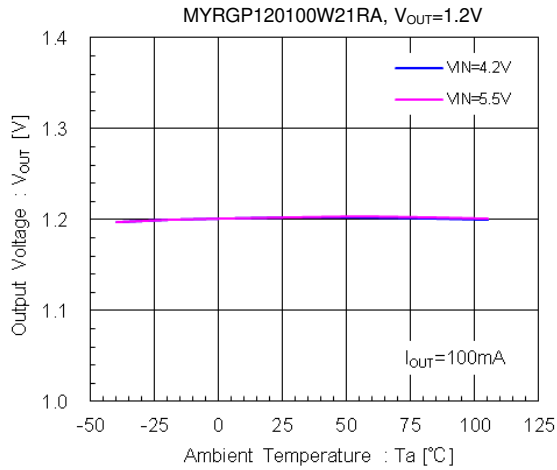
■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(3) Ripple Voltage vs. Output Current

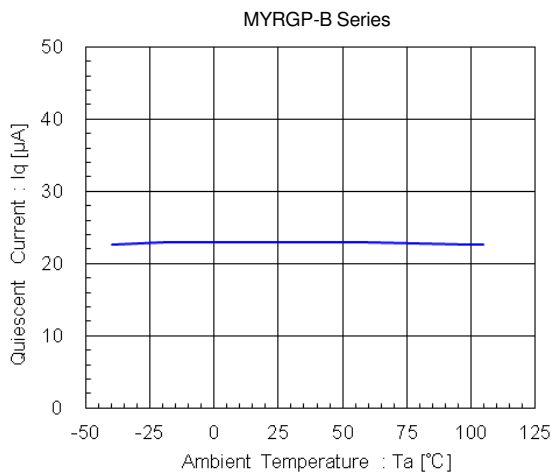


**TYPICAL PERFORMANCE CHARACTERISTICS (Continued)**

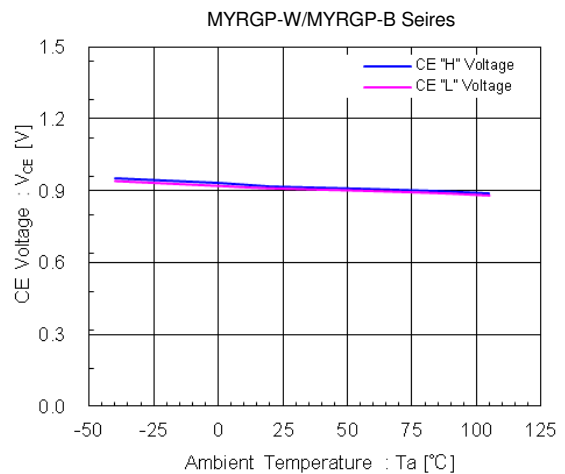
(4) Output Voltage vs. Ambient Temperature



(5) Quiescent Current vs. Ambient Temperature



(6) CE Voltage vs. Ambient Temperature

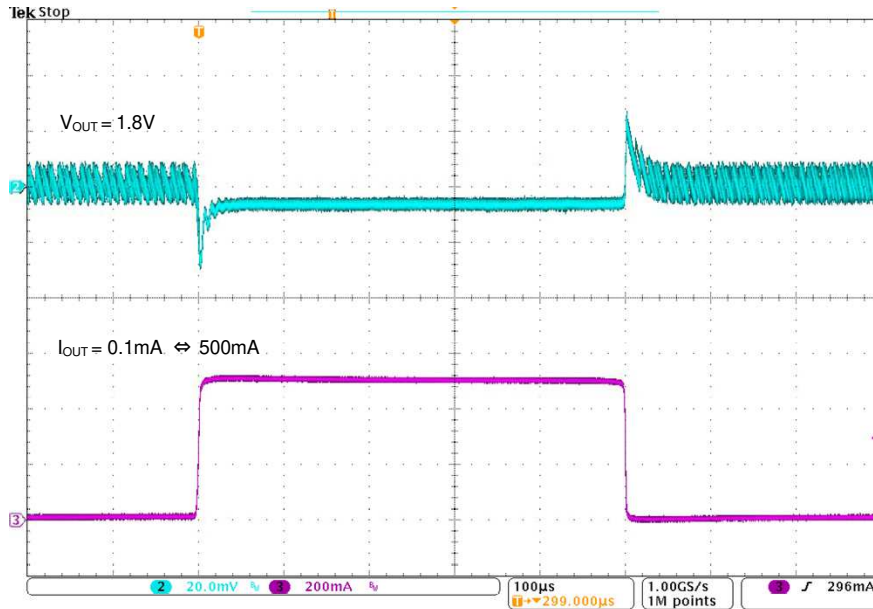




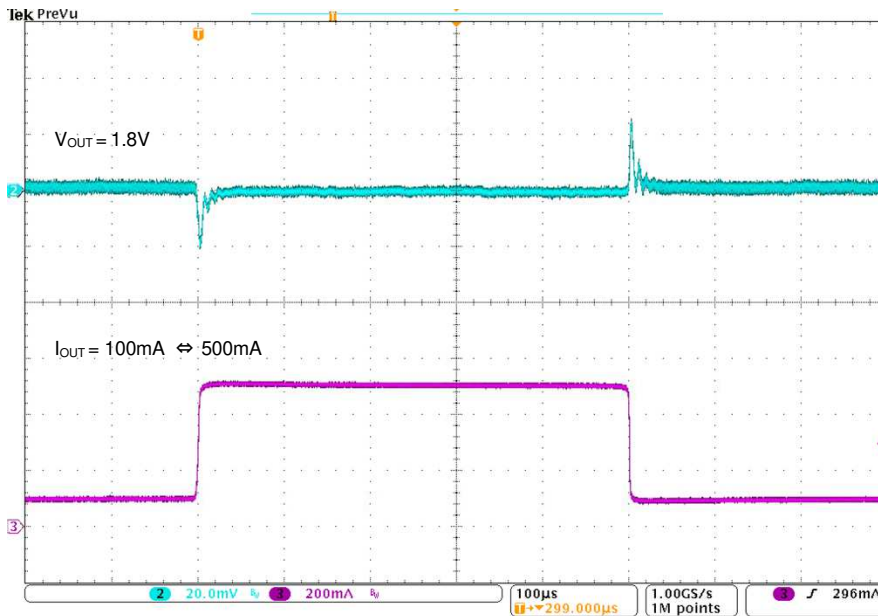
**TYPICAL PERFORMANCE CHARACTERISTICS (Continued)**

(7) Load Transient Response

(1) MYRGP180100B21RA,  $V_{IN}=4.2V$ ,  $V_{OUT}=1.8V$  /  $I_{OUT}=0.1mA \leftrightarrow 500mA$

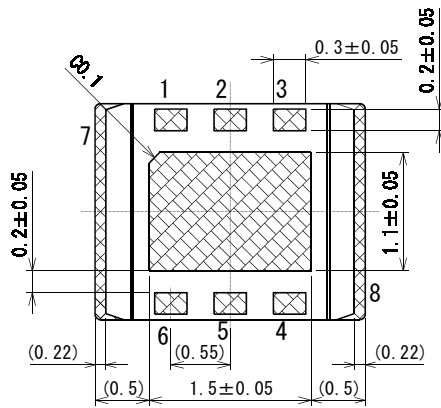
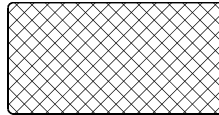
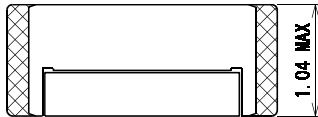
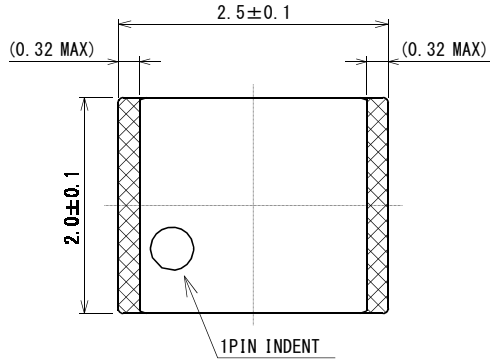


(2) MYRGP180100B21RA,  $V_{IN}=4.2V$ ,  $V_{OUT}=1.8V$  /  $I_{OUT}=100mA \leftrightarrow 500mA$



**PACKAGING INFORMATION**

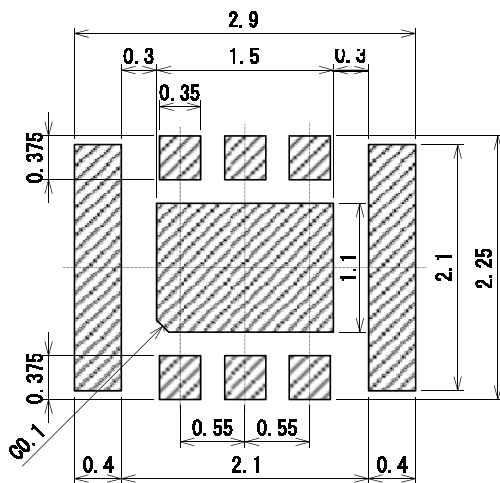
● Packaging (2.0mm × 2.5mm, h=1.0mm)



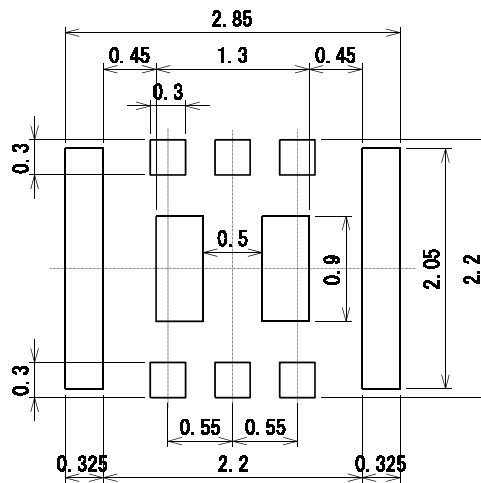
■ External Lead



● Reference Pattern Layout (unit:mm)



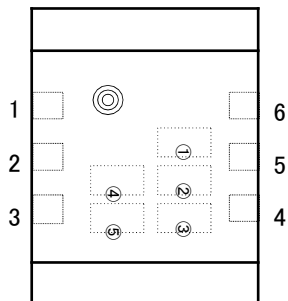
● Reference Metal Mask Design (unit:mm)



\* Implementation is recommended within accuracy 0.05mm / 0.05mm.

# “PicoBK™” MYRGP-W / MYRGP-B series

## 1.0A Inductor Built-in Step-Down DC/DC Converters



① represents products series

MARK	PRODUCT SERIES
2	MYRGP*****W21RA
3	MYRGP*****B21RA

② represents integer and oscillation frequency of the output voltage

MARK	TYPE	OUTPUT VOLTAGE(V)	SWITCHING FREQUENCY (MHz)	PRODUCT SERIES
N	B	0.x	3.0	MYRGP0**100*21RA
P		1.x		MYRGP1**100*21RA
R		2.x		MYRGP2**100*21RA
S		3.x		MYRGP3**100*21RA

③ represents the decimal part of output voltage

OUTPUT VOLTAGE(V)	MARK	PRODUCT SERIES
X.0	0	MYRGP*00100*21RA
X.05	A	MYRGP*05100*21RA
X.1	1	MYRGP*10100*21RA
X.15	B	MYRGP*15100*21RA
X.2	2	MYRGP*20100*21RA
X.25	C	MYRGP*25100*21RA
X.3	3	MYRGP*30100*21RA
X.35	D	MYRGP*35100*21RA
X.4	4	MYRGP*40100*21RA
X.45	E	MYRGP*45100*21RA
X.5	5	MYRGP*50100*21RA
X.55	F	MYRGP*55100*21RA
X.6	6	MYRGP*60100*21RA
X.65	H	MYRGP*65100*21RA
X.7	7	MYRGP*70100*21RA
X.75	K	MYRGP*75100*21RA
X.8	8	MYRGP*80100*21RA
X.85	L	MYRGP*85100*21RA
X.9	9	MYRGP*90100*21RA
X.95	M	MYRGP*95100*21RA

④,⑤ represents production lot number

01~09, 0A~0Z, 11~9Z, A1~A9, AA~AZ, B1~ZZ in order.

(G, I, J, O, Q, W excluded)

Note: No character inversion used.

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5. Although we make continuous efforts to improve the quality and reliability of our products; nevertheless Semiconductors are likely to fail with a certain probability. So in order to prevent personal injury and/or property damage resulting from such failure, customers are required to incorporate adequate safety measures in their designs, such as system fail safes, redundancy and fire prevention features.
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