ICS-41351

Top Port PDM Digital Output Multi-Mode Microphone

GENERAL DESCRIPTION

The ICS-41351 is a multi-mode, low noise digital MEMS microphone in a small package. The ICS-41351 consists of a MEMS microphone element and an impedance converter amplifier followed by a fourth-order Σ-Δ modulator. The digital interface allows the pulse density modulated (PDM) output of two microphones to be time multiplexed on a single data line using a single clock.

The ICS-41351 has multiple modes of operation: Low Power (AlwaysOn), Standard and Sleep. The ICS-41351 has high SNR and 120 dB SPL AOP in all operational modes.

The ICS-41351 is available in a standard 3.5 × 2.65 × 0.98 mm surface-mount package. It is reflow solder compatible with no sensitivity degradation.

APPLICATIONS

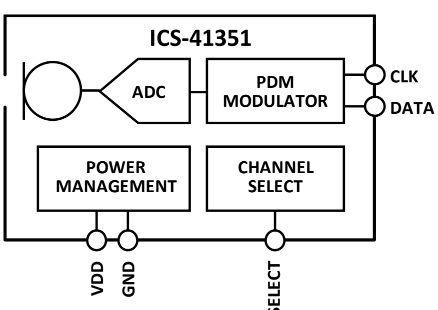
- Smartphones
- Microphone Arrays
- Tablets
- Cameras
- Bluetooth Headsets
- Notebook PCs
- Security and Surveillance

FEATURES

SPEC	STANDARD MODE	LOW-POWER MODE
Sensitivity	−26 dB FS ±1 dB	−26 dB FS ±1 dB
SNR	65 dBA	65 dBA
Current	600 µA	230 µA
AOP	120 dB SPL	120 dB SPL
Clock	2.4 MHz	768 kHz

- 3.5 × 2.65 × 0.98 mm surface-mount package
- Extended frequency response from 50 Hz to >20 kHz
- Low power: 230 µA in Low-Power Mode
- Sleep Mode: 12 µA
- High power supply rejection (PSR): −93 dB FS
- Fourth-order Σ-Δ modulator
- Digital pulse density modulation (PDM) output
- Compatible with Sn/Pb and Pb-free solder processes
- RoHS/WEEE compliant

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

PART	TEMP RANGE	PACKAGING
ICS-41351	−40°C to +85°C	13" Tape and Reel
EV_ICS-41351-FX	—	

TABLE OF CONTENTS

SPECIFICATIONS

TABLE 1. ACOUSTICAL/ELECTRICAL CHARACTERISTICS – GENERAL

T_A = 25°C, VDD = 1.8 to 3.3 V, SCK = 1.536 MHz, 32× decimation, C_{LOAD} = 30 pF unless otherwise noted. Typical specifications are not guaranteed.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
PERFORMANCE						
Directionality			Omni			
Output Polarity	Input acoustic pressure vs. output data		Non-Inverted			
Supply Voltage (V_{DD})		1.65		3.63	V	
Sleep Mode Current (I_S)	SCK < 200 kHz		12	20	µA	

TABLE 2. ACOUSTICAL/ELECTRICAL CHARACTERISTICS – STANDARD MODE

T_A = 25°C, VDD = 1.8 to 3.3 V, SCK = 2.4 MHz, 50× decimation, C_{LOAD} = 30 pF unless otherwise noted. Typical specifications are not guaranteed.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Sensitivity	1 kHz, 94 dB SPL	−27	−26	−25	dB FS	1
Signal-to-Noise Ratio (SNR)	20 kHz bandwidth, A-weighted		65		dBA	
Equivalent Input Noise (EIN)	20 kHz bandwidth, A-weighted		29		dBA SPL	
Dynamic Range	Derived from EIN and acoustic overload point		91		dB	
Total Harmonic Distortion (THD)	105 dB SPL		0.2	1	%	
Power Supply Rejection (PSR)	217 Hz, 100 mV p-p square wave superimposed on VDD = 1.8 V, A-weighted		−93		dB FS	
Power Supply Rejection—Swept Sine	1 kHz sine wave		90		dB FS	
Acoustic Overload Point	10% THD		120		dB SPL	
Supply Current (I_S)	V_{DD} = 1.8 V, no load		600	700	µA	

Note 1: Sensitivity is relative to the RMS level of a sine wave with positive amplitude equal to 100% 1s density and negative amplitude equal to 0% 1s density.

TABLE 3. ACOUSTICAL/ELECTRICAL CHARACTERISTICS – LOW-POWER MODE

T_A = 25°C, VDD = 1.8 to 3.3 V, SCK = 768 kHz, 48× decimation, C_{LOAD} = 30 pF unless otherwise noted. Typical specifications are not guaranteed.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Sensitivity	1 kHz, 94 dB SPL	−27	−26	−25	dB FS	1
Signal-to-Noise Ratio (SNR)	20 kHz bandwidth, A-weighted		65		dBA	
Equivalent Input Noise (EIN)	20 kHz bandwidth, A-weighted		29		dBA SPL	
Dynamic Range	Derived from EIN and acoustic overload point		91		dB	
Total Harmonic Distortion (THD)	105 dB SPL		0.2	1	%	
Power Supply Rejection (PSR)	217 Hz, 100 mV p-p square wave superimposed on VDD = 1.8 V, A-weighted		−93		dB FS	
Power Supply Rejection—Swept Sine	1 kHz sine wave		90		dB FS	
Acoustic Overload Point	10% THD		120		dB SPL	
Supply Current (I_S)	V_{DD} = 1.8 V, no load		230	275	µA	

Note 1: Sensitivity is relative to the RMS level of a sine wave with positive amplitude equal to 100% 1s density and negative amplitude equal to 0% 1s density.

TABLE 4. DIGITAL INPUT/OUTPUT CHARACTERISTICS

T_A = 25°C, 1.8 V < VDD < 3.3 V, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input Voltage High (V_{IH})		0.65 × V_{DD}			V	
Input Voltage Low (V_{IL})				0.35 × V_{DD}	V	
Output Voltage High (V_{OH})	I_{LOAD} = 0.5 mA	0.7 × V_{DD}	V_{DD}		V	
Output Voltage Low (V_{OL})	I_{LOAD} = 0.5 mA		0	0.3 × V_{DD}	V	
Output DC Offset	Percent of full scale		3		%	
Latency			<30		µs	

TABLE 5. PDM DIGITAL INPUT/OUTPUT

T_A = 25°C, 1.8 V < VDD < 3.3 V, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
MODE SWITCHING						
Sleep Time	Time from f_{CLK} falling <200 kHz			10	ms	
Wake-Up Time	Standard mode, Sleep Mode to f_{CLK} = 1.536 MHz, output within 1 dB of final sensitivity, power on			20	ms	
Wake-Up Time	Low-Power Mode, Sleep Mode to f_{CLK} = 768 kHz, output within 1 dB of final sensitivity, power on			20	ms	
Switching time	Between Low-Power and Standard Modes			10	ms	
INPUT						
Clock Frequency (CLK)	Sleep Mode			200	kHz	
	Low-Power Mode	690	768	800	kHz	
	Standard Mode	1.00	2.4	2.65	MHz	
Clock Duty Cycle	f_{CLK} < 2.65 MHz	45		55	%	
t_{RISE}	CLK rise time (10% to 90% level)			40	ns	1
t_{FALL}	CLK fall time (90% to 10% level)			40	ns	1
OUTPUT						
t_{1OUTEN}	DATA1 (right) driven after falling clock edge	31			ns	
$t_{1OUTDIS}$	DATA1 (right) disabled after rising clock edge	5		20	ns	
t_{2OUTEN}	DATA2 (left) driven after rising clock edge	31			ns	
$t_{2OUTDIS}$	DATA2 (left) disabled after falling clock edge	5		20	ns	

Note 1: Guaranteed by design

TIMING DIAGRAM

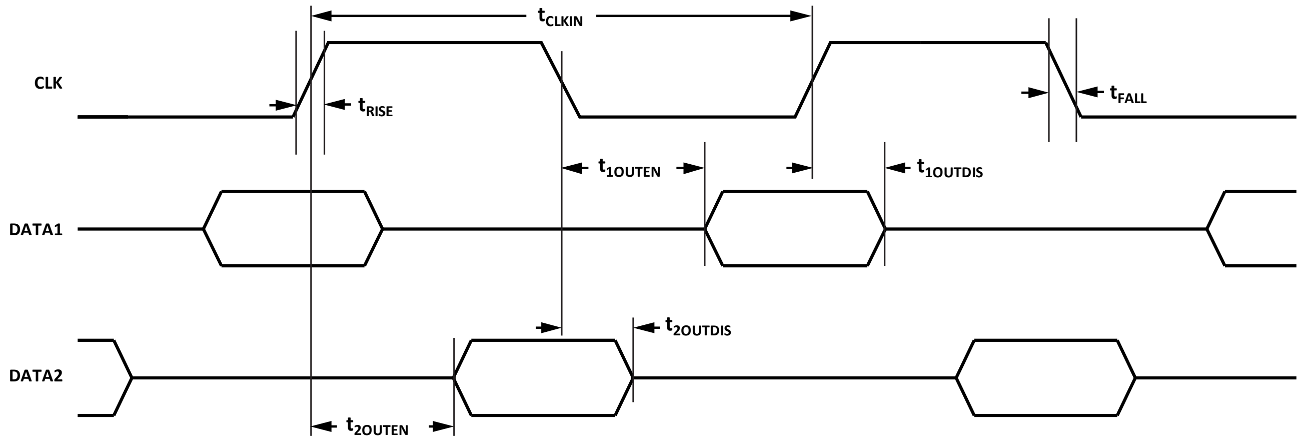


Figure 1. Pulse Density Modulated Output Timing

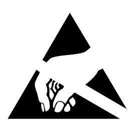
ABSOLUTE MAXIMUM RATINGS

Stress above those listed as Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

TABLE 6. ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Supply Voltage (V_{DD})	−0.3 V to +3.63 V
Digital Pin Input Voltage	−0.3 V to V_{DD} + 0.3 V or 3.63 V, whichever is less
Sound Pressure Level	160 dB
Mechanical Shock	10,000 *g*
Vibration	Per MIL-STD-883 Method 2007, Test Condition B
Temperature Range	
Biased	−40°C to +85°C
Storage	−55°C to +150°C

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

SOLDERING PROFILE

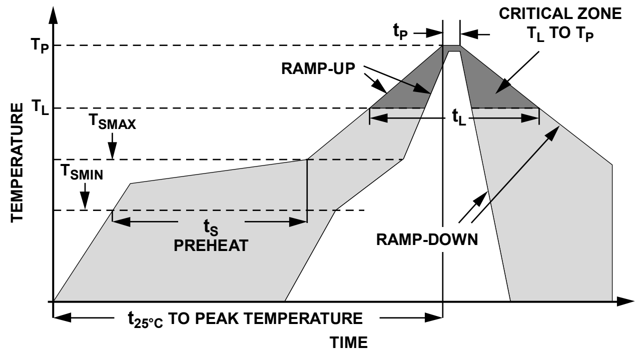


Figure 2. Recommended Soldering Profile Limits

TABLE 7. RECOMMENDED SOLDERING PROFILE*

PROFILE FEATURE		Sn63/Pb37	Pb-Free
Average Ramp Rate (T_L to T_P)		1.25°C/sec max	1.25°C/sec max
Preheat	Minimum Temperature (T_{SMIN})	100°C	100°C
	Maximum Temperature (T_{SMAX})	150°C	200°C
	Time (T_{SMIN} to T_{SMAX}), t_S	60 sec to 75 sec	60 sec to 75 sec
Ramp-Up Rate (T_{SMAX} to T_L)		1.25°C/sec	1.25°C/sec
Time Maintained Above Liquidous (t_L)		45 sec to 75 sec	~50 sec
Liquidous Temperature (T_L)		183°C	217°C
Peak Temperature (T_P)		215°C +3°C/−3°C	260°C +0°C/−5°C
Time Within +5°C of Actual Peak Temperature (t_P)		20 sec to 30 sec	20 sec to 30 sec
Ramp-Down Rate		3°C/sec max	3°C/sec max
Time +25°C ($t_{25°C}$) to Peak Temperature		5 min max	5 min max

**The reflow profile in Table 7 is recommended for board manufacturing with InvenSense MEMS microphones. All microphones are also compatible with the J-STD-020 profile*

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

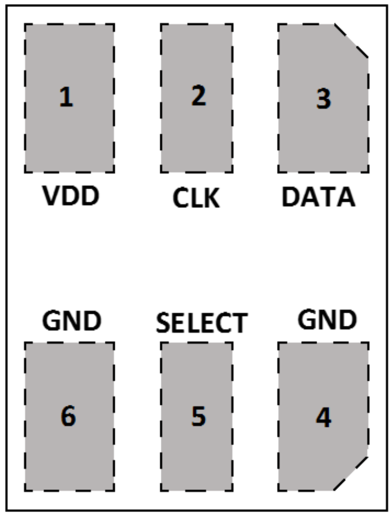


Figure 3. Pin Configuration Bottom View, Terminal Side Up)

TABLE 8. PIN FUNCTION DESCRIPTIONS

PIN	NAME	FUNCTION
1	VDD	Power Supply. For best performance and to avoid potential parasitic artifacts, place a 0.1 µF (100 nF) ceramic type X7R capacitor between Pin 1 (VDD) and ground. Place the capacitor as close to Pin 1 as possible.
2	CLK	Clock Input to Microphone
3	DATA	Digital Output Signal (DATA1 or DATA2)
4	GND	Ground
5	SELECT	Left Channel or Right Channel Select: DATA 1 (right): SELECT tied to GND DATA 2 (left): SELECT tied to VDD. In this setting, SELECT should be tied to the same voltage source as the VDD pin.
6	GND	Ground

TYPICAL PERFORMANCE CHARACTERISTICS

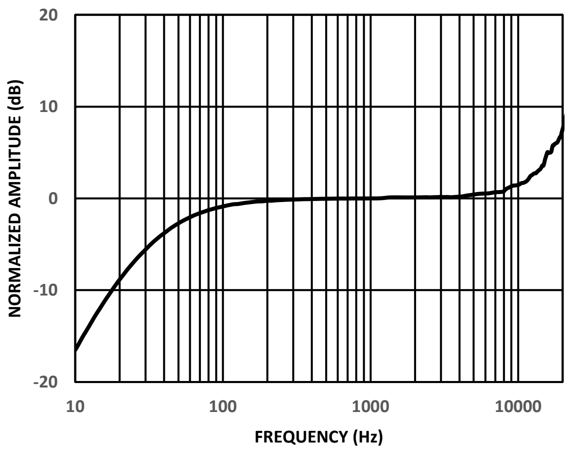


Figure 4. Typical Frequency Response, Standard Mode

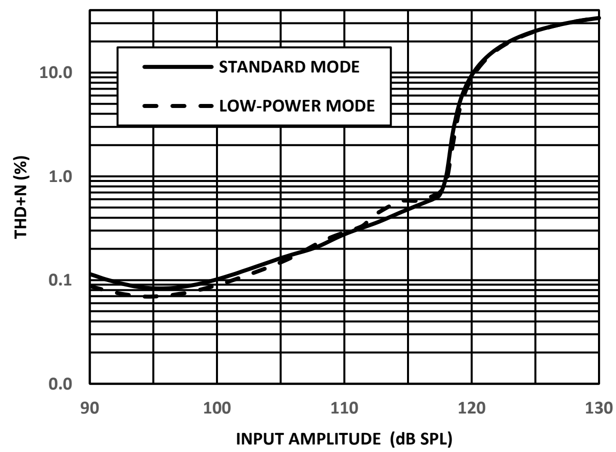


Figure 5. THD + N vs. Input Level, Standard and Low-Power Modes

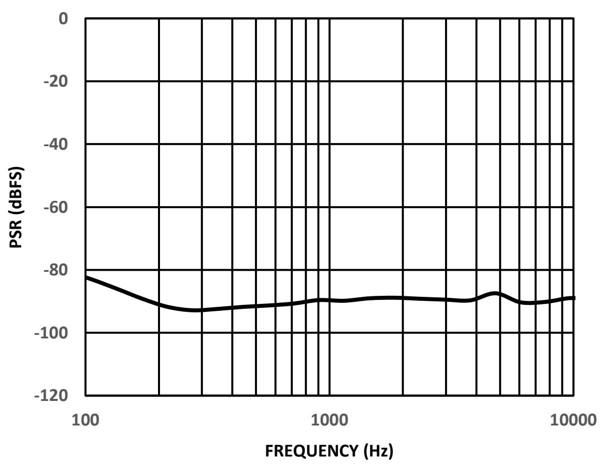


Figure 6. Power Supply Rejection (PSR) vs. Frequency, Standard Mode

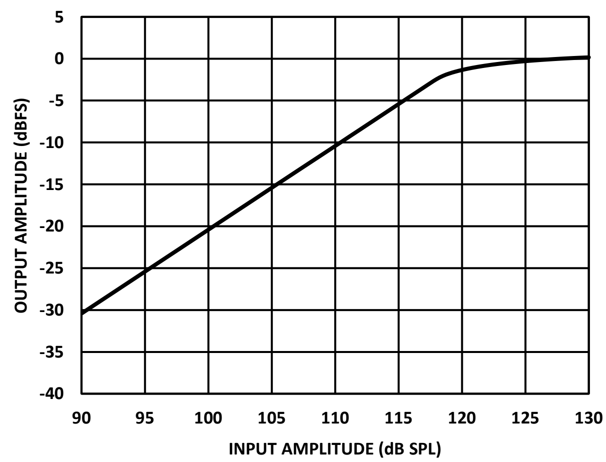


Figure 7. Linearity

THEORY OF OPERATION

PDM DATA FORMAT

The output from the DATA pin of the ICS-41351 is in pulse density modulated (PDM) format. This data is the 1-bit output of a fourth-order Σ-Δ modulator. The data is encoded so that the left channel is clocked on the falling edge of CLK, and the right channel is clocked on the rising edge of CLK. After driving the DATA signal high or low in the appropriate half frame of the CLK signal, the DATA driver of the microphone tristates. In this way, two microphones, one set to the left channel and the other to the right, can drive a single DATA line. See Figure 1 for a timing diagram of the PDM data format; the DATA1 and DATA2 lines shown in this figure are two halves of the single physical DATA signal. Figure shows a diagram of the two stereo channels sharing a common DATA line.

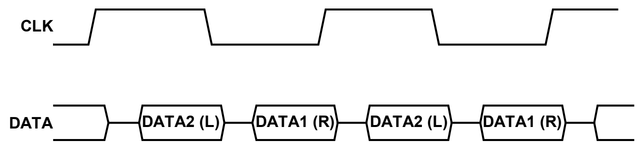


Figure 8. Stereo PDM Format

If only one microphone is connected to the DATA signal, the output is only clocked on a single edge (Figure). For example, a left channel microphone is never clocked on the rising edge of CLK. In a single microphone application, each bit of the DATA signal is typically held for the full CLK period until the next transition because the leakage of the DATA line is not enough to discharge the line while the driver is tristated.

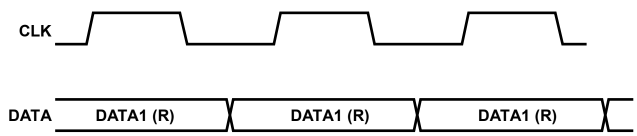


Figure 9. Mono PDM Format

See Table for the channel assignments according to the logic level on the SELECT pin.

TABLE 9. ICS-41351 CHANNEL SETTING

SELECT Pin Setting	Channel
Low (tie to GND)	Right (DATA1)
High (tie to VDD)	Left (DATA2)

For PDM data, the density of the pulses indicates the signal amplitude. A high density of high pulses indicates a signal near positive full scale, and a high density of low pulses indicates a signal near negative full scale. A perfect zero (dc) audio signal shows an alternating pattern of high and low pulses.

The output PDM data signal has a small dc offset of about 3% of full scale. A high-pass filter in the codec that is connected to the digital microphone and does not affect the performance of the microphone typically removes this dc signal.

PDM MICROPHONE SENSITIVITY

The sensitivity of a PDM output microphone is specified with the unit dB FS (decibels relative to digital full scale). A 0 dB FS sine wave is defined as a signal whose peak just touches the full-scale code of the digital word (see Figure). This measurement convention also means that signals with a different crest factor may have an RMS level higher than 0 dB FS. For example, a full-scale square wave has an RMS level of 3 dB FS.

This definition of a 0 dB FS signal must be understood when measuring the sensitivity of the ICS-41351. A 1 kHz sine wave at a 94 dB SPL acoustic input to the ICS-41351 results in an output signal with a −26 dB FS level. The output digital word peaks at −26 dB below the digital full-scale level. A common misunderstanding is that the output has an RMS level of −29 dB FS; however, this is not true because of the definition of the 0 dB FS sine wave.

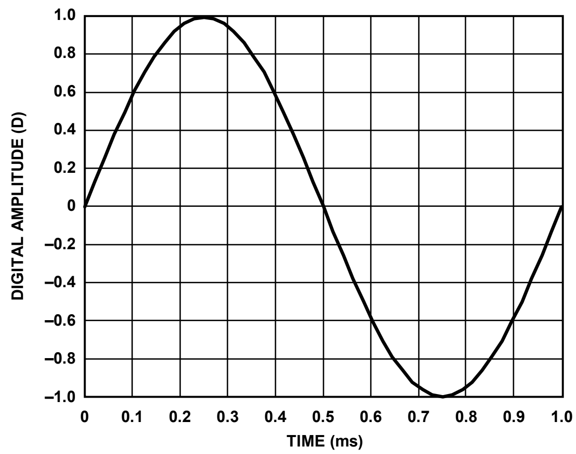


Figure 10. 1 kHz, 0 dB FS Sine Wave

There is not a commonly accepted unit of measurement to express the instantaneous level, as opposed to the RMS level of the signal, of a digital signal output from the microphone. Some measurement systems express the instantaneous level of an individual sample in units of D, where 1.0 D is digital full scale. In this case, a −26 dB FS sine wave has peaks at 0.05 D.

APPLICATIONS INFORMATION

LOW POWER MODE

Low Power Mode (LPM) enables the ICS-41351 to be used in an AlwaysOn listening mode for keyword spotting and ambient sound analysis. The ICS-41351 will enter LPM when the frequency of SCK is 768 kHz. In this mode, the microphone consumes only 250 µA while retaining high electro-acoustic performance.

When one microphone is in LPM for AlwaysOn listening, a second microphone sharing the same data line may be powered down. In this case, where one microphone is powered up and another is powered down by disabling the VDD supply or in sleep mode by reducing the frequency of a separate clock source, the disabled microphone does not present a load to the signal on the LPM microphone's DATA pin.

DYNAMIC RANGE CONSIDERATIONS

The microphone clips (THD = 10%) at 120 dB SPL (see Figure 5); however, it continues to output an increasingly distorted signal above that point. The peak output level, which is controlled by the modulator, limits at 0 dB FS.

To fully use the 97 dB dynamic range of the output data of the ICS-41351 in a design, the digital signal processor (DSP), analog-to-digital converter (ADC), or codec circuit following it must be chosen carefully. The decimation filter that inputs the PDM signal from the ICS-41351 must have a dynamic range sufficiently better than the dynamic range of the microphone so that the overall noise performance of the system is not degraded. If the decimation filter has a dynamic range of 10 dB better than the microphone, the overall system noise only degrades by 0.4 dB. This 107 dB filter dynamic range requires the filter to have at least 18 bit resolution.

CONNECTING PDM MICROPHONES

A PDM output microphone is typically connected to a codec with a dedicated PDM input. This codec separately decodes the left and right channels and filters the high sample rate modulated data back to the audio frequency band. This codec also generates the clock for the PDM microphones or is synchronous with the source that is generating the clock. Figure 7 and Figure 8 show mono and stereo connections of the ICS-41351 to a codec. The mono connection shows an ICS-41351 set to output data on the right channel. To output on the left channel, tie the SELECT pin to VDD instead of tying it to GND.

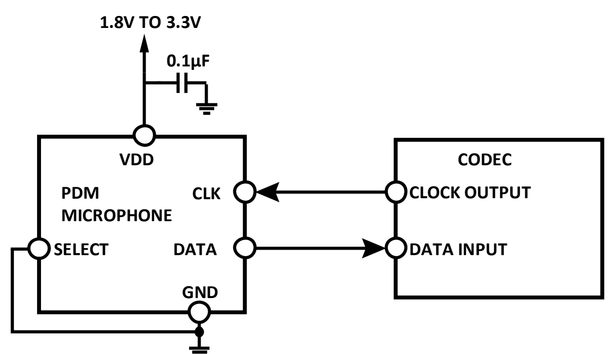


Figure 11. Mono PDM Microphone (Right Channel) Connection to Codec

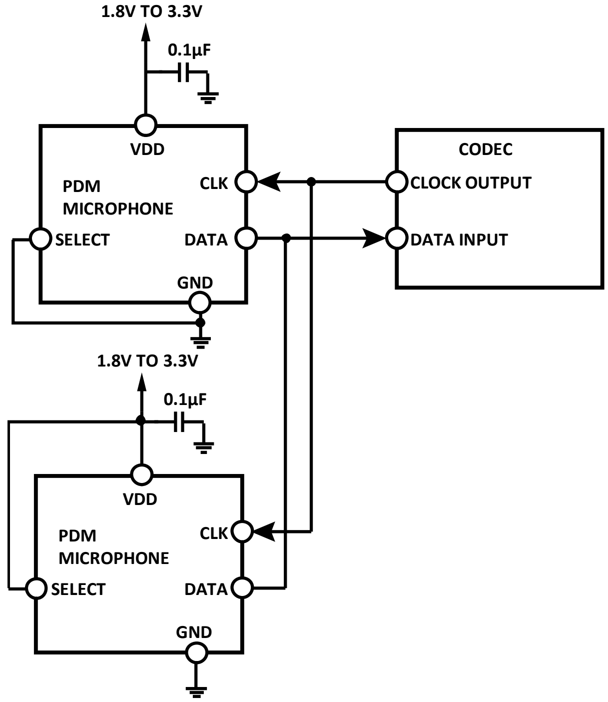


Figure 12. Stereo PDM Microphone Connection to Codec

Decouple the VDD pin of the ICS-41351 to GND with a 0.1 µF capacitor. Place this capacitor as close to VDD as the printed circuit board (PCB) layout allows.

Do not use a pull-up or pull-down resistor on the PDM data signal line because it can pull the signal to an incorrect state during the period that the signal line is tristated.

The DATA signal does not need to be buffered in normal use when the ICS-41351 microphone(s) is placed close to the codec on the PCB. If the DATA signal must be driven over a long cable (>15 cm) or other large capacitive load, a digital buffer may be required. Only use a signal buffer on the DATA line when one microphone is in use or after the point where two microphones are connected (see Figure). The DATA output of each microphone in a stereo configuration cannot be individually buffered because the two buffer outputs cannot drive a single signal line. If a buffer is used, take care to select one with low propagation delay so that the timing of the data connected to the codec is not corrupted.

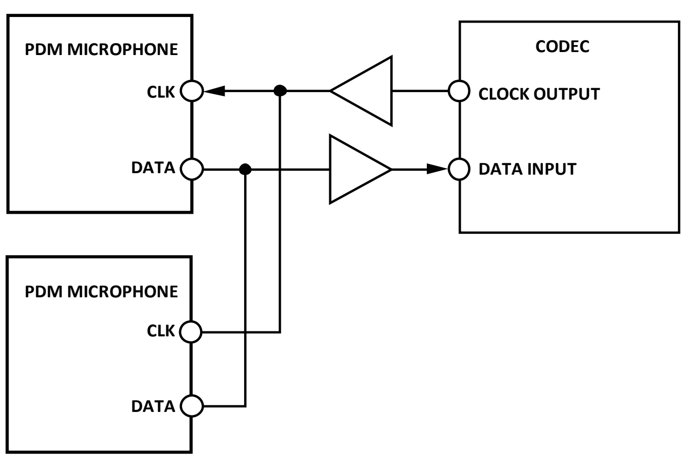


Figure 13. Buffered Connections Between Stereo ICS-41351s and a Codec

When long wires are used to connect the codec to the ICS-41351, a source termination resistor can be used on the clock output of the codec instead of a buffer to minimize signal overshoot or ringing. Match the value of this resistor to the characteristic impedance of the CLK trace on the PCB. Depending on the drive capability of the codec clock output, a buffer may still be needed, as shown in Figure .

SLEEP MODE

The microphone enters sleep mode when the clock frequency falls below 200 kHz. In this mode, the microphone data output is in a high impedance state. The current consumption in sleep mode is less than 20 µA.

The ICS-41351 enters sleep mode within 10 ms of the clock frequency falling below 200 kHz. The microphone wakes up from sleep mode and begins to output data within 10 ms after the clock becomes active. The wake-up time indicates the time from when the clock is enabled to when the ICS-41351 outputs data within 1 dB of its settled sensitivity.

START-UP TIME

The start-up time of the ICS-41351 is less than 20 ms, measured by the time from when power and clock are enabled until sensitivity of the output signal is within 1 dB of its settled sensitivity.

SUPPORTING DOCUMENTS

For additional information, see the following documents.

APPLICATION NOTES – GENERAL

AN-100, *MEMS Microphone Handling and Assembly Guide*
AN-1003: Recommendations for Mounting and Connecting the Invensense, Bottom-Ported MEMS Microphones
AN-1112: Microphone Specifications Explained
AN-1124: Recommendations for Sealing InvenSense Bottom-Port MEMS Microphones from Dust and Liquid Ingress
AN-1140: Microphone Array Beamforming

PCB DESIGN AND LAND PATTERN LAYOUT

The recommended PCB land pattern for the ICS-41351 is a 1:1 ratio of the solder pads on the microphone package, as shown in Figure 9. Avoid applying solder paste to the sound hole in the PCB. A suggested solder paste stencil pattern layout is shown in Figure 10.

The response of the ICS-41351 is not affected by the PCB hole size as long as the hole is not smaller than the sound port of the microphone (0.375 mm in diameter). A 0.5 mm to 1 mm diameter for the hole is recommended. Take care to align the hole in the microphone package with the hole in the PCB. The exact degree of the alignment does not affect the microphone performance as long as the holes are not partially or completely blocked.

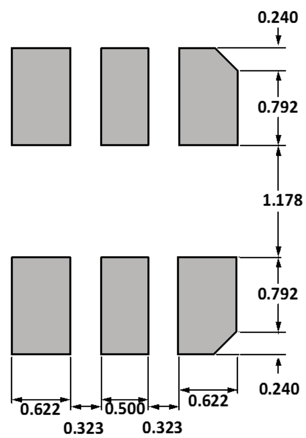


Figure 14. Recommended PCB Land Pattern Layout

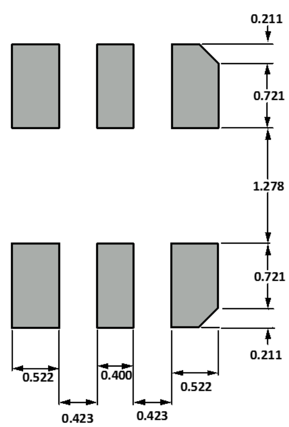


Figure 15. Suggested Solder Paste Stencil Pattern Layout

PCB MATERIAL AND THICKNESS

The ICS-41351 can be mounted on either a rigid or flexible PCB. A microphone's lid can be attached directly to the device housing with an adhesive layer. This mounting method offers a reliable seal around the sound port while providing the shortest acoustic path for good sound quality. The sound port can also be routed to the device housing through a port in a rubber boot. This boot should be designed to seal the connection between the microphone's lid and the rubber completely.

HANDLING INSTRUCTIONS

PICK AND PLACE EQUIPMENT

The MEMS microphone can be handled using standard pick-and-place and chip shooting equipment. Take care to avoid damage to the MEMS microphone structure as follows:

- Use a standard pickup tool to handle the microphone. Because the microphone hole is on the top of the package, the pickup tool should not be placed over the microphone port.
- Do not pull air out of or blow air into the microphone port.
- Do not use excessive force to place the microphone on the PCB.

REFLOW SOLDER

For best results, the soldering profile must be in accordance with the recommendations of the manufacturer of the solder paste used to attach the MEMS microphone to the PCB. It is recommended that the solder reflow profile not exceed the limit conditions specified in Figure 2 and Table 7.

BOARD WASH

When washing the PCB, ensure that water does not make contact with the microphone port. Do not use blow-off procedures or ultrasonic cleaning.

OUTLINE DIMENSIONS

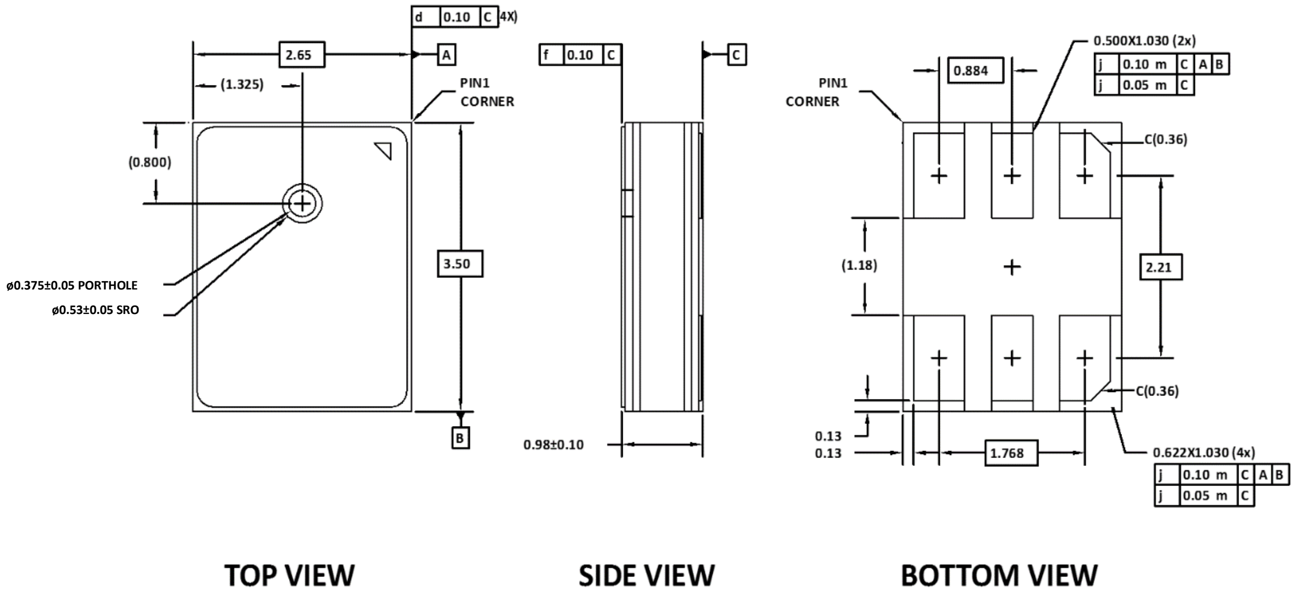


Figure 16. 6-Terminal Chip Array Small Outline No-Lead Cavity
3.50 mm × 2.65 mm × 0.98 mm Body

Dimensions shown in millimeters

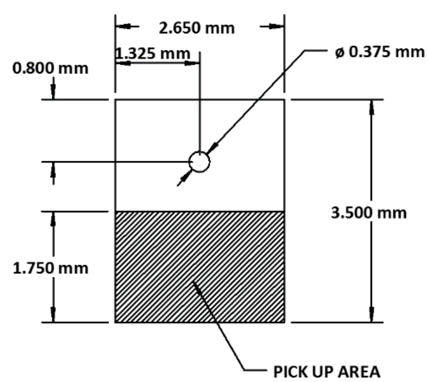


Figure 17. Recommended Vacuum Pick-up Area

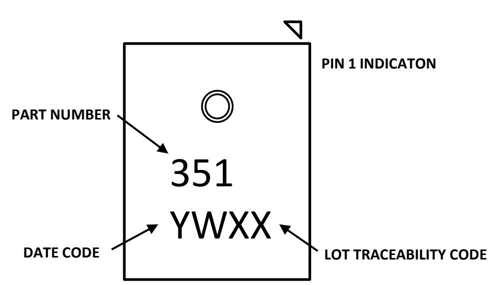


Figure 18. Package Marking Specification (Top View)

ORDERING GUIDE

PART	TEMP RANGE	PACKAGE	QUANTITY	PACKAGING
ICS-41351	−40°C to +85°C	5-Terminal LGA_CAV	10,000	13” Tape and Reel
EV_ICS-41351-FX	—	Evaluation Board	—	

REVISION HISTORY

REVISION DATE	REVISION	DESCRIPTION
1/15/2018	1.0	Initial Release
1/25/2018	1.1	Revised Mechanical Figures
7/2/2019	1.2	Revised Mechanical Figures and Document Header
11/15/2019	1.3	Updated Standard Mode clock frequency range and clock duty cycle conditions in Table 5

COMPLIANCE DECLARATION DISCLAIMER

InvenSense believes the environmental and other compliance information given in this document to be correct but cannot guarantee accuracy or completeness. Conformity documents substantiating the specifications and component characteristics are on file. InvenSense subcontracts manufacturing, and the information contained herein is based on data received from vendors and suppliers, which has not been validated by InvenSense.