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November 2013

### FDD5N50NZ

# N-Channel UniFET<sup>TM</sup> II MOSFET 500 V, 4 A, 1.5 $\Omega$

#### **Features**

- $R_{DS(on)}$  = 1.38  $\Omega$  (Typ.) @  $V_{GS}$  = 10 V,  $I_D$  = 2 A
- Low Gate Charge (Typ. 9 nC)
- Low C<sub>rss</sub> (Typ. 4 pF)
- 100% Avalanche Tested
- · Improved dv/dt Capability
- · ESD Imoroved Capability
- · RoHS Compliant

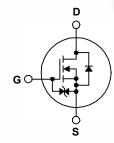
#### **Applications**

- LCD/LED/PDP TV
- · Lighting
- · Uninterruptible Power Supply

## **Description**

UniFET<sup>TM</sup> II MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET<sup>TM</sup> II MOSFET to withstand over 2kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts





#### Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol		Parameter	FDD5N50NZTM	Unit	
V <sub>DSS</sub>	Drain to Source Voltage		500	V	
V <sub>GSS</sub>	Gate to Source Voltage		±25	V	
	Decis Comment	- Continuous (T <sub>C</sub> = 25°C)	4		
ID	Drain Current	- Continuous (T <sub>C</sub> = 100°C)	2.4	A	
I <sub>DM</sub>	Drain Current	- Pulsed (Note	1) 16	Α	
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)		2) 304	mJ	
I <sub>AR</sub>	Avalanche Current (Note 1)		1) 4	Α	
E <sub>AR</sub>	Repetitive Avalanche Energy	Repetitive Avalanche Energy (Note 1)		mJ	
dv/dt	Peak Diode Recovery dv/dt	(Note	3) 10	V/ns	
D	Payer Dissipation	$(T_C = 25^{\circ}C)$	62	W	
$P_{D}$	Power Dissipation	- Derate Above 25°C	0.5	W/°C	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150	°C	
T <sub>L</sub>	Maximum Lead Temperature for	Soldering, 1/8" from Case for 5 Seconds	300	οС	

#### **Thermal Characteristics**

Symbol	Parameter FDD5N50NZTM			
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.0	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. 90		- C/VV	

## **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDD5N50NZTM	FDD5N50NZ	DPAK	Tape and Reel	330 mm	16 mm	2500 units

## **Electrical Characteristics** $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V, T_J = 25^{\circ} C$	500	-	-	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C	-	0.5	-	V/°C
1	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V	-	-	1	
DSS	Zero Gate Voltage Drain Current	$V_{DS} = 400 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	-	10	μА
I <sub>GSS</sub>	Gate to Body Leakage Current	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±10	μΑ

#### On Characteristics

V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu\text{A}$	3.0	-	5.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 2 \text{ A}$	-	1.38	1.5	Ω
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 2 A	-	3.54	-	S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V = 25 V V = 0 V		-	330	440	pF
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz	١.	-	50	70	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1 1011 12		-	4	6	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10V	V <sub>DS</sub> = 400 V I <sub>D</sub> = 4 A,		-	9	12	nC
$Q_{gs}$	Gate to Source Gate Charge	V <sub>GS</sub> = 10 V		-	2	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge	(Note	: 4)		4	-	nC

#### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time			-	12	35	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{DD} = 250 \text{ V}, I_{D} = 4 \text{ A},$		-	22	55	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS}$ = 10 V, $R_G$ = 25 $\Omega$		- /	28	65	ns
t <sub>f</sub>	Turn-Off Fall Time		(Note 4)	-	21	50	ns

#### **Drain-Source Diode Characteristics**

I <sub>S</sub>	Maximum Continuous Drain to Source Diode	Maximum Continuous Drain to Source Diode Forward Current		-	4	Α
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	16	Α
$V_{SD}$	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 4 A	-	-	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 4 A,	-	210	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	1.1	/ -	μС

#### Notes

- 1. Repetitive rating: pulse-width limited by maximum junction temperature.
- 2. L = 38 mH,  $I_{AS}$  = 4 A,  $V_{DD}$  = 50 V,  $R_G$  = 25  $\Omega$ , starting  $T_J$  = 25°C.
- 3. I  $_{SD} \leq$  4 A, di/dt  $\leq$  200 A/µs, V  $_{DD} \leq$  BV  $_{DSS},$  starting T  $_{J}$  = 25°C.
- 4. Essentially independent of operating temperature typical characteristics.

## **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

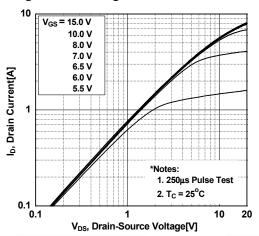


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

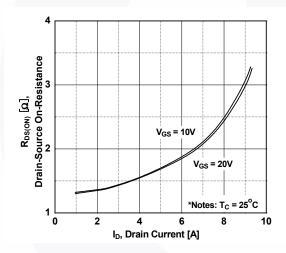


Figure 5. Capacitance Characteristics

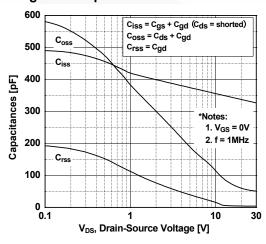


Figure 2. Transfer Characteristics

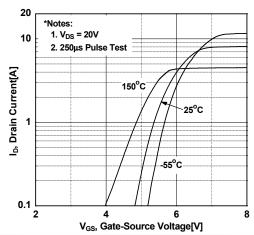


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

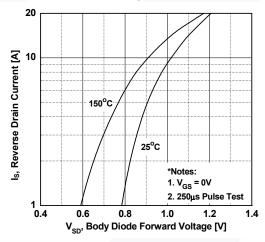
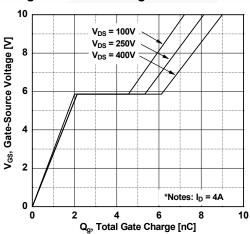


Figure 6. Gate Charge Characteristics



## **Typical Performance Characteristics** (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

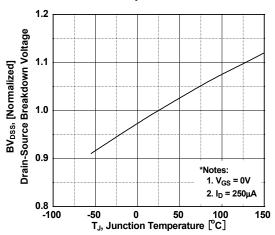


Figure 8. On-Resistance Variation vs. Temperature

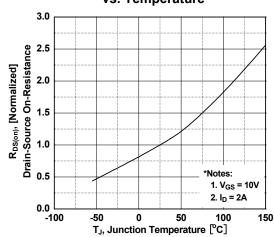


Figure 9. Maximum Safe Operating Area

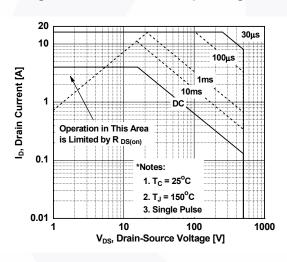


Figure 10. Maximum Drain Current vs. Case Temperature

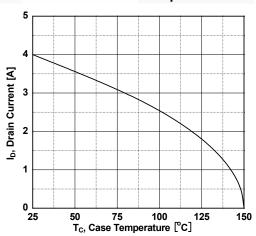
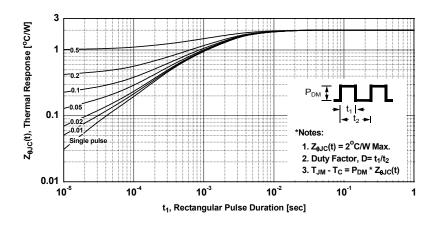


Figure 11. Transient Thermal Response Curve



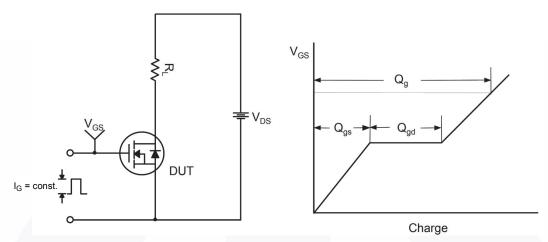


Figure 12. Gate Charge Test Circuit & Waveform



Figure 13. Resistive Switching Test Circuit & Waveforms



Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

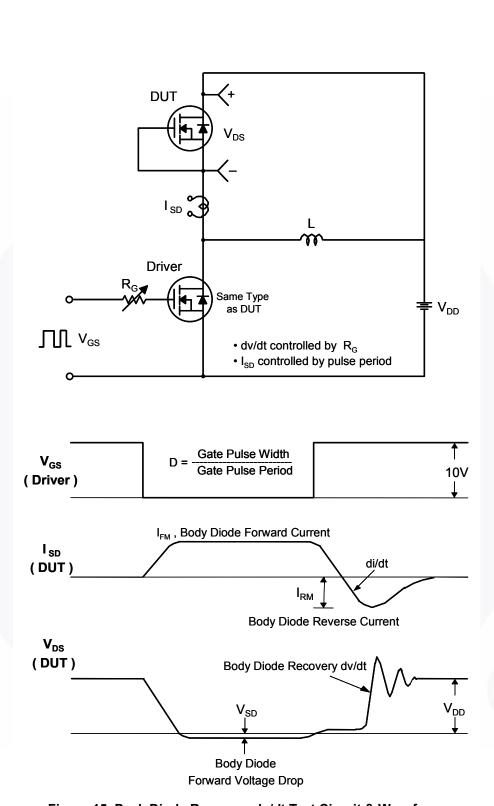


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

#### **Mechanical Dimensions**

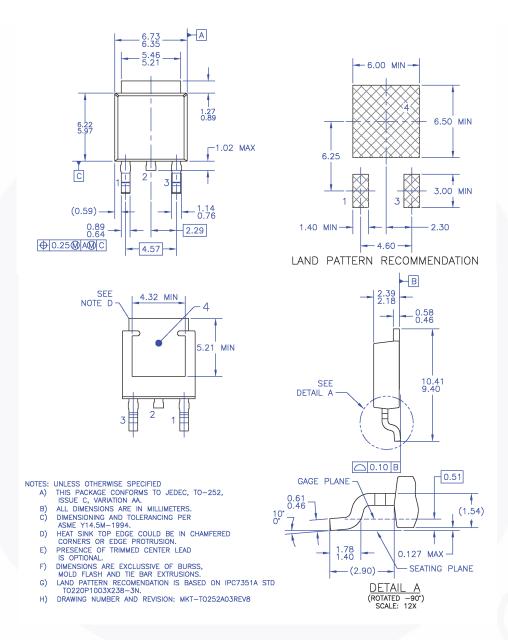


Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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